



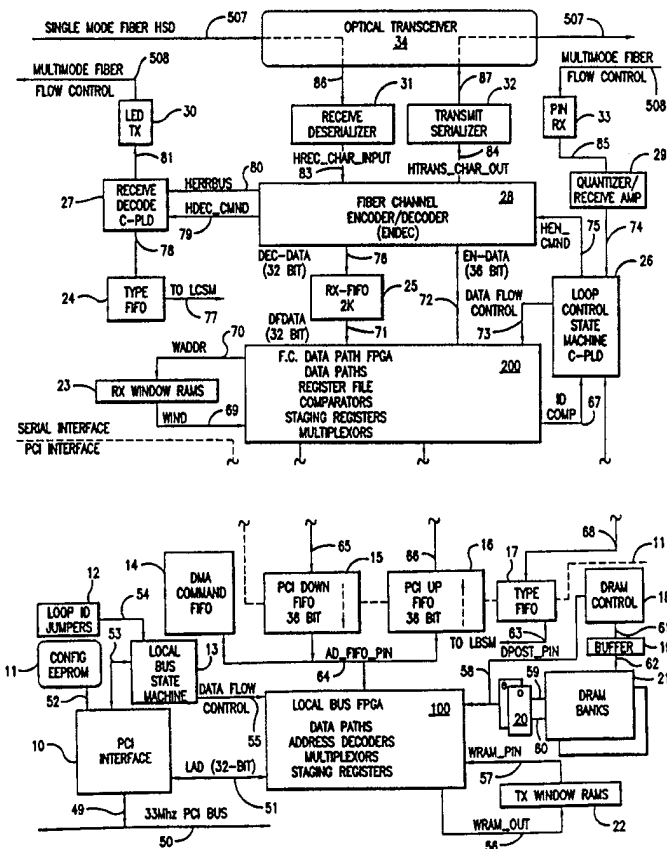
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<p>(21) International Application Number: PCT/US98/05785 (22) International Filing Date: 25 March 1998 (25.03.98) (30) Priority Data: 08/826,805 25 March 1997 (25.03.97) US (71) Applicant: SUN MICROSYSTEMS, INC. [US/US]; 901 San Antonio Road, Palo Alto, CA 94303 (US). (72) Inventors: ACTON, John, D.; 6041 S.W. 9th Street, Plantation, FL 33317 (US). DERBISH, Michael, D.; 3760 N.W. 103rd Avenue, Coral Springs, FL 33065 (US). GIBSON, Gavin, G.; 10805 Cypress Glen Drive, Coral Springs, FL 33071 (US). HARDY, Jack, M., Jr.; 13429 N.W. 8th Court, Sunrise, FL 33325 (US). HUMPHREYS, Hugh, M.; 8850 N.W. 17th Manor, Coral Springs, FL 33071 (US). KENT, Steven, P.; 1171 N.W. 133 Terrace, Sunrise, FL 33323 (US). SCHELONG, Steven, E.; 780 W. Plantation Circle, Plantation, FL 33324 (US). YONG, Ricardo; 16450 N.E. 2nd Avenue, North Miami Beach, FL 33162 (US). DeROLF, William, B.; 5840 S.W. 15th Street, Plantation, FL 33317 (US).</p>	<p>(74) Agents: FLEIT, PA, Martin et al.; Evenson, McKeown, Edwards & Lenahan, PLLC, Suite 700, 1200 G Street, N.W., Washington, DC 20005-3814 (US). (81) Designated States: CA, CN, JP, KR, MX, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> (88) Date of publication of the international search report: 30 December 1998 (30.12.98)</p>	

(54) Title: NOVEL MULTIPROCESSOR DISTRIBUTED MEMORY SYSTEM AND BOARD AND METHODS THEREFOR

(57) Abstract

A data processing system includes a plurality of nodes (501-504), a serial data bus (50) interconnecting the nodes in series in a closed loop for passing address and data information, and at least one processing node (501). In one construction, this processing node (501) has a processor (510), a printed circuit board (500), a memory partitioned into first and second sections and a local bus (13) connecting the processor (510), a block sharable memory section of the memory, and the printed circuit board (500). The local bus (13) is used for transferring data in parallel from the processor (510) to a directly sharable memory (518) section of the memory on the printed circuit board. The printed circuit board (500) includes a sensor for sensing when data is transferred into the directly sharable memory (518), a queuing device for queuing the sensed data, a serializer (32) for serializing the queued data, a transmitter for transmitting the serialized data onto the serial data bus to the next successive processing node (501), a receiver for receiving serialized data from next preceding processing node (501), and a deserializer (31) for deserializing the received serialized data into parallel data.



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/05785

A. CLASSIFICATION OF SUBJECT MATTER
 IPC(6) :G06F 13/00, 15/16, 9/00
 US CL :395/200.44, 395/800.3
 According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
 Minimum documentation searched (classification system followed by classification symbols)
 U.S. : 395/200.44, 395/800.3

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
 NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 data processing, processing nodes, serializer, deserializer, sensor , transmitter, receiver, serial data bus and circuit board.


C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 5,617,537 A (YAMADA ET AL.) 01 April 1997, see col. 6, lines 18-67 and col. 7, lines 1-68.	1-33
Y	US 5,327,570 A (FOSTER ET AL.) 05 July 1994, see col. 4, lines 1-68 and col. 5, lines 21-68.	1-33

Further documents are listed in the continuation of Box C. See patent family annex.

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