SOLID STATE WATCH

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Int. Cl. ........................................ G04b 19/30
Field of Search ................................ 58/23, 50, 85.5

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Assistant Examiner—E. C. Simmons
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ABSTRACT

Disclosed is a solid state watch which requires no moving parts for timekeeping and display. The watch comprises a crystal controlled oscillator connected through an integrated circuit binary frequency divider to an electro-optical display in the form of light emitting diodes. The display is energized only on demand and the level of the light output is controlled in accordance with ambient light conditions. The watch is energized from a rechargeable battery.

17 Claims, 26 Drawing Figures
PROGRAMABLE 12, 10 AND 6

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>COUNTER</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CARRY OUT</td>
</tr>
</tbody>
</table>

FIG. 10A

FIG. 10B

FIG. 11
Fig. 12

Fig. 13
FIG. 14

- IN
- Q1
- Q2
- Q3
- Q4
- D0
- D1
- D2
- D3
- D4
- D5
- D6
- D7
- D8

Four levels of output (402) waveforms corresponding to levels A, B, C, and D.
### FIG. 15A

<table>
<thead>
<tr>
<th>BINARY NUMBER</th>
<th>TENS</th>
<th>DECIMAL</th>
<th>7+1 SEGMENT DISPLAY</th>
<th>LST OUTPUT</th>
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<tr>
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<td></td>
<td>0</td>
<td>I I I I I I 0 0</td>
<td></td>
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<td>1 0 0 0 0</td>
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<td>1 1 0 0 0</td>
<td></td>
<td>3</td>
<td>I I I I I 0 0 0</td>
<td></td>
</tr>
<tr>
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<td></td>
<td>4</td>
<td>0 I I I 0 1 I 0</td>
<td></td>
</tr>
<tr>
<td>1 0 1 0 0</td>
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<td>5</td>
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<td>8</td>
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<td>10</td>
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<tr>
<td>1 0 0 0 1</td>
<td></td>
<td>11</td>
<td>0 I I 0 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>0 1 0 0 1</td>
<td></td>
<td>12</td>
<td>I I 0 1 1 0 1 I</td>
<td></td>
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<td>2</td>
<td>I I 0 1 I I 0 0</td>
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### FIG. 15B

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<th>TENS</th>
<th>DECIMAL</th>
<th>7+1 SEGMENT DISPLAY</th>
<th>TENS</th>
<th>FAST OUTPUT</th>
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<td></td>
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<tr>
<td>0 0 0 0 0 0 0 1 1 1 1 1 1 0 0 %₁</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>1 0 0 0 0 1 0 1 0 0 0 0 0 0 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
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<td></td>
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<td></td>
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</tbody>
</table>
### Table: Binary Number \( Q_1, Q_2, Q_3, Q_4, Q_5 \) vs. 7+1 Segment Display

| \( Q_1, Q_2, Q_3, Q_4, Q_5 \) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
| 1 0 0 0 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |
| 0 1 0 0 0 | 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
| 1 1 0 0 0 | 3 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
| 0 0 1 0 0 | 4 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
| 1 0 1 0 0 | 5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 | 6 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | % | 1 |  |  |  |  |  |  |  |  |  |  |
| 1 0 0 0 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
| 0 1 0 0 0 | 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
Incorporated in the watch case is a miniature 3 or 4-V rechargeable battery which is easily replaced by the wearer. The battery will last about five or six months under average wearing conditions before recharging becomes necessary and need for replacement is indicated by a dim display but the time accuracy of the watch is not affected by the reduced capacity power supply. Each watch is sold with an extra rechargeable battery connected through a recharging circuit to provide the correct recharging current. The spent battery is simply removed by the wearer and replaced by the fully recharged spare. No computed time is lost in this battery exchange since a third energy source permanently located inside the electronic module supplies sufficient power to run the time computer module during the exchange cycle.

The watch display consists of a T.V. screen-like colored filter which passes the cold red light from GaAsP light emitting diodes. A 27 dot or, alternatively, a 7 segment array forms each individual number at the appropriate moment at a brightness determined by a specially designed dimmer circuit. This dimmer circuit utilizes photodetectors to measure ambient lighting conditions so that dimness intensity provides viewing comfort under all day or nighttime lighting conditions.

Setting is accomplished quickly and accurately by inserting any suitable probe (pencil, pen, small stick, etc.) into one of two clearly marked recesses. The “Hour Set” rapidly advances the hours without disturbing the accuracy of the minutes or seconds. The “Minute Set” automatically zeros the seconds while it advances the minutes to the desired setting. The whole procedure, even though seldom required, takes a matter of a few seconds.

The watch of the present invention is virtually shockproof and waterproof, regardless of the environment in which it is placed. The computer module, including the display, is encapsulated with a clear potting compound so that no mechanical forces or corrosive elements can enter. Since there is no conventional stem for winding or setting, the small shaft sealing problem is eliminated. No maintenance or repair is normally necessary since all three ingredients are individually sealed and inaccessible to influences from the outside world. All solid state electronic components, including the light emitting diode displays, have a virtually unlimited life.

It is therefore one object of the present invention to provide an improved electronic wristwatch.

Another object of the present invention is to provide a wristwatch which utilizes no moving parts for performing the timing function.

Another object of the present invention is to provide a completely solid state electronic wristwatch in which the display is in the form of a plurality of light emitting diodes.

Another object of the present invention is to provide an electronic wristwatch including an illuminated display in which the light level is automatically compensated to the viewing conditions for increased eye comfort and reduced power drain.

Another object of the present invention is to provide an improved electronic wristwatch incorporating an electro optic display with an improved arrangement for resetting the display and one which includes automatically zeroing of the seconds display.

Another object of the present invention is to provide an improved electronic wristwatch incorporating a rechargeable battery.

Another object of the present invention is to provide an improved wristwatch having a permanent internal sustaining battery or the like so that no timekeeping is lost when the battery is replaced.

Another object of the present invention is to provide a wristwatch size device which functions as a fixed program computer.
These and further objects and advantages of the invention will be more apparent upon reference to the following specification, claims, and appended drawings, wherein:

FIG. 1A–1C are views of the face of a watch constructed in accordance with the present invention under differing conditions of operation;

FIG. 2 is a simplified block diagram of the major components of the solid state watch of this invention;

FIG. 3 is an exploded view showing the physical construction of the novel solid state watch of this invention;

FIG. 4 is a diagram of the assembly of the electrical circuit for the solid state watch of FIG. 3;

FIG. 5, 5A, 5B and 5C are detailed wiring diagrams for the watch of FIG. 3;

FIG. 6 shows a plurality of waveforms illustrating the operation of the light dimmer forming a part of the watch of FIG. 3;

FIG. 7 shows the details of one of the decoder drivers forming a part of the electrical circuit of the watch of FIGS. 3–5;

FIG. 8 shows a modified crystal controlled oscillator circuit for the watch of the present invention utilizing complementary MOS circuits;

FIG. 9 shows a modified display element for the watch of the present invention in the form of a 7-bar segment construction of light emitting diodes;

FIG. 10 is a detailed wiring diagram for a modified watch construction utilizing the display of FIG. 9 in which the program counter and decoder for the 7 segment display are all formed on a single monolithic integrated circuit chip;

FIG. 10A is a table showing the connections to the power supply terminals A and B in FIG. 10 when the circuit of FIG. 10 is used for different display digits;

FIG. 10B shows the alphabetical nomenclature for the 7 bar segment display of W of a "ones" digit and the corresponding diode Y of the "10's" digit in the hours display;

FIG. 11 shows waveforms at various locations in the circuit of FIG. 10 when it is used to count to 12 (1–12) for the hours display;

FIG. 12 shows similar waveforms for the circuit of FIG. 10 when it is used to count to 10 (0–9) for the "ones" digits of the minutes and seconds display;

FIG. 13 shows corresponding waveforms for the circuit of FIG. 10 when it is used to count to 6 (0–5) for the "10's" digits of the minutes and seconds display;

FIG. 14 is a waveform and timing diagram for the BCD to decimal decoder forming a part of the circuit of FIG. 10;

FIG. 15A is a table showing the relationship between the input signals, the BCD output of the counter (counting 1–12) and the 7 diode segments (8 segments with the 10's Y) for the hours display;

FIG. 15B is a similar table showing the relationship when the counter is counting to 10 (0–9); and

FIG. 15C is a corresponding table for when the counter is counting to 6 (0–5).

Referring to the drawings, the novel watch of the present invention is generally indicated at 10 in FIG. 1A. The watch is shown in FIG. 1A to actual size and is constructed to fit into a watch case of approximately the size of a conventional man's wristwatch. The case 12 is shown connected to a wristwatch strap 14 and includes a display window 16 through which the time is displayed in digital form and a pushbutton 18 for operating a demand switch through which the display is activated.

FIG. 1A shows the watch as it normally appears when the time is not being displayed. That is, in FIG. 1A no time indication is visible through window 16 and this is the normal condition. Such a watch is used in order to conserve battery energy in the watch. However, even though the time is not displayed through the window 16, it is understood that the watch 10 continuously keeps accurate time and is capable of accurately displaying this time at any instant of the day or night. When the wearer desires to ascertain the correct time, he depresses pushbutton 18 with his finger and the correct time immediately is displayed through the window 16 which illustrates a dot display giving the correct time reading as 10:10, namely ten minutes after ten o'clock, as indicated at 20 in FIG. 1B. The hours and minutes, i.e., 10:10, are displayed through the window 16 for a predetermined length of time, preferably 1-4 seconds, irrespective of whether or not pushbutton 18 remains depressed. The exact time of the display is chosen to give the wearer adequate time to consult the display to determine the hour and minute of the time. Should the minutes change during the time of the display, this change is immediately indicated by advancement of the minute reading to the next number, i.e., 11, if the watch is being worn. If pushbutton 18 remains depressed, at the end of 1-4 seconds, the hours and minutes of the display are extinguished, i.e., they disappear, and simultaneously the seconds reading, i.e., 59, is displayed through the window 16 as indicated at 22 in FIG. 1C. The advancing seconds cycling from 0 to 59 continue to be visible through window 16 until the pushbutton 18 is released.

FIG. 2 is a simplified block diagram of the electrical circuit for the watch of FIG. 1. The circuit comprises a time base or frequency standard 26 including a crystal to provide a very accurate frequency such that the frequency standard or oscillator oscillates at 32,768 Hz. This relatively high frequency is supplied by lead 28 to a frequency converter 30 in the form of a divider which divides down the frequency from the standard so that the output from the converter 30 appearing on lead 32 is at a frequency of 1 Hz. The 1 Hz signal is applied to a display actuator 34 which, in turn, drives the displays 20 and 22 of the watch 10 by way of electrical lead 36.

FIG. 3 is an exploded view showing the physical construction of a watch formed in accordance with the present invention. Watch 10 in FIG. 3 comprises the casing 12 carrying the pushbutton or display button 18 and provided with a window 16 through which the display may be read. Inserted into the window 16 and sealed there by a suitable epoxy resin is a light filter 38 which screens out much of the light which might otherwise get through the window. Of course, the filter 38 may be formed of a clear transparent material which passes all light but in the preferred embodiment it takes the form of a suitable red colored plastic, such as Plexiglas, which acts as a red filter (bandpass) passing light from the light emitting diodes of the display which, by way of example only, operate at a wave length of approximately 6,500 Angstroms in the visible red region. In some instances, it may be desirable to construct the filter 38 to pass blue, as well as red wave lengths so that the blue of the sky gets absorbed in the watch, thus enhancing somewhat visibility of the light emitting diodes during daytime conditions. The filter 38 may be formed of any suitable material, in addition to plastic, such as transparent colored glass or of ruby material having sufficient hardness that it will not scratch.

Received within case 12 are a pair of abutting back-to-back shims (shown separated for the sake of clarity), namely, a display shim 40 and a logic shim 42. The shims are preferably formed of a good strong heat conducting material, such as beryllium copper to take away any heat that might be generated by the display. Mounted on the underside of the logic shim 42, as indicated by phantom lines at 44, is the integrated logic circuitry. Secured to the top surface of display shim 40 are six display modules 46, 48, 50, 52, 54 and 56. Display modules 46 and 48 are for displaying the hours from 1 to 12, modules 50 and 52 are for displaying the minutes from 0 to 59, and modules 54 and 56 are for displaying the seconds from 0 to 59. Each of the modules is formed as a 27 dot array, i.e., each carries 27 light emitting diodes with the exception that minute module 50 carries the additional colon diodes 58 and hours 10's digit module 46 only carries one colon diode. The colon symbol of the display is played as a "1", that is the tens digit of the hours display is either 1 or 0 and is not illuminated. While a 27 dot array is illustrated, the display modules may take any desired form and may consist of 13 dot arrays or a 7 segment bar array as disclosed in copending application Ser. No. 818,227, filed Apr. 22, 1969. By way of example only, the 27 dot array illustrated in FIG. 3 may be formed on modules of the type manufactured
by the Hewlett-Packard Company of Palo Alto, California, identified as solid state numeric indicator HP 5082-7,000. These modules have the light emitting diodes mounted on them and are formed of a ceramic base with integrated circuit chips such as the chips 60, 62, 64, 66 and 68 mounted on the ceramic base and connected to the diodes and the logic circuits by suitable leads, laminated, printed or etched directly on the ceramic substrates. Connection from the display modules to the logic circuit 44 is by way of leads 70 which extend over the adjacent edges of the display shim 40 and the logic shim 42. In the preferred embodiment, the display modules are made slightly narrower than is customary for solid state numeric indicators but they are in all other respects similar to the commercially available solid state numeric indicators identified above.

While two separate shims are illustrated, it is understood that by using suitable monolithic integrated circuit construction it is possible to mount the logic circuits and display circuits on the top of a single shim, thus eliminating the necessity for the second shim illustrated in FIG. 3. In the preferred embodiment, the display shim 40 and the logic shim with the respective circuits attached are potted by coating the upper surface of shim 40, the shim edges and the lower surface of shim 42 with a clear silicone rubber potting compound. This isolates the electronics from the surrounding environment and enhances the reliability of operation of the circuits.

Depending from the underside of logic shim 42 is a quartz crystal 22 which, when the watch is on as shown in the back cover of FIG. 2, is a battery case 84 which houses a conventional rechargeable 4.5 V silver zinc battery (not shown). The battery may be of a 3 1/4 V cell construction to give a total battery output of 4.4/2 volts with a life of approximately 250 millionaire hours. Assuming standard usage, i.e., an average of approximately 24 interrogations per day, the battery will last on the order of 5 or 6 months before recharging is necessary. The battery employs a potassium hydroxide electrolyte and batteries of this type are commercially available from Yardney, Inc. of New York City. Power is supplied from the battery in case 84 by way of a pair of pins 86 and 88 which slide into receptacles 90 and 92 in the battery case to make contact with the battery and the upper ends of which contact with the electrical circuitry on the underside of logic shim 42. Receptacle 92 is connected by a pair of two-part receptacles extending through the back cover of the watch, the two parts of one of the reset pins being illustrated at 92A and 92B in FIG. 3. Finally, the various elements of the watch are mechanically secured together by the screws 94.

It is a feature of the watch 10 that the substrates of the display modules are removable attached to the upper surface of the display shim 40. That is, the substrates of the display modules 46, 48, 50, 52, 54, and 56 are attached by Borden's epoxy to the shim, which epoxy softens at about 300° F. and permits removal of the display modules from the shim for repair or replacement. The light emitting diodes mounted on the substrates are interconnected with the remaining circuitry by 0.001 inch aluminum wires ultrasonically bonded for interconnection.

FIGS. 4, 4A and 4B show an overall block diagram of the electrical circuit of the watch of the present invention. Watch 10 comprises an oscillator 96 which is controlled by the crystal 72 of FIG. 3 to produce an output on lead 98, i.e., a pulse train on that lead having a pulse repetition rate of 32,768 Hz. The crystal output passes through a complementary symmetry MOS coupler 100 of the type shown and described in assignee's copending application Ser. No. 768,076, filed Oct. 16, 1968, which acts as a divider, dividing the output by 2, i.e., a 7 stage counter, to produce an output on lead 102 having a pulse repetition rate of 256 Hz. This signal is divided by 2 in counter 104, by 2 again in counter 106, by 6 (20) in counter 108, and by 4 (21) counter 110. An 8 Hz output on lead 112 from counter 108 is applied to a set-hold circuit 114 where the 8 Hz. repetition rate pulse train appears as an output on lead 116. The 8 Hz. signal on lead 116 is applied to counter 118 where it is divided by 8 (25) to produce a 1 Hz. output pulse train on lead 120. The 1 Hz. pulse train is divided by 10 in counter 122, divided by 6 in counter 124, divided by 10 again in counter 126, divided by 6 again in counter 128, and the output of this counter is finally applied to counter 130 which divides by 12. The output of counter 122 appearing on leads 132, 134, and 136, and 138 is a binary coded decimal 1248 code which is applied to the decoder-driver 140 which, in turn, energizes the tens digits of the seconds display indicated at 142. The ones digits of the seconds display indicated at 144 are similarly actuated from counter 124 by way of seconds decoder-driver 146. Similar decoder-drivers 148, 150, and 152 actuate the tens digits of the minutes display at 154, the ones digits of the minutes display at 156, and the hours display at 158. Counter 130 has five output leads to decoder-driver 152 for a purpose more fully described below. The other decoder-drivers 146, 148 and 150 are actuated by BCD 1248 codes from their respective counters 124, 126, and 128 in the same manner as decoder-driver 140 is actuated from counter 122.

As previously stated, in order to conserve energy, the light emitting diodes are only energized on demand, i.e., when the pushbutton 18 of FIGS. 1A-IC is depressed by the wearer's finger. Even when the button is depressed, the lights are not always continuously lit but instead, in order to conserve power, are intermittently lighted during less than full daylight conditions at a frequency sufficiently high to give the appearance of continuity due to the light retention properties of the human eye. The pulses for intermittently lighting or pulsing the seconds display are derived from a display control driver 160 which applies the on-off pulses by way of lead 162 to the seconds decoder-drivers 140 and 146. Similar intermittent pulses from the display control drivers 160 are applied by lead 164 to the minutes decoder-drivers 148 and 150 and by lead 166 to the hours decoder-driver 152. The exact frequency at which the displays are turned on and off while always sufficiently high to give the impression to the human eye of continuous light is determined by a light control circuit 168 which supplies a light control signal by lead 170 to display control drivers 160. The light control signal is either DC (full daylight) or a combination of a 64 Hz signal supplied from counter 106 by way of lead 172, a 128 Hz signal from counter 104 by way of lead 174, and a 256 Hz signal supplied from the output of counter 100 by way of lead 176. These signals are combined in the light control circuit 168 in a manner determined by the output signal on lead 178 to the light control circuit from ambient light sensors 180. These light sensors are in the form of three phototransistors mounted on the display shim at 180 in FIG. 3 and act to produce increased illumination from the light emitting diodes during strong daylight conditions and less illumination from the diodes under nighttime or reduced light conditions. In the preferred embodiment, light sensors 180 provide four different light levels from the light emitting diodes so that the watch face may be read with equal facility and comfort under all possible lighting conditions while at the same time conserving energy at times when less light is needed from the diodes to make them visible, such as is the case when the watch is read in at least partial darkness.

As previously stated, the watch face is ordinarily not illuminated. The hours and minutes diodes only light up when the demand switch is depressed. Actuation of the demand button by the wearer causes the read switch 184 in FIG. 4b to close, causing the positive side of the power supply to be connected by way of leads 186 and 188 to the display control drivers 160. Energization of these drivers permits passage through them of the signal from the light control circuit 168 which is passed on
to the decoder-drivers causing the minutes and hours displays to be illuminated. No output from the display control diodes 160 appears on lead 162 at this time and the seconds displays are not illuminated. Closure of read switch 184 also applies B+ by way of lead 190 to set-hold circuit 114 which immediately resets a display timer 192 by way of lead 194. Display timer 192 is a divide by 10 counter and has applied to its input the 8 Hz pulse train on lead 112. This timer divides the 8 Hz by 10 and after 1-1/4 seconds produces an output pulse on lead 196 which is applied to display control driver 160. This pulse causes the display control driver to change state, removing the output from leads 164 and 166 and causing the minutes and hours display to be extinguished. At the same time, the output is switched to lead 162 causing the seconds display to be illuminated simultaneously with the extinguishment of the hours and minutes display.

An important feature of the watch of the present invention lies in the fact that the hours may be set independently of the minutes and seconds and at a very rapid rate. Closure of hours set switch 198, which is actuated from the back cover of the watch by a double pin setting arrangement of the type illustrated at 92A and 92B in FIG. 3 grounds one input of an hours set circuit 200 by way of leads 202 and 204. Hours set circuit 200 receives a 2 Hz pulse train from counter 110 by way of lead 206 and actuation of the hours set circuit by closure of hours set switch 198 causes the hours set circuit 200 to pass the 2 Hz signal on lead 206 to counter 110 by way of lead 208. Hours set switch 198 is also connected to the display control drivers 160 to cause an output to appear on leads 164 and 166 assuring that the hours and minutes are displayed when the hours are being reset during closure of switch 198. A minute set switch 212 is connected by leads 214 and 216 to a minute set circuit 218. As before, actuation of this circuit causes it to pass a 2 Hz pulse train on lead 220 from counter 218 by way of lead 222 to the divide by 10 counter 126 driving the minute display. Minute set switch 212 is likewise connected by lead 224 to display control drivers 160 again to insure an output on leads 164 and 166 during resetting.

It is a feature of the watch of the present invention that actuation of the minute set switch 212 automatically zeroes the seconds display. The reason for this is that most time signals, such as those given over the radio and the like, are given on the hour or on the minute and in order to start the watch in synchronism with the correct time as given by such a signal, it is necessary that the seconds display be at zero at the time the radio tone or other time signal is heard. In order to accomplish this, the minute set switch 212 is connected by leads 214 and 216 and a further lead 226 to set-hold circuit 114. Energization of this circuit from lead 226 produces an output pulse on output lead 228 which is applied to the reset terminals of counters 118, 122, and 124 by way of leads 230, 232, and 234 resetting these counters to zero and causing the seconds display to be automatically zeroed.

FIGS. 5, 5A, 5B and 5C show a detailed circuit diagram of the watch of the present invention shown in block form in FIG. 4. In FIG. 5, like parts bear like reference numerals. In FIG. 5, the elements corresponding to the blocks in FIG. 4 are enclosed in dashed boxes and the various decoder-drivers 140, 146, 148, 150, and 152 are shown as including a plurality of logic NOR gates for a purpose more fully described below. The display control drivers 160 are shown in two separate dashed boxes at different points in the circuit of FIG. 5 as is the light control circuit 168. Oscillator 96, including quartz crystal 72, takes the form of a complementary bipolar transistor construction including transistors T1 and T2 which are connected to form a free running crystal controlled multivibrator producing substantial squarewave pulse output.

Alternatively, oscillator 96 may take the form of a complementary MOS transistor of the type shown and described in assignee's copending application Ser. No. 768,076, filed Oct. 16, 1968, or it may take the form of the oscillator shown and described in assignee's copending application Ser. No. 802,571, filed Feb. 26, 1969. In the preferred embodiment, oscillator 96 is connected to the positive side of the battery through a current limiting resistor 229 and capacitor 228. The light sensors, which are preferably mounted on the top surface of the logic shim 40 of FIG. 3 so as to be exposed to ambient light passing through the filter 38 of that FIG., take the form of three photosensitive transistors 333, 333, and 335, labeled LS1, LS2, and LS3, respectively. These are conventional transistors in which the conductance of the emitter-collector circuit of the transistor is modified in accordance with the amount of light radiation impinging on the transistor base.

Following is a detailed description of the operation of the circuit of FIG. 5.

The transistors T1 and T2 with the crystal and associated parts oscillate at a frequency of 32,768 Hz. This frequency is divided by 2 by counter 282. The output frequency of this counter is 256 Hz. This frequency is fed into counter 283 which has outputs of 128 Hz, 64 Hz, 8 Hz and 2 Hz. The frequencies 256 Hz, 128 Hz, and 64 Hz are used in the light control or light dimmer circuit 168 which will be explained later. The 2 Hz is used in the setting circuits also to be explained later. The 8 Hz signal is used to drive the seconds counter and as the time base for the output control.

For timekeeping, the 8 Hz signals feed into the 7 stage counter 310. The first three stages of this counter act to divide by 8 and correspond to counter 118 of FIG. 4. Output 44 gives a pulse every second, Q5 gives a pulse every two seconds, Q6 every four seconds, and Q7 every eight seconds. This is known as a binary coded decimal (BCD) output. The decoder-driver requires a negative BCD input which is achieved by passing the signal through the NOR gates 301, 302, 303, and 304. The decoder-driver converts the BCD input into the proper form to light a numeral with light emitting diodes in a 27 dot matrix. The counter 310 is supposed to count to 10 but would normally count to 16. By detecting the numbers two and four are detected by NAND gate 328 and inverting these into a NAND gate 308 and inverter 309, it is possible to get a reset signal which passes through NOR gates 315 and 316 to the reset input. The reset signal from inverter 309 is also fed into the counter 313. This counter has outputs of one, two and four. This BCD number is converted to a negative BCD number by NOR gates 305, 306 and 307 and fed into the decoder-driver. The number two is detected by NAND gate 311 and inverter 312 and turned into a reset signal which passes through NOR gates 318 and 317 to the reset of counter 313 so that it counts six. This input pulse is lengthened by the 10 pf capacitor 236 at the input of NOR gate 314 and passed through this gate to be the input signal of counter 326. The output of counter 326 is fed to counter 327 and is amplified by NAND gate 1, 2, 4, 8. This output is converted to a negative BCD number by NOR gates 319, 320, 321 and 322 and fed into the decoder-driver. The numbers two and four are detected by the NAND gate 328 and the inverter 329 converts this to a reset signal to control counter 326 count 10. This reset signal is also used as an input signal for counter 327. Counter 327 is gated to divide by 6. The BCD output is converted to negative BCD by NOR gates 323, 324 and 325 for use by the decoder-driver. The numbers two and four are detected by the NAND gate 330 and converted to a reset signal by inverter 331. This signal passes through NOR gate 332 to flip-flop 339. The Q output of this flip-flop provides the one output of the BCD output. The two, four, and eight outputs are detected by NAND gate 342 and converted to a reset signal by inverter 343. This reset signal passes through NOR gates 346 and 347 to reset counter 340 only. It is not necessary to reset flip-flop 339 because at the count of 10 its output is zero. The reset signal is also fed into flip-flop 341. This sends a signal to NOR gate 338 which puts a signal into the negative BCD input of the decoder-driver which lights the one of the hour counter for the numbers 10, 11 and 12; however, when the number thirteen is detected by signals from flip-flop 339, counter 340 and flip-flop 341, being fed into NAND gate 344, a reset signal is generated by NOR gate 345 which actuates pulse generator 79. This signal resets counter 340 to zero and flip-flop 341.
When flip-flop 341 is reset, a signal is sent to NOR gate 337. This gate is connected to the four and eight inputs of the decoder-driver. This would be decoded as the number twelve which is impossible and therefore there is no output and no LEDs are lit. Since flip-flop 339 is not reset when the number 13 is detected, the output remains at zero and the decoder reads the number one. Therefore, the hours count from 1 to 12 and back to one again.

In the above paragraphs, the timing signal was generated, counted down and stored but there was no readout since readout is on demand only. Except during readout, power is removed from the decoder-driver circuit and the light emitting diodes. At the same time, a positive signal is applied to the alternate inputs of the NOR gates 301, 302, 303, 304, 305, 306, 307, 319, 320, 321, 322, 323, 324, 325, 333, 334, 335, 336, 337 and 338. This causes the outputs of all these NOR gates to go to ground. This is necessary because the gates and all other logic is made using complementary MOS while the decoder-drivers are made using bipolar transistors. If the outputs of the gates were allowed to alternate between high and low as the outputs of the counters changed, the operating current would be excessively high. The reason for this is because the inputs of the decoder-drivers are base-emitter junctions of bipolar transistors and a positive voltage at this point would cause current to flow through this base-emitter junction.

In order to light the display, it is necessary to push switch SW1. If this switch is released, the minutes and hours will light for 1.4 seconds. Closing switch SW1 causes a signal to pass through NOR gates 271 and 272. This signal changes the state of flip-flop 273A. This causes the signal to be removed from Q1 of flip-flop 273A, which opens the NOR gate 275 and allows the 8 Hz. signal to pass through to counter 275. The two and eight outputs are fed into the inputs of NAND gate 277. After 10 pulses or 1.4 seconds, NAND gate 277 and inverter 278 form a reset signal which resets counter 276 and flip-flop 273A which causes the hours and minutes display to extinguish. These displays were lit because when switch SW1 is closed, it toggled flip-flop 273A which removed the signal from Q1. This caused a signal to appear at the output of NOR gate 264. This signal passed through NOR gate 260 and inverter 259 to one input of NAND gates 256 and 257. If the other inputs of these gates also have a signal present, transistors T6 and T7 will cause transistors T5 and T7 to conduct and supply power to the decoder-drivers for the minutes and hours. At the same time, the signal disappears from the outputs of the inverters 280 and 281 which allows NOR gates 279, 319, 320, 321, 322, 333, 334, 335, 336, 337 and 338 to be turned off. The binary numbers stored at the associated counters to the decoder-drivers so that the proper numbers are displayed. If the read switch SW1 remains depressed after the counter 276 has reset and removed the signals from NAND gates 256 and 257, a signal will be transmitted through inverter 248 and NOR gate 249 to NAND gate 255. However, any signal on an input of NOR gate 249 will close this gate and keep the seconds display from being actuated. When the hours and minutes are lit, a signal will close gate 249 because the signal to turn on the hours and minutes coming from NOR gate 264 which is controlled by flip-flop 273A will keep any signal from passing through NOR gate 249. However, after this signal disappears, a signal can appear on NAND gate 255 which will turn on transistor T4 and cause transistor T3 to conduct which supplies power to the seconds decoder-driver and lights the seconds. At the same time, the signal is removed from the output of inverter 279 which allows the BCD numbers stored in the seconds counters to pass through to the seconds decoder-driver.

The intensity of the displays is controlled by the percentage of time the display is lit. Therefore, if four percentages 100 percent, 50 percent, 25 percent and 12.5 percent. These percentages are obtained by mixing various frequencies. The presence of these frequencies is controlled by three light sensitive transistors 180. High ambient light will cause the displays to have 100 percent duty cycle because all three light sensors L5, L52, and L53 will be conducting. When light sensor L52 conducts, it closes NOR gate 253 which will not allow NAND gate 262 to pass the 125 Hz. This puts a signal on the inputs of NAND gates 255, 256, and 257. When light sensor L53 conducts, it closes NOR gate 254 which will not allow the 64 Hz. signal to pass through NAND gates 261 or 258. This puts a signal on inputs of NAND gates 255 and 257 due to the action of NAND gate 261 and also puts a signal on the input of NAND gate 256 due to NAND gate 258. When light sensor L51 conducts, a signal appears at the output of NOR gate 252. This signal closes NOR gate 263 so that the 256 Hz. cannot pass through. This causes a signal to appear at the output of NOR gate 264 which closes NOR gate 260 so that a signal will appear at the output of inverter 259. There are now signals on all three inputs of NAND gates 256 and 257 which turn on the hours and minutes display 100 percent by the means described above. At the same time, the output of NOR gate 263 is connected to the input of NOR gate 249 which is closed while hours and minutes are displayed. However, if the read switch SW1 is still depressed and the hours and minutes displays have extinguished, a signal will appear on all three inputs of NAND gate 255 which will cause the seconds display to turn on for a 12.5 percent duty cycle. In order to conserve power, the light sensors are removed from the power source except when the displays are lit. The light sensors derive their power from the output signal of inverter 251. NOR gate 250 turns on the inverter 251 either by closing the switch or from the control signal coming from inverter 259.

Under lesser light conditions, light sensor LS3 does not conduct enough to close NOR gate 254 so that a signal will appear on one input of NAND gate 261 which will allow the 64 Hz. signal on the other input to pass through. This 64 Hz. signal goes directly to NAND gates 255 and 257 and through NAND gate 258 to NAND gate 256. The 64 Hz. signals at NAND gate 256 are 180° out of phase with the signals at NAND gate 257. Therefore, except during 100 percent duty cycle conditions, only one set of displays will be on at any time. Assuming proper conditions outlined above, either the hours and minutes or seconds only will be displayed with 50 percent duty cycle.

With less light conditions, light sensor LS2 will not conduct sufficiently to close NOR gate 253 and therefore NAND gate 256 will pass the 128 Hz. signal. This signal is fed to the inputs of NAND gates 255, 256, and 257. Under proper conditions, a D.C. signal will appear on one input of the three input NAND gates, a 64 Hz. signal on a second input and a 128 Hz. signal on the third input. The displays will be turned on only when all three signals are positive simultaneously which is 25 percent of the time.

Under low level light conditions, none of the light sensors conducts. Therefore, the 64 Hz. and 128 Hz. signals will be passed as explained above. Also, NOR gate 252 will be closed. This will allow the 256 Hz. signal to pass through NOR gates 256 and 249 and then through NOR gates 249 and 260. When minutes and hours are being read, the 256 Hz. signal passes through inverter 259 and appears at inputs on NAND gates 256 and 257. Under these conditions, all three signals appear at the inputs of the NAND gates 256 and 257. The displays will be turned on only when all three signals are positive simultaneously which is 12.5 percent of the time. The same thing occurs when the seconds are read since the 256 Hz. signal comes through NOR gates 263 and 249 to the input of NAND gate 255. The other two inputs have 128 Hz. and 64 Hz., respectively. Again the duty cycle is 12.5 percent. The hours and the minutes are set by depressing separate buttons. Setting the hours is accomplished without disturbing the timekeeping of the watch; however, setting the minutes stops the watch and resets the seconds to 00. The watch starts when the read button is pressed.

The hours are set by depressing switch 198, labeled SW3. This generates a signal at the output of NOR gate 256 which passes through NOR gate 260 and inverter 259 to provide a turn on signal to NAND gates 256 and 257 which turns on the
minutes and hours display. This switch also opens NOR gate 268 to allow the 2 Hz signal to pass through to NOR gate 232 and index the hours ahead at a rate of two hours per second.

Designing switch 212, labeled SW2, also turns on the minutes and hours display by applying a signal to NOR gate 266 which passes through NOR gate 260 and inverter 259. This applies a signal to NAND gates 256 and 257 which turns on the hours and minutes display. At the same time, NOR gate 267 is opened to allow the 2 Hz signal to pass through. This signal does two things. First, it passes through NOR gates 269 and 270 to reset flip-flop 273B. This opens NOR gate 274 and stops the 8 Hz signal into the input of the seconds counter 310. This signal also passes through NOR gates 215 and 316 to reset the counter 310 so that the seconds read 00. The 2 Hz signal from NOR gate 270 also passes through NOR gates 271 and 272 to set flip-flop 273A in the proper state. The 2 Hz signal from NOR gate 267 passes through NOR gate 314 to advance the minutes at a rate of 2 minutes per second. When the minute set switch SW2 is released, the 2 Hz signal stops and the display goes out but the timekeeping does not begin until the read switch SW1 is depressed because the state of flip-flop 273B will not allow the 8 Hz timing signal to pass through NOR gate 274. However, when switch SW1 is pressed, a signal is put into flip-flop 273A and 273B. This causes flip-flop 273A to change state and allow the 8 Hz signal to pass through NOR gate 274 and begin timekeeping again.

FIG. 6 is a plot of waveforms illustrating the operation of the light control circuit 168, previously described. Waveform A indicated at 348 is a 64 Hz signal, waveform B at 350 shows waveform A divided by 2, i.e., 128 Hz, and waveform C shows waveform B divided by 2, i.e., 256 Hz signal. Waveform D shows the 12.5 percent duty cycle obtained during low light level, i.e., substantial darkness conditions, such as would occur at nighttime. It can be seen that the waveform D, indicated at 354, contains pulses which occur only when waveforms A, B, and C are all simultaneously positive. As previously mentioned, the 100 percent duty cycle is obtained by applying a D.C. signal to the light emitting diodes, a 50 percent duty cycle by applying a pulse train which represents a combination of waveforms A and B, i.e., contains a pulse for every positive coincidence of the A and B waves in FIG. 6. FIG. 7 is a plot of one of the bipolar drivers, such as a portion of the decoder-driver 140. One of the diodes forming a part of the seconds display circuit, i.e., one of the 27 dots used to form one of the seconds numbers, is illustrated at 356 in FIG. 7. Connected in series with this diode across the positive power supply terminal 358 and the negative or ground side 360 is a conventional bipolar or NPN junction transistor 362. Base 364 of the transistor 362 is connected to a pair of complementary MOS transistors 364 and 366 and more particularly to the common drains of a complementary P and N channel pair having their gates connected together as at 368. When MOS 366 is conducting, the base of transistor 362 is connected to ground so that diode 356 does not draw current when turned off. A change of state in the complementary pair, i.e., transistor 364 turning on and transistor 366 turning off, causes diode 356 to draw current through bipolar transistor 362 and become illuminated.

FIG. 8 shows a modified oscillator which may be substituted for the oscillator 96 of FIG. 5. The oscillator 370 in FIG. 8 comprises a pair of complementary MOS transistors 372 and 374 connected between the positive power supply terminal 366 and the grounded side of battery 378. Transistor 376 is a P channel type while transistor 374 is an N channel type, their gates and drains being connected in common. Feedback around the transistors is by way of a frequency controlling quartz crystal 380, resistor 382, and a variable capacitor 384 which forms a trimming capacitor for slightly modifying the frequency of the oscillator output. The output is developed from the oscillator between output terminal 386 connected to the drains and ground indicated at 388. Again, the frequency of operation of this oscillator is under the control of crystal 380 and is preferably at a frequency of 32,768 Hz.

While the watch as previously described employed a 27 dot matrix of light emitting diodes for each display number, this need not be the case and the display may take the form of a 7 bar segment as disclosed in assignee's copending application Ser. No. 818,228, filed Apr. 22, 1969. FIG. 9 shows 7 light emitting diodes 390, 392, 394, 396, 398, 400, and 402 of elongated shape and arranged so that by lighting an appropriate combination of the bars, any of the numbers 0 through 9 may be displayed. In certain applications, the 7 bar segment display of FIG. 9 is preferred in that it is a separate device by 8 counter北部 display than the 27 dot matrix previously described.

FIG. 10 is a detailed circuit diagram of a decoder-driver for actuating a 7 bar segment display of the type illustrated in FIG. 9. More specifically, the circuit of FIG. 10 shows a complete programmable counter-decoder for actuating a 7 segment display and may be substituted in FIG. 9 for the counters and decoder-drivers, i.e., elements such as the combined elements 124 and 146 of FIG. 5. The circuit of FIG. 10 is formed of all complementary MOS circuitry and may be fabricated on a single monolithic chip. The circuit is designed to be universal, i.e., may be used for any of the displays in FIG. 5, either the hours, minutes or seconds, since the circuit of FIG. 10 is capable of counting from 0 to 12. Substitution of the circuit of FIG. 10 for the seconds unit counter 122 and the decoder-driver 140 necessitates replacing the second segment circuit, corresponding to the first three stages of counter 310 for applying a 1 Hz input pulse train to the input terminal 402 of the counter-decoder 400 of FIG. 10. Input terminal 402 is connected through an inverter 404 to the input of flip-flop 406. The output of flip-flop 406 is, in turn, connected through flip-flop stages 408, 410, 412, 414, and a resetting flip-flop 416. Counter 400 is provided with a power supply terminals 418 and 420, labeled A and B in FIG. 9, and an output terminal 422 (for supplying a carry out signal to the next counter), labeled C. Power supply terminals A and B are wired in accordance with the diagram of FIG. 10A, depending upon whether the counter is used to count up to 12, up to 10 (0 through 9) or up to 6 (0 through 5). If the counter is used to indicate hours and to count to 12 (display numerals 1 through 12), then the terminals A and B are connected to the positive side of the power supply. If counter-decoder 400 is used for the minutes 10's or seconds 10's display, i.e., counting 0 through 5, then both terminals A and B are connected to the positive side of the power supply. A reset terminal 424 is used to apply an external reset signal to flip-flop 406. This terminal is only used to reset the seconds counter-decoder and is not used in the minutes and hours circuits.

The outputs from the various stages of the flip-flops are applied through NOR logic gates and inverters to a BCD to decimal decoding circuit, generally indicates at 442 and comprising NOR gates 444, 448, 452, 454, 456, 458, 460 and 462. The binary coded decimal output of the flip-flop stage is decoded in circuit 442 for application to the 7 diodes 390, 392, 394, 396, 398, 400, and 402 connected to respective terminals R through X. These diodes are connected through NOR gates 464, 466, 468, 470, 472, 474, and 478 to the decoding circuit 442. An extra diode in the form of a long vertical bar is indicated; since this diode is used only in the hours display to indicate the 1 when the hours have a value of 10, 11, or 12. This diode is either on or off since a 0 in the 10's digit of the hours is not displayed. Diode 480 is connected to the counter portion of the circuit through NOR gates 476, 482 and inverter 484. An on-off terminal 486 connects the demand switch to the other inputs of the NOR gates 464 through 478 so that the lights are only illuminated on demand in the manner previously described.
The following is a description of the operation of the counter-decoder circuit of Fig. 10 in conjunction with the explanatory waveforms of Figs. 11–14 and the tables in Figs. 15A–15C showing the logic relationships between the input, the counter outputs, and the signals to the bar segment diodes when the circuit of Fig. 10 is used to count to 12 (1–12), to 10 (0–9), or to 6 (0–5).

The input signal (IN) at 402 passes through inverter 404 and drives 4 flip-flops FF1, FF2, FF3, FF4, which gives on their positive outputs Q1, Q2, Q3, and Q4 a binary coded decimal (BCD) number in accordance with the input signals and the internal function of the circuit.

COUNTER TO 12

\[ A = 0, B = 0, \] and \[ R = 0 \]

The FF 1, 2, 3 and 4 are a BCD counter. The NOR gate 507 will "read" the number 10 (2^2 + 2) from Q4 and the output of the NOR gate 506 which works like an inverter \( (A = 0) \), while the NOR gate 505, because of the inverter 4, has a permanent \( "0" \) output. Each time the binary number of the counter passes at 10 (2^2 + 2), the output of the NOR gate 507 is "1" and enters the NOR gate 508 (whose second input is "0" at that time) and through the inverter 509 which drives both FF5 and FF6. Then the positive outputs Q of these two flip-flops are "1" and their negative outputs \( Q' \) of at "0". Now, gate 516 is able to read the number 3 (2^2 + 2) of the BCD counter when it next appears and the NOR gate 510 is able to pass the inverted input signal which will reset flip-flop 416 a half period later. In the meantime, FF6 resets the flip-flops FF2, 3 and 4 while FF1 is already at zero.

Flip-flop 416 being reset, the circuit keeps running and at 13 (2^2 + 2 on FF1 and FF2 and 1 on FF5), the NOR gate 516 shifts to "1" which, through the inverter 517, gives another "0" input in NOR gate 515 (B = "0") which makes its output to be a "1" and through the NOR gate 508 and the inverter 509 drives the flip-flop 5 which is now reset and FF6 which resets FF2, 3, and 4 before it is reset itself by the inverted input signal through the NOR gate 510, and the counter keeps running from it.

When the flip-flop FF5, at the number 10, shifts to "1", carry output (C) through the NOR gates 513 and 514 passes from "0" to "1". C goes back to "0" when FF5 is reset at 13. This is the pulse which must be used to drive the next stage (falling pulse).

COUNTER TO 10

To count to 10, B is connected to "1". Now, through the NOR gates and inverter 482, 484, and 475, we have a permanent "0" on the output Y. The resetting pulse read by the NOR gate 516 can no longer pass through the NOR gate 515 whose output is "0". The counter runs as before and each time the NOR gate 507 reads 10 (2^2 + 2), through the NOR gate 508 and the inverter 509, it shifts the flip-flops FF5 and FF6. The output of FF5 is stopped by the NOR gates 513, 515 and 482, and FF6 will reset FF 2, 3 and 4 before it is reset itself as already explained. When flip-flop FF6 is set, through the NOR gates 512 and 514, C passes from "1" to "0" (falling pulse). When FF6 is reset, C goes back to "1". A next stage would be driven by the falling pulse.

COUNTER TO 6

To count to 6, connect A to "1" also. \( (A = B = "1") \). Now, the NOR gate 507 will "read" the number 6 (2^2 + 2) through the NOR gate 505 while the output of the NOR gates 506 and 518 are "0". The output signal on C is the same as when counting by 10. It is assumed that the reset input at R 424 was at "0", if R is at "1" all the flip-flops FF 1, 2, 3, 4 and 5 are reset no matter how FF6 is. If FF6 was resetting FF 2, 3 and 4, when resetting the whole circuit, FF5 will be reset before FF1 shifts for the second time (when it drives FF2).

Q1, Q2, Q3, Q4 and Q5 are the positive outputs of the first five flip-flops as shown on the drawing and Q R is the output of the inverter 509. Figs. 11, 12, and 13 show timing diagrams for these outputs.

BCD TO DECIMAL DECODER

The six flip-flops FF1-6 are able to count to 12 (1 to 12), 10 (0-9), and 6 (0-5) providing a BCD output for the units and a single digit when desired for the 10's. It is necessary to decode this binary number in a 7 segments display for the units. The ten is directly driven from terminal Y by the flip-flop FF5 through the NOR gates and inverters 482, 484, and 475.

Assuming the "On-Off" input is at "On", that is to say at "0", and knowing how the tens (T) works, consider the 3 line decoder (R, S, T, U, V, W, X) only. The BCD output of the counter is always one of the following numbers and only these numbers as given in the following table:

<table>
<thead>
<tr>
<th>TABLE</th>
<th>Number</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset at 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>R</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>U</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>V</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>W</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The underlined digits in the Table are the minimum digits which must be read in order to read the corresponding number and this one only. In the first part of the circuit, the NOR gates 446 through 462 are a BCD to decimal decoder whose outputs are 0 through 8 (9 is not decoded). As an example, the NOR gate 446 has its 4 inputs connected at Q1, Q2, Q3, and Q4. That is to say that when these 4 numbers are at "0" \( Q1 = Q2 = Q3 = Q4 = 0 \) = BCD number 0), the output of this NOR gate 446 is "1". Now if one or several inputs of this gate are not at "0", i.e., at "1", the output of the NOR gate 446 is "0". That is to say that the output D0 is "1" if only its BCD input is 0; it is the same for each of the outputs D1, 2, ..., 7, and 8 which is "1" respectively for their BCD input 1, 2, 3,... 7 and 8. This is shown by the waveforms in Fig. 14.

DECIMAL TO 7 SEGMENTS DECODER

With the 7 segments of the display being R, S, T, U, V, W, and X, assume that the segments are "On" all the time except when lit with the exception for the segment V, which is turned "On" when needed.

Consider the segment R, as an example. D1 and D4, through the NOR gate 464 will turn off R (R at "0") each time D1 or D4 are at "1". So the segment R is "On" (R at "1") for any number except for I and 4. It is the same for T, U, S, W, X through the NOR gates 476, 466, 468, 470, and 474.

As far as V is concerned, the output of the NOR gate 472 is "0" when D0 3, 6 or 8 are at "1". The NOR gate 478 reverses this signal so that V is at "1" for the numbers 0, 3, 6 and 8. FIG. 15A shows the relationship between the input signals, the BCD output of the counter and the 7 segment output (8 segment with the 10's Y) when counting to 12 (the hours display). FIGS. 15B and 15C show similar relationships for counting to 10 and 6, respectively.

When the "On-Off" input at 486 is at "1", through the NOR gates 464, 476, 466, 468, 470, 474, and 475, all the outputs R, T, U, S, W, V, X and Y are at "0", that is, the counter-decoder is. This input is responsive to operation of the demand switch 18 and is used to turn off the display.
although the logic information is saved and the counter still working. A particular advantage of the circuit shown in FIG. 10, usable in conjunction with the 7 bar segment display of FIG. 9, and with the MOS complementary integrated circuit oscillator of FIG. 8, is that the monolithic single chip circuit of FIG. 10 minimizes the circuit necessary and makes it possible to construct the watch utilizing a conventional 3 V power supply. That is, the monolithic chip circuit of FIG. 10 is a universal circuit and only five are required, namely, one for the hours display, two for the minutes display (counting 6 and 10), and two for the seconds display (also counting 6 and 10).

It is apparent from the above that the present invention provides an improved watch construction and particularly a construction which has as an important feature a completely solid state construction requiring no moving parts for performing the timekeeping function and displaying it. In all cases, the display takes the form of a plurality of conventional light emitting diodes, preferably gallium arsenide phosphide operating at a wavelength of approximately 6,500 Angstroms. The watch incorporates a demand display in which time is accumulated and stored internally of the watch and only displayed on demand. The display is timed, that is, the hours and minutes are displayed for 1/4 second or any other suitable predetermined length of time) and then are automatically extinguished at the same time simultaneously turning on the seconds display which remains on as long as the demand button is depressed. In other words, the hours and minutes are only normally displayed and the seconds are displayed only on continued interrogation. The watch of the present invention incorporates the extreme accuracy and reliability of the quartz crystal controlled time base so as to give very accurate time readings over substantial periods with little variation.

The digital light readout is intensity controlled so that the light intensity of the diodes automatically accommodates to the amount of ambient light in which the watch is being read. This not only increases increased comfort since the light necessary to read during daylight can be quite uncomfortable in near darkness but also preserves energy since the lights are illuminated only to the extent necessary for reading. A further feature of the present invention is the provision of a rechargeable battery, preferably used in conjunction with a permanent internal sustaining battery. For a 27 dot display, a conventional nickel cadmium cell 4.5 V battery is employed which only requires recharging approximately every 5 or 6 months during normal use (assumed to be an average of 24 interrogations per day). In the modified embodiment incorporating the improved monolithic programmable counter-decoder of FIG. 10, in combination with the 7 bar segment display of FIG. 9, the battery may take the form of a conventional 2 cell 3.0 V battery, with an improved life between recharging of approximately 9 months. The battery may be readily recharged from a 6 V power source incorporating a current limiting resistor or other current limiting circuitry to limit the recharging current to no greater than approximately 25 milliampere. The battery can normally be recharged from almost a complete dead condition in 24 hours and recharged in most cases of normal usage less than about 12 hours. The watch is preferably sold in the box or container incorporating a recharge in the form of four 1.5 V dry cells connected to a current limiting resistor. Also, preferably incorporated in the box or container housing the charger is a spare battery. Indication that the battery needs recharging occurs when the lights dim or fade completely. It is understood, however, that this does not affect the time-keeping, i.e., accurate timekeeping in the watch goes on as long as the battery has sufficient life to drive the circuits. Preferably incorporated in the watch is a permanent internal sustaining device in the form of a small battery or large capacitor which continues to supply energy to the circuit to keep the watch running during the 5 to 10 minutes that it takes to remove a low battery and replace a newly recharged one.

Through the use of complementary MOS circuits almost throughout the entire watch, a maximum amount of energy is conserved. In some cases, it is desirable to use complementary bipolar drive circuits for the displays but much of the remainder of the circuitry is preferably complementary MOS which may be formed by monolithic integrated circuit techniques. The hours are independently resettable without affecting the other settings or without affecting timekeeping. Setting the minutes stops the timekeeping and resets the seconds to 00 which state is maintained until the read button is again depressed. The electronic circuits are sealed inside the case and preferably potted against the atmosphere. The light emitting diodes give off a "cold" light which generates very little heat so that heating of the electrical elements is minimized. The numerical display is pleasant and easy to read and, in conjunction with the potted electronics, provides significantly improved shock and moisture resistant structure for the watch.

Various changes and modifications to the watch are readily apparent in that it could be used as an event timer, an elapsed time counter, an alarm watch, a calendar watch, a count down timer, or a 24 hour watch. The device is basically a small portable fixed program computer or timer system and is readily adaptable to a variety of these well known functions. The basic electronics can be used to drive a large variety of displays, including liquid crystal, electroluminescent, and other devices. The circuits can be changed to make an analog type display, i.e., a dot dial analogous to a conventional watch, and the numbers could readily be made to count to 24 instead of 12. It should be noted that in the preferred embodiment, the hours go from 1 to 12 and then back to one and the zero of the hours is blank when not needed. This is preferred since it simplifies the watch construction.

The watch is preferably constructed in an attractive case made of a super alloy sold under the name HAVAR which is a trademark of the Hamilton Watch Company and which material is extremely corrosion and abrasion resistant. If desired, the demand button can be replaced by a magnetic or capacitive actuated internal structure so that the display can be demanded without the necessity of a movable button or penetration of the case, i.e., actuation from outside. The complementary bipolar oscillator 96 preferably uses super beta transistors for increased current gain.

To summarize, principal operation features of the watch include:

1. It is possible to change the hours at a rate of 2 Hz per second without disturbing any other part of the watch.
2. The minutes are also reset at 2 Hz with the following operating functions:
   a. The seconds are automatically reset to zero and automatically held there;
   b. The minutes are counted up to the desired setting and everything is stored until the push demand button is pressed. During this time the 8 Hz input is cut off and the automatic setting to zero second provides a Hack feature in the watch. Because of the incorporation of an 8 Hz frequency available at the input to the watch counter, the maximum possible setting error is one-eighth of a second.
3. The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed and desired to be secured by United States Letters Patent is:

1. A solid state timing device comprising a source of frequency controlled electrical timing signals, a time computer module coupled to said source including an integrated circuit divider for lowering the frequency of the signals from said electrical source to a solid state optical display coupled to said time computer module for displaying the timing signals from said module, and an electrical energy source coupled to
energize said timing source, said time computer module and said optical display, said time computer module including a plurality of NOR logic gates coupled between said divider and said optical display for driving said display, said divider comprising a binary counting chain.

A solid state wristwatch comprising a wristwatch case, a crystal controlled oscillator forming a timing frequency base mounted in said case, a time computer module in said case coupled to said oscillator and including an integrated circuit divider for lowering the frequency of the signals from said oscillator, a solid state optical display in said case coupled to said time computer module for displaying the timing signals from said module, and an electrical energy source mounted in said case and coupled to energize said oscillator, said time computer module and said optical display, said case including a window through which said display is visible from outside said case, and an optical bandpass filter mounted in said window.

A solid state wristwatch comprising a wristwatch case, a crystal controlled oscillator forming a timing frequency base mounted in said case, a time computer module in said case including solid state divider and logic circuits for forming electrical timing signals from the output of said oscillator, a plurality of light-emitting diodes in said case coupled to said time computer module for optically displaying the timing signals from said module, an electrical energy source mounted in said case and coupled to energize said oscillator, said time computer module, and said light-emitting diodes, said case including a transparent window through which the light from said diodes is visible, and a demand switch operable from outside said case and coupling said energy source to said diodes for energizing said diodes only when said demand switch is operated, said diodes being arranged in groups to digitally display to the base ten the hours, minutes and seconds of time, said computer module including a delay circuit responsive to operation of said demand switch for maintaining the hours and minutes diodes at least intermittently energized over a predetermined interval of time independent of the condition of said demand switch at the end of said interval.

A solid state wristwatch comprising a wristwatch case, a crystal controlled oscillator forming a timing frequency base mounted in said case, a time computer module in said case including solid state divider and logic circuits for forming electrical timing signals from the output of said oscillator, a plurality of light-emitting diodes in said case coupled to said time computer module for optically displaying the timing signals from said module, an electrical energy source mounted in said case and coupled to energize said oscillator, said time computer module and said light-emitting diodes, said case including a transparent window through which the light from said diodes is visible, and a demand switch operable from outside said case and coupling said energy source to said diodes for energizing said diodes only when said demand switch is operated, an ambient light photosensor carried by said case, said photosensor being coupled to said computer module for varying the electrical energy supplied from said energy source to said diodes in accordance with the amount of ambient light incident on said photosensor.

A solid state wristwatch comprising a wristwatch case, a crystal controlled oscillator forming a timing frequency base in said case, a plurality of display modules mounted in said case, each of said display modules including a group of light-emitting diodes arranged to display a digital number to the base ten, an integrated circuit divider in said case coupled to said oscillator for reducing the frequency of the output from said oscillator to said divider being in the form of a complementary MOS binary counter, solid state encoders in said case coupling said counter to said light-emitting diodes, said encoders acting to convert the output of said counter into timing signals for said diodes, a rechargeable energy source removably mounted in said case, said case including a window through which said diodes are visible from outside said case, and a demand switch in said case operable from outside said case coupling said energy source to said light-emitting diodes whereby said diodes are energized only when said demand switch is operated, a pair of shims mounted in said case, said modules being mounted on one of said shims and said divider being mounted on the other of said shims.

A solid state timing device comprising a wristwatch case, a source of frequency controlled electrical timing signals mounted in said case, a time computer module coupled to said source including an integrated circuit divider for lowering the frequency of the signals from said electrical source, a solid state optical display including an hours and minutes display coupled to said time computer module for displaying the timing signals from said module, an electrical energy source coupled to energize said timing source, said time computer module and said optical display, a minutes setting switch in said case operable from outside said case, means responsive to operation of said minutes setting switch for applying a signal from said divider at a frequency of greater than 1 Hz to said minutes display, said optical display including means for displaying seconds in decimal form, and means in said case responsive to operation of said minutes setting switch for resetting said seconds display to zero.

A timing device according to claim 1 wherein said divider comprises stages of complementary MOS transistor pairs.

A wristwatch according to claim 2 wherein said optical display includes a plurality of light emitting diodes giving off light in the visible red region, said filter acting to pass said red light.

A wristwatch according to claim 8 wherein said diodes give off light having a wavelength of about 6,500 Angstroms.

A wristwatch according to claim 9 wherein said diodes are made of gallium arsenide phosphide.

A watch according to claim 3 wherein said computer module includes a switching circuit coupled to said demand switch and said delay circuit for at least intermittently energizing said seconds diodes at the end of said interval if said demand switch in in an operative position.

A watch according to claim 11 in which said computer module includes a hold circuit for maintaining said seconds diodes at least intermittently energized after said interval as long as said demand switch is in an operative position.

A watch according to claim 12 wherein said delay circuit operates said switching circuit for a time delay of 1-1/4 seconds.

A watch according to claim 4 wherein said time computer module includes a duty cycle circuit coupled between said energy source and said diodes, said photosensor being coupled to said duty cycle circuit to vary its output to said diodes.

A watch according to claim 14 in which said duty cycle circuit has an output which may assume any one of four different levels of energy in response to the output of said photosensor, said duty cycle circuit output increasing in energy with increasing ambient light incident on said photosensor.

A watch according to claim 4 wherein said photosensor comprises a plurality of light sensitive transistors mounted in said case beneath said window.

A watch according to claim 6 including a demand switch, means in said case responsive to operation of said minutes setting switch for unbalancing said displays from the 1 Hz output of said divider, and means in said case responsive to subsequent operation of said demand switch to recouple said displays to said 1 Hz output.
UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,672,155 Dated June 27, 1972

Inventor(s) John M. Bergey and Richard S. Walton

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Column 1, line 25, "high frequency" should read --frequency--.

In Column 3, line 2, "will" should read --will--.

In Column 13, line 17, "Q₂" should read --Q₂--;
line 43, "if" should read --is--.

In Column 14, line 6, "(0-9," should read --(0-9),--.

In Column 18, line 42, Claim 11, "in in" should read --is in--.

Signed and sealed this 15th day of May 1973.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents
Disclaimer


Hereby enters this disclaimer to claims 4, 14, 15 and 16 of said patent.

[Official Gazette December 4, 1973.]
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Hereby disclaims the entire remaining term of said patent.
[Official Gazette March 16, 1976.]