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Plasma-assisted etching process

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FIG.1

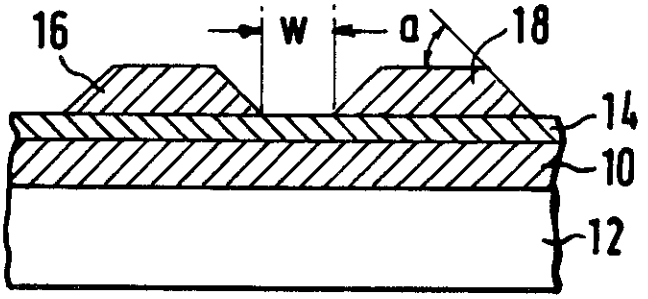


FIG.2
(PRIOR ART)

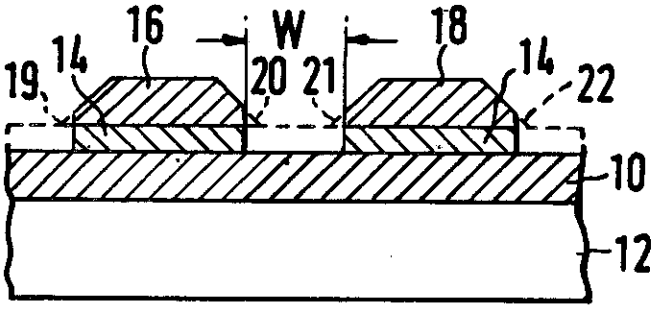


FIG. 4

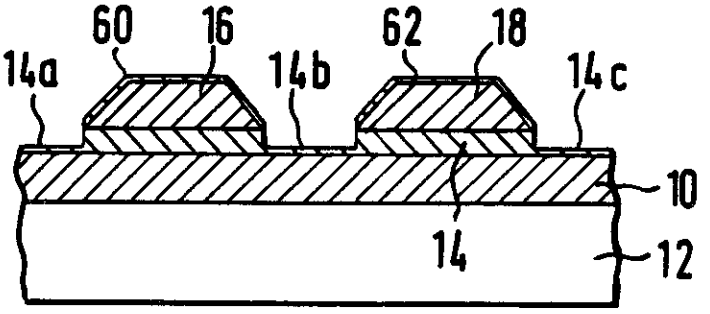
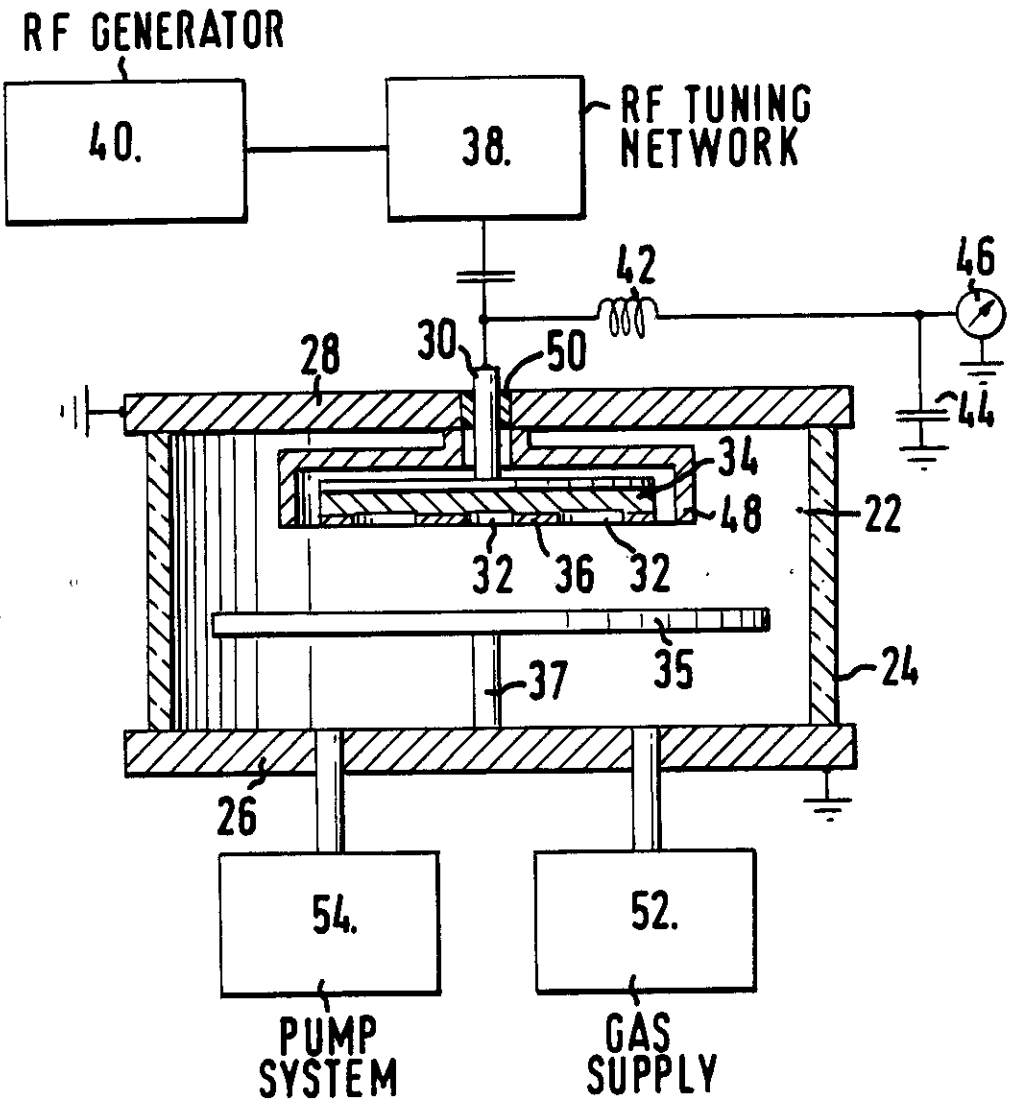


FIG. 3


RF GENERATOR
40.
38.
RF TUNING NETWORK
42
46
28
30
50
44
34
48
22
32
36
32
37
35
24
26
54.
52.
PUMP SYSTEM
GAS SUPPLY

PLASMA-ASSISTED ETCHING PROCESS

This invention relates to plasma-assisted etching processes such as are used, for example, in the fabrication of very-large-scale-integrated (VLSI) devices.

A particularly advantageous VLSI device fabrication process which can achieve submicron resolution with excellent linewidth control and step coverage is described by J.M. Moran and D. Maydan in "High Resolution, Steep Profile, Resist Patterns", in The Bell System Technical Journal, Vol. 58, No. 5, May-June 1979, pp. 1027-1036. This technique, which is sometimes referred to as the trilevel process, is also described in U.S. Patent number 4244799. In the trilevel process a relatively thin layer must be selectively etched using a thin high-resolution resist pattern as a mask. The relatively thin layer comprises, for example, a 0.12-micrometre (μm)-thick film of silicon dioxide (SiO_2).

When the trilevel process is used for micron and submicron pattern transfer, the material employed to form the required thin high-resolution resist pattern is typically an electron-sensitive polymer resist such as poly(glycidyl methacrylate-co-ethyl acrylate) also known as COP or poly(olefin sulfone) also known as PBS or an X-ray-sensitive resist such as a mixture of poly(2,3-dichloro-1-propyl acrylate) and poly(glycidyl methacrylate-co-ethyl acrylate) also known as DCOPA. As masking materials, these high-resolution resists do not,

however, always exhibit a sufficiently high resistance to the dry etching processes typically employed to etch the underlying SiO_2 layer. Thus, for example, when resist-masked SiO_2 is patterned in a reactive sputter etching step in a CHF_3 plasma, the SiO_2-to-resist etch ratio (etch selectivity) is in practice sometimes so low that the loss of linewidth that results from resist erosion during pattern transfer is unacceptably high for some VLSI device fabrication purposes.

Accordingly, continuing efforts have been made by workers in the VLSI device fabrication field directed at trying to improve the etch selectivity. It was recognized that such efforts, if successful, would make it feasible to use extremely thin resist masks in a device fabrication process which could achieve high-resolution features with excellent linewidth control.

Hence, an object of the present invention is to improve the etch selectivity of a plasma-assisted etching process.

In the invention as claimed a protective polymer layer is formed and maintained on a mask pattern of a polymer resist material while an underlying layer is being etched.

In one particular embodiment of the invention, the mask pattern is of PBS, COP or DCOPA and the underlying layer is of SiO_2. Reactive sputter etching of the SiO_2 layer is carried out in a plasma that contains at least fluorine and hydrogen species. In some cases, the plasma also contains nitrogen. The etching parameters are adjusted such that the protective polymer is formed and maintained on the resist material but not on the SiO_2. As a result, virtually no erosion of the resist pattern occurs during etching.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings of which:-

FIG. 1 is a schematic representation in cross-section of a portion of a structure which includes a resist-masked

layer to be etched;

FIG. 2 shows the FIG. 1 structure after etching of the resist-masked layer has been carried out in a conventional manner;

FIG. 3 depicts a specific illustrative system for etching VLSI structures in a process according to the invention;

and FIG. 4 shows the FIG. 1 structure after etching of the resist-masked layer has been partially carried out in accordance with this invention.

FIG. 1 represents a portion of a conventional VLSI structure (not to scale) at an intermediate point in the fabrication cycle thereof utilizing the aforespecified trilevel process. A thick organic layer 10 is shown deposited on a silicon substrate 12. Illustratively, the layer 10 comprises a 2.6-μm-thick layer of a standard photoresist such as HPR-206 made by the Hunt Chemical Company. On top of the layer 10 is a relatively thin intermediate layer 14 comprising, for example, a 0.12-μm-thick layer of plasma-deposited silicon dioxide (SiO_2). Lastly, a masking pattern comprising elements 16 and 18 is shown on the intermediate layer 14.

The regions of the intermediate layer 14 to be etched are not covered with resist material. As indicated in FIG. 1, one such region to be etched is defined between the resist elements 16 and 18. This region has a prescribed width w. Ideally, the region to be anisotropically etched in the layer 14 and, subsequently, the portion to be anisotropically etched in the relatively thick layer 10 should each have the same width w. If deviations from that width occur, the VLSI device being fabricated will vary from prescribed specifications.

By way of example, the pattern comprising the elements 16 and 18 (FIG. 1) is formed by initially depositing a 0.7-μm-thick layer of a standard high-resolution resist such as DCOPA on the layer 14. After conventional pattern exposure and development steps, the

thickness of the initially deposited resist is reduced to, for example, 0.35 μm. Moreover, after these steps only the masking elements 16 and 18 shown in FIG. 1 remain on the layer 14.

In practice, the edges of the elements 16 and 18 constituting the resist pattern are typically sloped as shown in FIG. 1. With a resist such as DCOPA, the angle a in FIG. 1 approximates 45 degrees. The etch resistance of DCOPA and some other high-resolution resists such as PBS and COP relative to that of SiO_2 in a standard etching plasma of, say, CHF_3 is relatively low. Hence, while the intermediate layer 14 is being anisotropically etched in such a plasma, side portions of the resist elements are also removed. This, of course, results in an undesired reduction of linewidth capability.

FIG. 2 illustrates the manner in which etching of side portions of the resist elements 16 and 18 causes the region removed from the layer 14 between the elements to have a width W that is greater than the prescribed width w shown in FIG. 1. (other regions defined by the resist mask in the layer 14 are, of course, similarly affected). In one actual case, the prescribed width w was 0.7 μm, whereas the width W actually achieved in the layer 14 as a result of plasma etching was 1.0 μm. In FIG. 2, the side portions 19, 20, 21 and 22 that are etched away from the elements 16 and 18, respectively, are shown in dashed outline.

In the process which we shall now describe virtually none of the patterned resist layer is eroded during the step in which mask-defined regions of the layer 14 are dry etched. This is done by forming and maintaining a protective layer only on the elements of the resist pattern during the etching operation. The exposed regions of the layer 14 are not so protected and are, accordingly, etched away. As a result, the pattern actually transferred from the resist mask layer into the layer 14 is a more faithful replica of the pattern defined in the resist than heretofore achieved in practice.

Our process can conveniently be carried out in a parallel-plate reactive sputter etching system of the type schematically represented in FIG. 3. The depicted system comprises an etching chamber 22 defined by a cylindrical conductive member 24 and two conductive end plates 26 and 28. A water-cooled conductive workpiece holder or cathode 30 is mounted in the chamber 22. Wafers 32, whose bottom surfaces are to be etched, are mounted on the bottom surface of a conductive plate 34 that is secured to the cathode 30 by any standard instrumentality (not shown) such as clamps or screws. The wafers 32 are maintained in place on the plate 34 by a cover plate 36 with holes in it. The plate 36 is made of a low-sputter-yield material that does not react chemically with the etching gas to form a nonvolatile material. Suitable such materials include fused quartz and Plexiglass (R.T.M.). Or the plate 36 may comprise a metallic member made, for example, of aluminium having a layer of silicon coated thereon.

The holes in the plate 36 are positioned in aligned registry with the wafers 32 and are each slightly smaller in diameter than the respectively aligned wafer. In that way, a major portion of the surface of each wafer is exposed for etching. By any standard means, the cover plate 36 is secured to the plate 34.

The FIG. 3 reactor also includes a conductive anode 35. The anode 35 is mechanically supported and electrically connected to the end plate 26 by a conductive post 37.

The cathode 30 of FIG. 3 is capacitively coupled via a radio-frequency tuning network 38 to a radio-frequency generator 40 which, by way of example, is designed to drive the cathode 30 at a frequency of 13.56 megahertz. Further, the cathode 30 is connected through a filter network, comprising an inductor 42 and a capacitor 44, to a meter 46 that indicates the peak value of the radio-frequency voltage applied to the cathode 30.

In FIG. 3, the end plates 26 and 28 are shown

connected to a point of reference potential such as ground. Accordingly, the anode 35 is also in effect connected to ground. The neck portion of the cathode 30 that extends through the plate 28 is electrically insulated from the plate 28 by a nonconductive bushing 50. Additionally, an open-ended cylindrical shield 34 surrounding the cathode 30 is connected to the plate 28 and thus to ground.

In one specific illustrative reactor of the type shown in FIG. 3 adapted to carry out applicants' inventive process, the anode-to-cathode separation was approximately 10 centimeters. In that reactor, the diameter of the plate 34 was about 25 centimeters and the diameter of the anode 35 was approximately 43 centimeters. The bottom of the plate 34 was designed to have seven 3-inch (7.5 cm) wafers to be etched placed thereon.

A specified gas atmosphere is established in the chamber 22 of FIG. 3. Gas is controlled to flow into the indicated chamber from a supply 52. Additionally, a prescribed low pressure condition is maintained in the chamber by means of a conventional pump system 54.

By introducing a particular gas or mixture of gases into the chamber 22 (FIG. 3) and establishing an electrical field between the cathode 30 and the anode 35, as specified in particular detail below, a reactive plasma is generated in the chamber 22. Volatile products formed at the workpiece surfaces during the etching process are exhausted from the chamber by the system 54.

A polymer material is formed and maintained on the aforedescribed resist elements 16 and 18, but not on the exposed regions of the layer 14, during plasma etching. This is accomplished by establishing a particular set of process conditions in the reactor.

In one illustrative case plasma etching of a resist-masked layer of SiO_2 was carried out with negligible erosion of the resist pattern. The layer of SiO_2 was approximately 0.12 μm thick, and the resist masking elements were made of DCOPA or PBS or COP approximately

0.35 μm thick. The gases introduced into the chamber 22 (FIG.3) from the supply 52 comprised a mixture of CHF_3, H_2 and N_2. The flow rates of the gases introduced into the chamber 22 were: CHF_3, 11.6 cubic centimetres per minute; H_2, 2.4 cubic centimetres per minute; and N_2, 0.6 cubic centimetres per minute. In addition, the pressure within the chamber 22 was established at approximately 7 μm, and the input power at the surface of the cathode was set at about 0.2 watts per square centimetre. Under these conditions, the SiO_2 layer was etched at a rate of approximately 215 Angstrom units (21.5nm) per minute. Significantly, the resist elements remained virtually dimensionally intact during the etching step.

The selective deposition of a polymer film on the resist elements during applicants' etching process is represented in FIG. 4. Thin protective films 60 and 62 (typically about 400-to-500 Angstrom units (40 to 50 nm) thick) are shown respectively covering the top surfaces of the resist elements 16 and 18. Midway during the anisotropic etching process, about one-half of the deposited layer 14 of SiO_2 has been removed from the structure being processed. These partially removed regions of the layer 14 are designated 14a, 14b and 14c in FIG.4. As indicated in FIG. 4, no polymer film exists on the unmasked regions 14a, 14b and 14c during etching.

Subsequently, as a result of the above-specified etching process, the SiO_2 regions 14a, 14b and 14c shown in FIG. 4 are completely removed, thereby exposing the surfaces of specified regions of the underlying layer 10 for processing. Importantly, since the masking pattern comprising the resist elements 16 and 18 suffers almost no dimensional degradation during etching, the SiO_2 regions underlying these masking elements suffer virtually no lateral erosion. Accordingly, the widths of the exposed regions of the layer 10 correspond substantially exactly to the dimensions originally defined by the resist pattern. Hence, when etching of the layer 10 is subsequently carried

out, utilizing the remaining SiO_2 regions as a mask, the pattern transferred into the layer 10 will be a highly faithful replica of the originally specified resist pattern.

Anisotropic etching of the layer 10 of FIG. 4 is done, for example, in a standard reactive sputter etching step employing a pure oxygen atmosphere at a pressure of about 5 μm, with an oxygen gas flow rate of about 12 cubic centimetres per minute and with the power input to the above-specified reactor being approximately 0.2 watts per square centimetre. In such a step, the resist pattern, including the elements 16 and 18 and the protective films 60 and 62 thereon, is removed while the pattern defined by the SiO_2 layer 14 is transferred into the relatively thick layer 10. Submicron resolution with essentially vertical walls in the layer 10 is thereby achieved. Thereafter, processing of the substrate 12 (or of a layer, not shown, interposed between the layer 10 and the substrate 12) is carried out using the patterned thick layer 10 as a mask in a manner known in the art. Such subsequent processing includes, for example, ion implantation, diffusion, etching, metallization, etc.

An exact theory explaining the basis for the aforespecified selective polymer deposition phenomenon discovered by the present inventors has not yet been formulated. One tentative explanation for the phenomenon is that during etching a polymer film derived from fluorine and hydrogen species in the plasma tends to form on both the masking resist elements and the unmasked or exposed SiO_2 regions. In accordance with that explanation, the film that tends to form on the SiO_2 is continually etched off the exposed regions by reactive and non-reactive sputtering, thereby subjecting the SiO_2 regions to the plasma etching process. On the other hand, film formation on the surface of the resist material (which itself is a polymer) occurs in an enhanced manner that leaves a net film thickness in place thereon even though reactive and non-reactive sputtering of the film is also continually

occurring there during etching. In turn, the polymer film thickness that persists on the resist pattern serves as an effective protective layer.

Whether or not that explanation is confirmed as being accurate, however, we have found that selective polymer formation and maintenance do in fact occur and can in practice be reliably and reproducibly utilized to improve an important VLSI device fabrication sequence significantly.

Although the introduction of nitrogen into the etching chamber from the gas supply is considered to be advantageous, its presence in the gas mixture is not necessary. In fact, CHF_3 alone is sufficient to achieve selective polymer deposition of the type specified herein when utilizing resists such as DCOPA, PBS or COP. For CHF_3 alone, it is advantageous to establish the following conditions in the FIG. 3 reactor to achieve such deposition: a pressure of about 10 μm, a gas flow rate of about 14 cubic centimetres per minute and a power input of approximately 0.15 watts per square centimetre.

Alternatively, $CHF_3 + H_2$, or $CHF_3 + N_2$, can be used in the FIG. 3 reactor to establish the selective polymer deposition phenomenon specified herein. For $CHF_3 + H_2$, the following conditions are advantageous: a CHF_3 gas flow rate of about 11.6 cubic centimetres per minute and an H_2 gas flow rate of about 2.4 cubic centimetres per minute; a pressure of approximately 7 μm; and a power input of about 0.2 watts per square centimetre. For $CHF_3 + N_2$, the corresponding parameters are: 14 cubic centimetres per minute (CHF_3), 2 cubic centimetres per minute (N_2), 15 μm and 0.2 watts per square centimetre.

A number of modifications of the described embodiments may be devised by those skilled in the art without departing from the scope of the invention. For example, although the primary emphasis herein has been directed to improving the etch selectivity between a resist mask pattern and an underlying layer made of SiO_2,

it is to be understood that the principles of this invention also apply to the etching of an underlying layer made of other materials such as silicon nitride, boron nitride or boron-doped polysilicon of the type described in copending British application number 8124744 (Serial No. 2085613). Moreover, although the principal practical applicability of the invention is presently considered to be in the trilevel process, it is to be understood that the invention can be used for other purposes. Thus, for example, wherever a resist-masked layer of SiO_2 or one of the above-specified alternative materials is to be etched in a high-resolution way in a plasma-assisted process, the selective polymer deposition technique of this invention may be applicable. Furthermore, it is apparent that the techniques described herein are not limited to the particular illustrative electron-sensitive and X-ray-sensitive resists specified above. These techniques are generally applicable to any process in which a thin high-resolution resist material is selectively irradiated and patterned to form an etching mask.

CLAIMS

1. A plasma-assisted etching process comprising depositing a polymer resist layer on a layer to be patterned, patterning the resist layer to define features therein and, using the patterned resist layer as a mask, dry etching the layer to be patterned in a plasma-assisted etching step in which a protective polymer film is formed and maintained only on the patterned resist layer while the layer to be patterned is etched.

2. A process as claimed in claim 1 wherein the etching step comprises establishing in a reaction chamber a plasma that includes fluorine and hydrogen species.

3. A process as claimed in claim 2 wherein the etching step comprises introducing into said chamber CHF_3 or $CHF_3 + H_2$.

4. A process as claimed in claim 2 wherein the plasma also includes a nitrogen species.

5. A process as claimed in claim 4 wherein the etching step comprises introducing into the chamber $CHF_3 + N_2$ or $CHF_3 + H_2 + N_2$.

6. A process as claimed in claim 5 wherein the body that includes the layer to be patterned is mounted on a cathode electrode within the chamber, the layer to be patterned is of SiO_2 and the etching step comprises introducing into the chamber $CHF_3 + H_2 + N_2$, establishing the following gas flow rates into said chamber: CHF_3 - approximately 11.6 cubic centimetres per minute, H_2 - approximately 2.4 cubic centimetres per minute and N_2 - approximately 0.6 cubic centimetres per minute, establishing a pressure within the chamber of approximately 7 μm and, by driving the cathode electrode via a capacitively coupled radio-frequency generator, establishing a power density of approximately 0.2 watts per square centimetre at the surface of the body.

7. A process as claimed in claim 6 wherein the SiO_2 layer is approximately 0.12 μm thick, the resist layer is approximately 0.35 μm thick and is of DCOPA,

PBS or COP, and the protective film is approximately 40-to-50 nanometres thick.

8. A process as in claim 7 wherein the SiO_2 layer is disposed on an organic layer approximately 2.6 μm thick and wherein, subsequent to the above-specified etching step, the organic layer is anisotropically etched in the chamber in a pure oxygen plasma etching step to transfer the pattern etched in the SiO_2 layer into the organic layer.

9. A process substantially as herein described with reference to FIGS. 3 and 4 of the accompanying drawings.

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RENEWAL DETAILS

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5th year due 15/10/85

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FOR THE COMPTROLLER

NOTE :

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2085809

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