



- (51) **International Patent Classification:**
H03F 1/02 (2006.01) **H03F 3/189** (2006.01)
H03F 1/30 (2006.01)
- (21) **International Application Number:**
PCT/US2016/017913
- (22) **International Filing Date:**
13 February 2016 (13.02.2016)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
62/116,415 14 February 2015 (14.02.2015) US
- (71) **Applicant:** SKYWORKS SOLUTIONS, INC. [US/US];
20 Sylvan Road, Woburn, MA 01801 (US).
- (72) **Inventors:** NG, Wendy; 710 Cilker Court, Los Gatos, CA 95032 (US). YEUNG, Yin, Chun; 1712 Snell Place, Milpitas, CA 95035 (US). SCHEEL, Michael, Lee; 2698 Hutchings Drive, San Jose, CA 95111 (US).
- (74) **Agent:** CHANG, James, W.; Fernando Hale & Chang LLP, 4199 Campus Drive, Suite 550, #115, Irvine, CA 92612 (US).
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

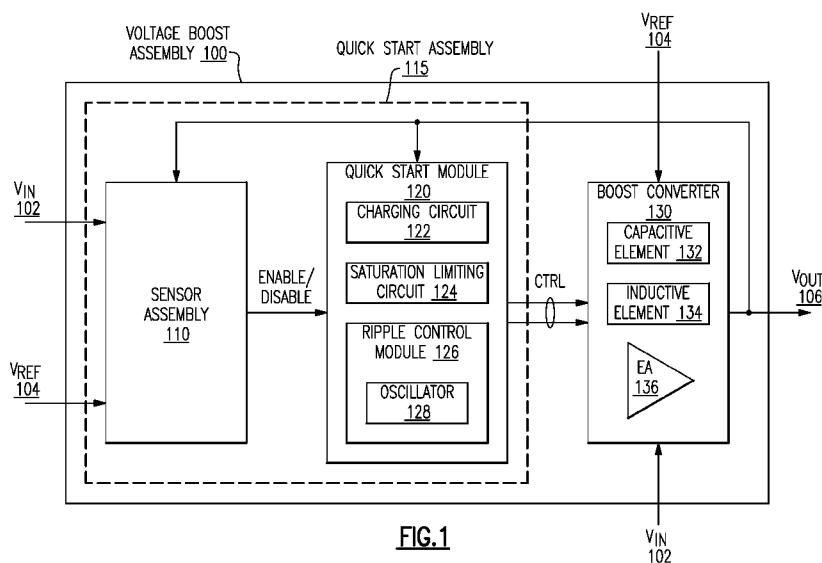
Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) **Title:** QUICK-START HIGH-VOLTAGE BOOST

**FIG.1**

(57) **Abstract:** In one implementation, a voltage boost assembly including a boost converter having a capacitive element arranged at an output, and an inductive element connectable to an electrical supply. The voltage boost assembly also includes a sensor assembly provided to generate a quick-start enable signal in response to detecting that an electrical condition relative to an electrical output of the boost converter has breached a first threshold. The voltage boost assembly further includes a quick-start module responsive to the quick-start enable signal, and configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge the capacitive element arranged at the output.

QUICK-START HIGH-VOLTAGE BOOST

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 62/116,415 filed February 14, 2015, entitled QUICK-START HIGH-VOLTAGE BOOST, the disclosure of which is hereby expressly incorporated by reference herein in its entirety.

BACKGROUND

Field

[0002] The present disclosure relates to power amplifiers in radio-frequency (RF) applications.

Description of the Related Art

[0003] Power amplifiers (PAs) are widely used in various communication networks to set the transmission power level of an information-bearing signal transmitted by one device to another device. For example, power amplifiers are used to set the pulse energy emitted by pulsed lasers in optical communication networks. Power amplifiers are also used in the radio frequency (RF) front-end components of wireless carrier network devices – such as base stations, repeaters, and mobile client devices (e.g. mobile phones, smartphones, tablet computers, etc.) – to set the power level of a wireless signal transmitted through an antenna. PAs are also used in local area networks of homes and offices to support both wired and wireless connectivity of servers, computers, laptops, and peripheral devices such as photocopiers and printers.

[0004] In some implementations, PAs use a boost converter for DC-to-DC power conversion when the PAs output voltage should be greater than its input voltage. Typically, a boost converter with a compensated error-amplifier has an intrinsic soft-start feature. With the capacitor at the error-amplifier output slowly being charged up, the duty cycle of the boost is slowly increased, leading to a slow increase of the boost output voltage. In some implementations, in order to use a

boost converter to power a high-voltage PA, the boost converter is specified to ramp up at a rate of 570 mV/ μ s in order to avoid any signal distortion at the output of the PA. The fast ramp-rate of the boost output voltage not only limits the value of the output capacitor, but also posts a challenge on circuit design and architecture to work against the slow soft-start nature of the error amplifier.

SUMMARY

[0005] In accordance with a number of implementations, the present disclosure relates to a voltage boost assembly including a boost converter having a capacitive element arranged at an output, and an inductive element connectable to an electrical supply. The voltage boost assembly also includes a sensor assembly provided to generate a quick-start enable signal in response to detecting that an electrical condition relative to an electrical output of the boost converter has breached a first threshold. The voltage boost assembly further includes a quick-start module responsive to the quick-start enable signal, and configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge the capacitive element arranged at the output.

[0006] In some implementations, the inductive element is provided to establish an output current level.

[0007] In some implementations, detecting that an electrical condition relative to an electrical output of the boost converter has breached the first threshold includes detecting that a reference voltage indicates demand for an electrical output (e.g., an output voltage) that is at least 10% higher than the current electrical output of the boost converter.

[0008] In some implementations, detecting that an electrical condition relative to an electrical output of the boost converter has breached the first threshold includes detecting that a reference voltage indicates demand for an electrical output (e.g., an output voltage) that is at least 20% higher than the current electrical output of the boost converter.

[0009] In some implementations, the quick-start module includes a charging circuit provided to charge the capacitive element so that an electrical output (e.g., an output voltage) of an associated error amplifier satisfies a third threshold in response to the quick-start enable signal. In some implementations,

the third threshold is characterized in relation to a high voltage level that can be sustained at the output of the error amplifier.

[0010] In some implementations, the quick-start module includes a saturation limiting circuit provided to limit current through the inductive element to establish the output current in response to the quick-start enable signal. In some implementations, the current through the inductive element is limited to a level that is characterized by a saturation condition of the inductive element.

[0011] In some implementations, the quick-start module includes a ripple control module provided to reduce current ripple in the output current level by adjustment of a switching frequency in response to the quick-start enable signal. In some implementations, the ripple control module includes an oscillator that provides a switching frequency that is increased in response to the quick-start enable signal.

[0012] In some implementations, the second threshold is characterized by a current level available to charge the capacitive element.

[0013] In some implementations, the sensor assembly is configured to turn off the quick-start enable signal in response to determining that the electrical output of the boost converter has satisfied a fourth threshold. In some implementations, the fourth threshold is approximately 95% of a set-point output level.

[0014] In some implementations, the present disclosure relates to a module that includes a packaging substrate configured to receive a plurality of components. The module also includes a power amplifier. The module further includes a voltage boost assembly, including a boost converter configured for a power amplifier included on at least a portion of the substrate, the boost converter having a capacitive element arranged at the output, and an inductive element connectable to an electrical supply. The voltage boost assembly also includes a sensor assembly provided to generate a quick-start enable signal in response to detecting that an electrical condition relative to an electrical output of the boost converter has breached a first threshold. The voltage boost assembly further includes a quick-start module responsive to the quick-start enable signal, and configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge the capacitive element arranged at the output.

[0015] In some implementations, the quick-start module includes a charging circuit provided to charge the capacitive element so that the output of an associated error amplifier satisfies a third threshold in response to the quick-start enable signal.

[0016] In some implementations, the quick-start module includes a saturation limiting circuit provided to limit current through the inductive element coupled to establish the output current level in response to the quick-start enable signal.

[0017] In some implementations, the quick-start module includes a ripple control module provided to reduce current ripple in the output current level by adjustment of a switching frequency in response to the quick-start enable signal.

[0018] In some implementations, the quick-start module is configured to turn off the quick-start enable signal in response to determining that the electrical output of the boost converter has satisfied a third threshold.

[0019] In some implementations, the module is at least one of a power amplifier module (PAM) or a front-end module (FEM). In accordance with some implementations, the voltage boost assembly of the module includes the functions and/or features of any of the voltage boost assemblies described herein.

[0020] According to some teachings, the present disclosure relates to a radio-frequency (RF) device that includes a transceiver generate to an RF signal. The RF device also includes a front-end module (FEM) in communication with the transceiver, the FEM including a packaging substrate configured to receive a plurality of components, the FEM further including a voltage boost assembly on the packaging substrate, the voltage boost assembly including a boost converter having a capacitive element arranged at the output, and an inductive element connectable to an electrical supply a sensor assembly provided to generate, the voltage boost assembly also including a quick-start enable signal in response to detecting that an electrical condition relative to an electrical output of the boost converter has breached a first threshold, and the voltage boost assembly further including a quick-start module responsive to the quick-start enable signal, and configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge the capacitive element arranged at the output. The RF device

further includes an antenna in communication with the FEM, the antenna configured to transmit the amplified RF signal.

[0021] In some implementations, the RF device includes a wireless device. In some implementations, the wireless device includes at least one of a base station, a repeater, a cellular phone, a smartphone, a computer, a laptop, a tablet computer, and a peripheral device. In accordance with some implementations, the voltage boost assembly of the FEM module includes the functions and/or features of any of voltage boost assemblies described herein.

[0022] According to some teaching, the present disclosure relates to a method of ramping up the output of a boost converter. The method includes sensing that an electrical condition relative to an electrical output of the boost converter has breached a first threshold. The method further also generating a quick-start enable signal in response to sensing the breach of the first threshold. The method further includes driving a boost converter to deliver an output current that satisfies a second threshold in order to charge a capacitive element arranged at the output of the boost converter by charging the capacitive element so that the output of an associated error amplifier satisfies a third threshold, limiting the current through an inductive element coupled to a supply, and increasing a switching frequency in order to reduce ripple.

[0023] For purposes of summarizing the disclosure, certain aspects, advantages and novel features of the inventions have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the invention. Thus, the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] So that the present disclosure can be understood in greater detail, a more particular description may be had by reference to the features of various implementations, some of which are illustrated in the appended drawings. The appended drawings, however, merely illustrate the more pertinent features of the present disclosure and are therefore not to be considered limiting, for the description may admit to other effective features.

[0025] Figure 1 is a block diagram of a voltage boost assembly according to some implementations.

[0026] Figure 2 is a schematic diagram of the voltage boost assembly in Figure 1 according to some implementations.

[0027] Figure 3 is a schematic diagram of a portion of the voltage boost assembly in Figure 1 according to some implementations.

[0028] Figure 4 shows example performance plots of the voltage boost assembly in Figure 1 according to some implementations.

[0029] Figure 5 is a flowchart representation of a method of operating the voltage boost assembly in Figure 1 according to some implementations.

[0030] Figure 6A-6C are block diagrams of different integrated circuit (IC) implementations of the voltage boost assembly in Figure 1 according to some implementations.

[0031] Figure 7 is a block diagram of an example module according to some implementations.

[0032] Figure 8 is a block diagram of an example radio frequency (RF) device according to some implementations.

[0033] In accordance with common practice the various features illustrated in the drawings may not be drawn to scale. Accordingly, the dimensions of the various features may be arbitrarily expanded or reduced for clarity. In addition, some of the drawings may not depict all of the components of a given system, method or device. Finally, like reference numerals may be used to denote like features throughout the specification and figures.

DETAILED DESCRIPTION OF SOME IMPLEMENTATIONS

[0034] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

[0035] As discussed above, in order to use a boost converter to power a high-voltage PA, a boost converter is specified to ramp up at a rate of 570 mV/ μ s in order to avoid any signal distortion at the output of the PA. In order to ramp up the boost output voltage quickly, for example, a 1 μ F capacitor is used as the output capacitor. According to some implementations, when the reference voltage V_{REF} from the controller interface (e.g., MIPI) requests that V_{OUT} be higher than V_{IN} , and

20% higher than the current output voltage value, the boost converter activates a quick-start module.

[0036] In some implementations, the quick-start circuit module includes at least one of a charging circuit, a saturation limiting circuit, or a ripple control module. In some implementations, the quick-start circuit module includes a charging circuit with a current source that is turned on to force the output voltage of the error amplifier satisfy a predefined value (e.g., 1.1 V or 1.2 V). In other words, the charging circuit requests the boost converter to run at maximum duty-cycle. In some implementations, the quick-start circuit module includes a saturation limiting circuit which sets the current-limit of the boost converter to a predetermined level (e.g., 2.5 A) to prevent an inductive element of the boost converter from being saturated. In other words, the saturation limiting circuit allows enough current into the output. In some implementations, the quick-start circuit module includes a ripple control module which increases the switching frequency of the boost converter above a predetermined switching frequency (e.g., from 2 MHz to 2.5 MHz) to achieve lower ripple through the inductive element.

[0037] In some implementations, when the output voltage of the boost converter is sensed to reach 95% of its set-point, the quick-start module is turned off. The quick-start module allows the boost to be operated at high duty-cycle, pumping a maximum amount of current to charge the capacitor at the boost output.

[0038] Figure 1 is a block diagram of a voltage boost assembly 100 according to some implementations. While pertinent features are shown, those of ordinary skill in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. To that end, in some implementations, the voltage boost assembly 100 includes a quick-start assembly 115 and a boost converter 130. According to some implementations, the quick-start assembly 115 includes a sensor assembly 110 and a quick-start module 120.

[0039] In some implementations, the sensor assembly 110 is configured to provide an enable signal to the quick-start module 120 when one or more predetermined quick-start enable conditions are satisfied. In one example, the quick-start enable conditions are satisfied when $V_{IN\ 102} < V_{REF\ 104}$ and $0.8 \cdot V_{REF\ 104} > V_{OUT\ 106}$. In some implementations, the sensor assembly 110 is configured

to provide a disable signal to the quick-start module 120 when one or more predetermined quick-start disable conditions are satisfied. In one example, the quick-start disable conditions are satisfied when $0.95 \cdot V_{REF\ 104} < V_{OUT\ 106}$ or $V_{IN\ 102} > V_{REF\ 104}$.

[0040] In some implementations, the quick-start module 120 includes a charging circuit 122, a saturation limiting circuit 124, and a ripple control module 126. In some implementations, the boost converter 130 includes a capacitive element 132, an inductive element 134, and an error amplifier 136. In some implementations, the inductive element 134 is provided to establish an output current level.

[0041] According to some implementations, the charging circuit 122 is configured to force the output of the error amplifier 136 to satisfy a predefined value (e.g., 1.1 V or 1.2 V). For example, in some implementations, this forces the error amplifier 136 to run at a duty cycle that satisfies a predefined threshold (e.g., 100% or maximum duty cycle). According to some implementations, the saturation limiting circuit 124 is configured to set a limit of the current flowing through the inductive element 134 to a predetermined output level (e.g., 2.5 A). For example, in some implementations, this prevents saturation of the inductive element 134. According to some implementations, the ripple control module 126 is configured to increase the switching frequency of an oscillator 128 above a predetermined switching frequency (e.g., from 2 MHz to 2.5 MHz). For example, in some implementations, this reduces ripple in the current flowing through the inductive element 134.

[0042] Figure 2 is a schematic diagram of the voltage boost assembly 100 in Figure 1 according to some implementations. While pertinent features are shown, those of ordinary skill in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. Elements common to Figures 1-2 include common reference numbers, and only the differences between Figures 1-2 are described herein for the sake of brevity. To that end, in some implementations, the voltage boost assembly 100 includes resistive elements 246 and 248, V_{OUT} precharge 204 (e.g., the output voltage prior to the capacitive element 132), and $V_{OUT\ 106}$ (e.g., the output voltage after the capacitive element 132). In some implementations, the

voltage boost assembly 100 includes a boost control 202 associated with a p-channel field-effect transistor (PFET) (e.g., with $R_{ds} = 0.27 \Omega$), which acts as a switch to enable and disable the voltage boost assembly 100. According to some implementations, the value of the inductive element 134 is, for example, $1.5 \mu\text{H}$, and the value of the capacitive element 132 is, for example, $1 \mu\text{F}$.

[0043] As shown in Figure 2, in some implementations, the quick-start assembly 115 is coupled with the output of error amplifier 136. For example, as discussed above with reference to Figure 1, the quick-start assembly 115 or a component thereof (e.g., the charging circuit 122 in Figure 1) is configured to force the output of the error amplifier 136 to satisfy a predefined value (e.g., 1.1 V or 1.2 V).

[0044] As shown in Figure 2, in some implementations, the quick-start assembly 115 provides an input to current limit comparator 224. For example, as discussed above with reference to Figure 1, the quick-start assembly 115 or a component thereof (e.g., the saturation limiting circuit 124 in Figure 1) is configured to set a limit of the current flowing through the inductive element 134 to a predetermined output level (e.g., 2.5 A).

[0045] As shown in Figure 2, in some implementations, the quick-start assembly 115 provides an input to summation element 236 to compensate for the oscillator slope. For example, as discussed above with reference to Figure 1, the quick-start assembly 115 or a component thereof (e.g., the ripple control module 126 in Figure 1) is configured to increase the switching frequency above a predetermined switching frequency (e.g., from 2 MHz to 2.5 MHz).

[0046] As shown in Figure 2, in some implementations, the output of the error amplifier 136 provides an input to pulse-width modulation (PWM) comparator 222. The output of the error amplifier 136 is also coupled with a shunt resistance element 242 (e.g., $80 \text{ k}\Omega$) and a shunt capacitance element 244 (e.g., 100 pF), which are connected in series to ground. The output of the PWM comparator 222 provides an input to OR gate 226, and the output of the current limit comparator 224 provides another input to the OR gate 226.

[0047] As shown in Figure 2, in some implementations, the output of the OR gate 226 provides an input to SR latch 228 (e.g., the R input) along with a clock (CLK) signal (e.g., the S input). The output of the SR latch 228 (e.g., the Q output) provides an input to a driver amplifier 230. The output of the driver amplifier 230 is

coupled with the gate of an n-channel field-effect transistor (NFET) (e.g., with $R_{ds} = 0.15 \Omega$) 230. The source of the NFET 230 is coupled with the output of the inductive element 134, and the drain of the NFET 230 is coupled with ground.

[0048] As shown in Figure 2, in some implementations, the output of the inductive element 134 provides an input to differential amplifier 232. The source of NFET 234 provides another input to the differential amplifier 232. As shown in Figure 2, in some implementations, the gate of NFET 234 is coupled with V_{OUT} 106, and the drain of NFET 234 is coupled with ground. The output of the differential amplifier 232 provides an input to the current limit comparator 224 and the summation element 236.

[0049] Figure 3 is a schematic diagram of a portion of the voltage boost assembly 100 in Figure 1 according to some implementations. While pertinent features are shown, those of ordinary skill in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. Elements common to Figures 1-3 include common reference numbers, and only the differences between Figures 1-3 are described herein for the sake of brevity. To that end, in some implementations, the quick-start assembly 115: includes comparators 302, 304, and 306; differential amplifiers 308 and 310; SR latch 314; AND gate 316; NFET 318; and current source 320.

[0050] As shown in Figure 3, in some implementations, the comparators 304 and 306 provide inputs to the SR latch 314 (e.g., the S and R inputs, respectively). As shown in Figure 3, in some implementations, the comparator 302 and the SR latch 314 (e.g., the Q output) provide inputs to the AND gate 316. When V_{IN} 102 < V_{REF} 104 and $0.8 \cdot V_{REF}$ 104 > V_{OUT} 106, the output of the AND gate 316 is logic high (e.g., 1) and the voltage boost assembly 100 operates under quick-start parameters. Under quick-start parameters, (A) the current flowing through the inductive element 134 is set to a predetermined output level (e.g., 2.5 A), (B) the switching frequency is increased above a predetermined switching frequency (e.g., from 2 MHz to 2.5 MHz), and (C) the current source 320 supplies a predefined current (e.g., 10 μ A) so that the output of the error amplifier 136 to satisfy a predefined value (e.g., 1.1 V or 1.2 V). When V_{IN} 102 > V_{REF} 104 or $0.95 \cdot V_{REF}$ 104

$< V_{OUT}$ 106, the output of the AND gate 316 is logic low (e.g., 0) and the voltage boost assembly 100 operates under regular parameters.

[0051] As shown in Figure 3, in some implementations, V_{REF} 104 and V_{OUT} 106 provide inputs to the differential amplifier 308. The output of the differential amplifier 308 and V_{bg} 312 provide inputs to the differential amplifier 310. The output of the differential amplifier 310 is coupled to the gate of NFET 318. In other words, in one example, the NFET 318 and differential amplifiers 308 and 310 clamp the output of the error amplifier 136 at 1.2 V.

[0052] Figure 4 shows example performance plots of the voltage boost assembly 100 in Figure 1 according to some implementations. While pertinent features are shown, those of ordinary skill in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. To that end, in some implementations, example performance plot 410 shows V_{OUT} 106 over time. For example, as shown in example performance plot 410, V_{OUT} 106 increases from approximately 3.8 V to 9.5 V in approximately 10 μ s.

[0053] According to some implementations, example performance plot 420 shows V_{REF} 104 versus time. For example, as shown in example performance plot 420, V_{REF} 104 increases from approximately 0.5 V to 2.0 V.

[0054] According to some implementations, example performance plot 430 shows the output voltage of the error amplifier 136 versus time. For example, as shown in example performance plot 430, the output voltage of the error amplifier 136 is clamped at 1.2 V during the quick-start period between 5 and 10 μ s.

[0055] According to some implementations, example performance plot 440 shows the current flowing through the inductive element 134 versus time. For example, as shown in example performance plot 440, the current flowing through the inductive element 134 is limited to 2.5 A during the quick-start period between 5 and 10 μ s.

[0056] Figure 5 is a flowchart representation of a method 500 of operating the voltage boost assembly 100 in Figure 1 in accordance with some implementations. In some implementations, the method 500 is performed by the voltage boost assembly 100 in Figure 1 or a controller associated therewith. While pertinent features are shown, those of ordinary skill in the art will appreciate from

the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. To that end, briefly, in some circumstances, the method 500 includes: powering on a voltage boost assembly; determining whether quick-start conditions are satisfied; operating the voltage boost assembly under regular parameters if the quick-start conditions are not satisfied; and operating the voltage boost assembly under quick-start parameters if the quick-start conditions are satisfied.

[0057] To that end, as represented by block 5-1, the method 500 includes powering on a voltage boost assembly. For example, with reference to Figure 1, the voltage boost assembly 100 initiates operation when the associated device (e.g., a mobile phone or the like) is powered on. For example, with reference to Figure 2, the voltage boost assembly 100 is powered on when the PFET associated with boost control 202 is in an “on” state, which allows current to flow from the inductive element 134 to the capacitive element 132.

[0058] As represented by block 5-2, the method 500 includes determining whether quick-start enable conditions are satisfied. For example, with reference to Figure 1, the sensor assembly 110 senses whether an electrical condition relative to an electrical output of the boost converter (e.g., V_{OUT} 106) has breached a first threshold. According to some implementations, for example, the quick-start enable conditions are satisfied when V_{IN} 102 < V_{REF} 104 and $0.8 \cdot V_{REF}$ 104 > V_{OUT} 106.

[0059] If the quick-start enable conditions are not satisfied, the method continues to block 5-3. If the quick-start enable conditions are satisfied, the method continues to block 5-4. For example, with reference to Figure 1, the sensor assembly 110 generates a quick-start enable signal and provides the quick-start enable signal to the quick-start module 120 in response to sensing that the first threshold has been breached. According to some implementations, detecting that an electrical condition relative to an electrical output of the boost converter has breached the first threshold includes detecting that a reference voltage indicates demand for an output voltage that is at least 10% higher than the current output voltage. In some implementations, detecting that an electrical condition relative to an electrical output of the boost converter has breached the first threshold includes detecting that a reference voltage indicates demand for an output voltage that is at

least 20% higher than the current output voltage. In another example, with reference to Figure 3, when $V_{IN\ 102} < V_{REF\ 104}$ and $0.8 \cdot V_{REF\ 104} > V_{OUT\ 106}$, the output of the AND gate 316 is logic high (e.g., 1) and the voltage boost assembly 100 operates under quick-start parameters.

[0060] As represented by block 5-3, the method 500 includes operating the voltage boost assembly under regular parameters.

[0061] As represented by block 5-4, the method 500 includes operating the voltage boost assembly under quick-start parameters. For example, with reference to Figure 1, the quick-start module 120 is configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge a capacitive element arranged at the output in response to the quick-start enable signal. According to some implementations, the second threshold is characterized by a current level available to charge the capacitive element.

[0062] According to some implementations, as represented by block 5-4a, the method 500 includes enabling the charging circuit. For example, with reference to Figure 1, the quick-start module 120 includes a charging circuit 122 provided to charge the capacitive element 132 so that the output of an associated error amplifier satisfies a third threshold in response to the quick-start enable signal. According to some implementations, the third threshold is characterized in relation to a high voltage level that can be sustained at the output of the error amplifier. In some implementations, the charging circuit 122 is configured to force the output of the error amplifier 136 to satisfy a predefined value (e.g., 1.1 V or 1.2 V). For example, in some implementations, this forces the error amplifier 136 to run at a duty cycle that satisfies a predefined threshold (e.g., 100% or maximum duty cycle).

[0063] According to some implementations, as represented by block 5-4b, the method 500 includes enabling the saturation limiting circuit. For example, with reference to Figure 1, the quick-start module 120 includes a saturation limiting circuit 124 provided to limit current through the inductive element 134 of the boost converter 130 to establish the output current level in response to the quick-start enable signal. According to some implementations, the current through the inductive element 134 is limited to a level that is characterized by a saturation condition of the inductive element 134. In some implementations, the saturation

limiting circuit 124 is configured to set a limit of the current flowing through the inductive element 134 to a predetermined output level (e.g., 2.5 A). For example, in some implementations, this prevents saturation of the inductive element 134.

[0064] According to some implementations, as represented by block 5-4c, the method 500 includes enabling the ripple control module. For example, with reference to Figure 1, the quick-start module 120 includes a ripple control module 136 provided to reduce current ripple in the output current level by adjustment of a switching frequency in response to the quick-start enable signal. According to some implementations, the ripple control module 134 includes an oscillator 128 that provides switching frequency that is increased in response to the quick-start enable signal. In some implementations, ripple control module 126 is configured to increase the switching frequency of an oscillator 128 above a predetermined switching frequency (e.g., from 2 MHz to 2.5 MHz). For example, in some implementations, this reduces ripple in the current flowing through the inductive element 134.

[0065] As represented by block 5-5, the method 500 includes determining whether quick-start disable conditions are satisfied. For example, with reference to Figure 1, the sensor assembly 110 is configured to turn off the quick-start enable signal in response to determining that the electrical output of the boost converter 130 (e.g., V_{OUT} 106) satisfies a fourth threshold. In some implementations, the fourth threshold is approximately 95% of a set-point output level. According to some implementations, for example, the quick-start disable conditions are satisfied when $0.95 \cdot V_{REF}$ 104 < V_{OUT} 106 or V_{IN} 102 > V_{REF} 104. For example, with reference to Figure 3, when V_{IN} 102 > V_{REF} 104 or $0.95 \cdot V_{REF}$ 104 < V_{OUT} 106, the output of the AND gate 316 is logic low (e.g., 0) and the voltage boost assembly 100 operates under regular parameters.

[0066] If the quick-start disable conditions are not satisfied, the method continues to block 5-4. If the quick-start disable conditions are satisfied, the method continues to block 5-2.

[0067] Figures 6A-6C are block diagrams of various integrated circuits (ICs) according to some implementations. While some example features are illustrated, those skilled in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed

herein. To that end, for example, Figure 6A shows that in some implementations, some or all portions of the quick-start assembly 115, which operates the voltage boost assembly 100 under quick-start parameters when quick-start conditions are satisfied, can be part of a semiconductor die 600. By way of an example, the quick-start assembly 115 can be formed on a substrate 602 of the die 600. A plurality of connection pads 604 can also be formed on the substrate 602 to facilitate functionalities associated with some or all portions of the quick-start assembly 115.

[0068] Figure 6B shows that in some implementations, a semiconductor die 600 having a substrate 602 can include some or all portions of the quick-start assembly 115 and some or all portions of the boost converter 130, which operates according to conventional boost converter techniques. A plurality of connection pads 604 can also be formed on the substrate 602 to facilitate functionalities associated with some or all portions of the quick-start assembly 115 and some or all portions of the boost converter 130.

[0069] Figure 6C shows that in some implementations, a semiconductor die 600 having a substrate 602 can include some or all portions of the quick-start assembly 115 and some or all portions of the boost converter 130, and some or all portions of the power amplifier (PA) 620. A plurality of connection pads 604 can also be formed on the substrate 602 to facilitate functionalities associated with some or all portions of the quick-start assembly 115 and some or all portions of the boost converter 130, and some or all portions of the PA 620.

[0070] In some implementations, one or more features described herein can be included in a module. Figure 7 is a schematic diagram of an implementation of a module 700 including the voltage boost assembly 100 in Figure 1 according to some implementations. While some example features are illustrated, those skilled in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. The module 700 includes a packaging substrate 752, connection pads 756, a CMOS (complementary metal-oxide semiconductor) die 600, a HBT (heterojunction bipolar transistor) die 710, a matching network 720, and one or more surface mount devices 760. In some implementations, the module 700 is at least one of a power amplifier module (PAM) or a front-end module (FEM).

[0071] The CMOS die 600 includes a substrate 602 including some or all portions of the bias circuit 200 and some or all portions of the bias circuit 610. A plurality of connection pads 604 is formed on the substrate 602 to facilitate functionalities associated with some or all portions of the quick-start assembly 115 and some or all portions of the boost converter 130. Similarly, the HBT die 710 includes a substrate 702 including some or all portions of the PA 620. The HBT die 710 also includes a plurality of connection pads 704 formed on the substrate 702 to facilitate functionalities associated with some or all portions of the PA 620.

[0072] The connection pads 756 on the packaging substrate 752 facilitate electrical connections to and from each of the CMOS die 600 and the HBT die 710. For example, the connection pads 756 facilitate the use of wirebonds 754 for passing various signals and supply currents and/or voltages to each of the CMOS die 600 and the HBT die 710.

[0073] In some implementations, the components mounted on the packaging substrate 752 or formed on or in the packaging substrate 752 can further include, for example, one or more surface mount devices (SMDs) (e.g., 760) and one or more matching networks (e.g., 720). In some implementations, the packaging substrate 752 can include a laminate substrate.

[0074] In some implementations, the module 700 can also include one or more packaging structures to, for example, provide protection and facilitate easier handling of the module 700. Such a packaging structure can include an overmold formed over the packaging substrate 752 and dimensioned to substantially encapsulate the various circuits and components thereon.

[0075] It will be understood that although the module 700 is described in the context of wirebond-based electrical connections, one or more features of the present disclosure can also be implemented in other packaging configurations, including flip-chip configurations.

[0076] Figure 8 schematically depicts an example radio-frequency (RF) device 800 having one or more advantageous features described herein. While pertinent features are shown, those of ordinary skill in the art will appreciate from the present disclosure that various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. To that end, in some implementations, the RF device 800 is a wireless device. In some implementations, such a wireless device

can include, for example, a cellular phone, a smart-phone, a hand-held wireless device with or without phone functionality, a computer, a laptop, a tablet computer, a peripheral device, a router, a repeater, a wireless access point, a base station, or the like.

[0077] In some implementations the RF device 800 includes one or more power amplifier (PAs) (e.g., the PA 620 in Figures 6C and 7) in a PA module 812 configured to receive their respective RF signals from a transceiver 810 that can be configured and operated in known manners to generate RF signals to be amplified and transmitted, and to process received signals. In some implementations, the PA module 812 can include one or more filters and/or one or more band/mode selection switches configured to provide duplexing and/or switching functionalities as described herein. According to some implementations, the PA module 812 includes the voltage boost assembly 100 described above with reference to Figures 1-3. For example, the voltage boost assembly 100 operates under quick-start parameters (e.g., the quick-start module 120 is enabled) when the quick-start enable conditions are satisfied, and the voltage boost assembly 100 operates under regular parameters (e.g., according to conventional boost converter techniques) when the quick-start enable conditions are not satisfied.

[0078] The transceiver 810 is shown to interact with a baseband sub-system 808 that is configured to provide conversion between data and/or voice signals suitable for a user and RF signals suitable for the transceiver 810. The transceiver 810 is also shown to be connected to a power management component 806 that is configured to manage power for the operation of the RF device 800. In some implementations, the power management component 806 can also control operations of the baseband sub-system 808 and other components of the RF device 800.

[0079] The baseband sub-system 808 is shown to be connected to a user interface 802 to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system 808 can also be connected to a memory 18804 that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

[0080] In some implementations, a matching network 814 is provided between the PA module 812 and the antenna switch module (ASM) 816. In some

implementations, the ASM 816 is connected to an antenna 820 and is configured to control which signals are transmitted via the antenna 820.

[0081] As shown in Figure 8, some received signals via the antenna 820 are shown to be routed from the ASM 816 to one or more low-noise amplifiers (LNAs) 824. Amplified signals from the one or more LNAs 824 are shown to be routed to the transceiver 810.

[0082] A number of other wireless device configurations can utilize one or more features described herein. For example, the RF device 800 does not need to be a multi-band device. In another example, the RF device 800 can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

[0083] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0084] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes

or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0085] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0086] While some implementations of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A voltage boost assembly comprising:
 - a boost converter having a capacitive element arranged at an output, and an inductive element connectable to an electrical supply;
 - a sensor assembly provided to generate a quick-start enable signal in response to detecting that an electrical condition relative to an electrical output of the boost converter has breached a first threshold; and
 - a quick-start module responsive to the quick-start enable signal, and configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge the capacitive element arranged at the output.
2. The voltage boost assembly of claim 1 wherein detecting that an electrical condition relative to the electrical output of the boost converter has breached the first threshold includes detecting that a reference voltage indicates demand for an electrical output that is at least 10% higher than the current electrical output of the boost converter.
3. The voltage boost assembly of claim 1 wherein detecting that an electrical condition relative to an electrical output of the boost converter has breached the first threshold includes detecting that a reference voltage indicates demand for an electrical output that is at least 20% higher than the electrical output of the boost converter.
4. The voltage boost assembly of claim 1 wherein the quick-start module includes a charging circuit provided to charge the capacitive element so that an electrical output of an associated error amplifier satisfies a third threshold in response to the quick-start enable signal.

5. The voltage boost assembly of claim 4 wherein the third threshold is characterized in relation to a high voltage level that can be sustained at the output of the error amplifier.

6. The voltage boost assembly of claim 1 wherein the quick-start module includes a saturation limiting circuit provided to limit current through the inductive element to establish the output current in response to the quick-start enable signal.

7. The voltage boost assembly of claim 6 wherein the current through the inductive element is limited to a level that is characterized by a saturation condition of the inductive element.

8. The voltage boost assembly of claim 1 wherein the quick-start module includes a ripple control module provided to reduce current ripple in the output current by adjustment of a switching frequency in response to the quick-start enable signal.

9. The voltage boost assembly of claim 8 wherein the ripple control module includes an oscillator that provides a switching frequency that is increased in response to the quick-start enable signal.

10. The voltage boost assembly of claim 1 wherein the second threshold is characterized by a current level available to charge the capacitive element.

11. The voltage boost assembly of claim 1 wherein the sensor assembly is configured to turn off the quick-start enable signal in response to determining that the electrical output of the boost converter has satisfied a fourth threshold.

12. The voltage boost assembly of claim 11 wherein the fourth threshold is approximately 95% of a set-point output level.

13. A module comprising:

a packaging substrate configured to receive a plurality of components;
a power amplifier; and

a voltage boost assembly including a boost converter having a capacitive element arranged at an output, and an inductive element connectable to an electrical supply, a sensor assembly provided to generate a quick-start enable signal in response to detecting that an electrical condition relative to an electrical output of the boost converter has breached a first threshold, and a quick-start module responsive to the quick-start enable signal, and configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge the capacitive element arranged at the output.

14. The module of claim 13 wherein the module is at least one of a power amplifier module (PAM) or a front-end module (FEM).

15. The module of claim 13 wherein the quick-start module includes a charging circuit provided to charge the capacitive element so that an electrical output of an associated error amplifier satisfies a third threshold in response to the quick-start enable signal.

16. The module of claim 13 wherein the quick-start module includes a saturation limiting circuit provided to limit current through the inductive element to establish the output current in response to the quick-start enable signal.

17. The module of claim 13 wherein the quick-start module includes a ripple control module provided to reduce current ripple in the output current level by adjustment of a switching frequency in response to the quick-start enable signal.

18. A radio frequency (RF) device comprising:
a transceiver configured to process RF signals;
a power amplifier coupled to the transceiver, the power amplifier configured to generate an amplified RF signal;
an antenna in communication with the transceiver, the antenna is configured to facilitate transmission of the amplified RF signal; and
a voltage boost assembly including a boost converter having a capacitive element arranged at an output, and an inductive element connectable to an electrical supply, a sensor assembly provided to generate a quick-start enable signal in response to detecting that an electrical condition relative to an electrical output of the boost converter has breached a first threshold, and a quick-start module responsive to the quick-start enable signal, and configured to drive the boost converter at a relatively high duty-cycle and so that the boost converter delivers an output current that satisfies a second threshold in order to charge the capacitive element arranged at the output.

19. The RF device of claim 18 wherein the RF device includes a wireless device.

20. The RF device of claim 19 wherein the wireless device includes at least one of a base station, a router, a repeater, a cellular phone, a smartphone, a computer, a laptop, a tablet computer, or a peripheral device.

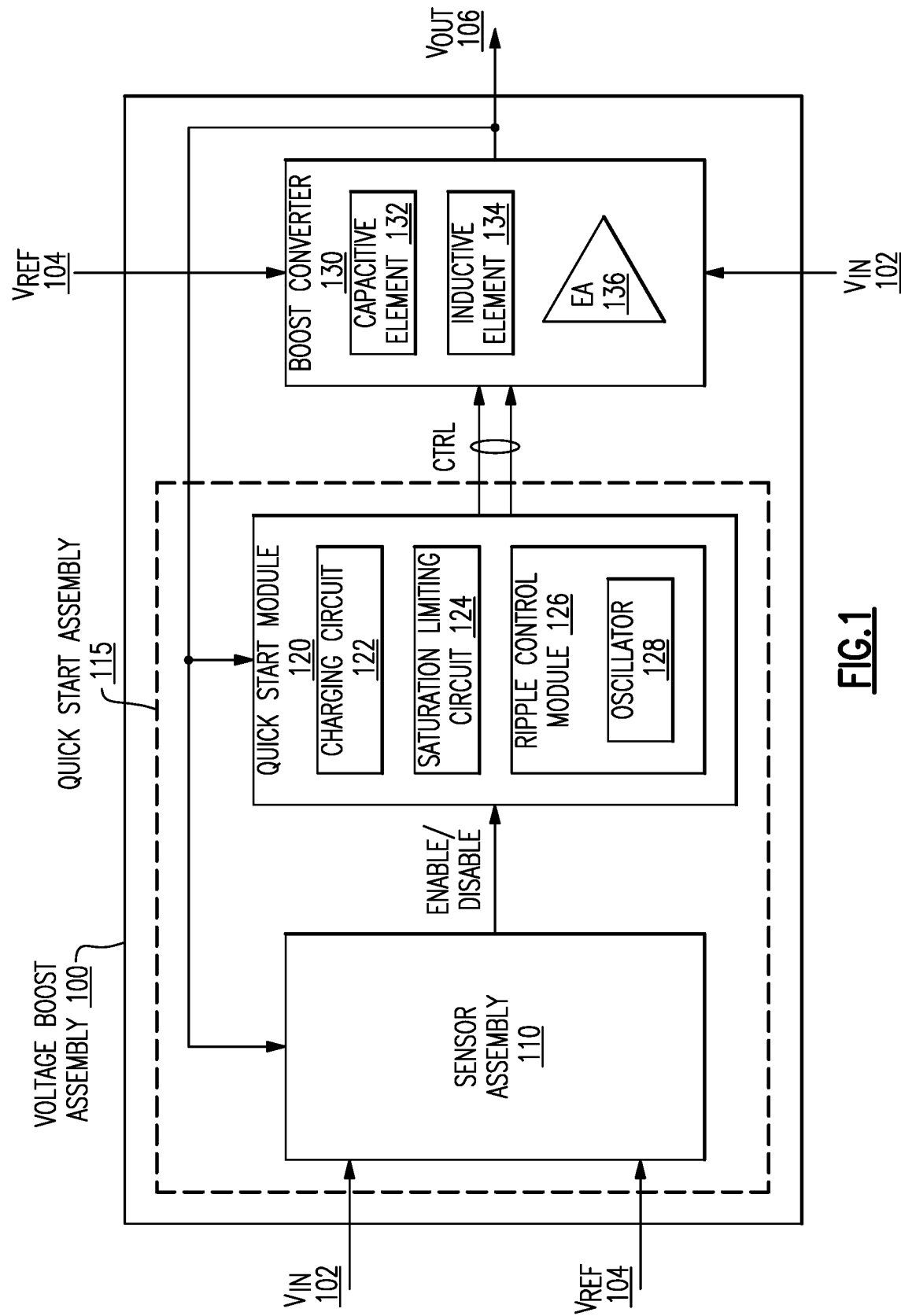


FIG.1

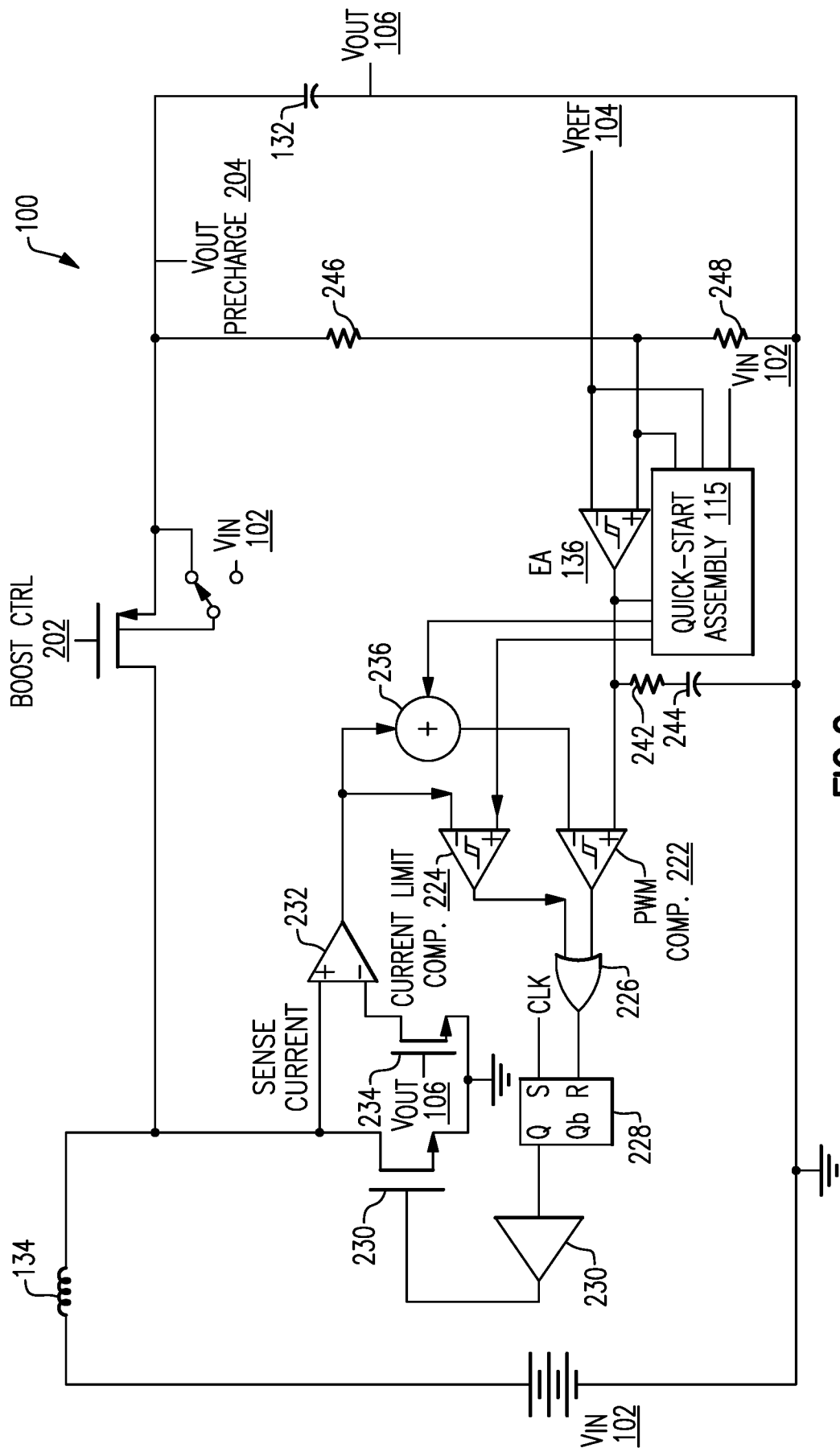


FIG. 2

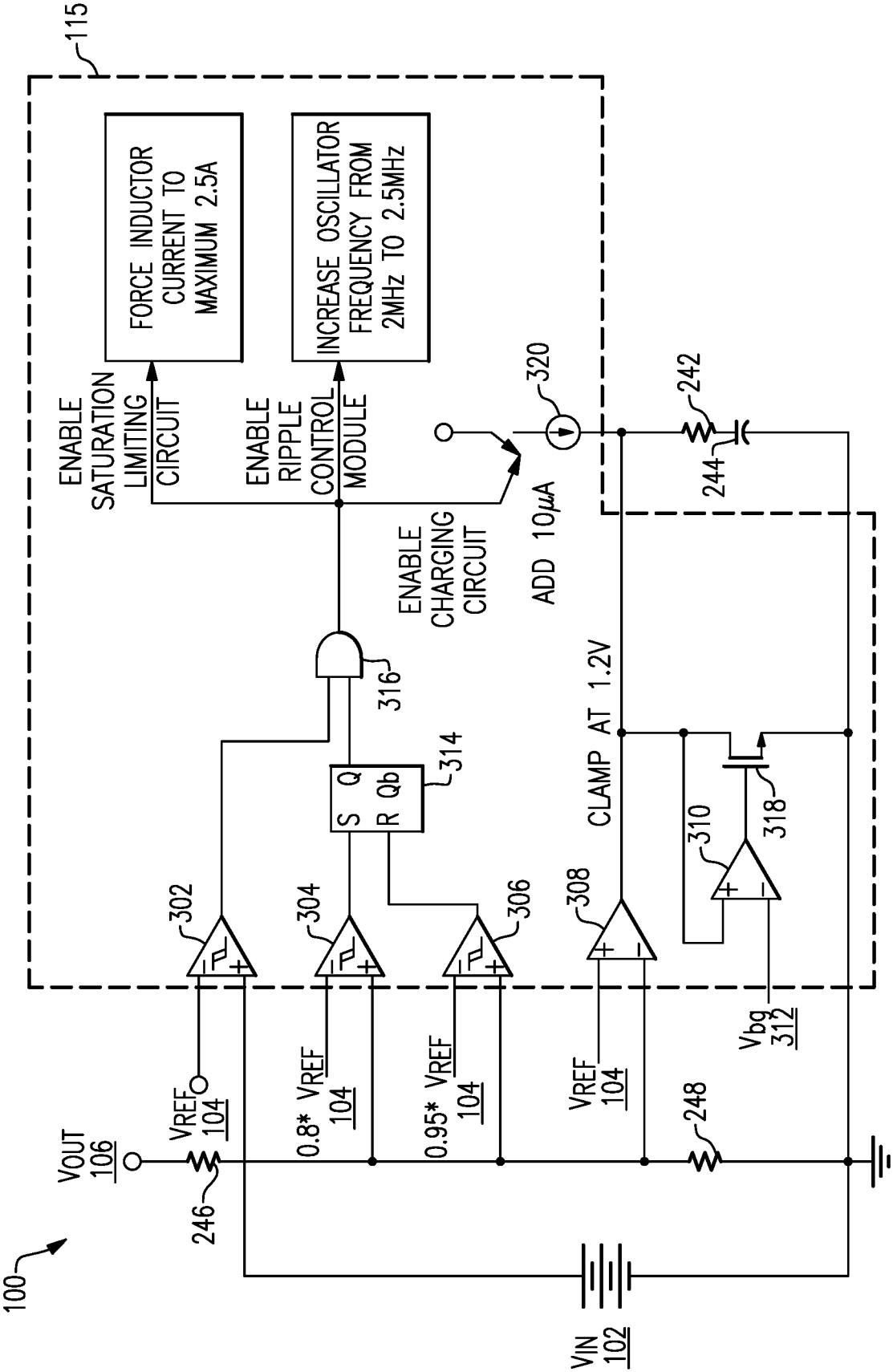


FIG.3

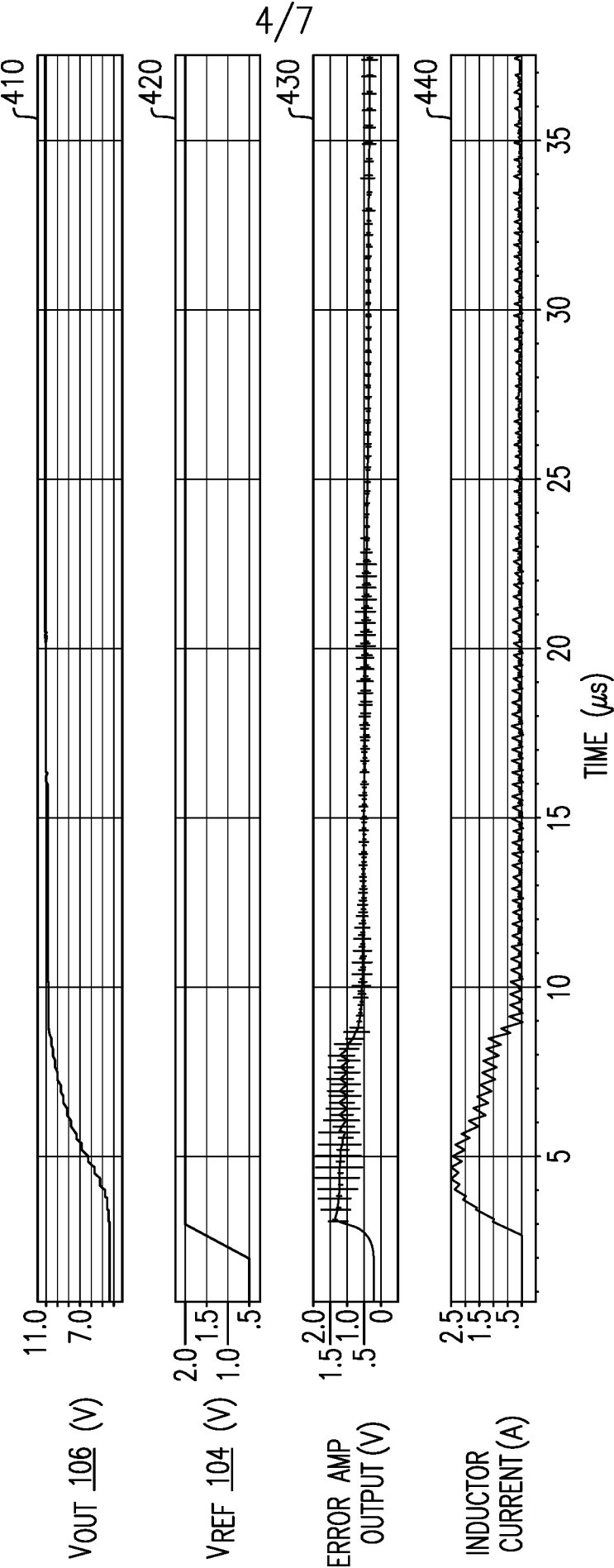
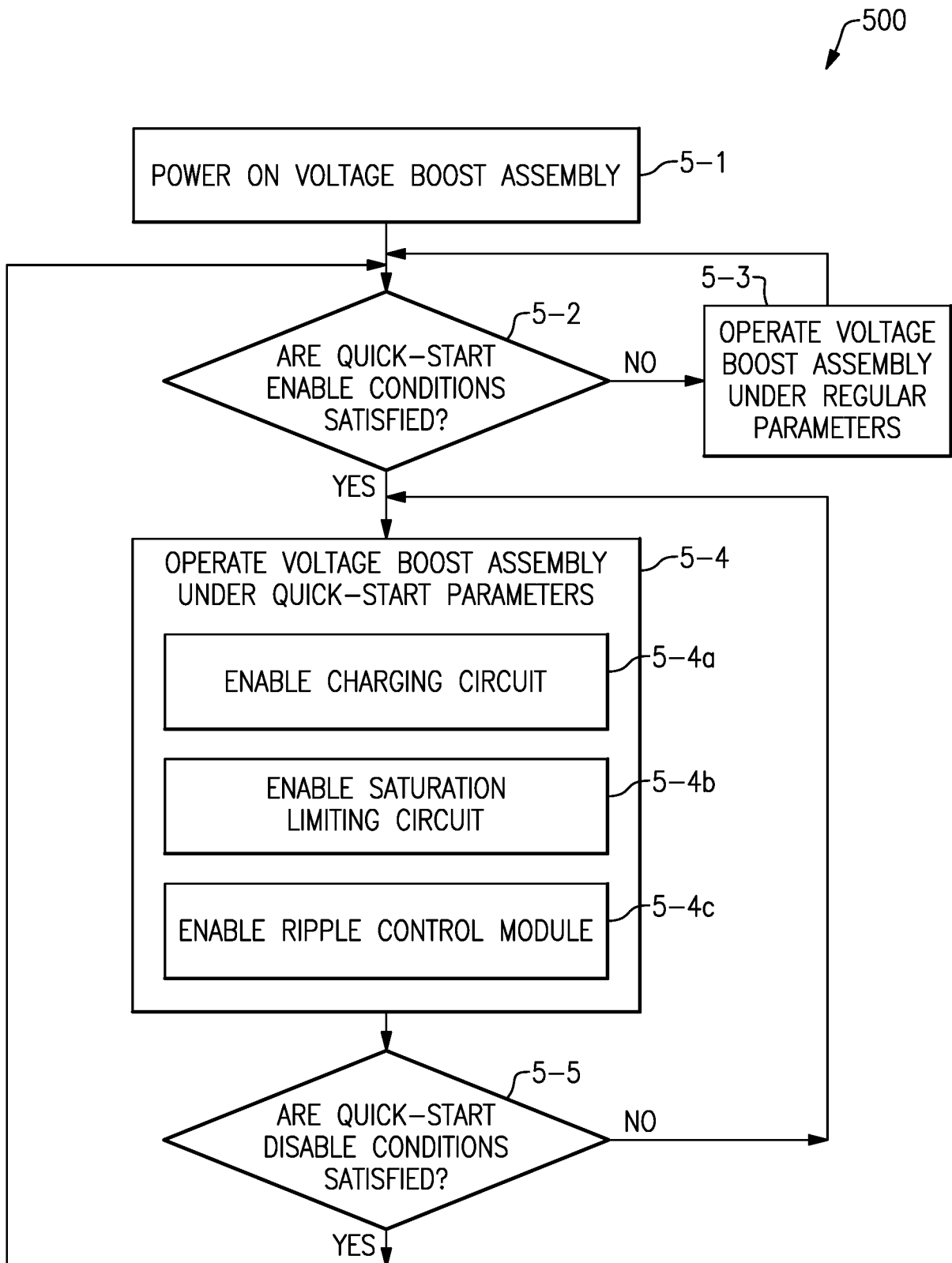
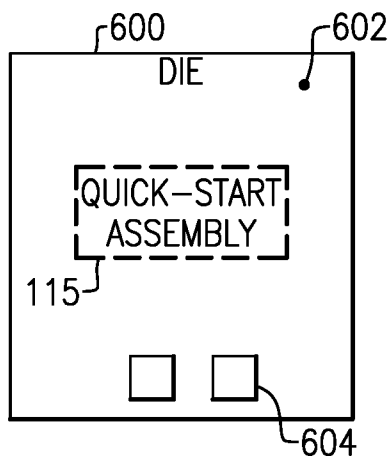
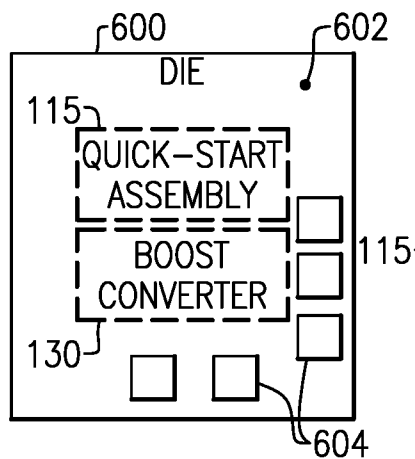
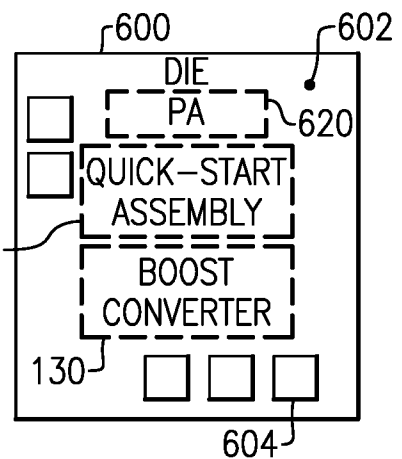
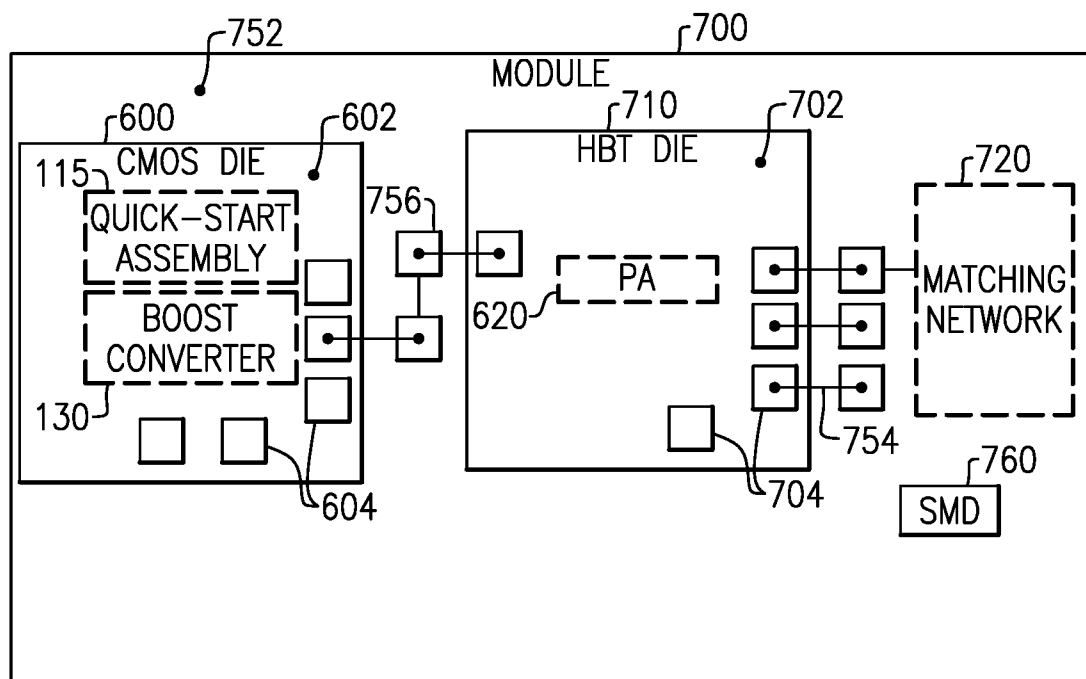


FIG. 4

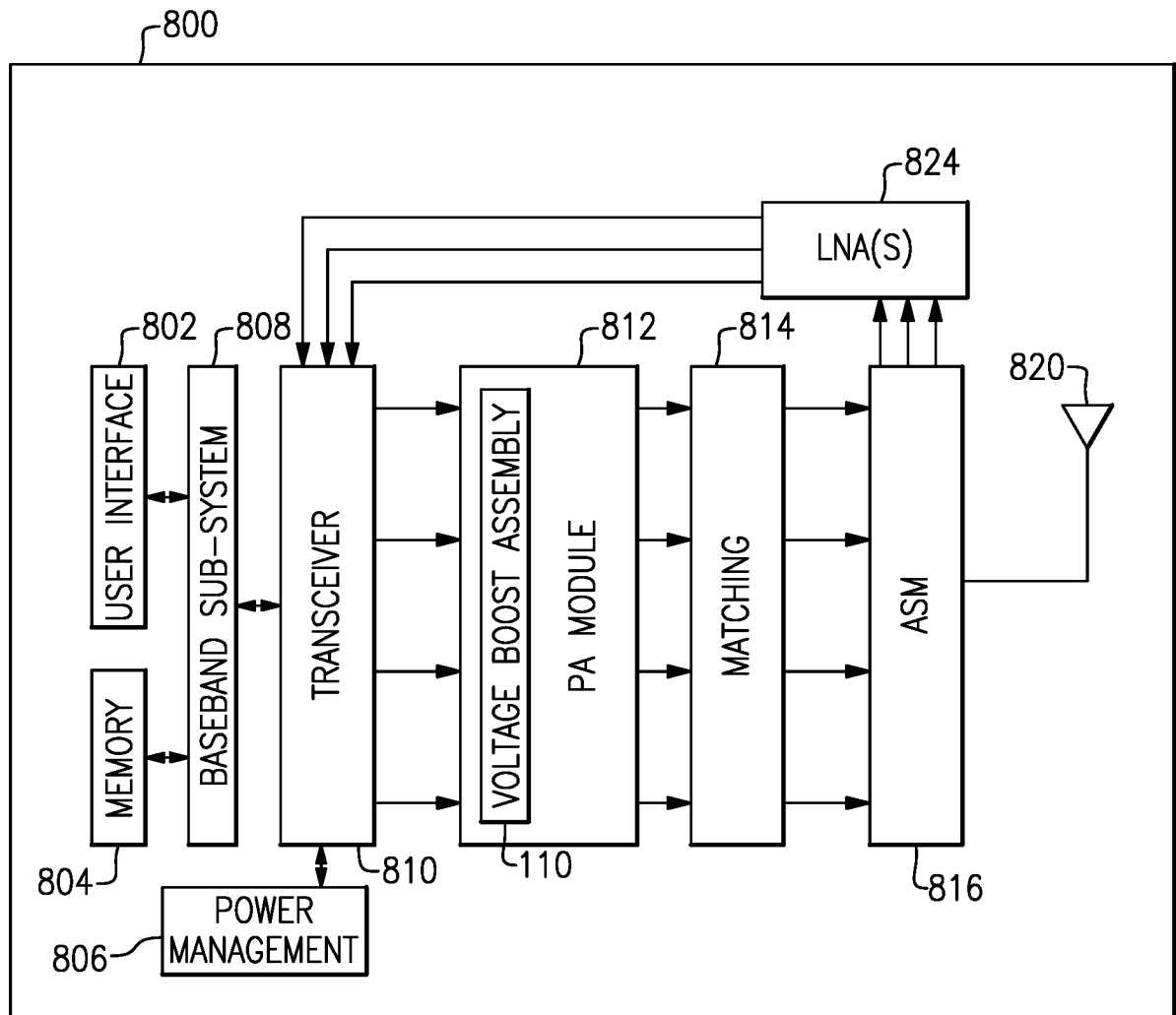
5/7

**FIG.5**

6/7

**FIG. 6A****FIG. 6B****FIG. 6C****FIG. 7**

7/7

**FIG.8**

A. CLASSIFICATION OF SUBJECT MATTER**H03F 1/02(2006.01)i, H03F 1/30(2006.01)i, H03F 3/189(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 1/02; H01Q 11/12; H03G 1/00; G08C 17/02; H03G 99/00; H04K 3/00; H03F 3/193; H03F 1/30; H03F 3/189

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: voltage boost, boost converter, sensor, quick start module, quick start enable signal, high duty-cycle

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0207770 A1 (ROBERT T. FAYFIELD et al.) 20 August 2009 See paragraphs [0009], [0028], claim 1, and figures 2-4.	1-20
A	US 2014-0210559 A1 (QUALCOMM INCORPORATED) 31 July 2014 See abstract, claim 1, and figures 2-4.	1-20
A	US 2014-0111276 A1 (QUALCOMM INCORPORATED) 24 April 2014 See claims 1-3, and figures 2, 4.	1-20
A	US 2013-0217345 A1 (SKYWORKS SOLUTIONS, INC.) 22 August 2013 See abstract, claims 1-5, and figures 5-7.	1-20
A	US 8401500 B1 (RUEDIGER BAUDER et al.) 19 March 2013 See abstract, claims 1-10, and figures 4-8.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 June 2016 (17.06.2016)

Date of mailing of the international search report

17 June 2016 (17.06.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KIM, Sung Gon

Telephone No. +82-42-481-8746



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/017913

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0207770 A1	20/08/2009	None	
US 2014-0210559 A1	31/07/2014	CN 104956588 A EP 2949041 A2 JP 2016-504892 A KR 10-2015-0110711 A US 2015-0002235 A1 US 8866547 B2 WO 2014-116608 A2	30/09/2015 02/12/2015 12/02/2016 02/10/2015 01/01/2015 21/10/2014 31/07/2014
US 2014-0111276 A1	24/04/2014	CN 104737441 A EP 2912768 A1 JP 2015-534411 A KR 10-2015-0077456 A US 8754707 B2 WO 2014-066694 A1	24/06/2015 02/09/2015 26/11/2015 07/07/2015 17/06/2014 01/05/2014
US 2013-0217345 A1	22/08/2013	CN 104185953 A HK 1199332 A1 KR 10-2014-0121868 A TW 201347400 A TW 201349739 A US 2013-0207731 A1 US 2015-0180421 A1 US 8981847 B2 US 9143096 B2 US 9294054 B2 WO 2013-119587 A1	03/12/2014 26/06/2015 16/10/2014 16/11/2013 01/12/2013 15/08/2013 25/06/2015 17/03/2015 22/09/2015 22/03/2016 15/08/2013
US 8401500 B1	19/03/2013	None	