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(54) Title: A CIRCUIT AND METHOD FOR OPERATION MODE SELECTION

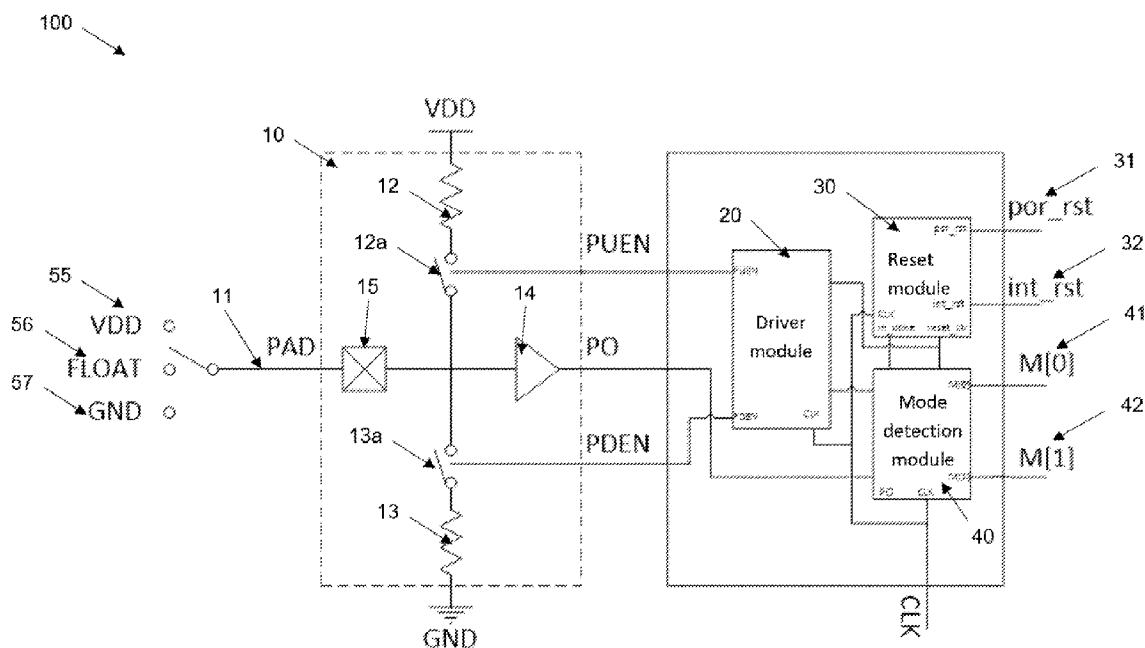


FIG. 1

(57) Abstract: The present invention relates to a circuit (100) and method for operation mode selection. The circuit (100) comprising an input pin (11) selectively coupled to a positive voltage output, VDD pin (55), a float pin (56) or a ground pin, GND pin (57), a pad pin (15), and a mode detection module (40). The mode detection module (40) is configured to capture value of power output signal and determine an operation mode selected for an operative circuit to run. The circuit (100) further comprising a voltage pull-up resistor (12) and a ground pull-down resistor (13) configured to provide the input pin (11) with pull-up enable, PUEN or pull-down enable PDEN capability by controlling the state of the input pin (11), and a driver module (20) configured to control timing and value of PUEN of the voltage pull-up resistor (12) and value of PDEN of the ground pull-down resistor (13).



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OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
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A CIRCUIT AND METHOD FOR OPERATION MODE SELECTION**FIELD OF INVENTION**

5 The present invention relates to a circuit and method for operation mode selection. More particularly, the present invention relates to a circuit and method for multiple operation modes selection using a minimum number of pin required for the mode selection.

BACKGROUND OF THE INVENTION

10 An integrated circuit also known as chip or microchip is a semiconductor wafer made of thousands or millions of tiny resistors, capacitors, and transistors. An integrated circuit may be configured to run in different modes or configurations. For example, the integrated circuit may be configured to run in different speed modes which are either low or high speed. Additionally, the integrated circuit may be
15 configured to run in different configurations such as serial parallel interface or inter-integrated circuit mode. A circuit and method for operation mode selection are used to determine which operation mode is selected for the integrated circuit to run.

An example of the circuit and method for operation mode selection is
20 disclosed in a United States Patent Publication No. 2006/0000917 A1 which relates to multi-mode integrated circuit devices and methods of operating the multi-mode integrated circuit device. One of the multi-mode integrated circuit devices includes a controller which is configured to operate in two modes, a first plurality of input/output pads associated with operations in the first mode, a second plurality of input/output
25 pads associated with operations in the second mode, and a mode detector circuit. The mode detector circuit is coupled to at least one of the second plurality of input/output pads and is configured to detect connection of the second plurality of input/output pads to the controller. If the second plurality of input/output pads are connected to the controller, the controller operates in the second mode. Otherwise,
30 the controller operates in the first mode.

Another example of the circuit and method for operation mode selection is disclosed in a PCT Patent Publication No. WO 2006/065452 A2 which relates to circuits and methods for mode selection in multiple-mode integrated circuits. In order
35 for a mode selection circuitry to select one of a plurality operational modes supported

by an integrated circuit, first, the mode selection circuitry has to detect a selected connection between an output pin of an integrated circuit and a mode control pin of the integrated circuit. The mode selection circuitry then decodes a code output from the output pin during power-up of the integrated circuit to identify the output pin from a plurality of output pins provided on the integrated circuit. Finally, the operational mode corresponding to the connection between the output pin and the mode control pin is selected.

Although there are many circuits and methods for operation mode selection, most of the circuits and methods for mode selection can only detect two modes per input pin. If the circuits and methods want to detect more than two operation modes, more input pins are required. Therefore, there is a need for a circuit and method for operation mode selection which addresses the above-mentioned problem.

SUMMARY OF INVENTION

The present invention relates to a circuit (100) and method for operation mode selection. The circuit (100) comprising an input pin (11), a pad pin (15) and a mode detection module (40). The input pin (11) is selectively coupled to a positive voltage output, VDD pin (55), a float pin (56) or a ground pin, GND pin (57). The pad pin (15) is configured to select which of the VDD pin (55), float pin (56) or GND pin (57) to be connected to the input pin (11). The mode detection module (40) is configured to capture value of power output signal and determine an operation mode selected for an operative circuit of an integrated circuit to run. The circuit (100) further comprising a voltage pull-up resistor (12), a ground pull-down resistor (13), and a driver module (20). The voltage pull-up resistor (12) and ground pull-down resistor (13) are configured to provide the input pin (11) with pull-up enable, PUEN or pull-down enable PDEN capability by controlling the state of the input pin (11), wherein the input pin (11) is either connected to the positive power supply or to the ground. The driver module (20) is configured to control timing and value of PUEN of the voltage pull-up resistor (12) and value of PDEN of the ground pull-down resistor (13).

The method for operation mode selection includes the steps of setting value of pull-up enable, PUEN to high and the value of pull-down enable, PDEN to low at the first period by a driver module (20), capturing a first value of power output, PO output signal received from an input pad (10) by a mode detection module (40), setting the

value of PUEN to low and value of PDEN to high by the driver module (20), and capturing a second value of PO signal received from the input pad (10) by the mode detection module (40). Finally, the operation mode for an operative circuit of an integrated circuit to run is determined based on a truth table, wherein the truth table
5 comprises a list of operation modes of the operative circuit configured to run and the predetermined value for each operation mode.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part
10 of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. 1 illustrates a schematic diagram of a circuit (100) for operation mode selection according to an embodiment of the present invention.

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FIG. 2 illustrates a flowchart of a method for operation mode selection according to an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

20 A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings. In the following description, well known functions or constructions are not described in detail since they would obscure the description with unnecessary detail.

25 Initial reference is made to **FIG. 1** which illustrates a schematic diagram of a circuit (100) for operation mode selection according to an embodiment of the present invention. The circuit (100) is connected to an operative circuit of an integrated circuit. Preferably, the circuit (100) may be integrated as an integrated circuit. The circuit (100) comprises an input pad (10), a driver module (20), a reset module (30), and a mode
30 detection module (40).

The input pad (10) comprises an input pin (11), a voltage pull-up resistor (12), a ground pull-down resistor (13), a buffer (14) and a pad pin (15). The input pin (11) is selectively coupled to a positive voltage output, VDD pin (55), a float pin (56) or a
35 ground pin, GND pin (57). The VDD pin (55) is connected to a positive power supply,

while the GND pin (57) is connected to the ground of the circuit (100). The float pin (56) is said to be floating, whereby the float pin (56) is not connected to any power supply or ground. The pad pin (15) which is connected to the input pin (11) is configured to select either the VDD pin (55), float pin (56) or GND pin (57) to be
5 connected to the input pin (11) based on a user selection.

The voltage pull-up resistor (12) and the ground pull-down resistor (13) are connected to the pad pin (15) in parallel. The voltage pull-up resistor (12) is connected to the positive power supply and a first switch (12a) in series, while the ground pull-down resistor (13) is connected to a second switch (13a) in series and is grounded.
10 The voltage pull-up resistor (12) and ground pull-down resistor (13) are configured to provide the input pin (11) with pull-up enable, PUEN or pull-down enable PDEN capability by controlling the state of the input pin (11). The state of the input pin (11) is controlled by connecting the input pin (11) to either the positive power supply or to the
15 ground or floating. When value of PUEN is set to high, the first switch (12a) is turned on and the input pin (11) is pulled to the positive power supply via the voltage pull-up resistor (12). On the other hand, when the value of PUEN is set to low, the first switch (12a) is turned off and the input pin (11) is disconnected from the positive power supply. When the value of PDEN is set to high, the second switch (13a) is turned on and the
20 input pin (11) is pulled to the ground. On the other hand, when the value of PDEN is set to low, the second switch (13a) is turned off and the input pin (11) is disconnected from the ground.

The buffer (14) is connected to the pad pin (15) in series. The buffer (14) is
25 configured to generate power output, PO signals based on selection made by the pad pin (15). Preferably, the PO signals has two values, wherein the two values are binary values known as a first value and a second value. The buffer (14) is further connected to the mode detection module (40) to send the PO signal to the mode detection module (40), wherein values of the PO signals are sent one after another. Preferably, the first
30 value of PO signal is sent before the second value of PO signal

The driver module (20) is connected to the voltage pull-up resistor (12) at a PUEN pin of the driver module (20) and the ground pull-down resistor (13) at a PDEN pin of the driver module (20). The driver module (20) is configured to control the timing
35 of the operation mode selection process by dividing the operation mode selection

process into a plurality of periods and ensuring each step of the mode detection process is performed within a predetermined period. The driver module (20) is also configured to control value of PUEN or PDEN to ensure correct values of PO signals are captured at a correct predetermined period by the mode detection module (40). By
5 ensuring the correct values of PO signals are captured at the correct predetermined period, the driver module (20) ensures that correct values of mode are determined, wherein the values of mode indicate the operational mode selected. If the driver module (20) sets the value of PUEN to high, the first switch (12a) is connected to the voltage pull-up resistor (12), whereas if the driver module (20) sets the value of PUEN
10 to low, the first switch (12a) is disconnected from the voltage pull-up resistor (12). If the driver module (20) sets the value of PDEN to high, the second switch (13a) is connected to the ground pull-down resistor (13), whereas if the driver module (20) sets the value of PDEN to low, the second switch (13a) is disconnected from the ground pull-down resistor (13).

15 The reset module (30) is connected to the driver module (20) and the mode detection module (40). The reset module (30) is configured to hold the logic of other modules or circuits of the integrated circuit in a reset state while the mode detection module (40) is in operation. The reset module (30) comprises a power-on-reset, POR
20 pin (31) and an internal reset, int_rst pin (32). The POR pin (31), which is constantly kept at a high state, is triggered with a low signal to activate the driver module (20) and the mode detection module (40) to start the operation mode selection. The int_rst pin (32) is kept at the high state when the mode detection module (40) is not in operation. The int_rst pin (32) is kept at the low state when the mode detection module (40) is in
25 operation to hold the logic of other modules or circuits of the integrated circuit in the reset state. For example, the logic the operative circuit of the integrated circuit is kept at the reset state, wherein during the reset state any pending errors or events are cleared from the operative circuit. Once the selected mode is determined by the mode detection module (40), the state of the int_rst pin (32) returns to the high state.

30 The mode detection module (40) is configured to capture the values of PO signals and determine an operation mode selected for the operative circuit to run. The values of PO signals which determine the value of mode for each operation mode are suitably pre-determined, while the selected operation mode is determined by
35 comparing the captured values of PO signals with a predetermined value in a truth

table. The truth table comprises a list of operation modes which the operative circuit may be configured to run. The truth table also comprises the predetermined values of mode for each operation mode. The values of mode which indicate the selected operation mode is sent to the operative circuit via two output mode pins (41, 42) in the form of output signals. For each operation mode, there are two values of mode. For first output mode, M[0] pin (41) sends first value of mode, while second output mode, M[1] pin (42) sends second value of mode. Preferably, the two output mode pins (41, 42) send the values of mode simultaneously.

Reference is now made to **FIG. 2** which illustrates a flowchart of a method for operation mode selection according to an embodiment of the present invention. Initially, the pad pin (15) selects either the VDD pin (55), float pin (56) or GND pin (57) to be connected to the input pin (11) based on the user selection. Once the input pin (11) is connected to either VDD pin (55), float pin (56) or GND pin (57), the buffer (14) generates the PO signals based on the pin that is connected to the input pin (11).

Thereon, the reset module (30) detects de-assertion of POR pin (31) and activates the driver module (20) and the mode detection module (40) for mode selection as in step 1100. Simultaneously, the int_rst pin (32) is kept at a low state and consequently, the reset module (30) keeps logics of other module or circuit of the integrated circuit in the reset state. For example, the logic the operative circuit of the integrated circuit is kept at the reset state, wherein during the reset state any pending errors or events are cleared from the operative circuit.

Typically, the driver module (20) divides the operation mode selection into multiple periods. During the first period, the driver module (20) sets the value of PUEN to high and the value of PDEN to low as in step 1200. As the PUEN value is set to high, the first switch (12a) is connected to the voltage pull-up resistor (12) and causes the power supply to flow through the voltage pull-up resistor (12). Simultaneously, as the PDEN value is set to low, the second switch (13a) is disconnected from the ground pull-down resistor (13) and cuts off the power supply from flowing through the ground pull-down resistor (13). The mode detection module (40) then captures and stores the first value of PO signal received from the buffer (14) as in step 1300.

During the second period, the driver module (20) sets the value of PUEN to low and value of PDEN to high as in step 1400. As the PUEN value is set to low, the first switch (12a) is disconnected from the voltage pull-up resistor (12) and cuts off the power supply from flowing through the voltage pull-up resistor (12). Concurrently, as the PDEN value is set to high, the second switch (13a) is connected to the ground pull-down resistor (13) and. The mode detection module (40) captures and stores the second value of PO signal received from the buffer (14) as in step 1500.

The mode detection module (40) then determines the operation mode selected for the operative circuit to run based on a truth table during the third period as in step 1600. The mode detection module (40) compares the captured values of PO signals with the predetermined value of the truth table. The captured values of PO signals include a combination of the first value of PO signal and the second value of the PO signal.

Table 1 illustrates an example of the truth table used to determine the selected operation mode. As shown in **Table 1**, if the input pin (11) is connected to the GND pin (57), the first and second values of the PO signals are (0,0). Therefore, based on **Table 1**, the operation mode selected is mode 0. Another example is when the input pin (11) is connected to the VDD pin (55). The first and second values PO signals are (1,1). Hence, the operation mode selected is mode 1. When the input pin (11) is said to be floating, whereby the input pin (11) is connected to the float pin (56) which is not connected to any power supply or ground, the first and second values of PO signals are (1,0). Thus, the operation mode selected is mode 2.

25

Table 1

time	PAD	PUEN	PDEN	PO	Mode = (M[0],M[1])
t1	GND	1	0	0	
t2	GND	0	1	0	Mode = 0 , (0,0)
t1	VDD	1	0	1	
t2	VDD	0	1	1	Mode = 1 , (1,1)
t1	Float	1	0	1	
t2	Float	0	1	0	Mode = 2 , (1,0)

Once the selected operation mode is determined, the output mode pins (41, 42) send the values of mode to the operative circuit in the form of output signals as in step 1700. The M[0] pin (41) sends the first value of mode while the M[1] pin (42) sends the second value of mode. Referring to the previous example in **Table 1**, if the selected operation mode is mode 0, both M[0] pin (41) and M[1] pin (42) send low output signals to the operative circuit. If the selected operation mode is mode 1, both M[0] pin (41) and M[1] pin (42) send high output signals to the operative circuit. If the selected operation mode is mode 2, the M[0] pin (41) sends a high output signal while the M[1] pin (42) sends a low output signal.

Finally, the reset module (30) de-activates the driver module (20) and mode detection module (40) as in step 1800. Simultaneously, the int-rst pin (31) returns to the high state and consequently, the reset module (30) triggers other logic of the integrated circuit out of the reset state.

While embodiments of the invention have been illustrated and described, it is not intended that these embodiments illustrate and describe all possible forms of the invention. Rather, the words used in the specifications are words of description rather

than limitation and various changes may be made without departing from the scope of the invention.

CLAIMS

1. A circuit (100) for operation mode selection comprising:
 - a) an input pin (11) selectively coupled to a positive voltage output, VDD pin (55), a float pin (56) or a ground pin, GND pin (57);
 - 5 b) a pad pin (15) configured to select which of the VDD pin (55), float pin (56) or GND pin (57) to be connected to the input pin (11); and
 - c) a mode detection module (40) configured to capture value of power output signal and determine an operation mode selected for an operative circuit of an integrated circuit to run;
- 10 characterised in that the circuit (100) further comprising:
 - d) a voltage pull-up resistor (12) configured to provide the input pin (11) with pull-up enable, PUEN capability by controlling the state of the input pin (11), wherein the input pin (11) is selectively connected to a positive power supply;
 - 15 e) a ground pull-down resistor (13) configured to provide the input pin (11) with pull-down enable PDEN capability by controlling the state of the input pin (11), wherein the input pin (11) is selectively connected to a ground; and
 - 20 f) a driver module (20) configured to control timing and value of PUEN of the voltage pull-up resistor (12) and value of PDEN of the ground pull-down resistor (13).
2. The circuit (100) as claimed in claim 1, wherein the circuit (100) further comprising a buffer (14) configured to generate power output signals based on
25 either VDD pin (55), float pin (56) or GND pin (57) is connected to the input pin (11).
3. The circuit (100) as claimed in claim 1, wherein the circuit (100) further comprising a reset module (30) configured to hold logic of other modules or
30 circuits of the integrated circuit in a reset state while the mode detection module (40) is in operation.
4. The circuit (100) as claimed in claim 3 wherein the reset module (30) comprises:

- a) a power-on-reset pin (31) that is consistently kept at a high state configured to activate the driver module (20) and the mode detection module (40) to start the operation mode selection, wherein the power-on-reset pin (31) is triggered with a low signal; and
- 5 b) an internal reset pin (32) that is kept at a low state while the mode detection module (40) is in operation to hold logic of other modules or circuits of the integrated circuit in a reset state.
5. The circuit (100) as claimed in claim 1, wherein the voltage pull-up resistor (12)
- 10 is connected to a first switch (12a) and the positive power supply in series, wherein the first switch (12a) is turned on when the value of PUEN is set to high and is turned off when the value of PUEN is set to low.
6. The circuit (100) as claimed in claim 1, wherein the ground pull-down resistor (13)
- 15 (13) is connected to a second switch (13a) and the ground in series, wherein the second switch (13a) is turned on when the value of PDEN is set to high and is turned off when the value of PDEN is set to low.
7. A method for operation mode selection is characterised by the steps of:
- 20 a) setting value of pull-up enable, PUEN to high and the value of pull-down enable, PDEN to low at a first period by a driver module (20);
- b) capturing a first value of power output, PO signal received from an input pad (10) by a mode detection module (40);
- c) setting the value of PUEN to low and value of PDEN to high at a second
- 25 period by the driver module (20);
- d) capturing a second value of PO signal received from the input pad (10) by the mode detection module (40); and
- e) determining an operation mode selected for an operative circuit of an integrated circuit to run based on a truth table, wherein the truth table
- 30 comprises a list of operation modes of the operative circuit configured to run and the predetermined value for each operation mode.
8. The method as claimed in claim 7, wherein the step of setting value of pull-up enable, PUEN to high and the value of pull-down enable, PDEN to low at the
- 35 first period by a driver module (20) is done once a reset module (30) detects de-assertion of a power-on-reset pin (31).

9. The method as claimed in claim **8**, wherein the step of detecting de-assertion of power-on-reset pin **(31)** includes the step of keeping an internal reset pin **(32)** at a low state to keep other logics of the integrated circuit in a reset state.
- 5
10. The method as claimed in claim **7**, wherein the method further includes the steps of:
- 10
- a) sending values of mode to an operative circuit in the form of output signals, wherein the values of mode indicate the operational mode selected;
 - b) de-activating the driver module **(20)** and the mode detection module **(40)**; and
 - c) triggering other logic of the integrated circuit out of a reset state by returning an internal reset pin **(32)** to a high state.
- 15

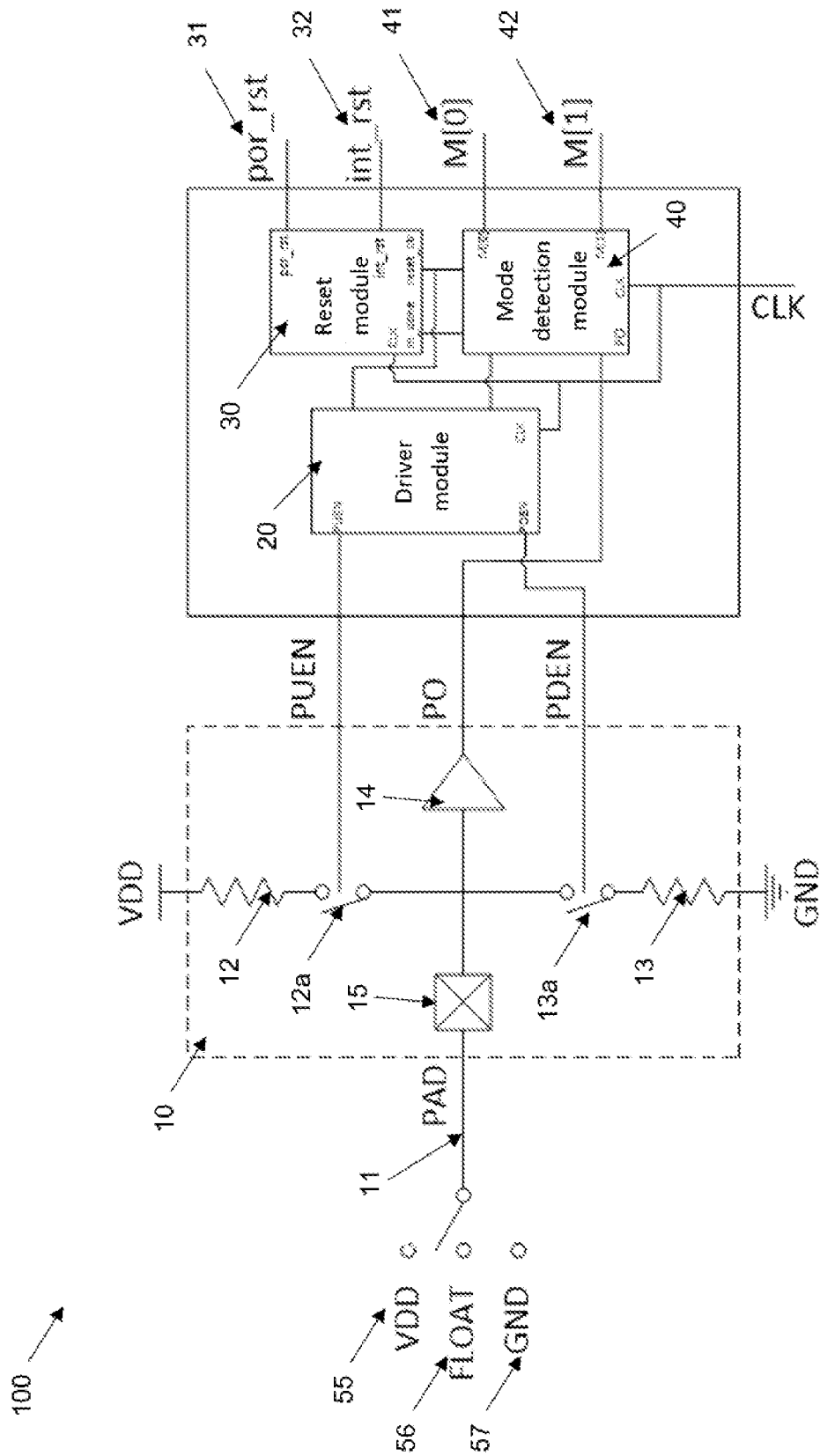


FIG. 1

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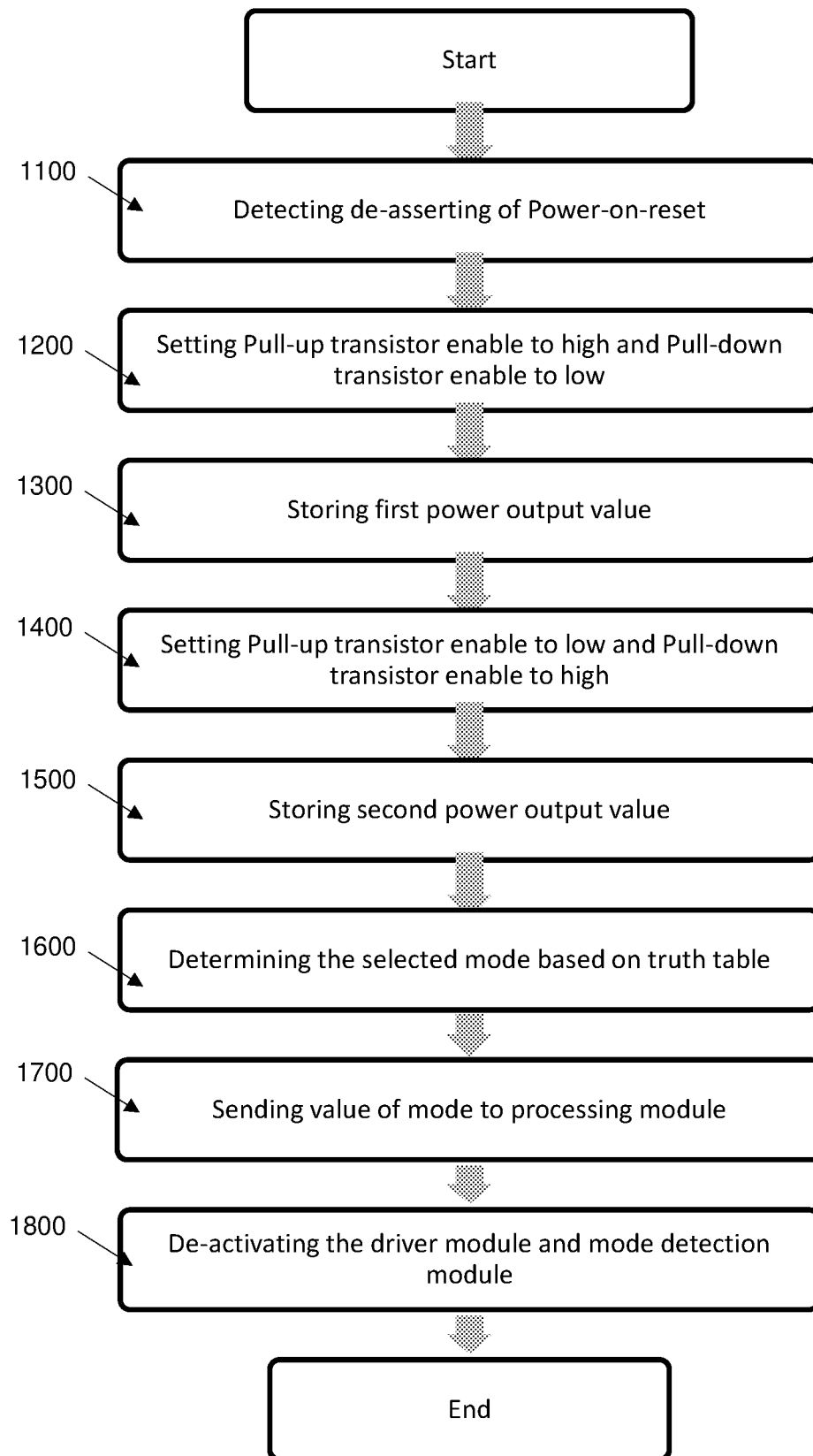


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2019/050038**A. CLASSIFICATION OF SUBJECT MATTER****G06F 1/22(2006.01)i, G06F 1/26(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/22; G01R 31/28; G06F 003/00; H02J 1/00; H03M 7/00; G06F 1/26

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: operation mode selection, pin, mode detection module, register

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006-0125661 A1 (KARTIK NANDA et al.) 15 June 2006 paragraphs [0019], [0025]; claims 1, 4, 13; and figures 1-3	1-10
A	US 8024630 B2 (JIA-QING HAN) 20 September 2011 column 1, line 46 - column 2, line 58; and figures 1-2	1-10
A	US 2011-0018522 A1 (CHIH-HUNG LI et al.) 27 January 2011 paragraphs [0018]-[0022]; and figure 1	1-10
A	US 2004-0107303 A1 (DANIEL MULLIGAN) 03 June 2004 paragraphs [0045]-[0052]; and figures 4-6	1-10



Further documents are listed in the continuation of Box C.



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17 December 2019 (17.12.2019)

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INTERNATIONAL SEARCH REPORT

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