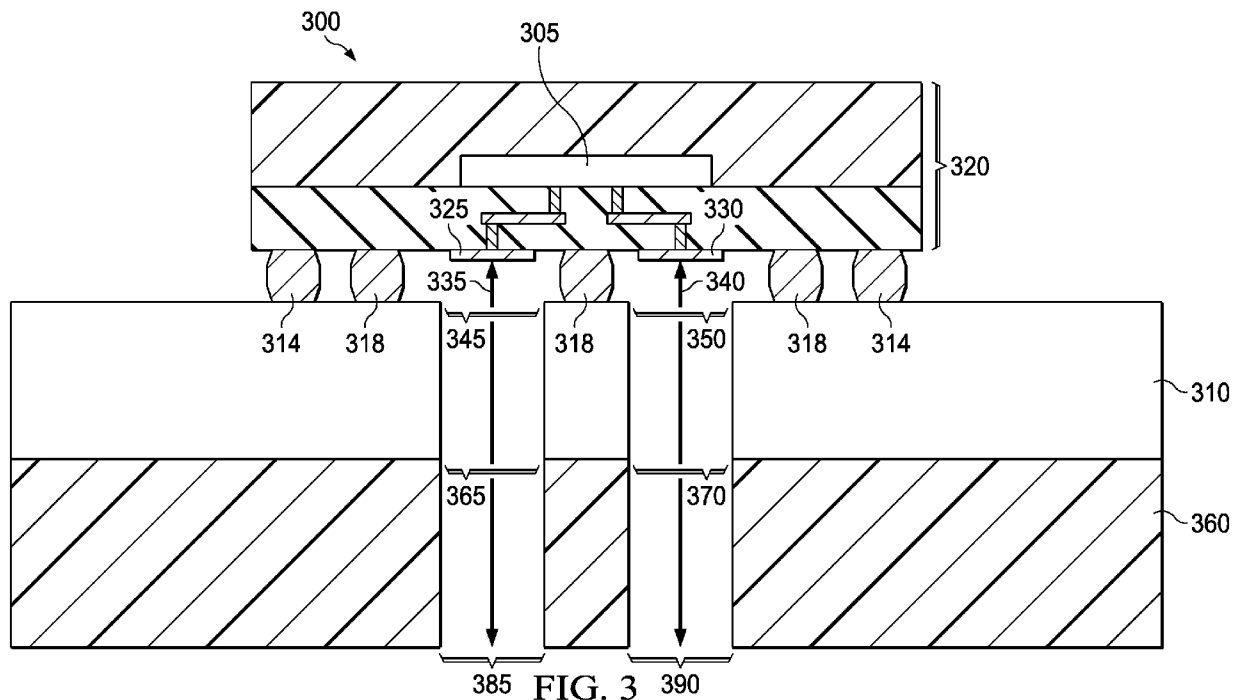




- (51) International Patent Classification:  
H01Q 21/00 (2006.01) H01L 23/498 (2006.01)  
G01S 7/03 (2006.01)
- (21) International Application Number:  
PCT/US2020/032312
- (22) International Filing Date:  
11 May 2020 (11.05.2020)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
62/847,422 14 May 2019 (14.05.2019) US  
16/853,814 21 April 2020 (21.04.2020) US
- (71) Applicant: TEXAS INSTRUMENTS INCORPORATED [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).
- (71) Applicant (for JP only): TEXAS INSTRUMENTS JAPAN LIMITED [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, 160-8366 (JP).
- (72) Inventors: MOALLEM, Meyam; 6821 Saddletree Trail, Plano, TX 75023 (US). GINSBURG, Brian, P.; 910 Wyncham Way, Allen, TX 75013 (US).
- (74) Agent: ABRAHAM, Ebby et al.; Texas Instruments Incorporated, P.o.box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,

(54) Title: GROUNDED BGA WAVE-GUIDING INTERFACE



(57) Abstract: A device comprises a package substrate (320) and a ball grid array (BGA) (314, 318). The package substrate encapsulates an integrated circuit (IC) die (305) and comprises a signal launch (325) configured to emit or receive a signal on a surface of the package substrate. The BGA is affixed to the surface and comprises a set of grounded solder balls (318) arranged as a boundary around the signal launch. The device may further comprise a printed circuit board (PCB) substrate (310) having a waveguide interface side opposite a secondary waveguide side and a through-hole cavity that extends from the waveguide interface side to the secondary waveguide side, perpendicular to a plane of the PCB substrate. The BGA couples the package substrate to the waveguide interface side such that the surface of the package substrate faces the through-hole cavity and the signal launch and through-hole cavity are substantially aligned.



WO 2020/231905 A1

DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

**(84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

**Published:**

- *with international search report (Art. 21(3))*

## GROUNDING BGA WAVE-GUIDING INTERFACE

### BACKGROUND

**[0001]** High frequency integrated circuits (ICs) generate millimeter wave signals such as those used for automotive radar, from approximately 76 GigaHertz (GHz) to 81 GHz. In conventional IC packaging, these signals are transitioned to planar transmission lines on a printed circuit board (PCB), for example through a ball grid array (BGA). Planar transmission lines carry the signal from one location on the PCB to another, such as from a signal ball pad to an external waveguide launch. The external waveguide can be used to feed a three-dimensional (3D) antenna. However, routing high frequency signals through planar transmission lines increases the complexity and cost of manufacturing the PCB and often results in signal power loss. Some ICs use a direct interface between the packaged device and external waveguides, rather than planar transmission lines. However, direct interfaces must have low coupling losses and high isolation between signal channels and be robust to manufacturing and assembly tolerances.

### SUMMARY

**[0002]** An example device includes a package substrate and a BGA. The package substrate encapsulates an IC die and comprises a signal launch on the surface of the package substrate that is configured to emit or receive a signal. The BGA is affixed to the surface of the package substrate and comprises a set of grounded solder balls arranged as a boundary around the signal launch on the surface of the package substrate. Some implementations also include a PCB substrate having a waveguide interface side, a secondary waveguide side opposite the waveguide interface side, and a through-hole cavity perpendicular to a plane of the PCB substrate and extending from the waveguide interface side to the secondary waveguide side. The BGA couples the package substrate to the waveguide interface side such that the surface of the package substrate faces the through-hole cavity and such that the signal launch and the through-hole cavity are substantially aligned.

**[0003]** In some examples, the set of grounded solder balls forms a wave-guiding interface between the signal launch and the through-hole cavity. In some implementations, the device further comprises an external waveguide coupled to the secondary waveguide side of the PCB substrate

such that the external waveguide and the through-hole cavity are substantially aligned. The external waveguide is included in a 3D antenna in some implementations. The set of grounded solder balls is arranged as a circular boundary around the signal launch and the through-hole cavity in some examples, and arranged as a rectangular boundary in other examples.

**[0004]** In some implementations, the signal launch is a first signal launch configured to emit or receive a first signal, and the set of grounded solder balls comprises a first set of grounded solder balls arranged as a boundary around the first signal launch. The package substrate further comprises a second signal launch on the surface of the package substrate that is configured to emit or receive a second signal, and the BGA further comprises a second set of grounded solder balls arranged as a boundary around the second signal launch on the surface of the package substrate. The first and second sets of grounded solder balls have at least one grounded solder ball in common in some examples, and none in common in other examples. The first and second sets of grounded solder balls are arranged such that the first and second signals are isolated from each other by a threshold amount in some implementations.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0005]** For a detailed description of various examples, reference will now be made to the accompanying drawings in which:

**[0006]** FIG. 1 illustrates a direct interface between a packaged radar device, a waveguide, and a 3D antenna.

**[0007]** FIG. 2 illustrates another direct interface between a packaged radar device, a waveguide, and a 3D antenna.

**[0008]** FIG. 3 illustrates an example direct interface between a packaged radar device and a 3D antenna through a waveguide interface and printed circuit board through-holes.

**[0009]** FIGS. 4A-D illustrate angled and side views of an example signal launch included in an IC chip package configured to interface with a 3D antenna directly, as well as a simulation plot of a signal through the direct interface and a plot illustrating insertion loss and return loss for the direct interface.

**[0010]** FIGS. 5A-C illustrate side views of example direct interfaces between a packaged radar device and a 3D antenna with variations in grounded solder ball height, as well as a plot illustrating insertion loss and return loss for differing grounded solder ball heights.

**[0011]** FIGS. 6A-B illustrate example layouts of packaged radar devices and grounded solder

balls.

#### DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0012]** The disclosed IC chips provide an interface to external waveguides that is robust to manufacturing and assembly tolerances and offer high isolation and low insertion losses. The disclosed IC chips include a radar device with a waveguide interface comprising an integrated signal launch on the package encapsulating the IC chip and grounded solder balls arranged as a fence around the signal launch on the surface of the package. The grounded solder balls isolate the signal launch and its received or transmitted signals from adjacent signal channels and improve insertion loss between the signal launch and external waveguides to which the IC chip can be coupled. The grounded solder balls can be included in a BGA affixed to the package encapsulating the radar device.

**[0013]** In some examples, the disclosed devices include a PCB substrate having first and second surfaces opposite each other and a substrate waveguide between the first and second surface, substantially orthogonal to the plane of the PCB substrate. The grounded solder balls couple the package encapsulating the radar device to the first surface of the PCB substrate such that the surface of the package faces the first surface and such that the signal launch and the substrate waveguide are substantially aligned. An external waveguide or an external antenna having a waveguide opening can be coupled to the second surface of the PCB substrate. The waveguide interface, the substrate waveguide, and the external waveguide or waveguide opening form a signal channel between the signal launch and the external antenna.

**[0014]** FIG. 1 illustrates a direct interface between a packaged radar device and a 3D antenna with waveguide feeds. The package-to-waveguide interface 100 includes a packaged radar device 120 coupled to a PCB substrate 110 by an array of solder balls 115, and a 3D antenna 160 with waveguide feeds. The 3D antenna 160 is placed on PCB substrate 110 over and around packaged radar device 120, separated from packaged radar device 120 by a gap 150. The packaged radar device 120 includes an IC die 105 and signal launches 125 and 130, which emit and/or receive signals to and from 3D antenna 160. Waveguide openings 185 and 190 reroute, fan out, split, and the like to other parts of 3D antenna 160 based on the particular antenna design. The rerouting, fanning out, splitting, and the like are not shown here, and do not impact the interface between waveguide openings 165 and 170 and signal launches 125 and 130 on packaged radar device 120. Only the waveguide openings 185 and 190 of 3D antenna 160 are shown here; other portions of 3D

antenna 160 are omitted for ease of explanation.

**[0015]** Signal launch 125 emits signals to and/or receives signals from waveguide opening 185 in 3D antenna 160 through signal channel 135. The signal channel 135 is made up of gap 150 and waveguide opening 165. Signal launch 130 emits signals to and/or receives signals from waveguide opening 190 in 3D antenna 160 through signal channel 140. The signal channel 140 is made up of gap 150 and waveguide opening 170. The width of gap 150 varies due to manufacturing and assembly tolerances, for example due to changes in the height of the solder balls 115 in the BGA coupling the packaged radar device 120 to PCB substrate 110.

**[0016]** Variations in the width of gap 150 can have significant effects on the performance of the package-to-waveguide interface 100. Isolation between adjacent signal launches 125 and 130 decreases as the width of gap 150 increases, causing a signal from one signal launch to leak from its signal channel to another signal channel and interfere with signals through adjacent signal channels. Similarly, the insertion loss for the signal channels increases as the width of gap 150 increases, degrading signal integrity through the signal channels.

**[0017]** FIG. 2 illustrates another direct interface between a packaged radar device and a 3D antenna with waveguide feeds. The package-to-waveguide interface 200 is similar to package-to-waveguide interface 100 shown in FIG. 1, but 3D antenna 260 is separated from packaged radar device 220 by interposers 248A-C. During manufacturing, a layer of the interposing material is glued to packaged radar device 220, and both the glue and the interposing material are selectively removed from over antenna launches 225 and 230. The resulting sections of glue 244A-C and interposers 248A-C are separated from 3D antenna 260 by a gap 250.

**[0018]** Although the interposers 248A-C reduce the impact of variability on performance somewhat, the width of gap 250 can still vary enough to affect the performance of PCB 200, specifically the isolation between signal channels 235 and 240 and insertion losses for each signal channel. The additional manufacturing steps to glue the interposing material to the packaged radar device 220 and selectively remove the glue and interposing material over antenna launches 225 and 230 as well as the complex assembly to align antenna launches 225 and 230, interposers 248A-C, and waveguide openings 265 and 270 increase the manufacturing cost for package-to-waveguide interface 200.

**[0019]** FIG. 3 illustrates an example direct interface between a packaged radar device and a 3D antenna through a waveguide interface and PCB through-holes. Package-to-waveguide interface

300 includes a packaged radar device 320 coupled to a waveguide interface side of a PCB substrate 310 by an array of solder balls 314 and 318. A 3D antenna 360 is coupled to the opposite, secondary waveguide side of PCB substrate 310 from the packaged radar device 320. There are no gaps between packaged radar device 320, PCB substrate 310, and 3D antenna 360. Waveguide openings 385 and 390 reroute, fan out, split, and the like to other parts of 3D antenna 360 based on the particular antenna design. The rerouting, fanning out, splitting, and the like are not shown here, and do not impact the interface between waveguide openings 365 and 370 and signal launches 325 and 330 on packaged radar device 320. Only the waveguide openings 385 and 390 of 3D antenna 360 are shown here; other portions of 3D antenna 360 are omitted for ease of explanation.

**[0020]** Packaged radar device 320 includes an IC die 305 and signal launches 325 and 330. As used herein, the package encapsulating IC die 305 includes a package substrate on which the IC die 305 is mounted. In the case of top-mounted flip chip BGA packaging, the IC die 305 is mounted on top of the package substrate and a mold compound covers the top and side of the IC die 305 and a portion of the package substrate. The mold compound may be a plastic, ceramic, resin, or other appropriate material for encapsulating the IC die 305. In the case of under-mounted flip chip BGA packaging, shown in FIGS. 1 and 2, the IC die 305 is mounted on the bottom side of the package substrate, the same side as the BGA, and is left exposed; no mold compound is used.

**[0021]** Signal launch 325 is substantially aligned with the waveguide opening 385 of 3D antenna 360 and emits and/or receives signals through signal channel 335. The signal channel 335 is made up of solder balls 318, PCB through-hole 345, and waveguide opening 365 in 3D antenna 360. Signal launch 330 is substantially aligned with the waveguide opening 390 of 3D antenna 360 and emits and/or receives signals through signal channel 340. The signal channel 340 is made up of solder balls 318, PCB through-hole 350, and waveguide opening 370 in 3D antenna 360. The BGA package for radar device 320 includes open spaces over antenna launches 325 and 330, without solder balls. Solder balls 318 around antenna launches 325 and 330 are grounded and act as a wave-guiding structure between the signal launches 325 and 330 and the PCB through-holes 345 and 350.

**[0022]** The wave-guiding structures comprising solder balls 318 isolate signal channels 335 and 340 from each other and other adjacent signal channels and improve impedance matching between signal launches 325 and 330 and 3D antenna 360. Solder balls 318 also decrease insertion loss between signal launches 325 and 330 and waveguide openings 385 and 390 of 3D antenna 360.

Because solder balls 318 act as a wave guiding structure between packaged radar device 320 and PCB substrate 310, which is directly connected to the waveguide feeds of 3D antenna 360, the performance of package-to-waveguide interface 300 does not vary significantly based on the width of a gap between the packaged radar device 320 and 3D antenna 360. PCB 300 also does not include additional components like interposers 248A-C and can be made without additional manufacturing steps such as gluing on an interposing material and selectively removing the glue and interposing materials over the antenna launches.

**[0023]** FIGS. 4A-D illustrate angled top and side views of an example signal launch included in an integrated circuit (IC) chip package configured to interface with a 3D antenna directly, as well as a simulation plot of a signal through the direct interface and a plot illustrating insertion loss and return loss for the direct interface. FIG. 4A illustrates an angled top view of the example IC package 400, which includes an “E” shaped signal launch 425. A signal trace 440 carries a signal to signal launch 425. Grounded vias 430 create a substrate-integrated cavity around the launch which improves isolation between signal launch 425 and other launches and components on the IC package 400. Grounded solder balls 418 on the surface of IC package 400 are arranged as a boundary around signal launch 425 and are configured to couple the IC package 400 to a PCB substrate.

**[0024]** FIG. 4B illustrates a side view of the example IC package 400 coupled to a PCB substrate 410. The grounded solder balls 418 and signal launch 425 are aligned with a PCB through-hole cavity 435 which acts as a waveguide through the PCB substrate 410. During manufacturing and assembly, the grounded solder balls 418, the through-hole cavity 435, and antenna launch 425 are aligned. FIG. 4C shows a simulation plot of a signal through the grounded solder balls 418 and through-hole cavity 435. The field strength of the electromagnetic wave is indicated by the shaded regions. The electromagnetic field plot shows a well-matched transition from signal launch 425 to PCB through-hole cavity 435 with very little signal leakage in the IC package 400 or the region between the packaged radar device and the PCB coupled by the grounded solder balls 418.

**[0025]** The waveguide interface formed by grounded solder balls 418 around signal launch 425 contains the signal and reduces signal leakage between the signal launch 425 and PCB through-hole cavity 435. FIG. 4D shows a plot of insertion loss 492, return loss on the antenna side 494, and return loss on the waveguide side 496 in decibels (dB) across a frequency range of 72-84 GHz. The direct interface shown in FIG. 4B produces an insertion loss of approximately one dB and a

bandwidth of approximately 7.8 GHz.

**[0026]** FIGS. 5A-C illustrate side views of example direct interfaces between a packaged radar device and a 3D antenna with variations in grounded solder ball height, as well as a plot illustrating insertion loss and return loss for differing grounded solder ball heights. FIG. 5A illustrates an example direct interface 500A with an IC package 510 coupled to a PCB substrate 520 by grounded solder balls 518A, which have a height that is 20% shorter than the height of grounded solder balls 418 shown in FIGS. 4A-B. FIG. 5B illustrates an example direct interface 500B with the IC package 510 coupled to the PCB substrate 520 by grounded solder balls 518B, which have a height that is 20% taller than the height of grounded solder balls 418 shown in FIGS. 4A-B. The variations in height between grounded solder balls 418, 518A, and 518B illustrate possible manufacturing variations for the grounded solder balls.

**[0027]** FIG. 5C shows a plot of insertion loss 492, return loss on the antenna side 494, and return loss on the waveguide side 496 from FIG. 4D with insertion loss 592A, return loss on the antenna side 594A, and return loss on the waveguide side 596A for the direct interface 500A shown in FIG. 5A and the insertion loss 592B, return loss on the antenna side 594B, and return loss on the waveguide side 596B for the direct interface 500B shown in FIG. 5B. As the overlapping plots illustrate, the variations in height between grounded solder balls 418, 518A, and 518B do not substantially affect the insertion loss or bandwidth of the direct interfaces.

**[0028]** FIGS. 6A-B illustrate example layouts of packaged radar devices and grounded solder balls. A packaged radar device can include any number of signal launches with a variety of shapes and arrangements. FIG. 6A illustrates an example layout 600 of rectangular signal launches 610A-G and grounded solder balls 620 around each signal launch. Signal launches 610A-G are arranged close together, such that some grounded solder balls 620 are included in the boundaries around multiple signal launches. Solder balls 630 are included in a BGA package for an IC chip comprising antenna launches 610A-G and can be grounded or carry signals. Both grounded solder balls 620 and solder balls 630 are configured to couple the IC die to a PCB substrate.

**[0029]** FIG. 6B illustrates an example layout 650 of signal launches 660A-G and grounded solder balls 670 arranged in a circular boundary around each signal launch. Circular boundaries can be used for designs with circular PCB through-hole cavities. In layout 650, signal launches 660A-G can be circular or rectangular shaped. Grounded solder balls 670 are arranged in a circular shape around each signal launch, such that the shape of cross sections of the corresponding signal

channels is defined by the grounded solder balls 670 fencing in the transmitted or received signal around the signal launches 660A-G. Similar to layout 600 shown in FIG. 6A, grounded solder balls 670 can be shared between boundaries around multiple signal launches 660A-G, and are included with solder balls 680 in a BGA package for an IC die comprising signal launches 660A-G and configured to couple the IC die to a PCB substrate.

**[0030]** The term “couple” is used throughout the specification. The term may cover connections, communications, or signal paths that enable a functional relationship consistent with the description of the present disclosure. For example, if device A generates a signal to control device B to perform an action, in a first example device A is coupled to device B, or in a second example device A is coupled to device B through intervening component C if intervening component C does not substantially alter the functional relationship between device A and device B such that device B is controlled by device A via the control signal generated by device A. Unless otherwise stated, in this description, “aligned” or “substantially aligned” means the two are ninety percent or more aligned with each other.

**[0031]** Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

## CLAIMS

What is claimed is:

1. A device, comprising:

a package substrate encapsulating an integrated circuit (IC) die and comprising a signal launch on a surface of the package substrate and configured to emit or receive a signal; and

a ball grid array (BGA) affixed to the surface of the package substrate and comprising a set of grounded solder balls arranged as a boundary around the signal launch on the surface of the package substrate.

2. The device of claim 1, further comprising a printed circuit board (PCB) substrate having:

a waveguide interface side;

a secondary waveguide side opposite the waveguide interface side; and

a through-hole cavity perpendicular to a plane of the PCB substrate and extending from the waveguide interface side to the secondary waveguide side, wherein the BGA couples the package substrate to the waveguide interface side such that the surface of the package substrate faces the through-hole cavity and such that the signal launch and the through-hole cavity are substantially aligned.

3. The device of claim 2, wherein the set of grounded solder balls forms a wave-guiding interface between the signal launch and the through-hole cavity.

4. The device of claim 2, further comprising an external waveguide coupled to the secondary waveguide side such that the external waveguide and the through-hole cavity are substantially aligned.

5. The device of claim 4, wherein the external waveguide is included in a three-dimensional antenna.

6. The device of claim 2, wherein the set of grounded solder balls is arranged as a circular boundary around the signal launch and the through-hole cavity.

7. The device of claim 2, wherein the set of grounded solder balls is arranged as a rectangular boundary around the signal launch and the through-hole cavity.

8. The device of claim 1, wherein:

the signal launch comprises a first signal launch configured to emit or receive a first signal;

the set of grounded solder balls comprises a first set of grounded solder balls arranged as a boundary around the first signal launch;

the package substrate further comprises a second signal launch on the surface of the package substrate configured to emit or receive a second signal; and

the BGA further comprises a second set of grounded solder balls arranged as a boundary around the second signal launch on the surface of the package substrate.

9. The device of claim 8, wherein the first and second sets of grounded solder balls have at least one grounded solder ball in common.

10. The device of claim 8, wherein the first and second sets of grounded solder balls have no grounded solder balls in common.

11. The device of claim 8, wherein the first and second sets of grounded solder balls are arranged such that the first and second signals are isolated from each other by a threshold amount.

12. A printed circuit board (PCB), comprising:

a PCB substrate having a first surface and a second surface opposite the first surface, the PCB substrate further having a through-hole cavity from the first surface to the second surface;

an integrated circuit (IC) package substrate comprising a signal launch on a surface of the IC package substrate;

a wave-guiding interface comprising a set of grounded solder balls and coupling the IC package substrate to the first surface of the PCB substrate such that the surface of the IC package substrate faces the first surface of the PCB;

an external antenna comprising a waveguide and coupled to the second surface of the PCB substrate; and

a signal channel between the signal launch and the external antenna comprising:

the wave-guiding interface,

the through-hole cavity, and

the waveguide, wherein the signal launch, the through-hole cavity, and the waveguide are substantially aligned, and wherein a shape of a cross section of the signal channel is defined by a fence around the signal launch comprising the set of grounded solder balls.

13. The PCB of claim 12, further comprising a ball grid array (BGA) affixed to the surface of the IC package substrate and coupling the IC package substrate to the first surface of the PCB substrate, wherein the BGA comprises the wave-guiding interface.

14. The PCB of claim 12, wherein the shape of the cross section of the signal channel is circular, and wherein the set of grounded solder balls are arranged in a circular fence around the signal

launch.

15. The PCB of claim 12, wherein the shape of the cross section of the signal channel is rectangular, and wherein the set of grounded solder balls are arranged in a rectangular fence around the signal launch.

16. The PCB of claim 12, wherein:

the PCB substrate further comprises a second through-hole cavity from the first surface to the second surface;

the IC package substrate further comprises a second signal launch on the surface of the IC package substrate;

the external antenna further comprises a second waveguide; and

the PCB further comprises:

a second wave-guiding interface comprising a second set of grounded solder balls; and

a second signal channel between the second signal launch and the external antenna comprising the second wave-guiding interface, the second through-hole cavity, and the second waveguide, wherein:

the second signal launch, the second through-hole cavity, and the second waveguide are substantially aligned, and

a shape of a cross section of the second signal channel is defined by a fence around the second signal launch comprising the second set of grounded solder balls.

17. An integrated circuit (IC) chip, comprising:

a radar device comprising a signal launch on a surface of the radar device; and

a wave-guiding interface comprising a set of grounded solder balls arranged as a fence around the signal launch on the surface of the radar device.

18. The IC chip of claim 17, wherein the wave-guiding interface defines a shape of a cross section of a signal channel corresponding to the signal launch.

19. The IC chip of claim 17, further comprising a ball grid array (BGA) package encapsulating the radar device and comprising the set of grounded solder balls included in the wave-guiding interface.

20. The IC chip of claim 17, wherein the IC chip is coupled to a PCB substrate having:

a first surface;

a second surface opposite the first surface; and

a substrate through-hole waveguide from the first surface to the second surface, wherein the set of grounded solder balls couples the radar device to the first surface such that the surface of the radar device faces the first surface and such that the signal launch and the substrate through-hole waveguide are substantially aligned.

21. The IC chip of claim 20, wherein an external antenna is coupled to the second surface of the PCB substrate and comprises a waveguide opening, wherein the wave-guiding interface, the substrate through-hole waveguide, and the waveguide opening form a signal channel between the signal launch and the external antenna.

22. The IC chip of claim 21, wherein a shape of a cross section of the signal channel is defined by the set of grounded solder balls arranged as the fence around the signal launch.

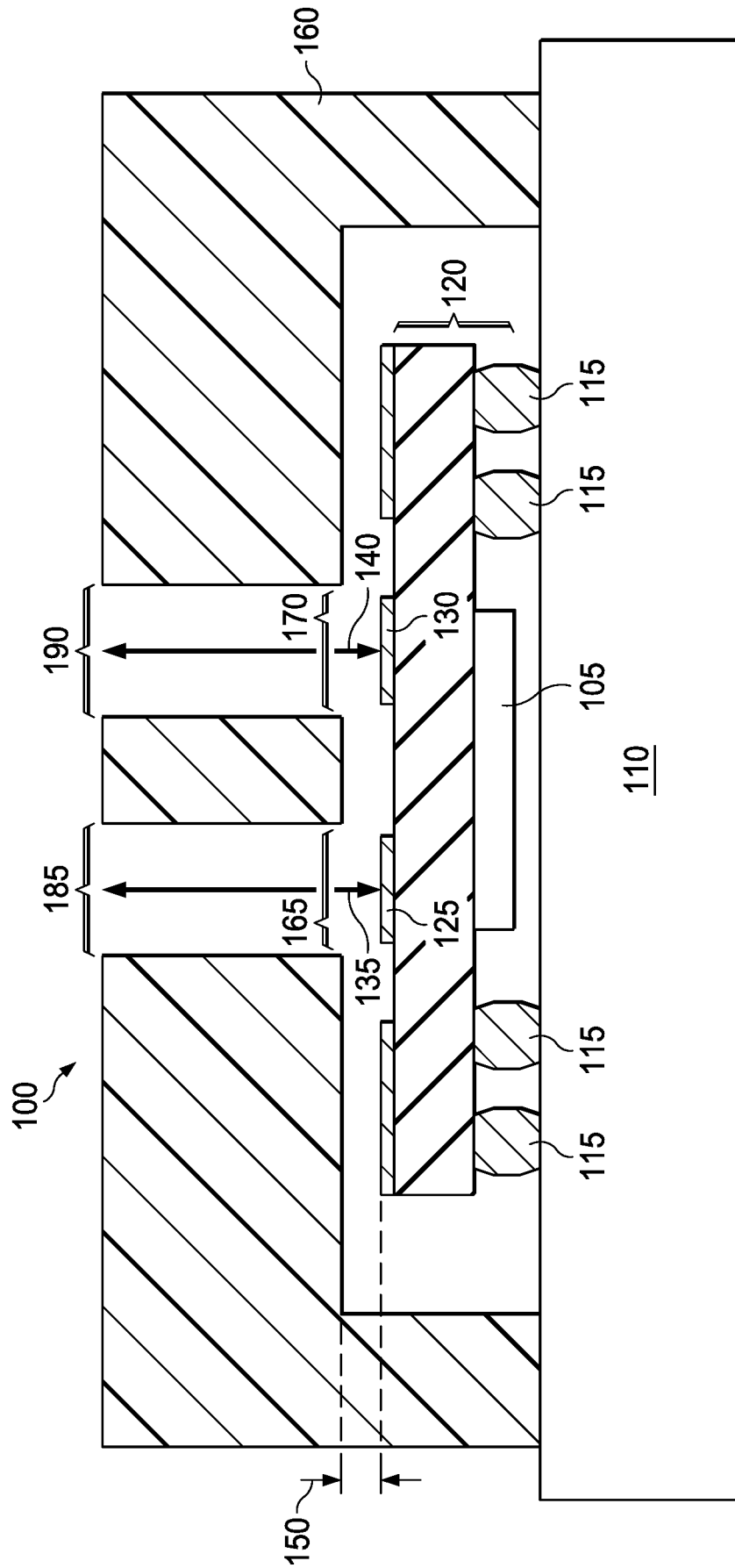


FIG. 1

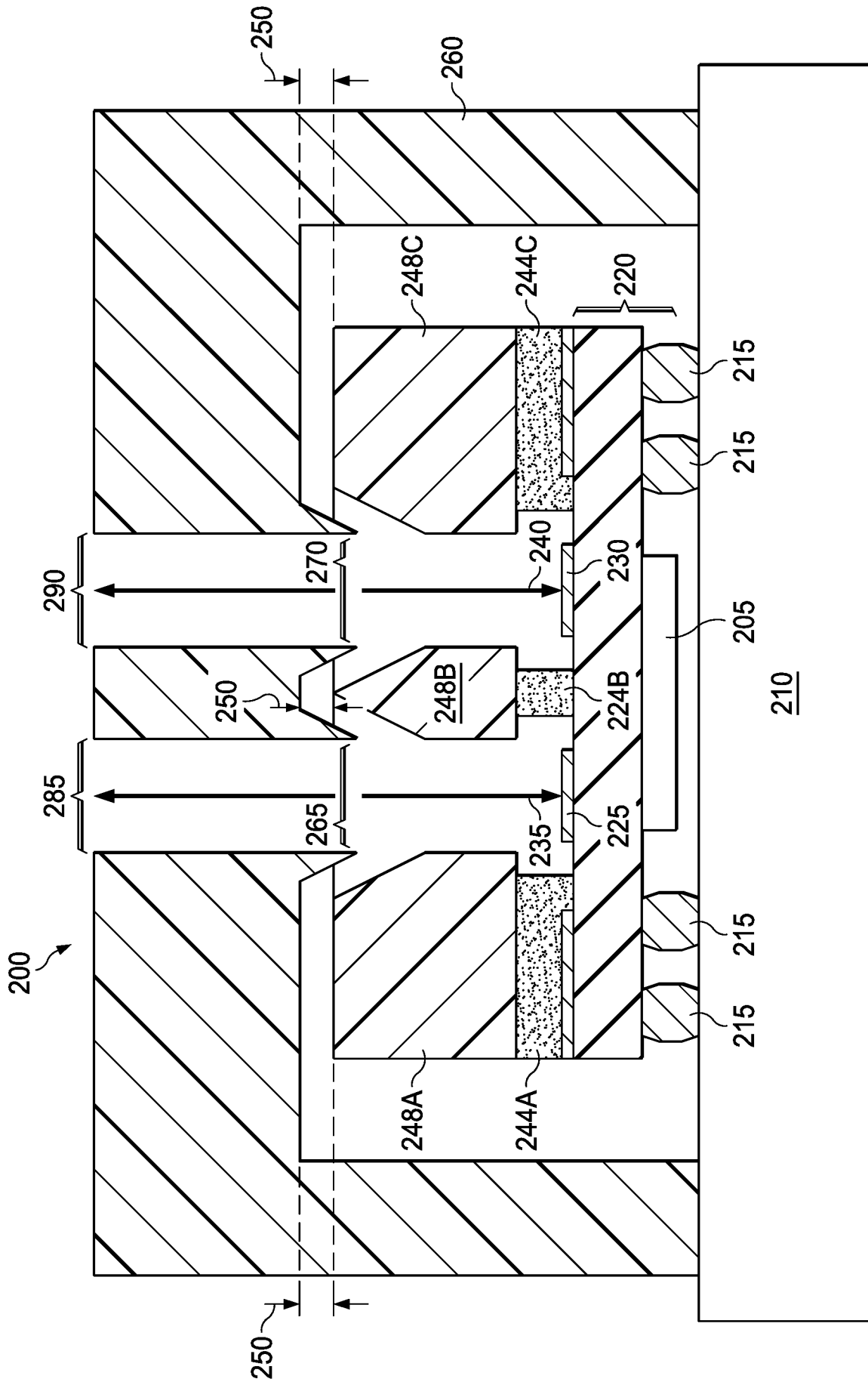
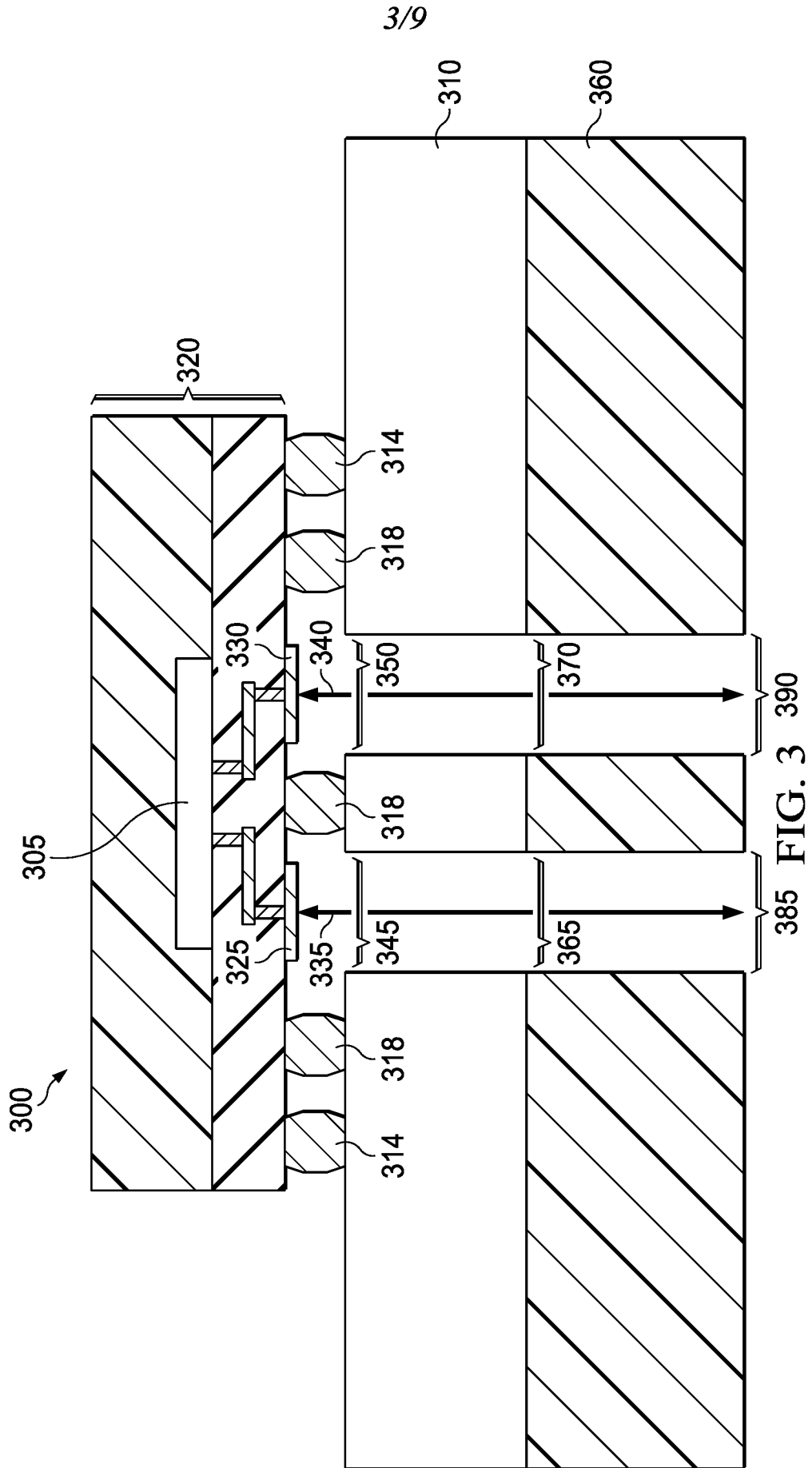


FIG. 2



3/9

385 FIG. 3 390

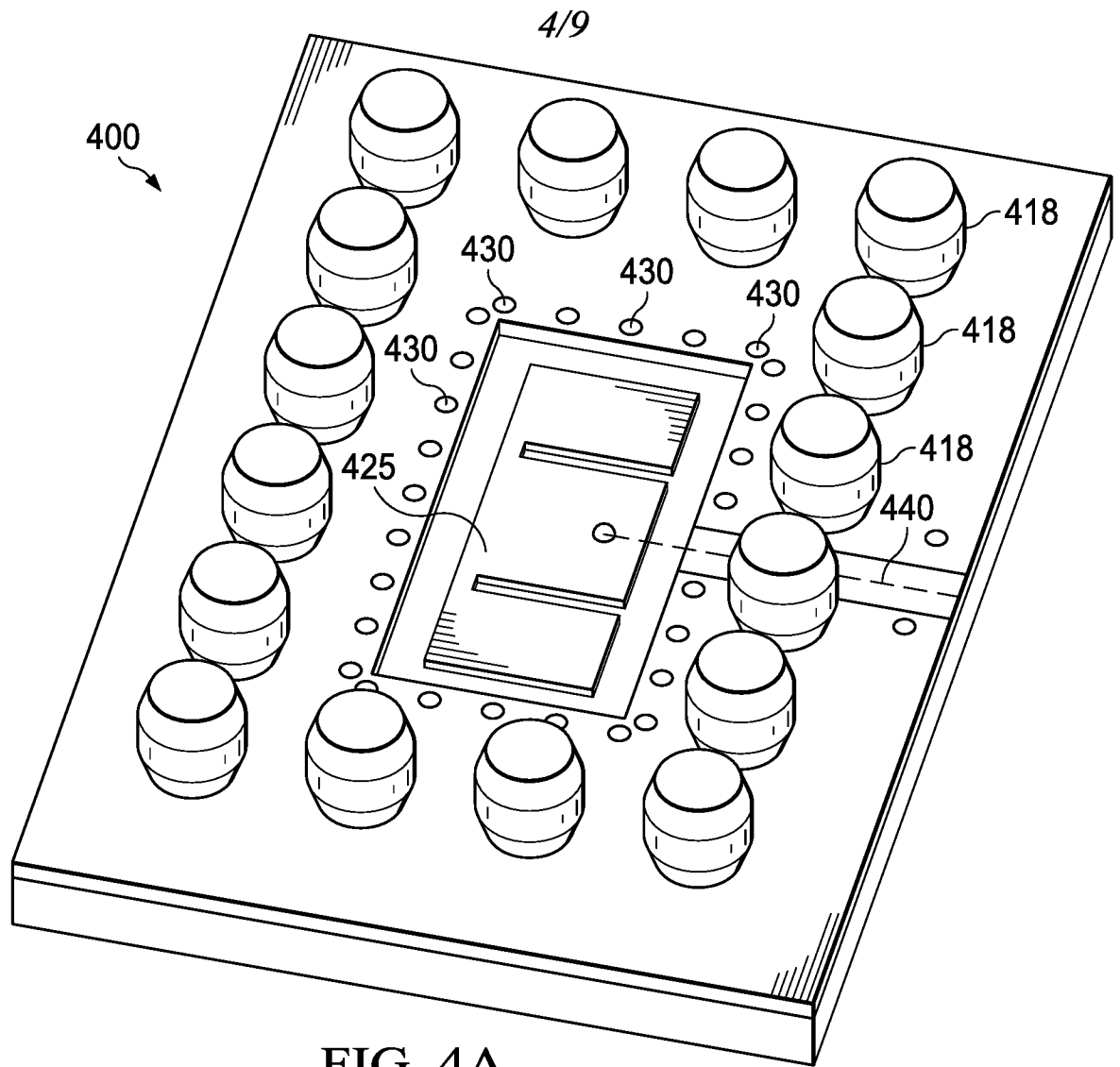


FIG. 4A

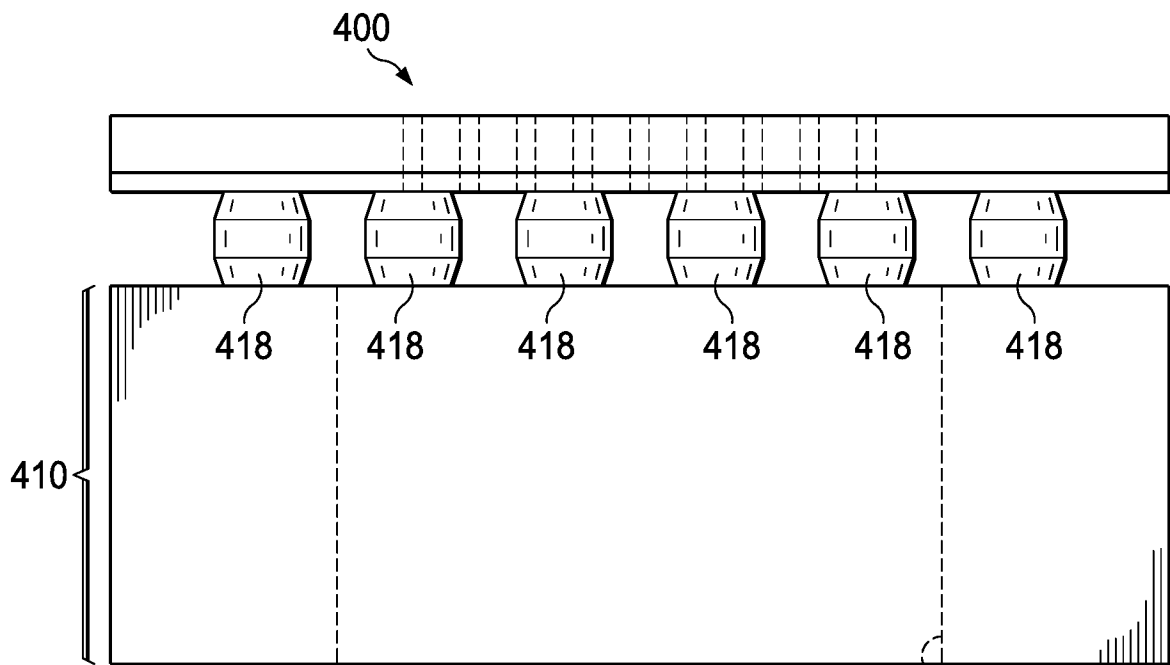


FIG. 4B

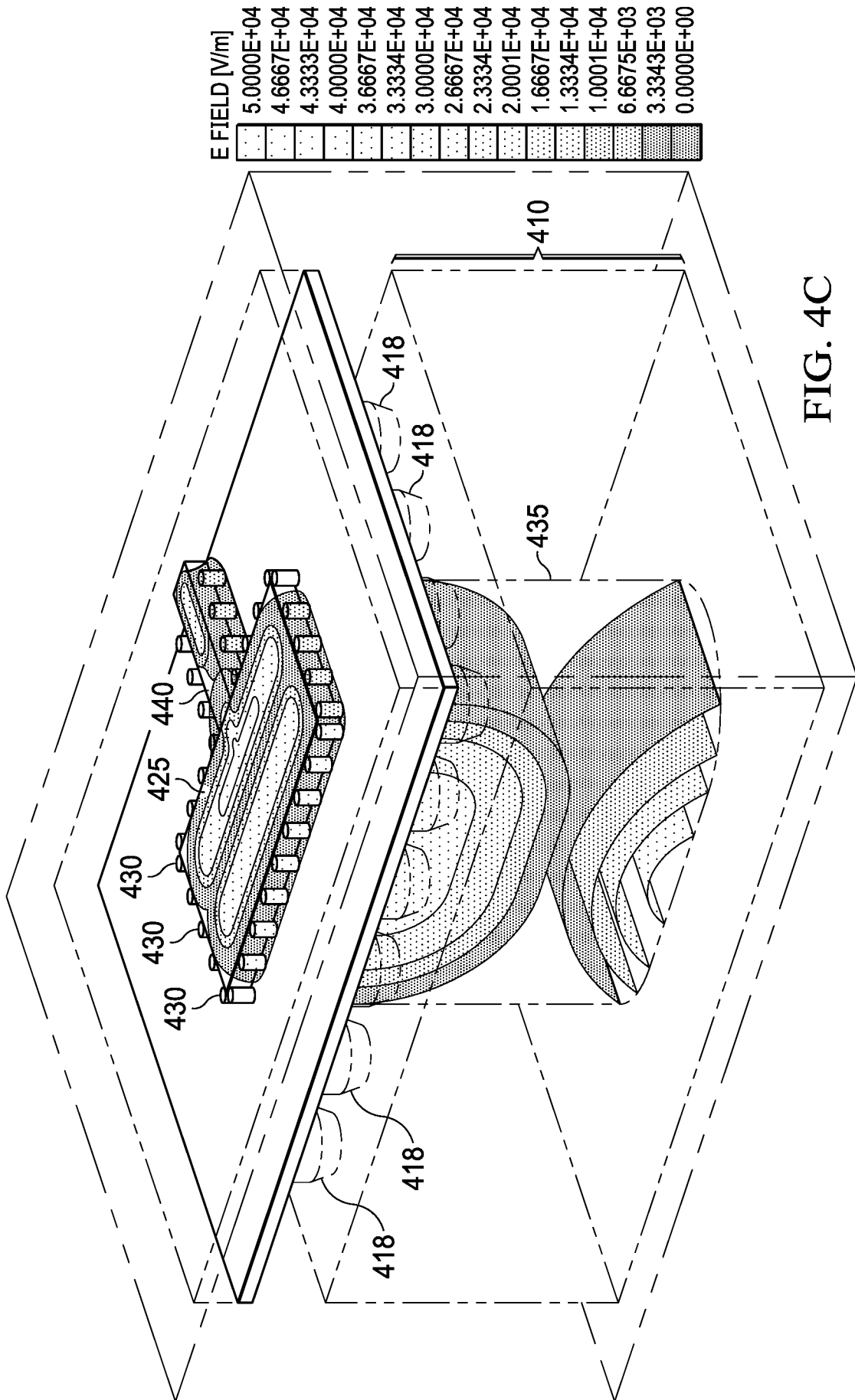
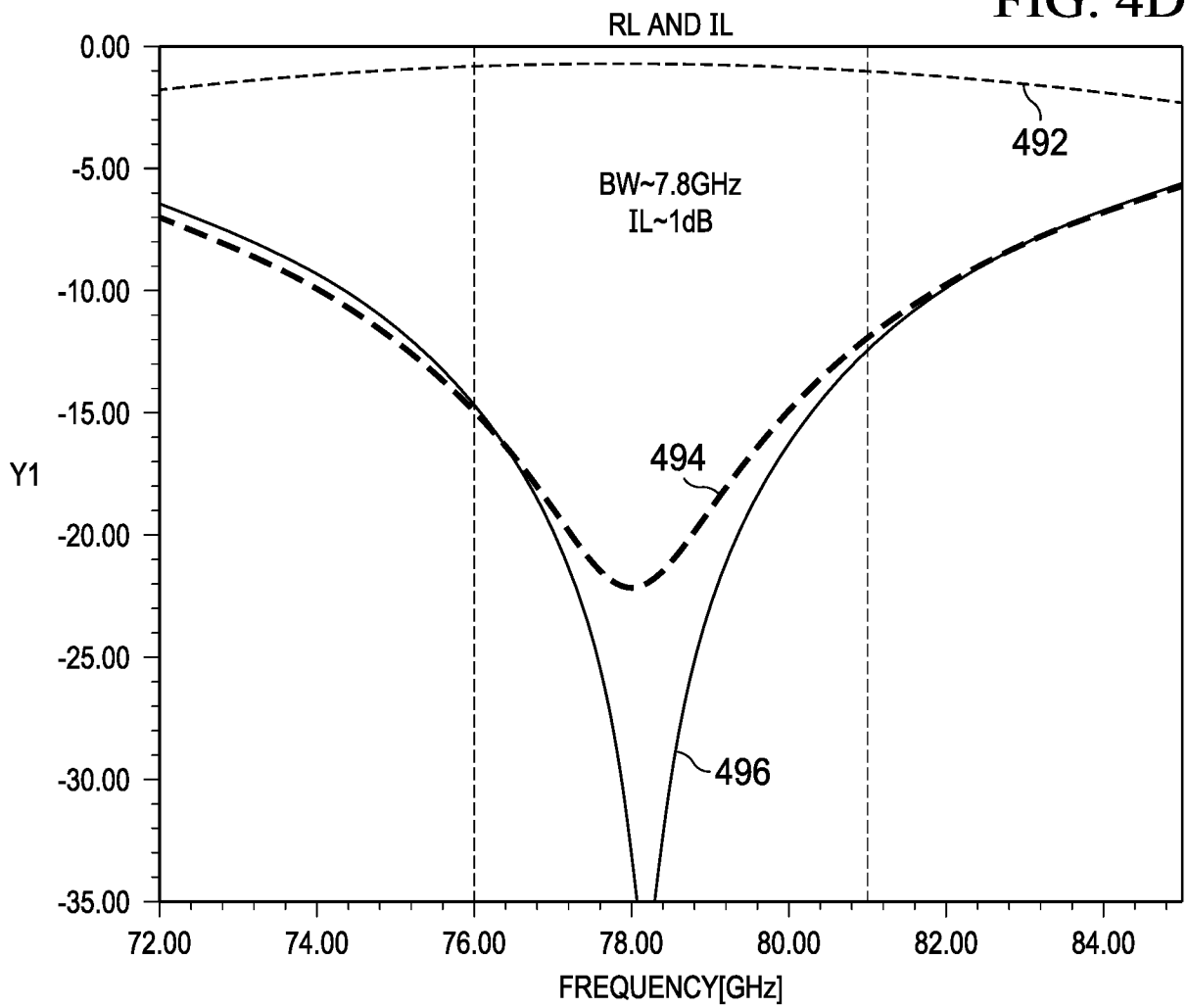


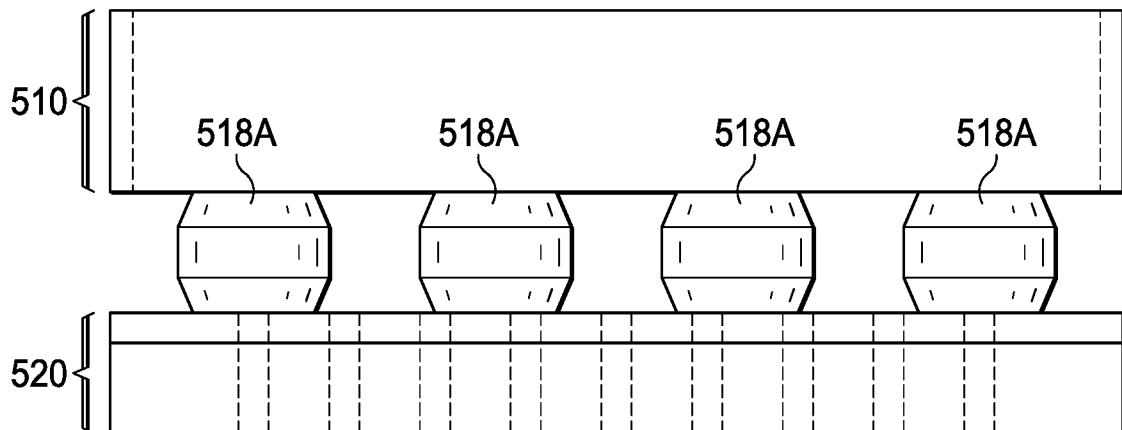
FIG. 4C

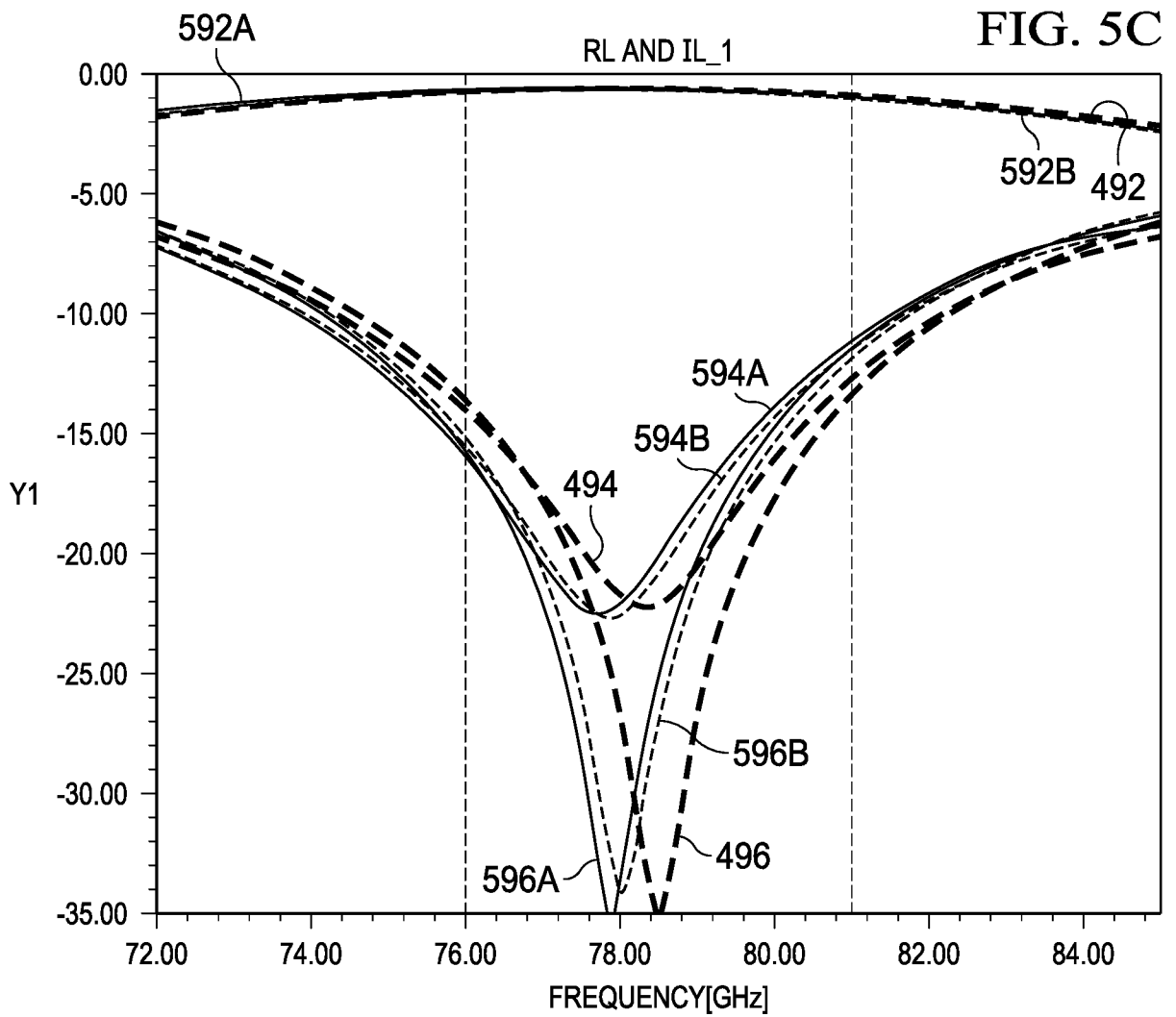
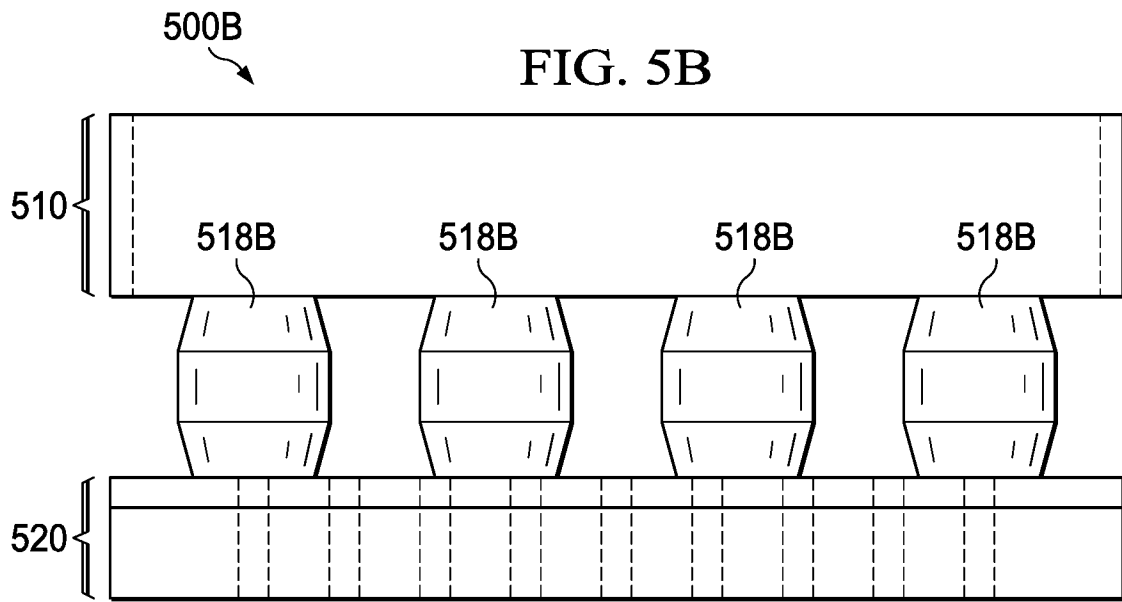
FIG. 4D



500A

FIG. 5A





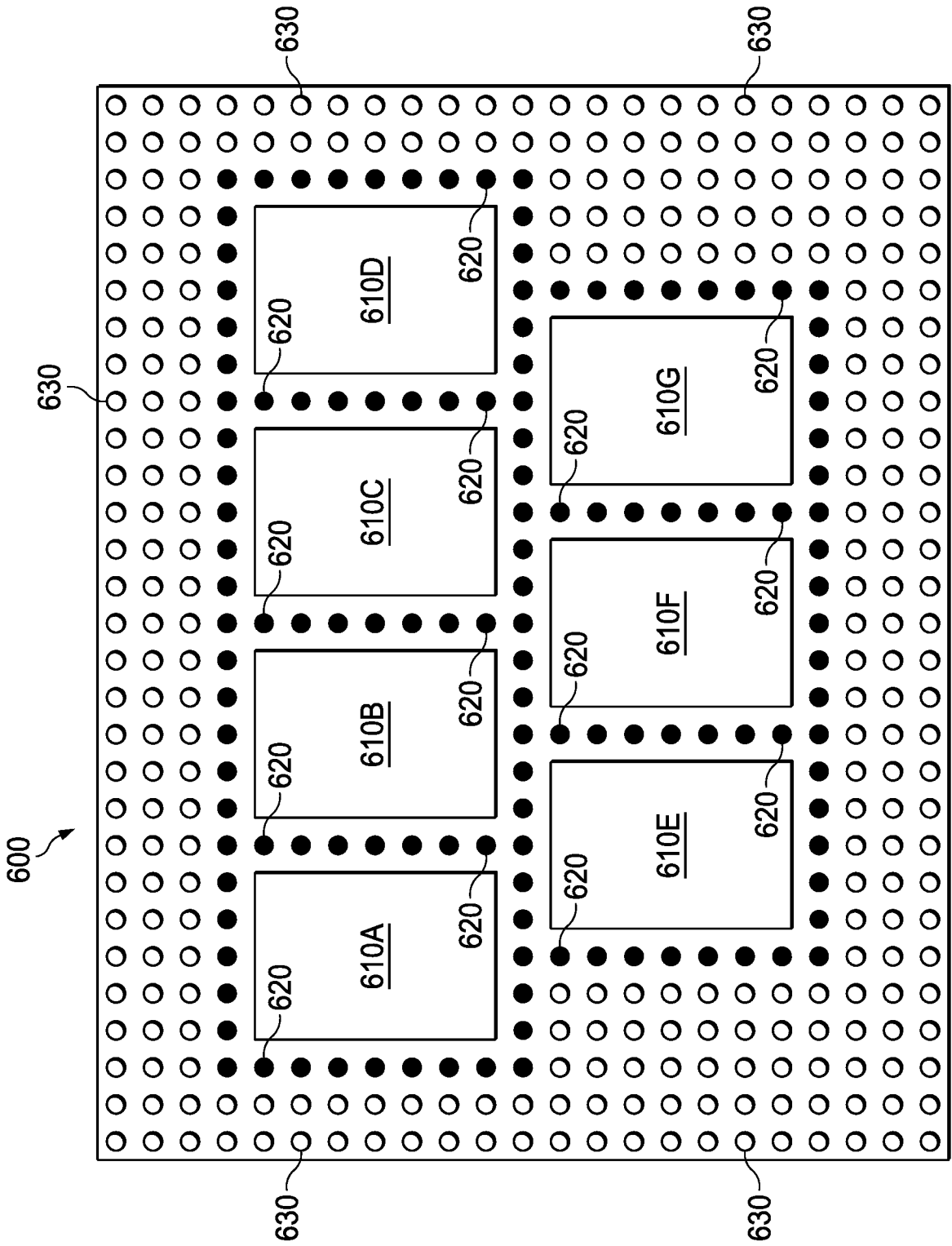


FIG. 6A

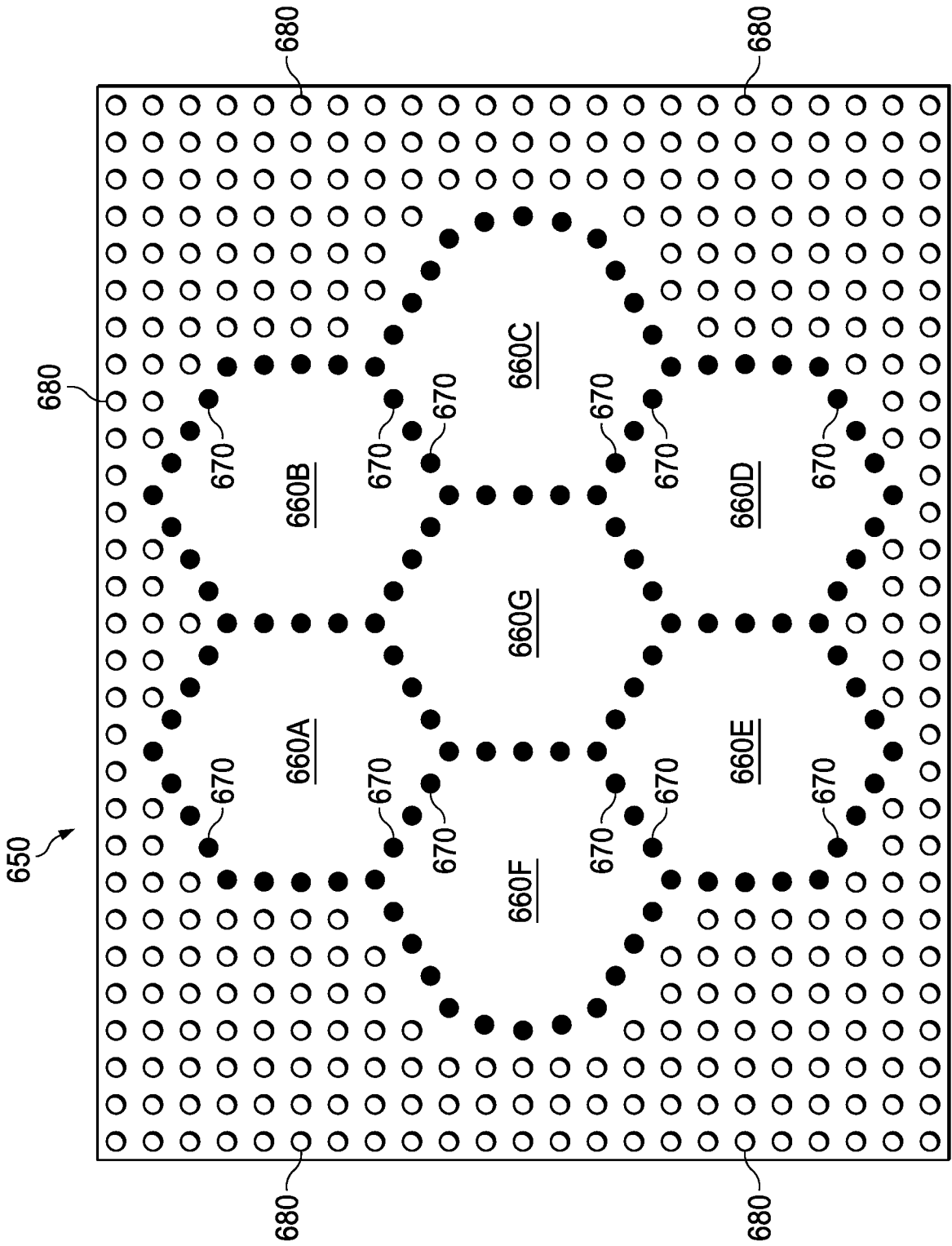


FIG. 6B

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2020/032312

A. CLASSIFICATION OF SUBJECT MATTER		<p style="text-align: center;"><b>H01Q 21/00 (2006.01)</b>  <b>G01S 7/03 (2006.01)</b>  <b>H01L 23/498 (2006.01)</b></p> <p>According to International Patent Classification (IPC) or to both national classification and IPC</p>	
B. FIELDS SEARCHED			
Minimum documentation searched (classification system followed by classification symbols)			
G01S 7/00, 7/02, 7/03, H01L 23/48, 23/488, 23/498, H01Q 21/00			
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched			
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)			
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS			
C. DOCUMENTS CONSIDERED TO BE RELEVANT			
Category*	Citation of document, with indication, where appropriate, of the relevant passages		Relevant to claim No.
Y A	US 2019/0101636 A1 (INFINION TECHNOLOGIES AG) 04.04.2019, paragraphs [0027], [0030], [0038], [0054]-[0059], [0062]- [0065], [0074], fig. 2A, 2B, 3		1-7, 12-15, 17-22 8-11, 16
Y	US 2007/0040626 A1 (APPLIED MICRO CIRCUITS CORPORATION) 22.02.2007, paragraphs [0060], [0005], fig. 10, 11		1-7, 12-15, 17- 22
Y	JP 2018-148105 A (DENSO WAVE INCORPORATED) 20.09.2018		6, 14
X, P	US 2019/0346814 A1 (TEXAS INSTRUMENTS INCORPORATED) 14.11.2019, paragraphs [0037]-[0038], fig. 2A, 4A, 4B		1, 17 - 19
<input type="checkbox"/> Further documents are listed in the continuation of Box C.		<input type="checkbox"/> See patent family annex.	
* Special categories of cited documents:		<p>“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>“&amp;” document member of the same patent family</p>	
“A”	document defining the general state of the art which is not considered to be of particular relevance		
“D”	document cited by the applicant in the international application		
“E”	earlier document but published on or after the international filing date		
“L”	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)		
“O”	document referring to an oral disclosure, use, exhibition or other means		
“P”	document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search		Date of mailing of the international search report	
24 July 2020 (24.07.2020)		06 August 2020 (06.08.2020)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer  V. Renteev  Telephone No. (495) 531-64-81	