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(54) METHOD OF PRODUCING A THIN LAYER OF SEMICONDUCTOR MATERIAL

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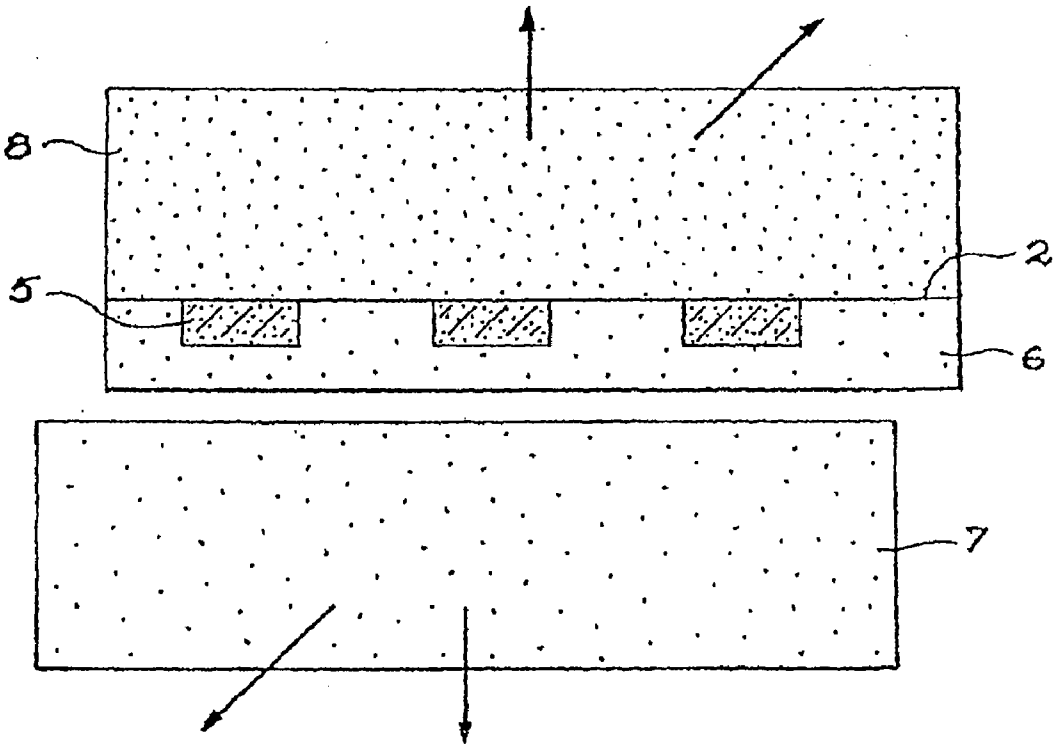
(57) **ABSTRACT**

A semiconductor structure includes a thin semiconductor layer fixed on an applicator or flexible support, the thin layer having an exposed surface characterized by fractured solid bridges spaced apart by cavities. A method of producing the thin layer of semiconductor material includes implanting ions into the semiconductor wafer to define a reference plane, where the ion dose is above a minimum dose, but below a critical dose so as to avoid degrading the wafer surface. The method further includes applying a thermal treatment to define a layer of microcavities and applying stress to free the thin layer from the wafer.



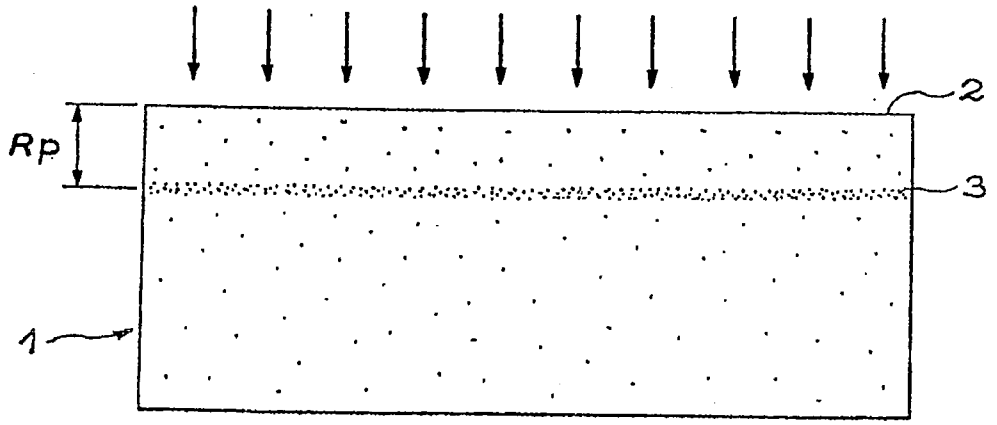


FIG. 1

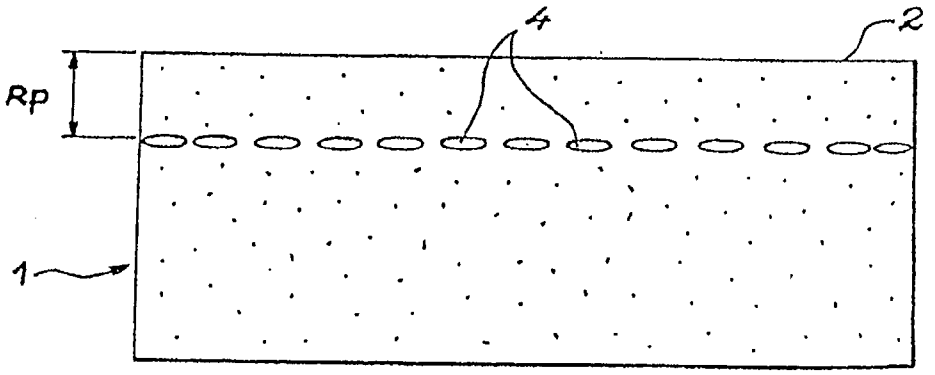


FIG. 2

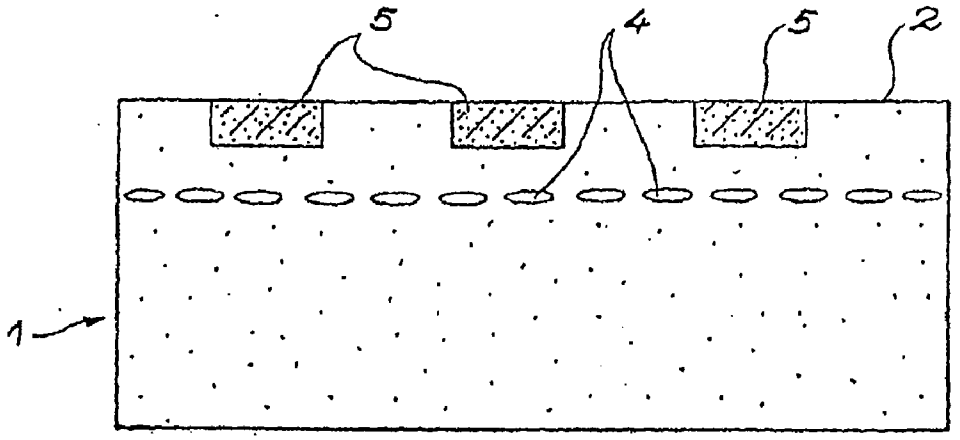


FIG. 3

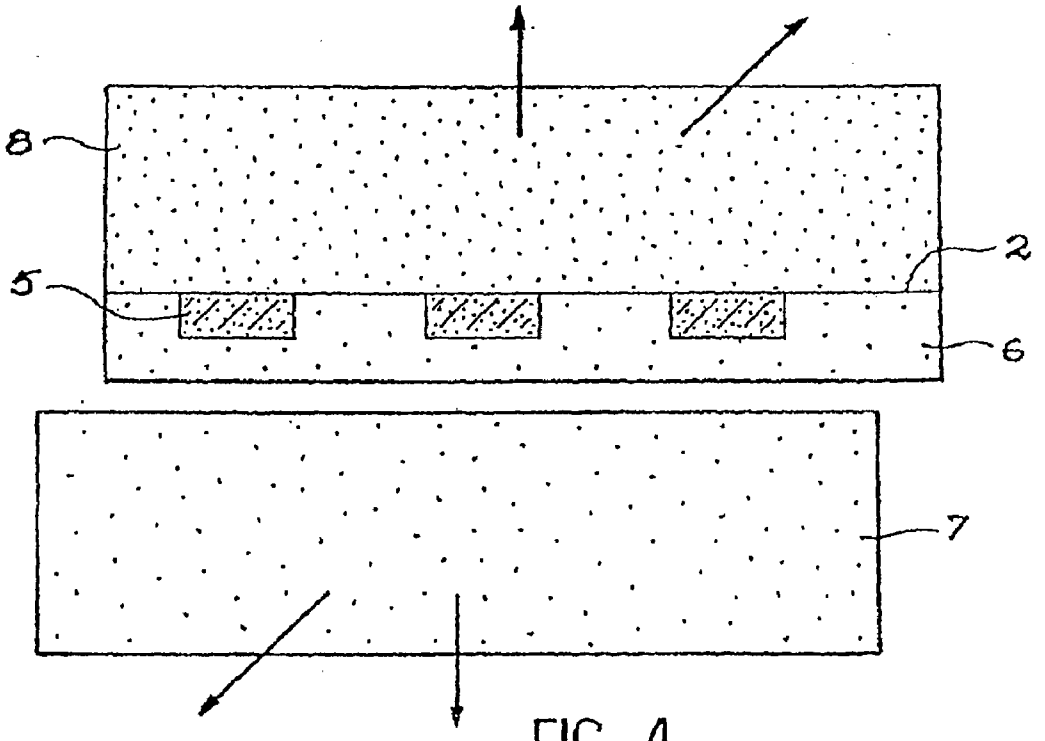


FIG. 4

METHOD OF PRODUCING A THIN LAYER OF SEMICONDUCTOR MATERIAL

RELATED U.S. APPLICATIONS

[0001] This application is a divisional application of application Ser. No. 12/334,086, filed Dec. 12, 2008, which is a continuation of application Ser. No. 11/327,906, filed Jan. 9, 2006, now U.S. Pat. No. 7,498,234, which is a continuation of prior U.S. application Ser. No. 10/784,601, now U.S. Pat. No. 7,067,396, which is a continuation of U.S. application Ser. No. 09/777,516, filed Feb. 6, 2001, now U.S. Pat. No. 6,809,009, which in turn is a continuation of prior U.S. application Ser. No. 09/299,683, filed Apr. 26, 1999, now U.S. Pat. No. 6,225,192 granted May 1, 2001, which in turn is a continuation of U.S. application Ser. No. 08/856,275, filed May 14, 1997, now U.S. Pat. No. 6,020,252, all of which are incorporated by reference herein.

TECHNICAL FIELD

[0002] This invention relates to a method of producing a thin layer of semiconductor material. The thin layer produced can possibly be provided with electronic components.

[0003] The invention permits the production of thin layers of either monocrystalline or polycrystalline or even amorphous semiconductor and, for example the production of substrates of the Silicon on Insulator type or the production of self-supporting thin layers of monocrystalline semiconductor. Electronic circuits and/or microstructures can be either completely or in part created in these layers or in these substrates.

BACKGROUND

[0004] It is known that implanting ions of a rare gas or of hydrogen in a semiconductor material induces the formation of microcavities at a depth proximate to the mean penetration depth of the ions. French Patent Application No. FR-A-2 681 472 discloses a method which uses this property in order to obtain a thin film of semiconductor. This method consists of subjecting a wafer of the desired semiconductor material that includes a flat face, to the following steps a first implantation step by bombarding the flat face of the wafer with ions creating, within the volume of the wafer and at a depth proximate to the penetration depth of the ions, a layer of microcavities separating the wafer into a lower region constituting the mass of the substrate and an upper region constituting the thin film, the ions being chosen from among the ions of rare gases or of hydrogen gas and the temperature of the wafer being maintained below the temperature at which the implanted ions can escape from the semiconductor by diffusion.

[0005] a second step of bringing the flat face of the wafer into close contact with a support made up of at least one layer of rigid material. This close contact may be created, for example using an adhesive substance, or by the effect of a preliminary preparation of the surfaces and possibly a thermal and/or electrostatic treatment in order to promote interatomic bonding between the support and the wafer;

[0006] a third step of thermal treatment of the wafer-support assembly at a temperature greater than the temperature at which the implantation was carried out and sufficient to create, through a crystal rearrangement effect in the wafer and through the pressure of the microcavities, a separation between the thin film and the mass of the substrate. This temperature is, for example 500° C. for silicon.

[0007] This implantation is capable of creating a layer of gaseous microbubbles. This layer of microbubbles thus created within the volume of the wafer; at a depth proximate to the mean penetration depth of the ions demarcates, within the volume of the wafer, two regions separated by this layer: one region intended to constitute the thin film and one region forming the rest of the substrate.

[0008] According to the implantation conditions, after implantation of a gas, such as, for example hydrogen, cavities or microbubbles may or may not be observable by transmission electronic microscopy. In the case of silicon, it can be obtained microcavities, the size of which can vary from a few nm to several hundreds of nm. Hence, particularly when the implantation temperature is low, these cavities are only observable during the thermal treatment stage, a step during which nucleation is brought about in order to end up with the coalescence of the microcavities at the end of the thermal treatment.

[0009] The method described in French Patent Application No. FR-A-2 681 472 does not allow the production of electronic circuits in or at the surface of the flat face of the wafer after the ion implantation step. Indeed, the creation of such circuits implies the carrying out of certain classic microelectronics operations (diffusion annealing, deposition etc.) that require thermal treatment stages (typically from 40° C. to 700° C.) according to the steps for silicon. At these temperatures, blisters form on the surface of the flat face of the implanted wafer. By way of example, for an implantation of hydrogen ions at a dose of 5.10^{16} protons/cm^2 and at 100 keV energy in a silicon wafer, a thermal treatment carried out at 500° C. for 30 min. leads to degradation of 50% of the surface of the flat face of the wafer, this degradation resulting in the appearance of blisters and to their bursting. It is then no longer possible to properly ensure that the flat face of the wafer is brought into close contact with the support (which will be called the applicator in the subsequent description) so as to detach the semiconductor layer from the rest of the wafer.

[0010] This phenomenon of the formation of blisters and craters in the surface of a silicon wafer implanted with hydrogen ions after annealing has been discussed in the article "Investigation of the bubble formation mechanism in a-Si:H films by Fourier-transform infrared microspectroscopy" by Y. Mishima and T. Yagishita, that appeared in the J. Appl. Phys. 64 (8), 15th Oct. 1988, pages 3972-3974.

SUMMARY

[0011] This invention has been conceived in order to improve the method described in French Patent Application No. FR-A-2 681 472. After a step of ion implantation within a range of appropriate doses and before the separation step, it allows to carry out a thermal treatment of the part of the wafer corresponding to the future thin layer, in particular between 400° C. and 700° C. for silicon, without degrading the surface condition of the flat face of the wafer and without separation of the thin layer. This intermediate thermal treatment can form part of the operations for developing electronic components or can be applied for other reasons.

[0012] The invention is also applicable in the case where the thickness of the thin layer is sufficient to confer good mechanical characteristics on it, in which case it is not necessary to use an applicator in order to achieve the separation of the thin layer from the rest of the wafer, but where it is desired, despite everything, to avoid surface defects in the flat face.

[0013] Therefore an objective of the invention is a method of production of a thin layer of semiconductor material from a wafer of said material having a flat face, including an ion implantation step consisting of bombarding said flat face with ions chosen from among the ions of rare gases or of hydrogen, at a specific temperature and a specific dose in order to create, in a plane called a reference plane and situated at a depth proximate to the mean depth of penetration of the ions, microcavities, the method also including a subsequent thermal treatment step at a temperature sufficient to achieve separation of the wafer into two parts, across the reference plane, the part situated on the side of the flat face constituting the thin layer, characterised in that:

[0014] the ion implantation step is carried out with an ion dose between a minimum dose and a maximum dose, the minimum dose being that from which there will be sufficient creation of microcavities to obtain the embrittlement of the wafer along the reference plane, the maximum dose, or critical dose being that above which, during the thermal treatment step, there is separation of the wafer,

[0015] a separation step of separating the wafer into two parts, across the reference plane, is provided after or during the thermal treatment step, this separation step comprising the application of mechanical forces between the two parts of the wafer.

[0016] These mechanical forces can be tensile forces, shear forces or bending forces applied alone or in combination.

[0017] In the application, by microcavities, one understands cavities that can be of any form; for example, the cavities can be of a flat shape, that is to say of small height (a few interatomic distances) or of substantially spherical shape or any other different shape. These cavities can contain a free gaseous phase and/or atoms of gas arising from the implanted ions fixed to atoms of the material forming the walls of the cavities. In Anglo-Saxon terminology, these cavities are generally called "platelets", "microblisters" or even "bubbles".

[0018] The thermal treatment carried out with the purpose of achieving separation of the thin layer from the rest of the wafer, allows the microcavities to be brought to a stable state. Indeed, under the effect of temperature, the microcavities coalesce to reach a final definitive condition. Hence, the temperature is chosen in such a way that this condition is obtained.

[0019] According to French Patent Application No. FR-A-2 681 472, the doses implanted are such that, under the effect of the thermal treatment, a layer of microcavities is obtained that allows the separation to be achieved directly.

[0020] According to this invention, the doses implanted are insufficient to achieve a separation during the thermal treatment, the doses implanted only allow an embrittlement of the wafer at the reference plane, the separation requires an extra step of applying mechanical forces. Furthermore, the critical dose, as defined in the invention, is less than the dose at which during the ion implantation and thermal treatment steps, there is blister formation on the flat face of the wafer. The problem of blisters does not therefore arise in the invention.

[0021] The method according to the invention can include, between the thermal treatment step and the separation step, a step consisting of producing all or part of at least one electronic component in the part of the wafer before forming the thin layer.

[0022] If the production of this electronic component requires phases of heat treatment, these are preferably carried out at a temperature below that of the thermal treatment.

[0023] If needed, just before the separation step, an extra step is provided, consisting of bringing said wafer, on the side of said flat face, into close contact with and rigidly fixing it to a support through which mechanical forces such as tensile and/or shearing forces will be applied.

[0024] This support can be a flexible support, for example a sheet of Kapton®. It can also be a rigid support such as a wafer of oxidised silicon.

BRIEF DESCRIPTION OF THE DRAWING

[0025] The invention will be better understood and other advantages and features will become apparent on reading the description that follows, giving by way of a non-limitative example, in which:

[0026] FIG. **1** represents diagrammatically a wafer of semiconductor material, one face of which is being subjected to ion bombardment in application of the method according to this invention,

[0027] FIG. **2** represents diagrammatically the preceding wafer, at the end of the thermal treatment step intended to cause the microcavities to coalesce, according to this invention,

[0028] FIG. **3** represents diagrammatically the preceding wafer, after formation of electronic components in the part corresponding to the desired thin layer,

[0029] FIG. **4** represents diagrammatically the step of separating the preceding wafer into two parts, in accordance with this invention.

DETAILED DESCRIPTION

[0030] An important feature of this invention lies in the implantation of hydrogen or rare gas ions at a dose less than or equal to the dose above which there would be separation during the thermal treatment. The dose used is such that it permits embrittlement of the material at a depth R.sub.p corresponding to the mean distance travelled by the ions in the material, but the wafer remains sufficiently mechanically resistant to support all the thermal treatment steps necessary to produce the electronic circuits. In other terms, the implanted wafer has, in the area of the microcavities, solid bridges linking the part of the wafer designed to form the thin layer and the remaining part of the wafer.

[0031] The description is now going to be directed to the production of a thin layer of semiconductor material from a thick substrate having a flat face. The starting substrate may or may not be covered on this flat face with one or several layers of materials, such as, for example, encapsulating materials such as a dielectric.

[0032] FIG. **1** illustrates the ion implantation step of a wafer **1** of semiconductor material. The flat face **2** of the wafer receives the ionic bombardment represented by arrows. In the case where the flat face **2** of the wafer is covered with one or several non-semiconductor materials, the energy of the ions is chosen to be sufficient for them to penetrate into the mass of semiconductor material.

[0033] If the case arises, the thickness of the implanted semiconductor material must be such that all or part of electronic components and/or microstructures can be produced in the thin layer. By way of example, the mean penetration of hydrogen ions is 2.mu.m at 200 keV in silicon.

[0034] The ion implantation of these types of ions into the semiconductor substrate creates, at a depth proximate to the depth corresponding to the mean distance R.sub.p travelled

by the ions along a perpendicular to the flat face, an area **3** with a high concentration of atoms giving rise to microcavities. For example, the maximum concentration of hydrogen is 10^{21} H^+/cm^3 for an implantation dose of 2.10^{16} H^+/cm^2 at 100 keV. This ion implantation step must be carried out at a temperature such that the implanted gas ions do not diffuse any great distance as the implantation step goes along. This would interfere with or ruin the formation of microcavities. For example, in the case of an implantation of hydrogen ions in silicon, the implantation will be carried out at a temperature below 350° C.

[0035] The implantation dose (number of ions received per unit surface area during the implantation period) is chosen in such a way that the dose is less than or equal to a dose, called the critical dose, such that, above this critical dose, during the subsequent thermal treatment step, there is separation of the thin layer from the rest of the wafer. In the case of implantation of hydrogen ions, this critical dose is of the order of 4.10^{16} H^+/cm^2 for an energy of 160 keV.

[0036] The implantation dose is also chosen to be greater than a minimum dose from which during the subsequent thermal treatment step, the formation of microcavities and the interaction between them is sufficient, that is to say it permits the embrittlement of the implanted material in the area of the microcavities **3**. This means that solid bridges of semiconductor material still exist between the microcavities. In the case of an implantation of ions of hydrogen gas into a silicon substrate, this minimum dose is of the order of $1.10^{16}/cm^2$ at an energy of 100 keV.

[0037] The following step of the method according to the invention consists of a thermal treatment of the wafer at a temperature that is sufficient to allow coalescence of the microcavities along the reference plane. In the case of an implantation, at a temperature below 350° C., of ions of hydrogen gas into a silicon substrate and a dose of $3.10^{16}H^+/cm^2$ at an energy of 100 keV, after a thermal treatment of thirty minutes at 550° C., it is observed by transmission electronic microscopy in section, cavities of height equal to a few fractions of nanometers and with an extension, along the reference plane of several nanometers or indeed several tens of nanometers. This thermal treatment permits, at the same time, the precipitation and then stabilisation of the atoms of implanted gas in the form of microcavities.

[0038] The microcavities **4** (see FIG. **2**) occupy, along the reference plane, a surface area approximately equal to the surface area implanted. The cavities are not situated exactly in the same plane. They are in planes parallel to the reference plane, some nanometers or tens of nanometers from this reference plane. For this reason, the upper part of the substrate situated between the reference plane and the flat face **2** is not totally separated from the body of the substrate, the body of the substrate being defined as the rest of the substrate between the reference plane and the faces of the substrate other than the flat face. The remaining bonds are sufficiently strong to support the steps of manipulation and of annealing brought about by the technological steps taken in the creation of the integrated circuits. However, the bond between the upper part and the mass of the substrate is very much weakened since this bond is only made through bridges of semiconductor material situated between the cavities.

[0039] All or a part of electronic components, circuits and microstructures can then be created on the flat face **2** (at the surface or under the surface).

[0040] The ion implantation energy of the hydrogen or rare gas ions in the first step has been chosen in such a way that the depth of the area of microcavities is sufficient for it not to be disturbed by the creation of components, electronic circuits and/or microstructures during this step. Furthermore, the whole of the thermal annealing operations that the development of electronic circuits or microstructures requires, is chosen in such a way that possible diffusion of the implanted ions is minimised. For example, in the case of a wafer of monocrystalline silicon, the maximum temperature of the various phases of the method will be limited to 900° C.

[0041] FIG. **3** illustrates the case where several electronic components, reference number **5**, have been developed on the flat face **2** and in the part of the wafer intended to form the thin layer.

[0042] The separation step then follows. It consists of applying separating mechanical forces, for example, tensile forces between the parts of the wafer or substrate situated on each side of the reference plane in a manner that fractures the remaining solid bridges. This operation allows to obtain the thin layer of semiconductor material fitted with electronic components in the case described. FIG. **4** illustrates this separation step in the course of which the thin layer **6** is separated from the remaining mass **7** of the substrate by the action of forces acting in the opposite direction and represented by the arrows.

[0043] Experience shows that the tensile stress necessary to separate the upper part of the body of the substrate is low particularly when a shearing stress is applied between the upper part and the body of the substrate, that is to say when the stresses applied have a component applied along the reference plane. This is simply explained by the fact that the shear stress promotes the propagation of fractures and cavities within the reference plane.

[0044] The upper part of the substrate, being by nature thin, the tensile stress and/or the shear stress cannot in most cases be comfortably applied directly to it. It is then preferable, before the separation step, to make the wafer, via its flat face **2**, integral with a support or applicator through which the mechanical forces will be applied to the upper part of the wafer. This applicator is represented in FIG. **4** under reference number **8**.

[0045] The applicator can be a rigid or a flexible support. By the term rigidly fixing the applicator onto the wafer, one understands here any sticking operation or operation of preparing the surfaces and bringing them into contact that allows sufficient bonding energy to be provided between the applicator and the flat face of the wafer to resist the tensile and/or shear and/or bending process(es) of the separation step.

[0046] The applicator can be, for example, a sheet of plastic material such as Kapton® which has been made adherent to the flat face of the substrate. In this example, after application of the method according to the invention, a thin layer of monocrystalline semiconductor on a sheet of Kapton® is obtained.

[0047] So as to properly transmit the stresses to the whole of the upper thin layer, the circuits created in and at the surface of the upper layer can have been covered with a protective layer, possibly making it flat, during the step of developing the electronic components. The applicator is then rigidly fixed to the upper thin layer of the wafer through this protective layer.

[0048] The applicator may also be a rigid support, for example a silicon wafer, the surface of which has been cov-

ered with a dielectric layer. An appropriate physico-chemical treatment is, for example, carried out on the flat face of the wafer and/or the surface of the applicator (carrying a dielectric layer or not) so that bringing them into contact, possibly associated with a heat treatment, rigidly fixes the flat face of the wafer and the applicator together.

[0049] In the case mentioned as an example where the applicator is a silicon wafer carrying a layer of oxide on its surface and where the semiconductor substrate is a wafer of monocrystalline silicon, after application of the method according to the invention, a wafer of silicon on insulator is obtained where the surface layer of silicon is the fine layer provided by the upper part of the substrate.

[0050] Furthermore, after separation of the thin layer from the rest of the wafer, the free face of this layer can allow the further repeat use of a substrate that can be fitted with electronic components produced completely or partially on the substrate. Such a stacking allows a "three dimensional" assembly of electronic circuits, the stiffener itself possibly including electronic components.

1.-**12**. (canceled)

13. A semiconductor structure comprising a thin layer of silicon fixed on an applicator, wherein the thin layer includes an exposed surface characterized by fractured solid bridges spaced apart by cavities.

14. The semiconductor structure of claim **13**, wherein the applicator comprises a flexible support.

15. The semiconductor structure of claim **14**, wherein the flexible support comprises a plastic sheet.

16. The semiconductor structure of claim **13** further comprising a protective layer between the thin layer and the applicator.

17. The semiconductor structure of claim **13**, wherein the applicator comprises a silicon wafer.

18. The semiconductor structure of claim **17**, wherein the silicon wafer includes electronic components therein.

19. A semiconductor structure comprising a thin semiconductor layer bonded to an applicator, wherein the thin semiconductor layer includes electronic components therein and further includes an exposed surface characterized by fractured solid bridges spaced apart by cavities, and wherein the bond between the applicator and the thin semiconductor layer has sufficient energy to resist stress applied to the exposed surface during creation of the fractured solid bridges.

20. The semiconductor structure of claim **19**, wherein the applicator comprises a flexible support.

21. The semiconductor structure of claim **20**, wherein the flexible support comprises a plastic sheet.

22. The semiconductor structure of claim **19** further comprising a protective layer between the thin layer and the applicator, wherein the applicator is bonded to the protective layer.

23. The semiconductor structure of claim **19**, wherein the applicator comprises a silicon wafer.

24. The semiconductor structure of claim **23**, wherein the silicon wafer includes electronic components therein.

25. A method for producing a thin film comprising:
providing a first substrate having a face surface;
introducing ions into the first substrate at the face surface, such that microcavities are formed in the first substrate during or after introducing the ions,
wherein a thin film layer is defined from the face surface to the microcavities and the microcavities reside between solid bridges of the first substrate;
bonding a second substrate to the face surface of the first substrate; and
applying an external force to fracture the solid bridges and release the thin film layer from the first substrate.

26. A method for producing a thin film comprising:
providing a first substrate having a face surface;
introducing hydrogen ions into the first substrate at the face surface, such that microcavities are formed in the first substrate during or after introducing the ions,
wherein a thin film layer is defined from the face surface to the microcavities and the microcavities reside between solid bridges of the first substrate, and the hydrogen ions are introduced into the first substrate at a temperature and at a total amount so as not to fracture the solid bridges during energizing of the first substrate;
bonding a second substrate to the face surface of the first substrate; and
applying an external force to fracture the solid bridges and release the thin film layer from the first substrate.

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