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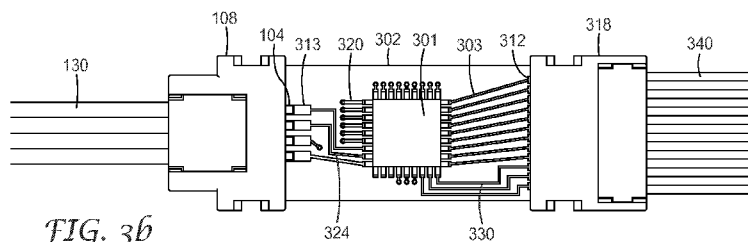
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(54) Title: ELECTRONIC ASSEMBLY INCLUDING CIRCUIT BOARD HAVING FIXED ADDRESS-SETTING ELECTRICAL
PADS DISPOSED THEREON



(57) Abstract: Electronic assemblies are provided that include a of set of address-setting electrical pads disposed on a circuit board forming a fixed pattern and a set of address-setting electrical jumpers attached to a substrate forming a fixed pattern. The set of address-setting electrical jumpers selectively contacts the set of address-setting electrical pads thus determining an address of the integrated circuit. The substrate can include an electrical connector or BUS line connector attached to a circuit board, a protective cover mounted above or below the circuit board, or an address-setting chip mounted on the circuit board.



**ELECTRONIC ASSEMBLY INCLUDING CIRCUIT BOARD HAVING FIXED
ADDRESS-SETTING ELECTRICAL PADS DISPOSED THEREON**

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Field

This disclosure relates to network address-setting electronic assemblies.

Background

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Network address-setting is an important need in electronic networks that can be used, for example, to connect a host signal from an electronic host device to one or more electronic peripheral devices. The host signal can be generated by a master integrated circuit (IC), a main computer, or server. The electronic peripheral devices can be one or more of slave ICs, computers on a network, such as a local area network or LAN, or can be one or more electronic devices such as a printer, facsimile machine, scanning device, that are attached to the host device. Generally, it is necessary to convert the host signal to a format that is compatible with the electronic slave device. This conversion usually requires some electronic circuitry.

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Typically, the electronic circuitry that converts the host signal into a format that is compatible with the electronic slave device is mounted on a circuit board and is frequently contained in an IC chip mounted on the circuit board. The IC chip includes a number of circuits that are useful to convert a wide variety of host signals from a wide variety of electronic host devices to a wide variety of electronic slave devices. The IC chip accepts the host signal from the electronic host device and then shuttles that host signal through a specific circuit to the specific peripheral device also connected to the IC chip. Since the IC chip has multiple useable circuits, the specific circuit to which each host signal is channeled has a specific network address which can be set electronically by the electronic host device or can be set manually using, most typically, a DIP (dual in-line package) switch which is usually mounted on the circuit board between the host signal from the electronic host device and the IC. The DIP switch can be manually set to an address-setting which channels the host signal to the specific circuitry in the IC chip allowing the host signal to be converted into a format which is compatible with the electronic slave device (also connected to the IC chip). DIP switches with built-in active interfacing circuitry are discussed, for example, in U. S. Pat. Nos. 4,376,234 (Liataud) and 4,658,101 (Akimoto et al.).

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In order make electronic circuitry more economical, an IC that contains a multiple of separate electronic circuits (that can be compatible with many electronic host and electronic slave devices) can be used to take the host signal from a described host electronic device and provide the proper circuitry to make that host signal compatible with a desired slave electronic connected thereto. Typically, a DIP switch, as described above, can be inserted between the host electronic

device and the IC to allow the user to choose which of the multiple of electronic circuits to be used for the particular electronic host and slave device to be used.

DIP switches can be physically large and cumbersome to work with. They need to be manually set to the correct address-setting when incorporated into an electronic system that includes a particular host electronic device and a particular slave electronic device. Efforts have been made to replace the DIP switches with other address-setting devices. For example, Japanese Pat. Publ. Nos. 2005-276489 (Maeda et al.) and 2005-286471 (Yamaguchi et al.) disclose flexible wiring boards that are punched out to cut pre-determined address-setting patterns. Alternatively, an insertion member can be inserted into an insertion hole to perform address selection. The operations of punching out address-setting patterns on a circuit board or inserting additional elements onto a circuit board are time-intensive operations that require a physical operation at the site of circuit manufacture. Additionally, in the cited art, cables need to be directly connected to the terminals of the connector apparatus. U. S. Pat. No. 7,648,388 (Kanazawa et al.) also discloses address-setting by removing or cutting connecting circuits as disclosed in the Japanese Patent Publications listed above. Additionally Kanazawa et al. discloses the use of conducting terminals made of electrically-conductive materials for address-setting.

Japanese Patent Publication No. 2003-127646 (Inayoshi et al.) discloses an external connector, actuator device for an air conditioner in a vehicle. The connector includes a plurality of terminal holding parts for each of the plurality of terminals on each actuator side. An external connector is provided that includes a member for address-setting.

There is a need for small, compact, address-setting devices for connecting host electronic devices with integrated circuits that are compatible with the host electronic device and attached slave electronic peripheral devices. There is a need for less labor-intensive assembly of electronic systems that include address-setting devices and integrated circuits.

Summary

The present disclosure provides an electronic assembly that includes address-setting electrical pads and integrated circuits disposed upon a circuit board. The provided electronic assembly includes a set of host electrical pads disposed upon the circuit board for receiving an electronic signal, a set of peripheral electrical pads disposed upon the circuit board for transmitting an electronic signal to a desired destination, wherein the set of host electrical pads and the set of peripheral electrical pads are in electrical communication with the integrated circuit, a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern, and a set of address-setting jumpers attached to a substrate forming a fixed pattern, the set of address-setting electrical pads selectively contacting the set of address-setting electrical pads, the set of address-

setting jumpers determining an address of the integrated circuit. The use of a set of address-setting electrical jumpers attached to a substrate eliminates the need for a DIP switch which is bulky and needs to be set prior to use of the electronic assembly. Additionally, the use of the provided electronic assembly does not require punching or cutting circuit components that are a part of the electronic assembly prior to use.

In one aspect, an electronic assembly is provided that includes a substrate that comprises an electrical connector or BUS line connector. The substrate makes selective electrical contact with the set of host electrical pads. This selective electrical contact, discussed hereinafter, performs the address-setting function.

In another embodiment, an electronic assembly is provided that includes substrate in the form of a dust cover that substantially covers at least one side of the circuit board. The dust cover, in addition to providing protection from dirt and dust, is provided with address-setting electrical jumpers on its edges that make electrical contact with the integrated circuit through address-setting pads on the circuit board. The address-setting electrical jumpers on the dust cover identify a specific address that determines a desired address of the integrated circuit.

In a third embodiment, an electronic assembly is provided that includes a substrate that includes an address-setting chip. The address-setting chip includes at least one jumper disposed thereon. The jumper can make electrical contact with the integrated circuit disposed upon the circuit board through pads on the circuit board. The address-setting chip has address-setting jumpers that, when in contact with address-setting pads on the circuit board, perform the address setting function. The address-setting chip can further comprise attachment means to physically secure the address-setting chip to the circuit board.

In another aspect, an electronic system is provided that includes an host electronic device and an electronic assembly according to any the above embodiments, wherein the host electrical pads of the electronic assembly are in electrical contact with the host electronic device and a peripheral electronic device, wherein the peripheral electrical pads of the peripheral electrical pads of the electronic assembly are in electrical contact with the peripheral electronic device.

In yet another aspect, a method of setting an address for an electronic assembly is provided that includes providing an integrated circuit disposed upon a circuit board, the integrated circuit having at least one address, a set of host electrical pads disposed upon the circuit board for receiving an electronic signal, a set of peripheral electrical pads disposed upon the circuit board for transmitting an electronic signal to a desired destination, wherein the set of host electrical pads and the set of peripheral electrical pads are in electrical communication with the integrated circuit, and a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern; and attaching a substrate comprising a set of address-setting jumpers forming a fixed pattern to the

circuit board, the set of address-setting jumpers selectively contact the set of address-setting electrical pads, the set of address-setting jumpers determining an address of the integrated circuit. The substrate can be a BUS line connector, a protective dust cover or an address-setting chip.

As used herein:

5 "BUS line connector" refers to a computer subsystem that is used to transfer data from an host electronic device to at least one integrated circuit disposed upon the circuit board;

"fixed pattern" refers to an arrangement of electrical pads that is not changeable;

10 "chip" or "address-setting chip" refers to circuit boards or circuit board elements that are disposed upon very thin, flexible substrates and, in the present context, include address-setting jumpers;

"host" refers to ICs, pads, wires, jumpers, and electronic devices and elements that supply electrical information to a peripheral device that can be a slave IC, a slave computer, an electronic device, or another circuit board or element;

"master IC" refers to ICs that supply electrical information to slave ICs;

15 "IC" refers to integrated circuit;

"jumper" refers to an electronic component capable of making an electrical connection between two pads;

"pad" refers to a substantially flat or planar conductive element on a circuit board;

20 "peripheral" refers to ICs, pads, wires, jumpers, and electronic devices and elements that receive electronic information from a host and act in response to that information. It is recognized that both a host and peripheral electronic device exchange information but a host electronic device instructs or commands the peripheral device during normal operation;

"slave ICs" refers to ICs that receive electronic information from master ICs and act in response to that information; and

25 "integrated circuit" refers to a miniaturized electronic circuit consisting mainly of semiconductor devices and passive components.

30 The disclosed electronic assemblies eliminate the need for a DIP switch which is bulky and needs to be set prior to use of the assemblies. Additionally, the disclosed electronic assemblies do not require punching or cutting circuit components which is a time-consuming manufacturing process.

The above summary is not intended to describe each disclosed embodiment of every implementation of the present invention. The brief description of the drawings and the detailed description which follows more particularly exemplify illustrative embodiments.

Brief Description of the Drawings

Fig. 1 is a perspective view of a provided address-setting BUS line connector.

Figs. 2a and 2b are respective cross-sectional and top views illustrating the address-setting BUS line connector of Fig. 1 in contact with a circuit board.

5 Figs. 3a-3c are respective side, top, and bottom views schematics of an embodied electronic assembly.

Figs. 4a and 4b are perspective and bottom views of a provided address-setting dust cover used in an embodiment of a provided electronic assembly.

10 Figs. 5a and 5b are a top view and a perspective view of an address-setting pad jumper useful in the address-setting dust cover illustrated in Figs. 4a and 4b.

Figs. 6a-6c are respective side, top, and bottom views schematics of circuit board useful in an embodiment of a provided electronic assembly.

Fig. 6d is a bottom view schematic of the dust cover seen mounted in place in Fig. 6a.

15 Figs. 7a and 7b are respective bottom and side view schematics of a provided address-setting chip useful in an embodiment of a provided electronic assembly.

Figs. 7c and 7d are respective bottom and side view schematics of a provided address-setting chip that selects a different address than that illustrated in Figs. 7c and 7d.

20 Figs. 8a-8c are schematic illustrations of a side view, top view with exploded address-setting chip, to view with unexploded address-setting chip, and bottom view an embodiment of an assembled provided electronic assembly that includes an address-setting chip.

Detailed Description

25 In the following description, reference is made to the accompanying set of drawings that form a part of the description hereof and in which are shown by way of illustration several specific embodiments. It is to be understood that other embodiments are contemplated and may be made without departing from the scope or spirit of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense.

30 Unless otherwise indicated, all numbers expressing feature sizes, amounts, and physical properties used in the specification and claims are to be understood as being modified in all instances by the term "about." Accordingly, unless indicated to the contrary, the numerical parameters set forth in the foregoing specification and attached claims are approximations that can vary depending upon the desired properties sought to be obtained by those skilled in the art utilizing the teachings disclosed herein. The use of numerical ranges by endpoints includes all numbers within that range (e.g. 1 to 5 includes 1, 1.5, 2, 2.75, 3, 3.80, 4, and 5) and any range
35 within that range.

Electronic assemblies are provided that include address-setting electrical pads and integrated circuits disposed upon a circuit board. Embodiments of the provided electric assemblies are described below while referring to the drawings. The provided electronic assemblies can be used as address-setting devices for connecting host electronic devices with integrated circuits that are compatible with the host electronic device and attached electronic peripheral devices.

In one embodiment, the provided electronic assemblies also include a BUS line connector containing address-setting jumpers that makes electrical contact with the set of host electrical pads on the electronic assemblies. Fig. 1 is a perspective view of an embodiment of such BUS line connector. Fig. 1 illustrates BUS line connector 100 that includes substrate 108. BUS line connector 100 has set of host electrical wires 130 that connect with a host electronic device (not shown) on one end and electrical connectors 104 which are located in substrate 108 as shown. Substrate 108 also includes address-setting jumpers 110 that form a fixed pattern (by their presence or absence). In the illustrated embodiment in Fig. 1, there are four address-setting electrical pads 110a, 110b, 110c, and 110d that set the address as binary "100111", when attached to a circuit board as illustrated further in Figs. 2a-2b and 3a-3c. Second set of address-setting electrical jumpers 110a, 110b, 110c, and 110d form binary addresses "1" by their presence and binary address "0" by their absence as shown in Figs. 2a and 2b. BUS line connector 100 has slot 106 into which a circuit board can be inserted to make contact with electrical connectors 104 and address-setting jumpers 110. Each address-setting jumper 110 that represents binary "1" is in the form of an electrical conductor that can make two contacts with electrical pads on an attached circuit board. In the illustrated embodiment the electrical conductor or address-setting jumpers 110 is shown as an "M"-shaped flat piece of metallic conductor.

Fig. 2a is a cross-sectional view of BUS line connector 100 (from Fig. 1) that shows circuit board 202 inserted into the connector through slot 106. Circuit board 202 has peripheral electrical pads 212 on one end and pairs of address-setting electrical pads 214 on the other end. Circuit board 202 also has a set of host electrical pads (on the side of the circuit board opposite address-setting electrical pads 214) which are not shown in Figs 2a or 2b. Electrical connectors 104 on BUS line connector 100 make electrical contact with these host electrical pads when BUS line connector 100 is mated with circuit board 202 through slot 106. The presence or absence of address-setting jumpers 110 in BUS line connector 100 determines a specific binary address. Fig. 2b shows circuit board 202 with six pairs of address-setting electrical pads 214 and four address-setting jumpers 110a – 110d located to form a shorted electrical path between pairs of address-setting electrical pads to define the address as "100111". BUS line connectors are well known to those of ordinary skill in the art of computer networking.

Figs. 3a-3c are schematic illustrations of respective side, top, and bottom views the embodiment of an electronic assembly partially illustrated in Figs. 1 and 2a-b. The schematic illustrations show integrated circuit 301 mounted on one side (top) of circuit board 302 as shown in Fig. 3b. Host electrical wires 130 bring an electronic signal from a host electronic device (not shown) to substrate 108 which is in the form of a BUS line connector. BUS line connector 100 includes electrical contacts 104 that make electrical contact with host electrical pads 313 on the top side of circuit board 302 as shown in Fig. 3b. Host electrical wires 130 are in electrical contact with integrated circuit 301 through traces 324. Substrate 108 also includes four pairs of address-setting electrical pads (not shown in Figs. 3a-3c) that make electrical contact with a first set of address-setting electrical pads 314 disposed upon circuit board 302. Circuit board 302 also includes, on the opposite end, traces 303 exiting from integrated circuit 301 and electrically connecting integrated circuit 301 with electrical wires 340 through peripheral BUS line connector 318. Peripheral BUS line connector 318 includes electrical contacts (not shown), one for each peripheral electrical wire, which make electrical contact with electrical pads 312 disposed upon circuit board 302.

In another embodiment, an electronic assembly is provided that includes a dust cover as the substrate. Figs. 4a and 4b are perspective and bottom views of a substrate in the form of an address-setting dust cover used in an embodiment of a provided electronic assembly. Address-setting dust cover 400 includes dust cover chassis 402 and second set of address-setting jumpers 410 along at least one of the side edges of dust cover chassis 402. Locator pins 405 and sockets 406, optionally, are present to orient dust cover 400 to corresponding sockets and pins that can be located in an attached BUS line connector or in each other if there is both a top and bottom dust cover on the electronic assembly. An assembled electronic assembly is shown in Fig. 6d. Dust cover 400 can be made from a number of insulating materials including various resins such as polyacetal, polyamide, polycarbonate, modified polyphenylene ether, polybutylene terephthalate, polyethylene terephthalate, ultra high molecular weight polyethylene, syndiotactic polystyrene, amorphous polyacrylate, polysulfone, polyethersulfone, polyphenylene sulfide, polyetheretherketone (PEEK), polyimide, polyether imide, fluororesins, and liquid crystal polymers. Typically polycarbonate may be used.

Figs. 5a and 5b are a top view and a perspective view of an address-setting jumper according to this second embodiment. Address-setting jumper 500 is in the form of a "U"-shaped three-dimensional shorting connector that includes shorting bar 502 and two electrical connecting bars 503 and 504 attached to shorting bar 502. In the illustrated embodiment, address-setting pad 500 includes electrical contacts 506 and 507 at the ends of electrical connecting bars 503 and 504. They are curved inwards so that they can make electrical contact with a first set of address-setting

electrical pads disposed upon a circuit board. Figs. 6a-6d further illustrate this second embodiment.

Figs. 6a-6c are respective side, top, and bottom view schematics of a circuit board useful in a second embodiment of provided electronic assembly 600. Figs. 6a-6c show circuit board 602 with integrated circuit 601 disposed thereon. Host electrical pads 613 are shown disposed upon the top side of circuit board 602 for receiving a host electronic signal. They are in electrical contact with integrated circuit 601 through traces 624 (only one trace shown for purposes of brevity). In Fig. 6b, electrical connectors 604 are shown in electrical contact with host electrical pads 613 forming an electrical connection between host electrical wires 630 and integrated circuit 601. First set of pairs of address-setting electrical pads 614 are disposed along one edge of dust cover 603 and are in electrical contact with integrated circuit 601 through traces 620. Peripheral electrical pads (not shown) are disposed upon circuit board 602 and are in electrical communication (connection) with circuit board 602 and peripheral electrical wires 640 through traces that are not shown. Traces can electrically connect with integrated circuit 601 through circuit board 602 via holes (shown as small circles in the schematics). Fig. 6c is a bottom view of the same electronic assembly illustrated in Figs. 6a and 6b. Fig. 6c shows protective bottom dust cover 650 covering the underside of the circuit board. Further description of protective dust covers useful as protective bottom covers can be found, for example, in Japanese Pat. Appl. No. 2010-293434 (Miya).

In a third embodiment, an electronic assembly is provided that includes a substrate that includes an address-setting chip with at least one conductive element disposed upon the address-setting chip. Figs. 7a and 7b are respective bottom view and side views schematics of an address-setting chip useful in this embodiment. Address-setting chip 700 includes flexible dielectric 702 and at least one jumper 704. Figs. 7c and 7d are respective bottom and side view schematics of another address-setting chip useful in this embodiment. The address number or the position of each jumper is different from Figs. 7a and 7b. By using the address-setting chip illustrated in Figs. 7c and 7d, a different circuit on the IC can be activated. In some embodiments, address-setting chip 700 is shaped so that it can be positioned exactly on a circuit board as shown further in Figs. 8b and 8c. In some embodiments, address-setting chip 700 comprises attachment means (not shown in Figures) to physically secure it to circuit board 802 so that the at least one jumper 704 is in electrical contact with first set of pairs of address-setting electrical pads 810 disposed upon the circuit board 802 forming a first fixed pattern. Attachment means can include brackets, adhesives, tapes, clips, clamps, fixtures, or any other physical devices capable of holding address-setting chip 700 in place on circuit board 802 so that the at least one jumper 704 makes electrical contact with at least one pair of address-setting pads 810 disposed upon circuit board 802.

Figs. 8a-8c are schematic illustrations of a side view, top view with exploded address-setting chip, to view with unexploded address-setting chip, and bottom view an embodiment of an assembled provided electronic assembly that includes an address-setting chip. The schematic illustrations show integrated circuit 801 mounted on one side (top) of circuit board 802 as shown in Fig. 8a. Host electrical wires 830 bring an electronic signal from a host electronic device (not shown) to BUS line connector 808. BUS line connector 808 includes electrical connectors 804 that make electrical contact with host electrical pads 813 disposed upon the top side of circuit board 802 as shown in Fig. 8b to receive an electronic signal. Host electrical pads 813 are in electrical contact with integrated circuit 801 through traces 824. Circuit board 802 also includes at least one of a first set of address-setting electrical pads 814 disposed upon it that are also in electrical contact with integrated circuit 801 through traces 820. Circuit board 802 also includes, on the opposite end, traces 803 exiting from integrated circuit 801 and electrically connecting integrated circuit 801 with peripheral electrical wires 840 through peripheral BUS line connector 818. Peripheral BUS line connector 818 includes electrical contacts (not shown), one for each peripheral electrical wire 840, which make electrical contact with peripheral electrical pads (also not shown) disposed upon circuit board 802.

Address-setting chips are made by disposing circuit elements such as traces, or electronic components on flexible substrates. Typical flexible substrates that are insulating and include organic materials are flexible and have high temperature resistance. A typical substrate material for making address-setting chips is polyimide of which KAPTON (available from Dupont, Wilmington, DE) is a commonly used material.

A method of setting an address for an electronic assembly is provided that includes providing an integrated circuit disposed upon a circuit board, the integrated circuit having at least one address, a set of host electrical pads disposed upon the circuit board for receiving an electronic signal, a set of peripheral electrical pads disposed upon the circuit board for transmitting an electronic signal to a desired destination, wherein the set of host electrical pads and the set of peripheral electrical pads are in electrical communication with the integrated circuit, and a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern; and attaching a substrate comprising a set of address-setting jumpers forming a fixed pattern to the circuit board, the set of address-setting jumpers selectively contact the set of address-setting electrical pads, the set of address-setting jumpers determining an address of the integrated circuit. In various embodiments the substrate can comprise a protective cover that is in electrical contact with and encloses at least a portion of the circuit board, a BUS line connector, or an address-setting chip with at least one jumper.

The provided method can also include removing the substrate from the circuit board and replacing the substrate with a different address-setting chip having a different fixed pattern .

Various modifications and alterations to this invention will become apparent to those skilled in the art without departing from the scope and spirit of this invention. It should be understood that this invention is not intended to be unduly limited by the illustrative embodiments and examples set forth herein and that such examples and embodiments are presented by way of example only with the scope of the invention intended to be limited only by the claims set forth herein as follows. All references cited in this disclosure are herein incorporated by reference in their entirety.

Following are exemplary embodiments of an electronic assembly including circuit board having fixed address-setting electrical pads disposed thereon according to aspects of the present invention.

Embodiment 1 is an electronic assembly comprising: a circuit board; an integrated circuit comprising at least one address disposed upon the circuit board; a set of host electrical pads disposed upon the circuit board for receiving an electronic signal; a set of peripheral electrical pads disposed upon the circuit board for transmitting an electronic signal to a desired destination, wherein the set of host electrical pads and the set of peripheral electrical pads are in electrical communication with the integrated circuit; a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern; and a set of address-setting jumpers attached to a substrate forming a fixed pattern, the set of address-setting jumpers selectively contacting the set of address-setting electrical pads, the set of address-setting jumpers determining an address of the integrated circuit.

Embodiment 2 is an electronic assembly according to embodiment 1, wherein the substrate comprises a protective cover that is in contact with and encloses at least a portion of the circuit board.

Embodiment 3 is an electronic assembly according to embodiment 2, wherein the protective cover is a dust cover.

Embodiment 4 is an electronic assembly according to embodiment 1, wherein the substrate comprises a BUS line connector.

Embodiment 5 is an electronic assembly according to embodiment 1, wherein the substrate comprises an address-setting chip that includes at least one jumper disposed upon the address-setting chip.

5 Embodiment 6 is an electronic assembly according to embodiment 5, wherein the address-setting chip comprises attachment means to physically secure it to the circuit board so that the at least one conductive element is in electrical contact with a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern.

10 Embodiment 7 is an electronic assembly according to embodiment 6, wherein the attachment means are selected from brackets, adhesives, tapes, clips, clamps, and fixtures

Embodiment 8 is an electronic system comprising: a host electronic device; an electronic assembly according to any of embodiments 1 to 9, wherein the host electrical pads of the
15 electronic assembly are in electrical contact with the host electronic device; and a peripheral electronic device, wherein the peripheral electrical pads of the peripheral electrical pads of the electronic assembly are in electrical contact with the peripheral electronic device.

Embodiment 9 is an electronic system according to embodiment 8, wherein the host
20 electric device comprises a master integrated circuit.

Embodiment 10 is an electronic system according to embodiment 8, wherein the peripheral electronic device comprises a slave integrated circuit.

25 Embodiment 11 is a method of setting an address for an electronic assembly comprising: providing an integrated circuit disposed upon a circuit board, the integrated circuit having at least one address, a set of host electrical pads disposed upon the circuit board for receiving an electronic signal, a set of peripheral electrical pads disposed upon the circuit board for transmitting an electronic signal to a desired destination, wherein the set of host electrical pads and the set of
30 peripheral electrical pads are in electrical communication with the integrated circuit, and a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern; and attaching a substrate comprising a set of address-setting jumpers forming a fixed pattern to the circuit board, the set of address-setting jumpers selectively contact the set of address-setting electrical pads, the set of address-setting jumpers determining an address of the integrated circuit.

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Embodiment 12 is a method of setting an address for an electronic assembly according to embodiment 11, wherein the substrate comprises a protective cover that is in contact with and encloses at least a portion of the circuit board.

5 Embodiment 13 is a method of setting an address for an electronic assembly according to embodiment 12, wherein the protective cover is a dust cover.

Embodiment 14 is a method of setting an address for an electronic assembly according to embodiment 11, wherein the substrate comprises a BUS line connector.

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Embodiment 15 is a method of setting an address for an electronic assembly according to embodiment 11, wherein the substrate comprises an address-setting chip that includes at least one jumper disposed upon the address-setting chip.

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Embodiment 16 is a method of setting an address for an electronic assembly according to Embodiment 15, wherein the address-setting chip comprises attachment means to physically secure it to the circuit board so that the at least one conductive element is in electrical contact with a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern.

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Embodiment 17 is a method of setting an address for an electronic assembly according to embodiment 16, wherein the attachment means are selected from brackets, adhesives, tapes, clips, clamps, and fixtures.

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Embodiment 18 is a method of setting an address for an electronic assembly according to embodiment 16, further comprising removing the address-setting chip from the circuit board and replacing the address-setting chip with a different address-setting chip having a different fixed pattern .

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Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. Those with skill in the mechanical, electro-mechanical, and electrical arts will readily appreciate that the present invention may be implemented in a very

35 wide variety of embodiments. This application is intended to cover any adoptions or variations of

the preferred embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An electronic assembly comprising:

a circuit board;

an integrated circuit comprising at least one address disposed upon the circuit board;

a set of host electrical pads disposed upon the circuit board for receiving an electronic signal;

a set of peripheral electrical pads disposed upon the circuit board for transmitting an electronic signal to a desired destination, wherein the set of host electrical pads and the set of peripheral electrical pads are in electrical communication with the integrated circuit;

a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern; and

a set of address-setting jumpers attached to a substrate forming a fixed pattern, the set of address-setting jumpers selectively contacting the set of address-setting electrical pads, the set of address-setting jumpers determining an address of the integrated circuit.

2. An electronic assembly according to claim 1, wherein the substrate comprises a protective cover that is in contact with and encloses at least a portion of the circuit board.

3. An electronic assembly according to claim 1, wherein the substrate comprises an address-setting chip that includes at least one jumper disposed upon the address-setting chip.

4. An electronic assembly according to claim 3, wherein the address-setting chip comprises attachment means to physically secure it to the circuit board so that the at least one conductive element is in electrical contact with a set of address-setting electrical pads disposed upon the circuit board forming a fixed pattern.

5. An electronic system comprising:

an host electronic device;

an electronic assembly according to any of claims 1 to 4, wherein the host electrical pads of
5 the electronic assembly are in electrical contact with the host electronic device; and

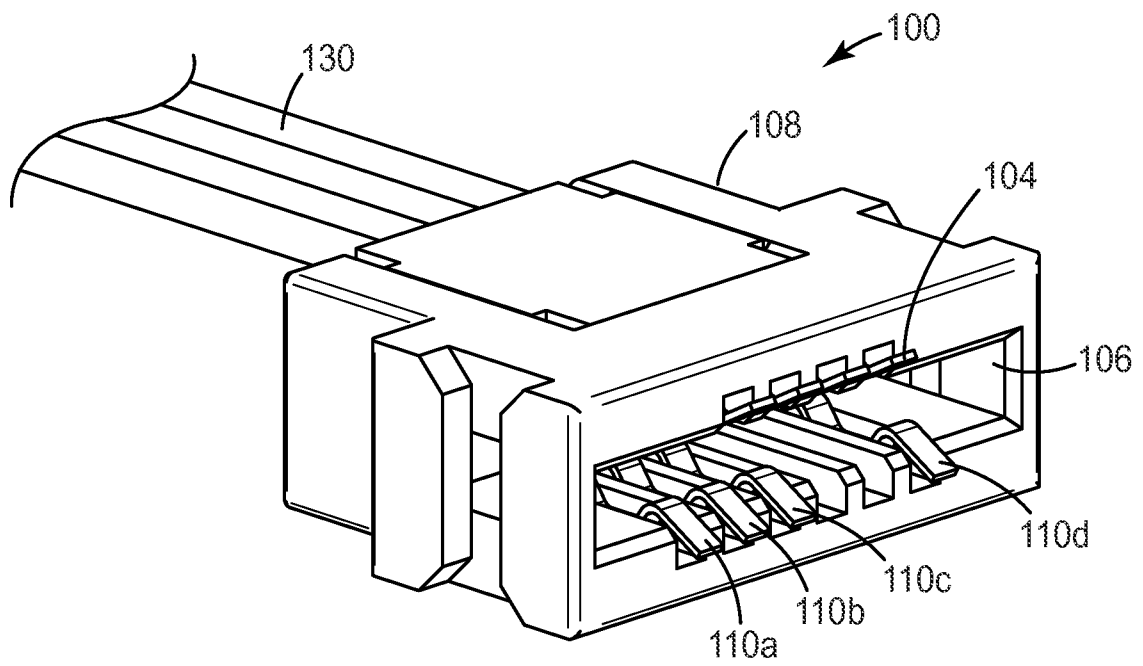
a peripheral electronic device, wherein the peripheral electrical pads of the peripheral
electrical pads of the electronic assembly are in electrical contact with the peripheral electronic
device.

10 6. An electronic system according to claim 5, wherein the host electric device comprises a master
integrated circuit.

7. An electronic system according to claim 5, wherein the peripheral electronic device comprises
a slave integrated circuit.

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*FIG. 1*

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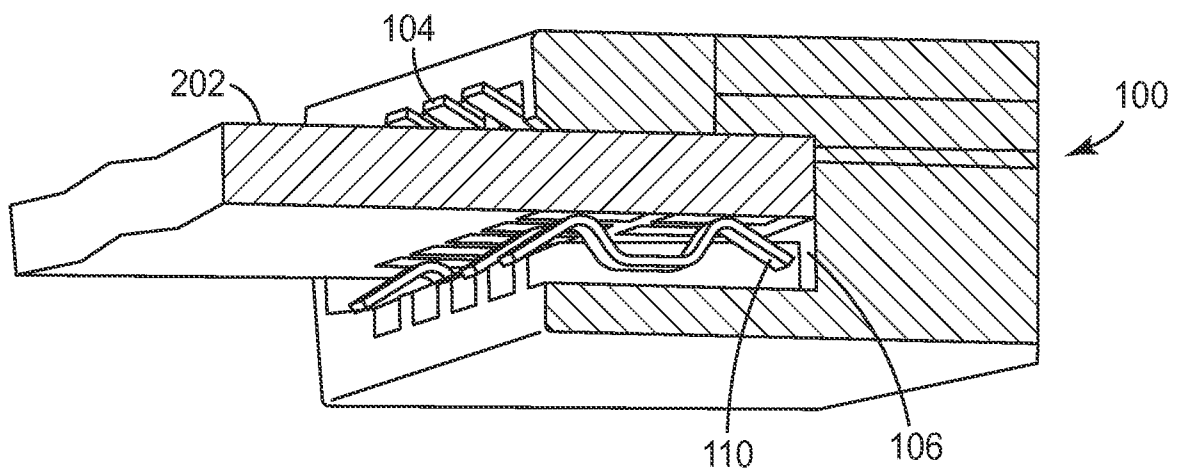


FIG. 2a

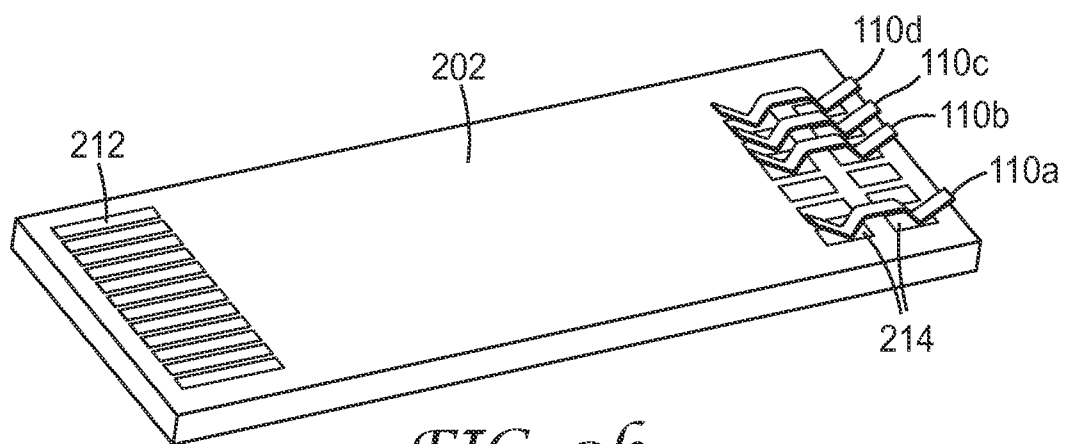
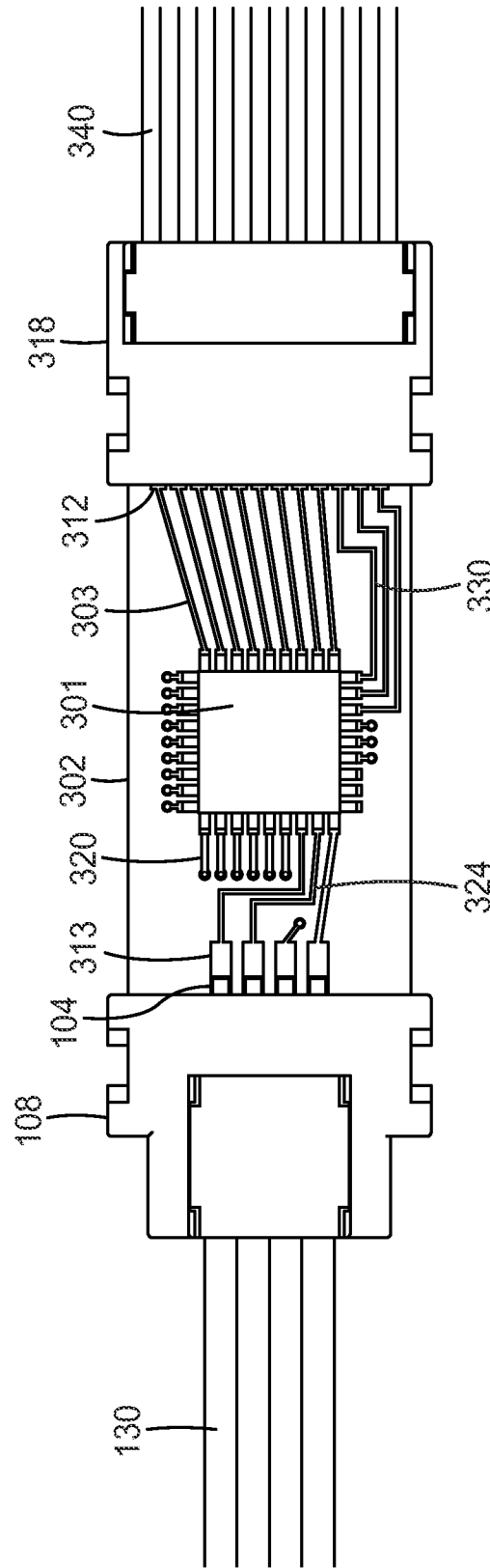
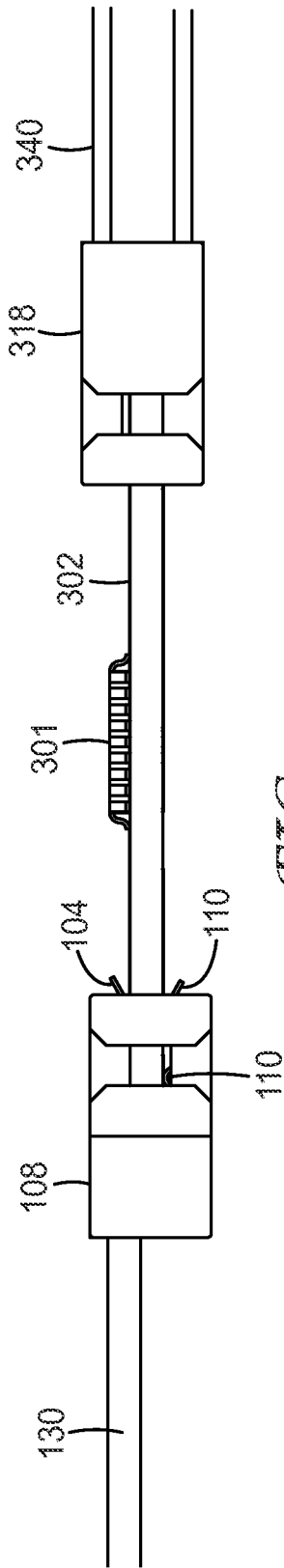


FIG. 2b



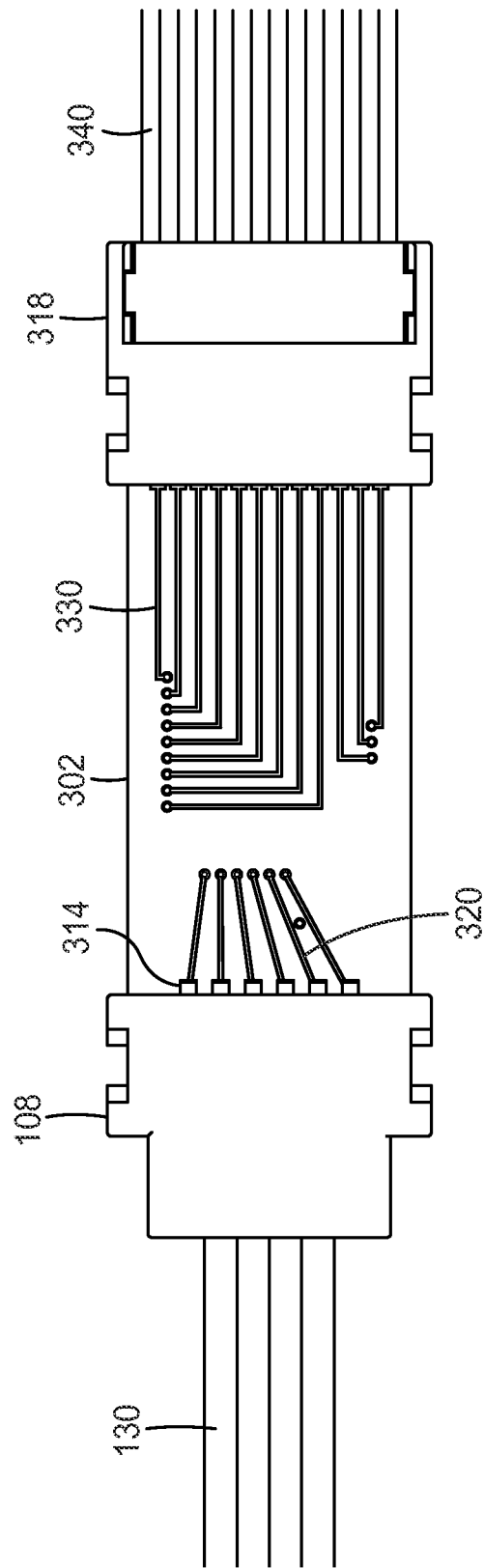


FIG. 3C

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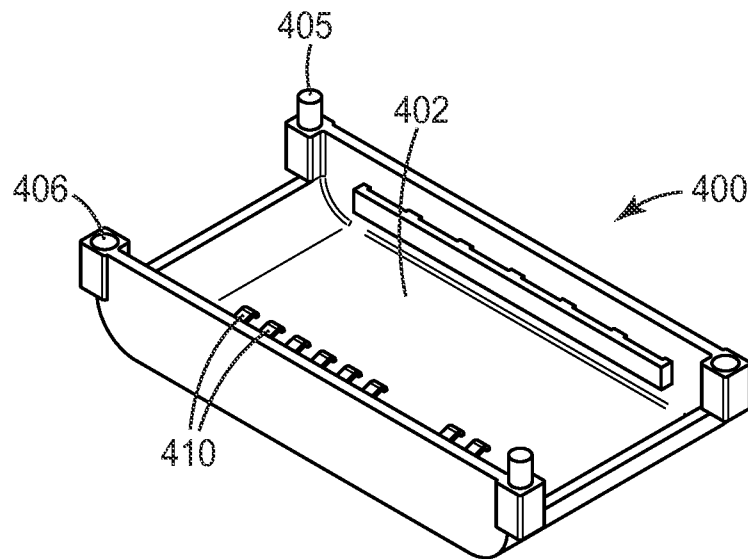


FIG. 4a

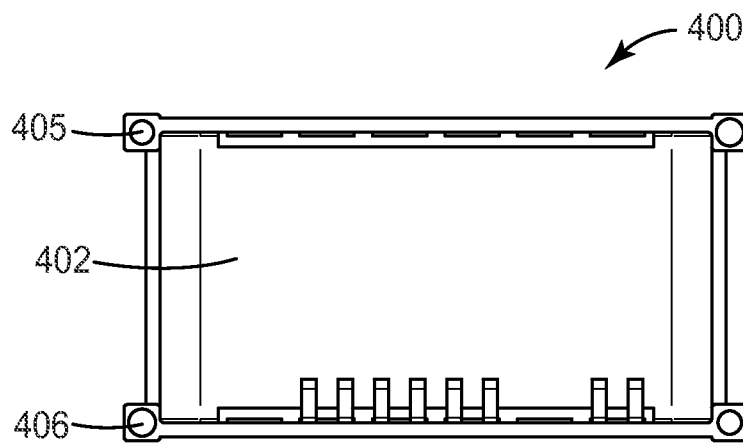


FIG. 4b

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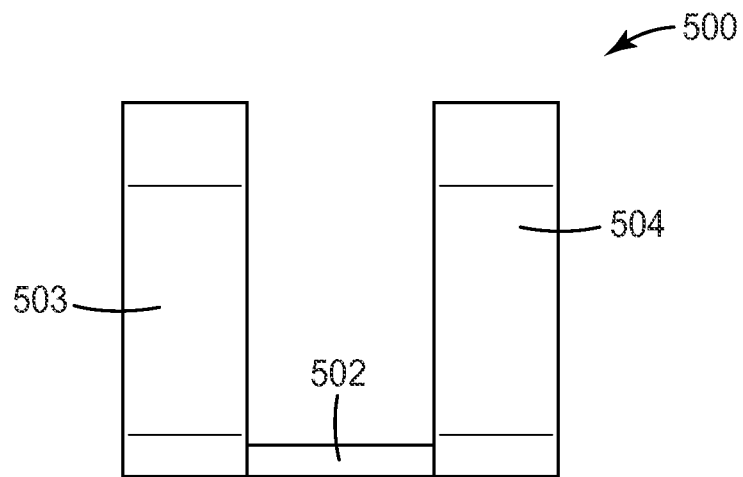


FIG. 5a

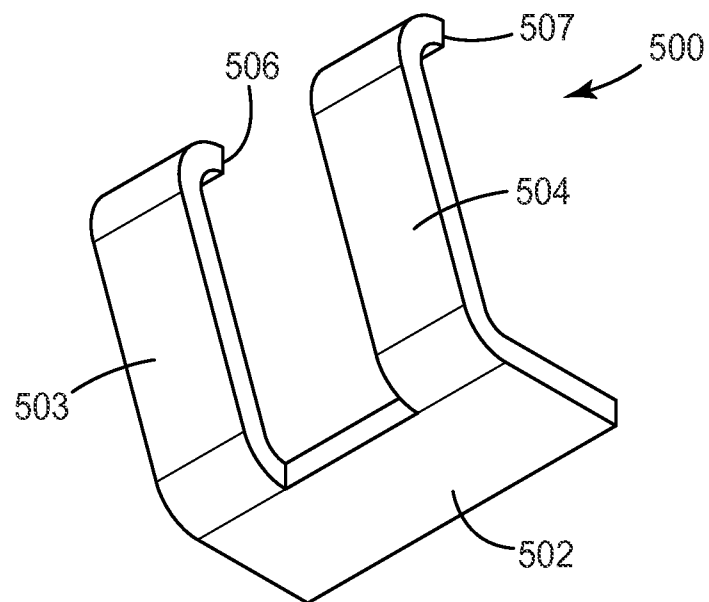
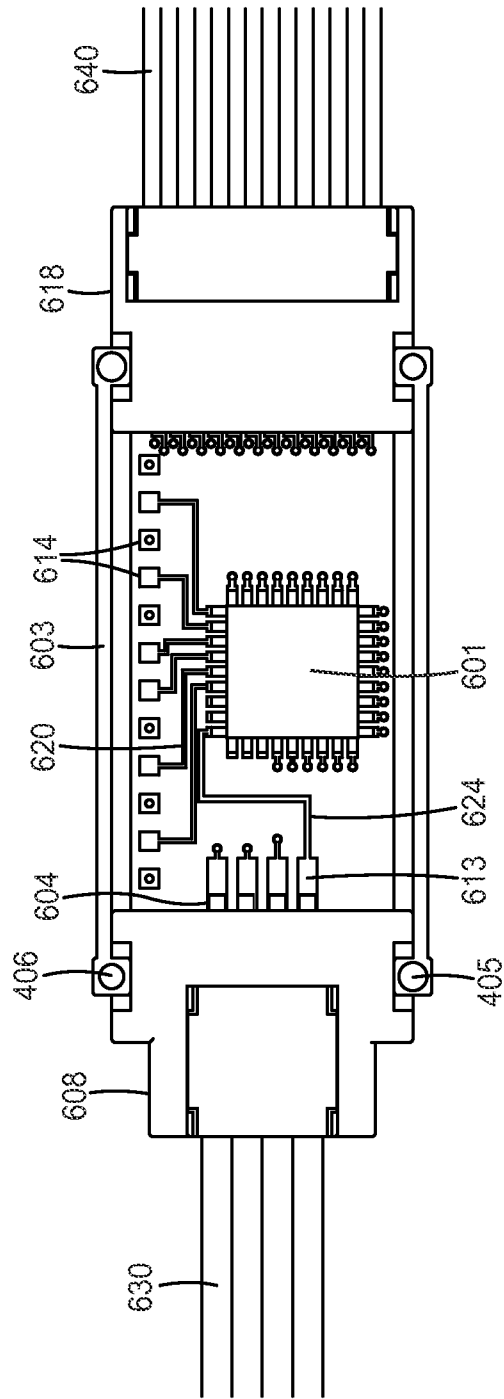
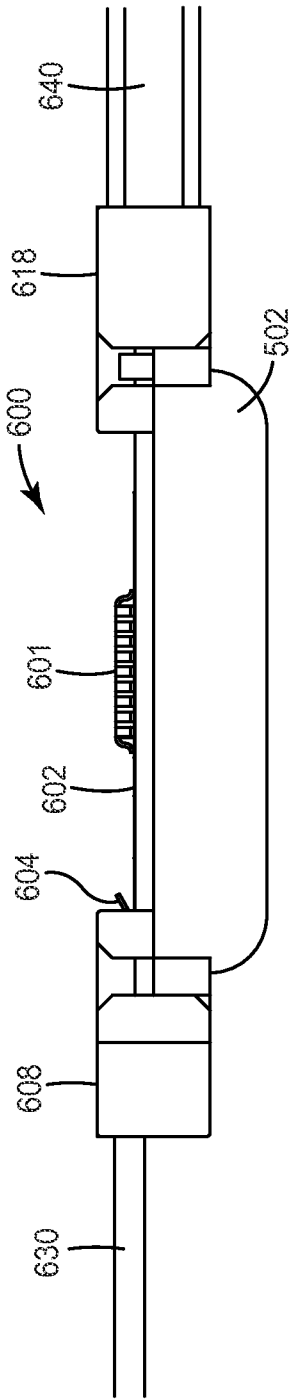


FIG. 5b



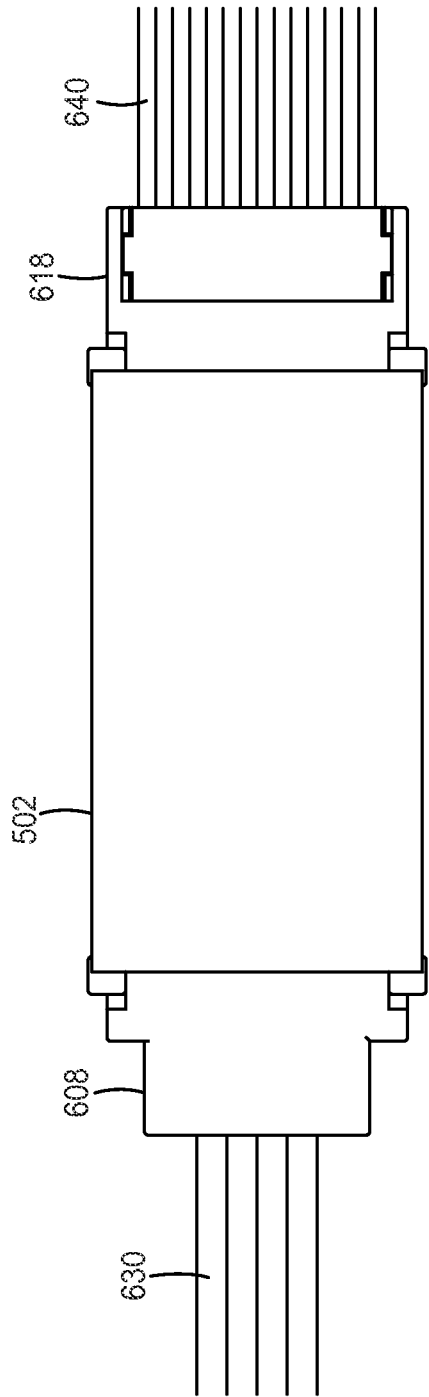


FIG. 6c

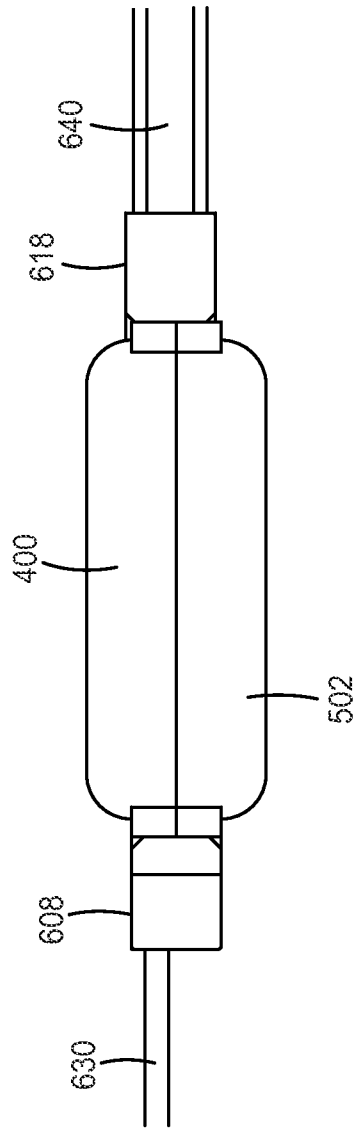


FIG. 6d

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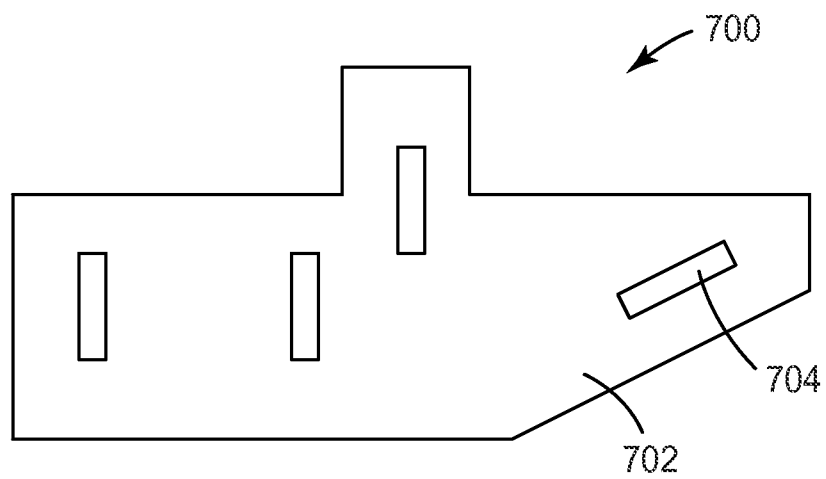


FIG. 7a



FIG. 7b

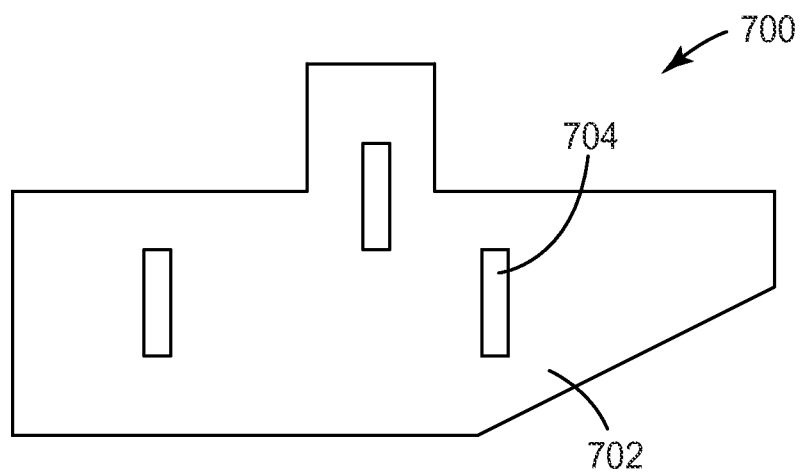


FIG. 7c

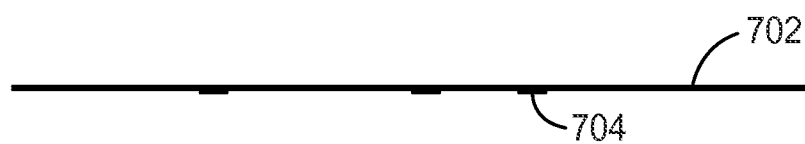


FIG. 7d

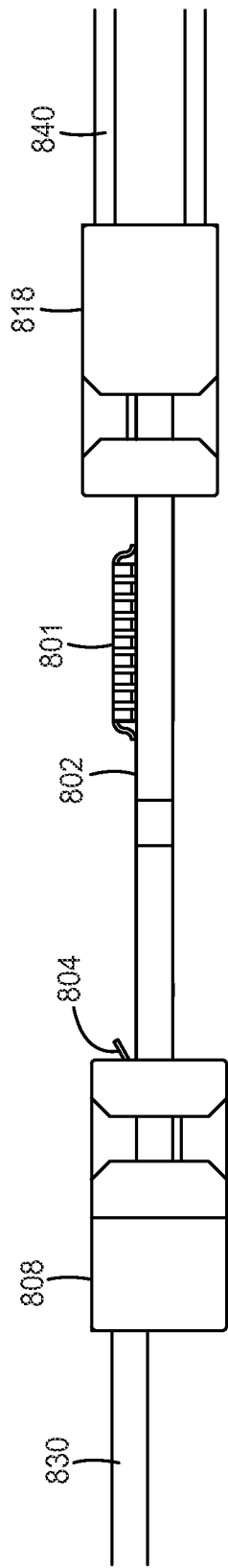


FIG. 8a

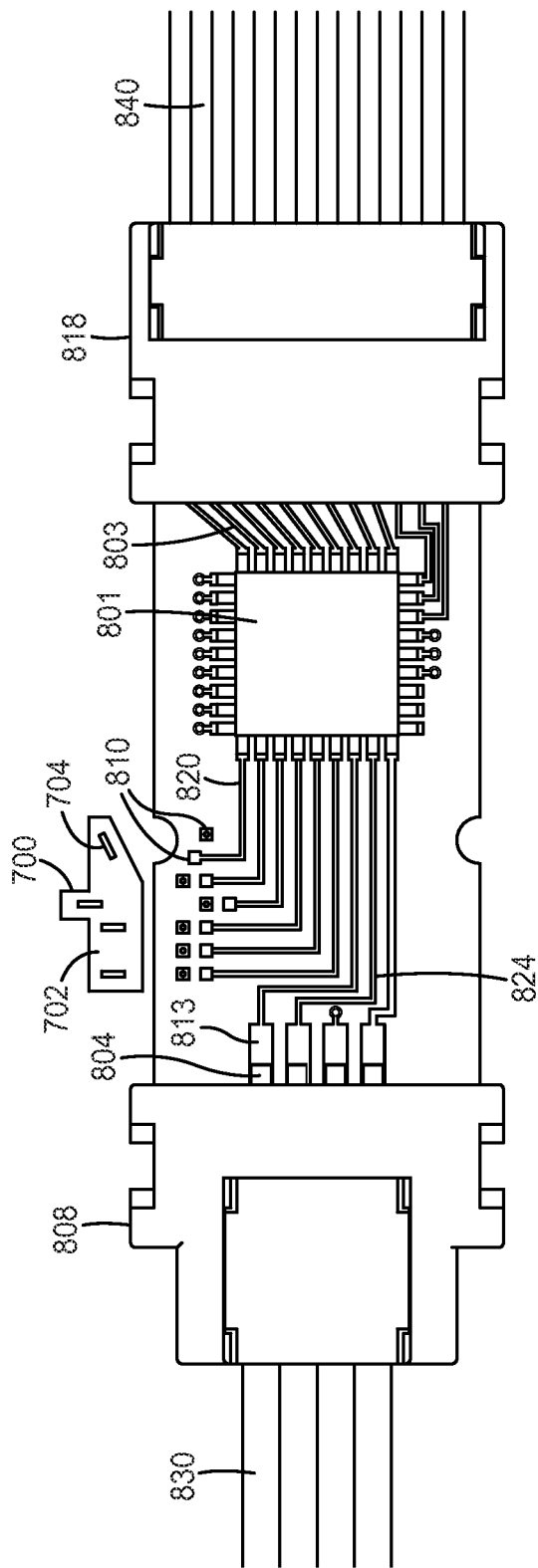


FIG. 8b

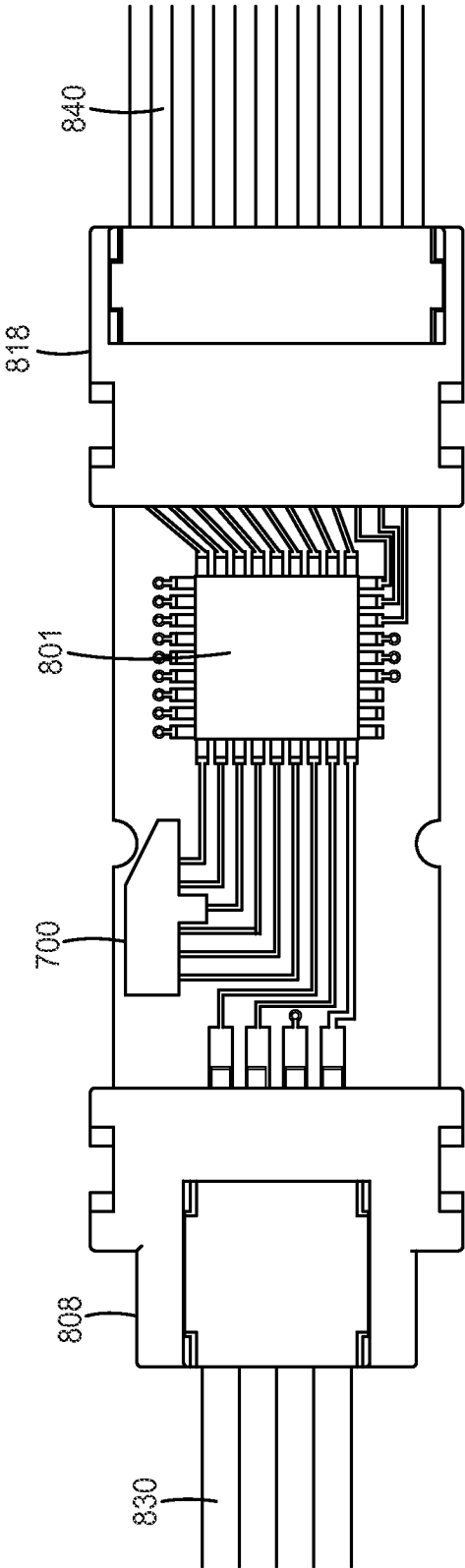


FIG. 8c

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/022312

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/40
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 044 949 A1 (IBM [US]) 3 February 1982 (1982-02-03) abstract page 6, last paragraph - page 9, paragraph 3	1-7
X	----- US 5 428 748 A (DAVIDSON ANDREW M [GB] ET AL) 27 June 1995 (1995-06-27) column 1, line 27 - column 2, line 2 column 10, line 30 - line 58 figure 6	1-7
X	----- JP 62 005424 A (MATSUSHITA ELECTRIC IND CO LTD) 12 January 1987 (1987-01-12) abstract figures 1, 3, 4 ----- -/-	1-7

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

3 May 2012

Date of mailing of the international search report

21/05/2012

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INTERNATIONAL SEARCH REPORT

International application No

PCT/US2012/022312

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	JP 1 265697 A (MATSUSHITA ELECTRIC WORKS LTD) 23 October 1989 (1989-10-23) abstract -----	1-7
A	JP 2005 286471 A (AUTO NETWORK GIJUTSU KENKYUSHO; SUMITOMO WIRING SYSTEMS; SUMITOMO ELEC) 13 October 2005 (2005-10-13) abstract -----	1-7

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2012/022312

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