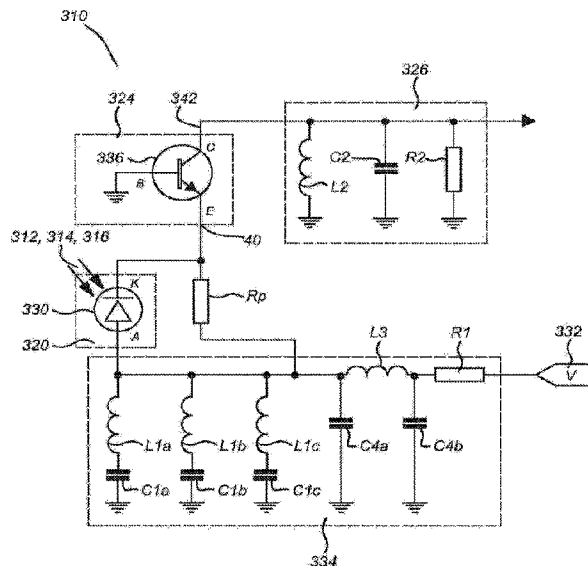




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(57) **Abrégé/Abstract:**

A sensor circuit (10), including a silicon photomultiplier, SiPM, sensor (20), a voltage source (32), a current-to-voltage converter (24), and a limiting bias circuit (34). The SiPM sensor (20) has avalanche photodiode, APD, elements (30) connected in parallel between a cathode (K) and an anode (A). The voltage source (32) is configured to apply a reversed bias voltage (V_b) across the SiPM sensor, so that each APD element operates in reverse-biased Geiger mode, and the APD elements operate in integration mode. The bias circuit (34) is connected between the voltage source (32) and the anode (A), and is configured to limit currents through the APD elements, and to present an AC load impedance for an alternating current within a predetermined operating frequency range (f_o) generated by the APD elements at the anode (A) as well as a DC load impedance, such that said AC load impedance is lower than said DC load impedance.

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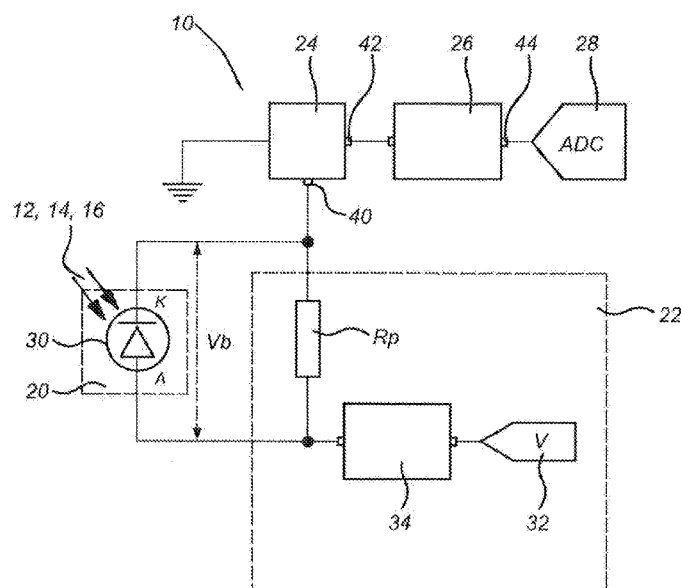
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Fig. 3A



(57) **Abstract:** A sensor circuit (10), including a silicon photomultiplier, SiPM, sensor (20), a voltage source (32), a current-to-voltage converter (24), and a limiting bias circuit (34). The SiPM sensor (20) has avalanche photodiode, APD, elements (30) connected in parallel between a cathode (K) and an anode (A). The voltage source (32) is configured to apply a reversed bias voltage (V_b) across the SiPM sensor, so that each APD element operates in reverse-biased Geiger mode, and the APD elements operate in integration mode. The bias circuit (34) is connected between the voltage source (32) and the anode, and is configured to limit currents through the APD elements, and to present an AC load impedance for an alternating current within a predetermined operating frequency range (f_o) generated by the APD elements at the anode (A) as well as a DC load impedance, such that said AC load impedance is lower than said DC load impedance.

[Continued on next page]



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Sensor Front End

Technical Field

[0001] The invention relates to a front-end circuit for a non-linear sensor. Furthermore,
5 the invention relates to a method for operating such a circuit.

Background Art

[0002] Electronic sensors, as used in measurement devices and communication
devices, often exhibit non-linear behaviour. Such non-linear behaviour could influence
10 the intended measurements or receptions by intermodulation. Intermodulation (IM) or
intermodulation distortion (IMD) is the amplitude modulation of signals containing two or
more different frequencies, caused by nonlinearities or time variance in a system.

[0003] Non-linear electronic sensors can be sensors such as a Light Dependent
Resistor (LDR), photodiodes (PD), avalanche photodiodes (APD), Silicon
15 Photomultipliers (SiPM), Hall effect sensors, negative temperature coefficient (NTC)
resistors or positive temperature coefficient (PTC) resistors. All said detectors have in
common that the sensed property will change the electrical behaviour of the sensor, e.g.
by allowing a greater current at a given bias voltage.

[0004] A sensor of a particular type, the Silicon Photomultiplier (SiPM), has emerged
20 as an interesting photo-detection solution for sensing applications with very low intensity
levels down to a single photon. A SiPM-based sensor offers several advantages, such as
low operational voltage, good photon detection efficiency (PDE), high detection gain, and
fast response times. These properties render SiPM sensors very useful as photon
counting devices in scientific or medical instruments. A SiPM is formed by an array of
25 avalanche photodiode (APD) pixel elements that are operated in Geiger mode. In this
mode, the APD elements are subjected to a reverse bias voltage for which the absolute
value is higher than the characteristic breakdown voltage of each APD element. When a
photon hits an APD element, an avalanche breakdown is triggered, which leads to the
generation of an output current pulse. The APD can thus function in a so-called "photo
30 counting mode", in which single photon detections can be recorded and counted. An
APD element operated in this mode is referred to as a single photo avalanche diode
(SPAD). The fundamental difference between SPADs and APDs is that SPADs are
specifically designed to operate with a reverse bias voltage well above the breakdown
voltage.

35 [0005] The above-mentioned properties make SiPM sensors suitable for applications in
free space visible light communication (VLC) systems, and in particular for underwater

VLC systems. However, when optical communication methods are used that rely on amplitude modulation for coding information into the light beam, the SiPM should be operated in a so-called "integration mode". In said mode, an output signal is generated that represents a statistical average of a large number of photons from the impinging light beam. For this mode, the SiPM preferably includes a very large number of APD elements, e.g. in the order of thousands or more elements, which are connected in parallel. An amplitude-modulated optical signal with certain intensity may then simultaneously trigger many temporally overlapping avalanche discharges in the SiPM, so that a SiPM output signal can be obtained that is formed from a sum of many photon detection currents from the individual APD elements. If the number of simultaneous detections is sufficiently large, the sum of detection currents will closely follow the amplitude modulation of the incoming light beam. This mode of operation imposes new design challenges when using SiPM sensors.

[0006] In general, most circuits of the prior art are concerned with photo counting mode and therefore cannot be easily applied to integration mode, which is advantageous for free space VLC systems.

[0007] A VLC receiver is a communication receiver with all the associated design challenges. Such receivers should have a low noise floor, good frequency selectivity, low intermodulation (IM) distortion, high dynamic range, etc. Good frequency selectivity and high dynamic range are important when there are multiple light sources that may interfere with the light communication signal. Examples of such conditions could be an office environment having ambient and modulated light sources like fluorescent lighting, flat panel backlights, infrared (IR) communications, etc., or an underwater environment, where an ROV might be equipped with mounted laser scanners, dimmable floodlights or other systems using modulated light.

[0008] These modulated light sources might interfere with the communication signal in an improperly operated SiPM causing a distortion effect called intermodulation. The wanted and unwanted signals are then impossible to separate during later processing.

[0009] SiPM sensors are vulnerable to over-currents. In order to overcome this problem, commonly current-limited power supplies are used, as shown in the SiPM Experiment Guide by Sensl. Current-limiting circuits have a non-zero source resistance when operating at or near their current limit. A non-zero source resistance will cause the voltage over the SiPM to vary with the current through the SiPM, thereby varying the gain which may cause intermodulation distortion.

[0010] Patent document US 2016/0181459 A1 describes a method for improving the dynamic range in integration mode by applying an automatic gain control method.

However, this document does not solve the intermodulation distortion when using a SiPM in a visible light communication system in integration mode.

[0011] It would be desirable to provide a protective front-end circuit for a SiPM sensor in a free space VLC receiver.

5

Summary of Invention

[0012] The present invention addresses the above-mentioned challenges, most importantly the inherent intermodulation distortion caused by state of the art front-end circuits.

- 10 [0013] According to a first aspect, there is provided a sensor circuit comprising, as illustrative embodiment, a silicon photomultiplier (SiPM) sensor, a voltage source, a current-to-voltage converter, and a limiting bias circuit. The SiPM sensor includes an array of avalanche photodiode (APD) elements that are connected in parallel between a common cathode and a common anode. The voltage source is configured to apply a
- 15 reversed bias voltage across the APD elements, to let each of the APD elements operate in reverse-biased mode, and to let the array of APD elements operate in integration mode. The current-to-voltage converter is electrically connected with an input terminal to the common cathode of the APD elements, and configured to convert a current from the common cathode into a voltage and provide said voltage on an output terminal of said
- 20 converter. The limiting bias circuit is connected between the voltage source and the common anode of the APD elements. This filter is configured to limit currents through the APD elements, and configured to present an AC load impedance for an alternating current within a predetermined operating frequency range f_o of the light modulation generated by the APD elements at the common anode as well as a DC load
- 25 impedances, such that said AC load impedance is lower than said DC load impedance. The AC load impedance may for instance be in a range of 10 to 10000 times lower than the DC load impedance. Depending on circumstances, said AC load impedance to said DC load impedance may differ by other factors, given that said AC load impedance is always lower than said DC load impedance.
- 30 [0014] Briefly stated, the present invention minimizes the intermodulation distortion and maximizes the dynamic range by using a different front-end circuit making a SiPM thus suitable to be used in a VLC system. In situations with ambient light sources, a noise floor is created which, in conventional circuits would reduce the dynamic range of a VLC receiver,
- 35 [0015] SiPM sensors are known to have a gain characteristic in which the detection output current increases with increasing value of reversed bias overvoltage applied

across the APD elements. The limiting bias circuit limits the maximum current passing through the APD elements during avalanche discharge, and simultaneously presents a low load impedance for alternating currents generated within the APD elements, at least for current oscillations within a predetermined operating frequency range f_0 representing the optical signals that the SiPM is expected to receive. This operating frequency range f_0 covers not only the (sub-)band Δf_c for the actual VLC signal (with centre frequency f_c), but also additional frequency components associated with interfering light that oscillates at different frequencies than the VLC frequency range. The bias circuit is designed such that the voltage over the SiPM is kept as constant as possible, thereby realising an overvoltage regularization. Because of this overvoltage regularization, the signal gain provided by the SiPM sensor is kept as constant as possible, so that the SiPM output responds as linearly as possible to amplitude variations in the detected light. Due to the near constant gain and linear amplitude response, the SiPM sensor converts a harmonic incoming light signal into an essentially harmonic electrical output signal, while avoiding creating higher order harmonic components in the electrical output signal. When the SiPM sensor is simultaneously receiving multiple optical signals with at least two distinct frequency components, e.g. both a communication signal and an interference signal on another frequency, the occurrence of intermodulation in the SiPM output current is reduced or even eliminated.

[0016] In embodiments, the bias circuit presents an AC load impedance lower than the DC load impedance for frequencies above a lower frequency bound. This is to allow for slow changes in ambient light conditions to prevent overheating of the SiPM sensor. Further, this allows for slow changes in ambient light to change the bias voltage over the SiPM and thus regulate the gain and PDE of the SiPM. The lower bound of said frequencies may for instance be 100 kHz, 10 kHz, 1 kHz, 100 Hz, 10 Hz, 1 Hz or 0,1 Hz. In addition, said bias circuit may optionally have an upper frequency bound. The upper frequency bound may for instance be one of 1 MHz, 10 MHz, and 100 MHz.

[0017] In embodiments, the DC load impedance of the bias circuit is such that the current through the SiPM is limited to a value that prevents overheating of the SiPM.

Further, the DC load impedance may be optimized to reduce the power consumption of the SiPM in high ambient lighting. Even further, the DC load impedance may act as an AGC by reducing the bias voltage under high ambient lighting. The DC load impedance may be, for example, in a range of 100 k Ω – 10 Ω . The AC load impedance for said operating frequency range is in a range between 0 Ω and 1 k Ω , more preferably between 0 Ω and 100 Ω and most preferably between 0 Ω and 10 Ω .

[0018] In embodiments, the bias circuit comprises a limiter resistor R1, which is connected in series between the voltage source and the common anode of the SiPM.

[0019] The resistor R1 electrically interconnects the SiPM and the voltage source, and acts to limit the maximum current drawn from the voltage source that will pass through the SiPM. This resistor R1 may simultaneously form or substantially contribute to the DC load impedance seen by the SiPM at the common anode.

[0020] The linear range of a SiPM is limited by the number of APD elements contained within the SiPM. The SiPM will saturate if all APD elements are firing at the same time. By reducing the voltage over the SiPM, the photo detection efficiency and gain are reduced as well thereby limiting the number of simultaneous firing APD elements. Therefore, in some embodiments, the output voltage of the voltage source and a resistance of the limiter resistor are selected so that the resulting average overvoltage across the SiPM causes operation in a linear part of a photon detection efficiency response characteristic and gain characteristic of the SiPM sensor.

[0021] Both the photon detection efficiency and the gain of the SiPM sensor are dependent on the bias voltage or bias over-voltage across the APD elements. As long as the SiPM sensor is not operating in a saturated portion of its PDE and gain characteristics, more incident light that hits the APD elements will cause more current to flow through the resistor R1 (at least for quasi-static i.e. relatively slow variations in the incident light intensity). Because of the constant output of voltage source 32 and fixed value for R1, this current increase will cause the bias voltage across the APD elements to become lower. In this manner, both the gain and the PDE are automatically reduced, at least for slow light intensity fluctuations that have longer characteristic time scales than the response time for the shunting function of the filter. For instance the breakdown voltage of the APD elements may be about 24.5 Volts (or within a range of 24.2 Volts to 24.7 Volts), an overvoltage of the APD elements may be within a range of 1.0 Volts to 5.0 Volts, the output voltage of the voltage source may be about 27 Volts, and the limiter resistor may have a resistance of about 120 Ω .

[0022] In further embodiments, the bias circuit comprises a capacitor C1 that is connected between the resistor and the common anode on the one hand, and to ground on the other hand. This capacitor may for instance have a capacitance of at least 100 μF .

[0023] The limiter resistor and the capacitor jointly form a passive low-pass RC-filter, which is provided between (and electrically connected to) the SiPM sensor and the voltage source. The low-pass RC filter is configured to present a low load impedance for alternating currents within a predetermined operating frequency range fo originating from

the SiPM anode, such that current oscillations resulting from avalanche discharge due to incoming optical signals at frequencies within the predetermined operating frequency range f_0 are essentially shunted via the capacitor C_1 , and the bias voltage V_b across the SiPM is kept essentially constant for incoming optical signals within this operating frequency range. Intermodulation effects in the output response of the SiPM sensor are thus suppressed.

[0024] In alternative embodiments, the bias circuit comprises a resonant circuit section that is connected in parallel between the resistor and the common anode on the one hand, and to ground on the other hand. This circuit section includes a capacitor and an inductor connected in series, and is configured to present the low load impedance for alternating currents within at least part of the predetermined operating frequency range generated by the APD elements at the common anode.

[0025] The limiter resistor and series LC circuit section jointly form a passive band-stop LC-filter, which is provided between (and electrically connected to) the APD elements and the voltage source. The values for L and C in the resonant circuit section may be selected such that the complex impedance $Z(f) = j \cdot X_L(f) + j \cdot X_C(f) = 2\pi \cdot j \cdot f \cdot L - j / 2\pi \cdot f \cdot C$ vanishes at a centre frequency f_i and has generally low impedance values in the range Δf_i around this centre frequency, so that the LC resonant circuit section essentially acts as a shunt for the alternating APD currents within this operating frequency range.

[0026] In yet a further embodiment, the low-pass filter comprises further resonant circuit sections that are connected in parallel between the resistor and the common anode on the one hand, and to ground on the other hand. Each of the further circuit sections includes a further capacitor and a further inductor connected in series, and each is configured to present a low load impedance for alternating currents within further parts of the predetermined operating frequency range generated by the APD elements at the common anode.

[0027] A plurality of LC resonant circuit sections with different centre frequencies and adjacent and possibly overlapping resonant frequency bands can be used to form low load impedances for alternating currents from the APD element array over a wider operating frequency range. Each LC resonant section may cover a sub-band f_i of the operating frequency range f_0 representative of the optical signals that the SiPM sensor is expected to receive.

[0028] In circumstance where the interfering frequencies are known, the LC resonant circuits can be tuned to these frequencies such that the risk of intermodulation is reduced.

[0029] In alternative embodiments, the bias circuit may employ active components like transistors, operational amplifiers, signal processors using analogue to digital converters (ADC) and/or digital to analogue converters (DAC), microprocessors, DC to DC converters, inverters and similar such devices.

5 [0030] In one of such embodiments, the active circuit may act as a time-varying current limiter. Said active circuit uses an optimized time constant such that the load resistance for AC currents is as low as possible over the operating frequency range, while at the same time the SiPM is always operating within the safe operating area (SOA) similar to power semiconductor devices.

10 [0031] In another one of such embodiments, the active circuit may act as a plurality of time-varying current limiters. Each of said current limiters uses an optimized current limit. Further, each of said current limiters uses an optimized time constant. For example, one of said current limiters is optimized to operate the SiPM within the SOA. A second of said current limiters could be optimized to mitigate intermodulation effects from certain
15 ambient and/or artificial light sources. In embodiments with several current limiters, the first current limiter is optimized to protect the SiPM from overcurrent, while additional current limiters are optimized, e.g. in their time constant and current limiting effect, to mitigate effects of ambient light sources.

[0032] In a further of such embodiments, the passive components of said bias circuits
20 may be implemented using active circuitry which form gyrators, eg using operational amplifiers.

[0033] In embodiments, the current-to-voltage converter comprises a common-base circuit, including a transistor with an emitter that is connected to the common cathode of the SiPM sensor, with a base that is connected to ground, and with a collector that forms
25 a signal output.

[0034] The common-base circuit is configured to present at the emitter a low load impedance for an alternating current from the common cathode of the SiPM sensor, to assist the bias circuit in keeping the reverse bias voltage across the APD elements as constant as possible. The common base of the transistor electrically isolates the SiPM
30 sensor from the subsequent detector circuit components. The emitter of the transistor presents a further AC load impedance for the alternating current within the predetermined operating frequency range f_0 that is generated by the APD elements at the common cathode. This further AC load impedance may be in the order of Ohms to tens of Ohms, depending on the amplitude of the alternating current generated at the
35 cathode.

[0035] In embodiments, the current-to-voltage converter comprises an operational amplifier with an output, a non-inverting input that is connected to ground, and with an inverting input that is connected to the common cathode of the APD elements as well as to a feedback voltage from the output via a further resistor. Other types of amplifiers may be used in alternative embodiments.

[0036] In further embodiments, the sensor circuit includes a further resistor R_p that is connected in parallel with the SiPM sensor and between the current-to-voltage converter and the current limiting bias circuit. This further resistor is configured to maintain a non-zero baseline current through the current-to-voltage converter.

[0037] The further resistor R_p electrically interconnects the current-to-voltage converter and the current limiting bias circuit, preferably with one terminal of the further resistor connected between the resistor R_1 on the one hand, and the capacitor C_1 or the LC resonant circuit sections on the other hand.

[0038] In embodiments, the sensor circuit comprises a parallel resonant band-pass filter, which is provided between the output of the current-to-voltage converter and an analogue sensor output, and which is configured to pass only a frequency range corresponding to a carrier wave and a maximum bitrate of the communication signal to the analogue sensor output.

[0039] In a second aspect, and in accordance with the advantages and effects described herein above, there is provided a method for operating a sensor circuit according to the first aspect. The method comprises:

[0040] - applying, with the voltage source, a reversed bias voltage across the APD elements of the SiPM sensor, to let each of the APD elements operate in reverse-biased mode, and to let the array of APD elements operate in integration mode;

[0041] - receiving, with the APD elements, a plurality of amplitude-modulated light signals which oscillate in time corresponding to frequency bands within a predetermined operating frequency range f_0 ;

[0042] - converting, with the current-to-voltage converter, a current from the common cathode of the array of APD elements into a voltage, and providing said voltage on the output terminal of said converter, and;

[0043] - forming, with the bias circuit, an AC load impedance for an alternating current within the predetermined operating frequency range generated by the APD elements at the common anode, as well as a DC load impedance, such that said AC load impedance is lower than said DC load impedance, thereby reducing or minimizing intermodulation distortion in the current generated by the SiPM sensor in response to the received light

signals. The AC load impedance may for instance be 10 to 10000 times lower than the DC load impedance.

[0044] Exemplary embodiments of the present disclosure will be described herein below with reference to the accompanying drawings. However, the embodiments of the present disclosure are not limited to the specific embodiments and should be construed as including all modifications, changes, equivalent devices and methods, and/or alternative embodiments of the present disclosure.

[0045] The terms “have,” “may have,” “include,” and “may include” as used herein indicate the presence of corresponding features (for example, elements such as numerical values, functions, operations, or parts), and do not preclude the presence of additional features.

[0046] The terms “A or B,” “at least one of A or/and B,” or “one or more of A or/and B” as used herein include all possible combinations of items enumerated with them. For example, “A or B,” “at least one of A and B,” or “at least one of A or B” means (1) including at least one A, (2) including at least one B, or (3) including both at least one A and at least one B.

[0047] The terms such as “first” and “second” as used herein may modify various elements regardless of an order and/or importance of the corresponding elements, and do not limit the corresponding elements. These terms may be used for the purpose of distinguishing one element from another element. For example, a first element may be referred to as a second element without departing from the scope the present invention, and similarly, a second element may be referred to as a first element.

[0048] It will be understood that, when an element (for example, a first element) is “(operatively or communicatively) coupled with/to” or “connected to” another element (for example, a second element), the element may be directly coupled with/to another element, and there may be an intervening element (for example, a third element) between the element and another element. To the contrary, it will be understood that, when an element (for example, a first element) is “directly coupled with/to” or “directly connected to” another element (for example, a second element), there is no intervening element (for example, a third element) between the element and another element.

[0049] The expression “configured to (or set to)” as used herein may be used interchangeably with “suitable for” “having the capacity to” “designed to” “adapted to” “made to,” or “capable of” according to a context. The term “configured to (set to)” does not necessarily mean “specifically designed to” in a hardware level. Instead, the expression “apparatus configured to...” may mean that the apparatus is “capable of...” along with other devices or parts in a certain context.

[0050] The terms used in describing the various embodiments of the present disclosure are for the purpose of describing particular embodiments and are not intended to limit the present disclosure. As used herein, the singular forms are intended to include the plural forms as well, unless the context clearly indicates otherwise. All of the terms used herein including technical or scientific terms have the same meanings as those generally understood by an ordinary skilled person in the related art unless they are defined otherwise. The terms defined in a generally used dictionary should be interpreted as having the same or similar meanings as the contextual meanings of the relevant technology and should not be interpreted as having ideal or exaggerated meanings unless they are clearly defined herein. According to circumstances, even the terms defined in this disclosure should not be interpreted as excluding the embodiments of the present disclosure.

[0051] For the purpose of determining the extent of protection conferred by the claims of this document, due account shall be taken of any element which is equivalent to an element specified in the claims.

Brief Description of Drawings

[0052] Embodiments will now be described, by way of example only, with reference to the accompanying schematic drawings in which corresponding reference symbols indicate corresponding parts. In the drawings, like numerals designate like elements.

[0053] Figure 1 shows a graph with two exemplary current transfer functions for SiPM sensors connected to driving circuits with different load impedances;

[0054] Figure 2 shows a block diagram for a sensor circuit, according to an embodiment;

[0055] Figure 3A presents a diagram for a sensor circuit according to a further embodiment;

[0056] Figure 3B presents a detail from the circuit of figure 3A;

[0057] Figure 4 schematically shows further details for the embodiment from in figure 3A, and

[0058] Figures 5-8 show schematic diagrams for sensor circuits according to other embodiments.

[0059] The figures are meant for illustrative purposes only, and do not serve as restriction of the scope or the protection as laid down by the claims.

Description of Embodiments

[0060] The following is a description of certain embodiments of the invention, given by way of example only and with reference to the figures.

[0061] In general, a SiPM sensor may include a matrix of reverse-biased Geiger Mode avalanche photodiode (APD) elements, which are connected in parallel between a common cathode K and a common anode A. A reverse bias voltage V_b or V_{SiPM} applied across the APD elements is formed as a sum of a breakdown voltage V_{bd} and an overvoltage V_o . The breakdown voltage V_{bd} is a minimum reverse bias voltage that is needed to induce self-sustaining avalanche multiplication in an APD element upon detection of a photon. For this discussion, the breakdown voltage V_{bd} is selected to be 24.5 Volts, but in practice can have other values depending on the design of the SiPM sensor. The overvoltage V_o is the excess reverse bias voltage across the APD elements.

[0062] During operation, the APD elements receive optical signals and produce electrical photocurrents with magnitudes that depend on the intensity of the incident light. In addition, the signal gain produced by the SiPM sensor - which in this discussion is in the order of 10^6 - is highly dependent on the value for the overvoltage V_o across the common cathode and anode of the APD elements. For example, the gain of an exemplary SiPM sensor may be approximated by equation 1:

$$gain_{SiPM} = (V_{SiPM} - 24.5) \cdot 10^6 \quad (1)$$

[0063] In this equation, V_{SiPM} is the voltage applied across the common cathode and anode of the APD elements. The voltage dependency of the photo detection efficiency (PDE) has been ignored in equation 1 for simplicity. The current passing through the SiPM sensor may be calculated by equation 2:

$$I_{SiPM} = gain_{SiPM} \cdot I_{photo} \quad (2)$$

[0064] In this equation, I_{photo} is the induced photocurrent before multiplication.
[0065] It will be understood that a biasing circuit, which is directly electrically connected to the SiPM sensor, presents a complex load Z_{load} to the SiPM sensor. The voltage V_{SiPM} will thus depend on the current I_{SiPM} according to equation 3:

$$V_{SiPM} = V_{set} - Z_{load} \cdot I_{SiPM} \quad (3)$$

[0066] In this equation, V_{set} is the set-point voltage applied across the common cathode and anode of the APD elements, which corresponds to the voltage when no current is flowing through the SiPM. Substituting equations 1, 2 and 3 into each other yields equation 4, which describes the current through the SiPM as a function of the set-point voltage V_{set} , the induced photocurrent I_{photo} , and the load impedance Z_{load} .

$$I_{SiPM} = \frac{(V_{set} - 24.5) \cdot 10^6 \cdot I_{photo}}{1 + Z_{load} \cdot 10^6 \cdot I_{photo}} \quad (4)$$

[0067] From equation 4, it becomes clear that the current transfer function of the SiPM becomes a non-linear function of the photocurrent I_{photo} for load impedances other than 0 Ω . Figure 1 plots results for two exemplary load impedance values $|Z| = 0 \Omega$ and $|Z| = 50 \Omega$. It is apparent from figure 1 that the current transfer function becomes non-linear for even small values of $|Z|$.

[0068] One cause of the intermodulation in SiPM photo receivers in integration mode is non-linearity. Said non-linearity may be caused by varying gain and PDE. Said gain and PDE are dependent on the applied bias voltage. Another cause of intermodulation is saturation in the SiPM if too much incident light hits the surface of the SiPM. The solution to minimize the intermodulation distortion is thus to keep the bias voltage over the SiPM as constant as possible for AC signals while allowing some variation for DC signals. In addition, some form of automatic gain control is necessary to prevent the SiPM from saturating.

[0069] According to the present invention, the problem of this non-linearity is recognized, and is mitigated by keeping the load impedance as seen by the SiPM sensor as low as possible for modulated light in frequency ranges that the SiPM sensor is expected to receive.

[0070] Figures 2 and 3A-3B show block diagrams for a SiPM front end circuit 10, which may be used in a VLC receiver, for instance in a VLC receiver of an underwater communication system. As shown in figures 2 and 3A, the circuit 10 comprises a SiPM module 20, a bias circuit section 22, and a current-to-voltage converter stage 24. The sensor circuit 10 may further include a bandpass filter 26, and an analogue-to-digital converter (ADC) 28.

[0071] Figures 3A and 3B show that the SiPM sensor 20 comprises an array of APD elements 30, which are connected in parallel between a common cathode K and a common anode A. The APD elements 30 are collectively indicated in figure 3A by reference numeral 30 for simplicity, whereas figure 3B illustrates the parallel arrangement of individual elements 30k (k = a, b, c, ...) with associated internal resistors

Rk for passive quenching. The APD elements 30 are configured to allow sensing of optical signals 12, 14, 16 originating from various sources in the vicinity, and to produce electrical output currents that have magnitudes that relate to the intensity of the incident light.

5 [0072] The VLC signal 12 of interest may be light of a predetermined wavelength, which is first amplitude modulated at a fixed centre frequency f_c to form the data carrier (e.g. in the range of several Hz to several GHz), and in which the actual data is imprinted by further modulation using a modulation scheme with a predetermined maximum data bitrate that is substantially lower than the centre frequency f_c .

10 [0073] Light signals 16 from other amplitude-modulated sources may also be present, which may simultaneously impinge on the SiPM sensor 20 and cause interference with the VLC signals 12 of interest. These interfering light signals 16 may for instance fall within frequency ranges in a bandwidth from several Hz to several hundreds of MHz. Ambient light 14 with static or very slowly amplitude variation characteristics may also be
15 simultaneously received by the SiPM sensor 20.

[0074] For instance, in underwater VLC applications, VLC signals 12 may be formed by amplitude modulation of blue light using a carrier frequency f_c of 800 kHz. In this example, modulation with a predetermined maximum data bitrate is used.

[0075] In principle, a bitrate value between several bits per second to hundreds of
20 megabits per second may be used, depending on the carrier frequency and modulation type. Possible bitrates may be 5 bits/sec to 100 Mbps (mega bit per second). In some embodiments, bitrates of 10 bits/sec to 1Mbps may be advantageous. A preferred implementation uses a bit rate of 25 kbps.

[0076] The wavelength of the light is not generally limited to a certain range. However,
25 the optimum wavelength might be dictated by the propagation medium in which the VLC system operates. Further wavelength limitations can be caused by the choice of the sensor. Blue light can advantageously be used in sea water because of its penetration depth in deep sea water. However, other wave lengths than blue can be used, e.g. green/yellow light also works and can advantageously be used in coastal waters and
30 inland waters, e.g. fresh water, like a lake.

[0077] Of course, other carrier frequencies than 800 kHz can be chosen if desired. An example operating frequency range of the amplitude modulation may be 500-1500 kHz, preferably 700-1250 kHz and most preferably 750-850 kHz, with 800 kHz as a suitable example. However, higher values than 1500 kHz need be used when very high bit rates
35 are desired. A bit rate of 100 Mbps could require a minimum carrier frequency of 60 MHz.

[0078] The VLC signal 12 may for instance be formed by modulating data signals via binary phase shift keying (BPSK) or differential phase shift keying (DPSK) or any other well-known modulation technique with a predetermined maximum bitrate onto the carrier wave with frequency f_c . In an alternative embodiment, the data may be directly

5 modulated onto the light beam e.g. without a carrier, using pulse position modulation (PPM), pulse width modulation (PWM) or any other suitable modulation.

[0079] In a deep subsea environment, ambient sunlight is absent, but there may be other interfering light sources, for example an ROV or UAV may be equipped with LED spot- or floodlights. LED lights may be pulse width modulated (PWM)

10 dimmable/controllable light sources, and typical PWM LED driving frequencies range from several tens of Hz up to several hundreds of kHz.

[0080] In a shallow subsea environment, ambient sunlight could be present in addition to the aforementioned interfering light sources. Such ambient sunlight can exhibit variations in brightness, which might cause interference with the VLC receiver. The

15 embodiments of the present invention mitigate the effects caused by said interference.

[0081] The current-to-voltage converter 24 is configured to receive a current output of the SiPM sensor 20, and to produce a voltage suitable for subsequent processing. The current-to-voltage converter 24 is electrically connected with an input terminal 40 to the common cathode K of the APD elements 30, and configured to convert a current from

20 the common cathode K into a voltage and to provide said voltage on an output terminal 42 of the converter 24, as shown in more detail in figures 3A-B.

[0082] The load impedance Z as perceived by the SiPM module 20 is jointly determined by the bias circuit section 22 and the current-to-voltage converter 24. The bias circuit section 22 and the current-to-voltage converter 24 together present a low

25 load impedance $|Z|$ to the SiPM module 20 for all signal oscillations falling within operating frequency range f_0 in which both the amplitude-modulated VLC signals 12 and the amplitude-modulated interference signals 16 are expected to reside, to reduce oscillations in the bias voltage V_b across the SiPM sensor (20). Such operating

frequency range f_0 of the amplitude-modulated VLC signals 12 and the amplitude-

30 modulated interference signals 16 may e.g. be in the range of 1Hz to 100MHz. Sources of these interferences may be for example laser scanners, time-of-flight sensors, photographic strobe lights, indicating lights, or other data communication systems. A preferred impedance $|Z|$ presented by the bias circuit section 22 in the operating

frequency range f_0 of the amplitude-modulated VLC signals 12 and the amplitude-

35 modulated interference signals 16 may e.g. be $0 \text{ Ohm} < |Z| < 10 \text{ Ohm}$, more preferably $0 \text{ Ohm} < |Z| < 5 \text{ Ohm}$ and most preferably $0 \text{ Ohm} < |Z| < 2 \text{ Ohm}$ in order to obtain an as

high as possible linearity between SiPM current and induced photo current, see figure 1. As shown in figure 3A, the bias circuit section 22 comprises a voltage source 32, and a current limiting bias circuit 34. The voltage source 32 is configured to contribute to the reversed bias voltage V_b that is applied across the APD elements 30. This bias voltage V_b allows each of the APD elements 30 to operate in reverse-biased mode and to let the SiPM sensor 20 operate in integration mode.

[0083] The filter 34 is connected between the voltage source 32 and the anode A of the SiPM sensor 20. This filter 34 is configured to set a maximum average current passing through the SiPM sensor 20, to limit power dissipation. A maximum dissipation is determined by the type and size of the SiPM sensor 20 and other factors, but may be in the range of several milliwatts to several hundreds of milliwatts. The filter 34 is further configured to present a low impedance Z for oscillating currents within the predetermined operating frequency range f_o generated by the SiPM sensor 20 at the anode A, such that oscillations in the bias voltage V_b at frequencies within this range f_o are suppressed or eliminated to a predetermined low level. This may be achieved by presenting an AC load impedance $|Z|$ at anode A for alternating currents in the operating frequency range f_o of the amplitude-modulated VLC signals 12 and the amplitude-modulated interference signals 16 smaller than the DC impedance value of the current limiting bias circuit 34. In one example, the DC impedance of the bias circuit 34 is in a range of $50\ \Omega$ - $10\ \text{k}\Omega$, in another example in a range of $100\ \Omega$ - $5\ \text{k}\Omega$ and in a further example $500\ \Omega$ - $5\ \text{k}\Omega$. The actual chosen DC impedance depends on the implemented SiPM. Then, the AC load impedance $|Z|$ for said operating frequency range f_o may be in a range of $0\ \Omega < |Z| < 10\ \Omega$, more preferably $0\ \Omega < |Z| < 5\ \Omega$ and most preferably $0\ \Omega < |Z| < 2\ \Omega$.

[0084] In an embodiment, using a MicroFC-30020-SMT-A1 made by Sensl, a series current limiting resistor of $1.2\ \text{k}\Omega$ and a shunt capacitor of $10\ \mu\text{F}$ is used. The capacitor has an impedance of $-j16\ \Omega$ at $1\ \text{kHz}$ which decreases with increasing frequency. The series resistor or DC resistor depends on the maximum allowable power dissipation of the SiPM and can be quite large.

[0085] The choice of such a series current limiting resistor value is dictated by the maximum current one wishes to allow through the SiPM. The current limit may be dictated by the maximum allowed dissipation of the SiPM or the maximum power consumption one wishes to allow, in case of high ambient light levels, when supply power availability is limited, e.g. when using a battery supply.

[0086] The maximum shunt capacitor value in combination with a certain resistor (the RC time constant) is dictated by the maximum time one wishes to allow the system to adjust to a new level of average incident light, which translates into an average current.

In principle, one wishes this RC time constant to be as large as possible, but there are limits for both resistor and capacitor to keep the SiPM sensor in the safe operating area. In case of high expected ambient light levels, the series current limiting resistor value may have to be chosen low to avoid that the gain of the SiPM drops to unsatisfactory levels. In environments with low ambient light levels, e.g. in the deep ocean, resistor values can be chosen much higher.

[0087] Figure 4 shows an exemplary embodiment of a circuit 10, with further implementation details for the principles described with reference to figures 2 and 3A-B. The filter 34 includes a limiter resistor R1, for limiting the maximum average current through the SiPM sensor 20. The limiter resistor R1 is electrically connected in series, with one terminal to the voltage source 32, and with the other terminal to the anode A of the SiPM sensor 20. In this example, the limiter resistor R1 has a resistance of about 120 Ω . Using only resistor R1 would cause a voltage drop across the resistor R1 to vary with the current passing through the APD elements 30, which current follows the intensity variations in the received light 12, 14, 16. The voltage across the APD elements 30 would therefore vary as well, which in turn, causes the SiPM gain to vary, and to produce non-linear amplification of any signal. This non-linear response would be less problematic if the APD elements 30 would receive only an amplitude-modulated signal 12 at a specific frequency from a source of interest. If, however, the APD elements 30 simultaneously receive light signals from other sources, e.g. unmodulated background radiation 14 and/or modulated light 16 from interfering sources, the non-linear response of the SiPM sensor 20 will cause intermodulation distortion (IMD). This IMD is represented by additional signal output components at frequencies composed of sums and differences of integer multiples of the original signal frequencies in the received light signals.

[0088] To mitigate intermodulation issues, the exemplary filter 34 includes a capacitor C1, which is connected with one terminal between the resistor R1 and the common anode A, and with the other terminal to ground. In this example, the capacitor C1 is a polarized electrolytic capacitor having a capacitance C of, e.g. 100 μF . However, this is an example only: other suitable values may be used instead. With a capacitance C = 100 μF , the magnitude of the complex load impedance $Z(f) = -j / 2\pi \cdot f \cdot C$ of the capacitor C1 as seen by the alternating output from the SiPM sensor 20 at the anode A and with frequencies of 1 kHz or more, will remain below $|Z| = 1.5 \Omega$. Oscillations in the photocurrents around a mean, due to incoming optical signals oscillating at frequencies within the predetermined operating frequency range f_0 , are essentially shunted via the capacitor C1, instead of flowing via the resistor R1, so that the bias voltage V_b across

the SiPM sensor 20 is kept relatively constant. Intermodulation effects in the SiPM output current due to simultaneous reception of multiple signals in the operating frequency range f_0 are thus reduced. The resistor R1 and the capacitor C1 jointly form a passive low-pass RC-filter. In this example, the filter time constant $\tau = 2\pi \cdot R \cdot C$ is 75 milliseconds.

5 [0089] The RC-filter may be selected to have a large time constant as well a low complex impedance $Z(f) = -j / 2\pi \cdot f \cdot C$ for the capacitor. For a capacitor C1 of 100 microfarad, a resistor R1 of 120 Ω , and a frequency in the alternating APD current of 1 kHz, the filter time constant $\tau = 2\pi \cdot R \cdot C$ equals about 75 milliseconds, whereas the magnitude of the load impedance remains below 1.5 Ω . The cut-off frequency associated
10 with the selected RC time constant is such that slow intensity variations in ambient light 14 received by the SiPM sensor 20 are passed through, without being shunted via the capacitor C1. The bias voltage Vb may thus vary slowly along with the changing ambient light, to provide automatic gain compensation only for slow ambient light fluctuations.

[0090] So, in the circuit shown in figure 4, the bias voltage to the SiPM 20 is supplied
15 by RC low pass filter 34 comprising resistor R1 and capacitor C1 that is optimized such that it performs several functions at the same time:

- The cut-off frequency is such that slow variations in ambient light are passed through. This way the bias of the SiPM sensor stabilizes with respect to the ambient light. The cut-off frequency is much lower than the filters typically used in prior art circuits
- 20 • The resistance of resistor R1 is chosen such that the gain is automatically reduced under the influence of incident light. As explained, both the PDE and the gain are dependent on the bias voltage over the SiPM sensor. As more incident light hits the SiPM sensor, more current will flow through the resistor R1 causing the bias voltage to drop. This way both the gain and more importantly the PDE are reduced thus keeping
25 the SiPM sensor in its linear region. For this reason R1 is also chosen much higher than in typical prior art circuits.
- For modulated light sources the RC filter comprised of R1/C1 presents a low impedance to the SiPM sensor thus keeping the bias constant for AC signals within the operating frequency range. Because the bias, and thus the gain and PDE, is constant,
30 intermodulation for these frequencies will be reduced.

[0091] In the example of figure 4, the current-to-voltage converter 24 comprises a common-base amplifier with a transistor 36. The emitter E of this transistor 36 is connected to the cathode K of the SiPM sensor 20. The base B of the transistor 36 is connected to ground, and the collector C of the transistor 36 forms the output terminal 42
35 that is connected to the band-pass filter 26. This common-base amplifier is configured to present at the emitter E a low load impedance for alternating current output at the

cathode K of the SiPM sensor 20. The load impedance magnitude may range from several Ohms to several tens of Ohms in the predetermined operating frequency range f_o of the amplitude-modulated VLC signals 12 and the amplitude-modulated interference signals 16, depending on the current through the SiPM sensor 20. The filter 34 and transistor 36 cooperate to form a low load impedance for the SiPM sensor 20 in the operating frequency range f_o of the amplitude-modulated VLC signals 12 and the amplitude-modulated interference signals 16, and thus to keep the reverse bias voltage V_b across the APD elements 30 as constant as possible. The common base circuit with transistor 36 electrically isolates the SiPM sensor 20 from the subsequent detector circuit components, e.g. the filter stage 26 and the ADC 28. The common base circuit also isolates the capacitance of the SiPM from the filter stage 26 and amplifier so that a large bandwidth is realized.

[0092] The exemplary circuit 10 in figure 4 further includes a further resistor R_p , which is configured to maintain a minimum baseline current through the transistor 36 during sensor operation, even if no light is received by the APD elements 30. This further resistor R_p is connected in parallel with the SiPM sensor 20, with one terminal connected to the emitter E of the transistor 36, and with the other terminal connected to the filter 34 between the resistor R1 on the one hand and the capacitor C1 on the other hand. In this example, the further resistor R_p has a resistance of about 27 k Ω . Again, this value is only an example. Any other suitable value can be used instead.

[0093] The sensor circuit 10 further includes a RLC band-pass filter 26 to filter out the desired carrier frequency of the amplitude-modulated VLC signals 12 from the interfering frequencies and the ambient DC light. The RLC band-pass filter 26 includes an inductor L2, a capacitor C2, as well as a resistor R2 for tuning the filter bandwidth. The resistor R2, inductor L2, and capacitor C2 are electrically connected in parallel, each with one terminal connected to the collector C of transistor 36 and with another terminal connected to ground. This RLC-filter 26 is tuned via selection of appropriate values for L2, C2, and R2, to pass only the frequency band Δf_c corresponding with the carrier wave and the maximum bitrate of the received VLC signal 12. The subcarrier frequency f_c on which the VLC signal 12 is modulated, is purposefully selected higher, e.g. >500 kHz, than the highest expected frequency of the interfering signals 16 and possibly also higher harmonic frequencies. The RLC-filter 26 provides analogue pre-filtering, to suppress any frequency components outside the band of interest Δf_c , before the resulting signal is sampled and digitized by the ADC 28. The RLC-filter 26 is preferably tuned to pass the entire band Δf_c containing the VLC communication channel for the maximum data rate that it is designed for. The required bandwidth Δf_c for VLC signal 12 around the

subcarrier f_c equals the data rate. For example, a carrier frequency of about 800 kilohertz and a maximum bit rate of 25 kHz would require the RLC filter 26 to be tuned to a band of approximately 787 kHz to 813 kHz.

[0094] Figure 5 shows a schematic diagram for another embodiment of a sensor circuit 110. Features in this circuit 110 that have already been described above with reference to the circuit 10 from figures 1-3 may also be present in the circuit 110 in figure 5, and will not all be discussed here again. For the discussion with reference to figure 5, like features are designated with similar reference numerals preceded by 100 to distinguish the embodiments.

[0095] In this circuit 110, the bias circuit section includes a plurality of series LC resonant circuit sections $L1_i$, $C1_i$ ($i = a, b, c, \dots$). In this example, three of said filters are used. Each LC section functions as a band stop filter and covers a frequency band corresponding with a range of frequencies of amplitude-modulated optical signals 112, 116 that the SiPM sensor 120 is expected to receive. The resonant circuit sections $L1_i$, $C1_i$ are connected in parallel, with each resonant circuit section connected with one terminal between the resistor $R1$ and the common anode A of the APD elements 130, and with the other terminal to ground. Each circuit section includes its own capacitor $C1_i$ and inductor $L1_i$, which are connected in series. Each resonant circuit section is configured to present a low load impedance for alternating currents within subranges Δf_i of the predetermined operating frequency range f_o of the amplitude-modulated VLC signals 112 and the amplitude-modulated interference signals 116 for the oscillating SiPM current that appears at the common anode A. The LC resonant sections are tuned differently, to cover distinct sub-ranges Δf_i of the predetermined operating frequency range f_o of the amplitude-modulated VLC signals 112 and the amplitude-modulated interference signals 116.

[0096] Figure 6 shows a schematic diagram for yet another embodiment of a sensor circuit 210. Features that have been described in preceding embodiments may also be present in this circuit 210 and will not all be discussed here again. Like features have similar reference numerals, but preceded by 200.

[0097] In this circuit 210, the current-to-voltage converter 224 is formed as a trans impedance amplifier, which comprises an operational amplifier 238. The operational amplifier 238 is configured to present a low load impedance for alternating currents to the cathode K of the SiPM sensor 220 in the band of expected frequencies f_o of the amplitude-modulated VLC signals 212 and the amplitude-modulated interference signals 216. The operational amplifier 238 has a non-inverting input "+", an inverting input "-", and an output O. The non-inverting input of the amplifier 238 is connected to ground. The

inverting input of the amplifier 238 is connected to the common cathode K of the SiPM sensor 220, but also receives a negative feedback voltage from the output O via a transimpedance resistor R_t . This resistor R_t is connected between the inverting input and the output O of the amplifier 238. The gain of the current is determined by R_t .

5 [0098] The sensor circuit 210, like the sensor circuit 10 of figure 4, further includes RLC band-pass filter 226, which includes inductor L2, capacitor C2, as well as resistor R2 for tuning filter quality. Resistor R2 is connected in a different way than in the circuit of figure 4. I.e., the inductor L2, and capacitor C2 are electrically connected in parallel between ground and one terminal of resistor R2. The other terminal of resistor R2 is connected to
10 output O of operational amplifier 224. Again, this RLC-filter 226 is tuned via selection of appropriate values for L2, C2, and R2, to pass only the frequency band Δf_c corresponding with the carrier wave and the maximum bitrate of the received VLC signal 12.

[0099] Figure 7 shows a schematic diagram of another embodiment 310, where an
15 additional LC filter is used. The LC filter allows for a steeper transition between the low impedance AC operating frequency range and the high impedance current limiting range. Such LC filters could have a pi-topology, T-topology, L-topology and/or any variation thereof. In addition, resistors could be used to control the quality factor of the filter.

[0100] Figure 8 shows a schematic diagram of another embodiment 410, where the bias
20 controller 434 is implemented comprising active components like transistors, operational amplifiers, signal processors using analogue to digital converters (ADC) and/or digital to analogue converters (DAC), microprocessors, DC-DC converters, inverters and similar such devices. The bias controller 434 may be powered by a DC voltage supply 432, and is further connected to the anode of the SiPM sensor 420. The various supply voltages
25 needed by the various active components of the bias controller 434, including the reverse bias voltage supply are generated inside the bias controller module, e.g. using DC-DC converters. Alternative embodiments could use external power supplies. The output of this bias controller module provides the reverse bias voltage to the anode of the SiPM sensor, and simultaneously acts as a time varying current limiter. The time varying
30 current limiting characteristics of said module are tuned such that the load impedance for AC currents is as low as possible over the operating frequency range, while at the same time it ensures that the SiPM is always operating within the safe operating area (SOA). These two requirements are opposed to each other. To achieve a lower AC impedance for a certain frequency, the current limiting control loop requires to have a larger time
35 constant, meaning that the current limiting function will act slower. To protect the SiPM sensor against damage however, the current limiting function needs to be fast enough to

ensure the SiPM sensor stays within the safe operating area (SOA). In this embodiment an optimum current limiting characteristic can be achieved, which just satisfies the safe operating area (SOA) but at the same time ensures the lowest possible AC impedance seen from the anode of the SiPM sensor, for frequencies approaching the frequency band where the current limiting function is active.

[0101] In a further embodiment, the bias controller 434 may provide a plurality of current limiters each having specific characteristics, optimized for a specific requirement, but acting simultaneously. The first current limiter is optimized to just satisfy the safe operating area (SOA) of the SiPM sensor. The second current limiter however is configured to act at a lower current limit than the first one, and has a time constant much larger than the first current limiter which just satisfies the SOA requirement. If the current remains below the limits dictated by keeping the SiPM within its safe operating area, this second current limiter will be the only one guarding the current and adjusting the reverse bias voltage in case the configured current is exceeded. Further current limiters could be added to provide optimized bias voltage control for AC currents of a specific frequency range, e.g. the variations in current caused by surface wave motion exposed to ambient sun light in a subsea optical communication system, or the very slow variations in AC current caused by ambient sunlight changes over a day. It is important that the configured current limits are time constant dependent such that a limiter with a larger time constant is configured for a lower current limit than another current limiter. Not adhering to this rule would mean that the current limiter with a lower time constant would never activate and therefore be obsolete.

[0102] In embodiments comprising active components, microcontrollers can be used to realize more complex current limiting schemes. For example, the time constants could be different for the leading and trailing edge of the current limiting event. In such an embodiment, the leading edge time constant of the first current limiter could be made fast, i.e. steep, such that the bias voltage is reduced quickly in the event of sudden saturation thereby preventing exceeding the SOA of the device. A dynamic time constant, adapted for the circumstances, for the trailing edge ensures an optimized low AC impedance. In order to determine the dynamic trailing edge parameters machine learning algorithms or artificial intelligence systems could be used to control those parameters.

[0103] While the above embodiments make mainly use of SiPM sensors and APD arrays, this invention is not limited to such sensors. In principle, this invention augments front ends for non-linear sensors requiring a bias voltage or bias current. Sensors can be, but not limited to, Hall effector sensors, LDR, PTC or NTC resistors, photodiodes,

PIN photodiodes. Further, regular semiconductors, such as diodes and transistors can be used as temperature sensors. The skilled person would understand that such use of semi-conductor devices will benefit from a bias voltage and/or current.

List of Reference Symbols

Similar reference numbers that have been used in the description to indicate similar elements (but differing only in the hundreds) have been omitted from the list below, but should be considered implicitly included

5	10	sensor circuit
	12	optical signal
	14	ambient light
	16	interference signal
	20	SiPM sensor
10	22	bias circuit section
	24	current-to-voltage converter
	26	band pass filter
	28	ADC
	30	APD elements
15	32	bias voltage source
	34	current limiting bias circuit (e.g. RC low-pass filter)
	36	transistor
	40	input terminal
	42	output terminal
20	44	analogue sensor output
	134	current limiting bias circuit (e.g. band-stop filter with series LC shunt sections)
	238	operational amplifier
	A	common anode
	K	common cathode
25	E	emitter
	C	collector
	B	base
	C1	capacitor
	C2	further capacitor
30	L1	inductance
	L2	further inductance
	R1	resistor
	R2	further resistor
	Rp	parallel resistor
35	Rt	transimpedance resistor
	Δf_c	frequency band of communication signal

fo operating frequency range of expected optical signals

Claims

1. A sensor circuit (10), comprising:

- a silicon photomultiplier, SiPM, sensor (20) including an array of avalanche photodiode, APD, elements (30) that are connected in parallel between a common cathode (K) and a common anode (A);
- a voltage source (32), configured to apply a reversed bias voltage (V_b) across the SiPM sensor, to let each of the APD elements operate in reverse-biased Geiger mode, and to let the array of APD elements operate in integration mode;
- a current-to-voltage converter (24), electrically connected with an input terminal (40) to the cathode of the SiPM sensor, and configured to convert a current from the cathode of the SiPM sensor into a voltage and provide said voltage on an output terminal (42) of said converter;
- a limiting bias circuit (34) connected between the voltage source (32) and the anode of the SiPM sensor, wherein the bias circuit is configured to limit currents through the APD elements, and configured to present an AC load impedance for an alternating current within a predetermined operating frequency range (f_o) generated by the APD elements at the common anode (A) as well as a DC load impedance, such that said AC load impedance is lower than said DC load impedance.

2. The sensor circuit (10), according to claim 1, wherein the predetermined operating frequency range (f_o) in which the AC load impedance is at least 10 times lower than the DC load impedance.

3. The sensor circuit (10) according to claim 1 or 2, wherein the DC load impedance of the bias circuit (34) is in a range of $50\ \Omega$ - $10\ \text{k}\Omega$, for example in a range of $100\ \Omega$ - $5\ \text{k}\Omega$, or in a range of $500\ \Omega$ - $5\ \text{k}\Omega$, and the AC load impedance for said operating frequency range (f_o) is in a range between $0\ \Omega$ and $10\ \Omega$, more preferably between $0\ \Omega$ and $5\ \Omega$ and most preferably between $0\ \Omega$ and $2\ \Omega$.

4. The sensor circuit (10) according to any one of claims 1-3, wherein the bias circuit (34) comprises:

- a limiter resistor (R_1) connected in series between the voltage source (32) and the anode of the SiPM sensor, and configured to limit the current through the SiPM sensor.

5. The sensor circuit (10) according to claim 4, wherein the output voltage of the voltage source (32) and a resistance of the limiter resistor (R1) are selected so that the resulting average overvoltage across the APD elements (30) causes operation in a quasi linear part of a photon detection efficiency response characteristic and gain characteristic of the SiPM sensor (20).

6. The sensor circuit (10) according to claim 4 or 5, wherein the bias circuit (34) comprises:

- a capacitor (C1) connected between the resistor (R1) and the common anode (A) on the one hand, and to ground on the other hand.

7. The sensor circuit (10) according to claim 6, wherein the capacitor (C1) has a capacitance of at least 1 microfarad.

8. The sensor circuit (110) according to claim 4 or 5, wherein the bias circuit (134) comprises:

- a resonant circuit section connected between the anode (A) of the SiPM sensor and ground, wherein the circuit section includes a capacitor (C1a) and an inductor (L1a) connected in series, and is configured to present the low load impedance for alternating currents within at least part of the predetermined operating frequency range (fo) generated by the APD elements (30) at the common anode (A).

9. The sensor circuit (10) according to claim 8, wherein the low-pass filter (34) comprises:

- further resonant circuit sections (L1b, C1b; L1c, C1c) connected between the anode (A) of the SiPM sensor and ground, wherein each of the further circuit sections includes a further capacitor (C1b; C1c) and a further inductor (L1b; L1c) connected in series, and each configured to present a low load impedance for alternating currents within further parts of the predetermined operating frequency range (fo) generated by the APD elements (30) at the common anode (A).

10. The sensor circuit (10) according to any one of claims 1-9, wherein current-to-voltage converter (24) comprises a common-base circuit, including a transistor (36) with an emitter (E) that is connected to the cathode (K) of the SiPM sensor (20), with a base (B) that is connected to ground, and with a collector (C) that forms a signal output (42).

11. The sensor circuit (210) according to any one of claims 1-9, wherein said current-to-voltage converter (24) comprises an operational amplifier (238) with an output (O), a non-inverting input (+) that is connected to ground, and with an inverting input (-) that is connected to the cathode (K) of the SiPM sensor (20) as well as to a feedback voltage
5 from the output (O) via a further resistor (Rt).

12. The sensor circuit (10) according to claim 10 or 11, further comprising:
- a further resistor (Rp) connected between the current-to-voltage converter (24) and the current limiting bias circuit (34), and configured to maintain a minimum baseline
10 current through the current-to-voltage converter.

13. The sensor circuit (10) according to any one of claims 1-12, further comprising: a parallel resonant band-pass filter (26), which is provided between the output (42) of the current-to-voltage converter (24) and an analogue sensor output (44), and which is
15 configured to pass only a frequency band (Δf_c) corresponding to a carrier wave and a maximum bitrate of the communication signal (12) to the analogue sensor output (44).

14. The sensor circuit (10) according to claim 1, comprising at least one active electronic component.
20

15. The sensor circuit (10) according to claim 14, wherein the at least one active electronic component is at least one microcontroller, wherein the at least one microcontroller is configured to generate complex current limiting schemes.

25 16. The sensor circuit (10) according to claim 15, wherein the at least one microcontroller is configured to generate current limiting schemes in which the time constants could be different for the leading and trailing edge of a current limiting event.

17. The sensor circuit (10) according to claim 16, wherein the at least one
30 microcontroller is configured to generate current limiting schemes in which the leading edge time constant of the first current limiter could be made fast, such that the bias voltage is reduced quickly in the event of sudden saturation thereby preventing exceeding the SOA of the device.

18. The sensor circuit (10) according to claim 16, wherein the at least one microcontroller is configured to generate current limiting schemes in which the trailing edge ensures an optimized low AC impedance.

5 19. The sensor circuit (10) according to claims 16-18, wherein the at least one microcontroller is configured to generate current limiting schemes, wherein the leading and trailing edges' parameters are generated by means of machine learning algorithms and/or artificial intelligence systems.

10 20. A sensor circuit (10), comprising:

- a non-linear semi-conductor sensor;
- a bias circuit (34), configured to apply an electrical bias across the non-linear semi-conductor sensor;
- a signal sensing converter (24), electrically connected with an input terminal (40)

15 to the non-linear semi-conductor sensor, and configured to convert an electrical signal from the output terminal of the non-linear semi-conductor sensor into a measurement signal and provide said measurement signal on an output terminal (42) of said converter;

- a bias circuit (34) connected between an electrical source (32) and the input terminal of the non-linear semi-conductor sensor, wherein the bias circuit is configured to

20 limit the electrical bias through the non-linear semi-conductor sensor, and configured to present an AC load impedance for an alternating electrical signal within a predetermined operating frequency range (f_0) generated by the non-linear semi-conductor sensor as well as a DC load impedance, such that said AC load impedance is different from said DC load impedance.

25

21. A method for operating a sensor circuit (10) according to any one of claims 1-19, wherein the method comprises:

- applying, with the voltage source (32), a reversed bias voltage (V_b) across the avalanche photodiode, APD, elements (30) of the silicon photomultiplier, SiPM, sensor

30 (20), to let each of the APD elements operate in reverse-biased mode, and to let the array of APD elements operate in integration mode;

- receiving, with the APD elements, a plurality of amplitude-modulated light signals (12, 16) which oscillate in time corresponding to frequency bands within a predetermined operating frequency range (f_0);

- converting, with the current-to-voltage converter (24), a current from the common cathode (K) of the array of APD elements into a voltage, and providing said voltage on the output terminal (42) of said converter, and;
- forming, with the bias circuit, an AC load impedance for an alternating current within the predetermined operating frequency range (f_o) generated by the APD elements at the common anode (A), as well as a DC load impedance, such that said AC load impedance is at least 10 times, for instance 10 to 10000 times, lower than said DC load impedance, thereby reducing or minimizing intermodulation distortion in the current generated by the SiPM sensor in response to the received light signals.

10

22. A method for operating a sensor circuit (10) according to claim 20, wherein the method comprises:

- applying, with a bias circuit (34), an electrical bias across a non-linear semi-conductor sensor;
- 15 - receiving, with the non-linear semi-conductor sensor, a plurality of modulated signals (12, 16) which oscillate in time corresponding to frequency bands within a predetermined operating frequency range (f_o);
- converting, with the signal sensing converter (24), an electrical signal from the non-linear semi-conductor sensor into a measurement signal, and providing said measurement signal on the output terminal (42) of said converter, and;
- 20 - forming, with the bias circuit, an AC load impedance for an alternating electrical signal within the predetermined operating frequency range (f_o) generated by the non-linear semi-conductor sensor, as well as a DC load impedance, such that said AC load impedance is different from said DC load impedance, as to reduce or minimize
- 25 intermodulation distortion in the electrical signal generated by the non-linear semi-conductor sensor in response to the modulated signals.

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Fig. 1

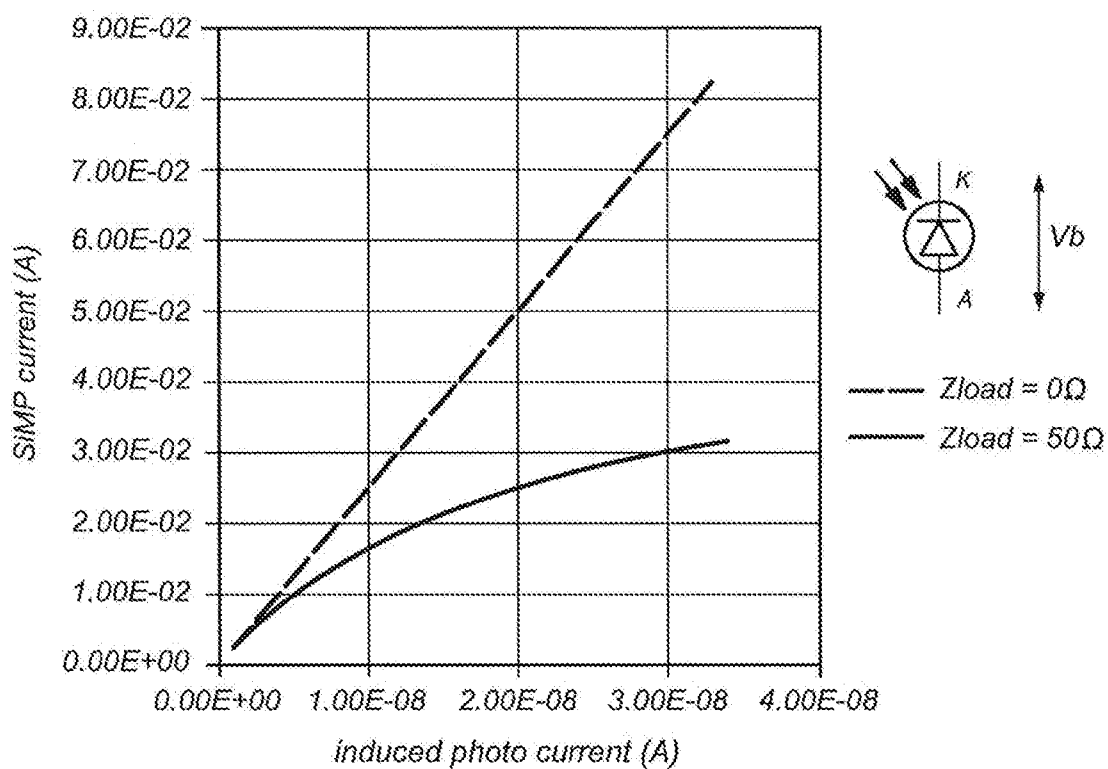
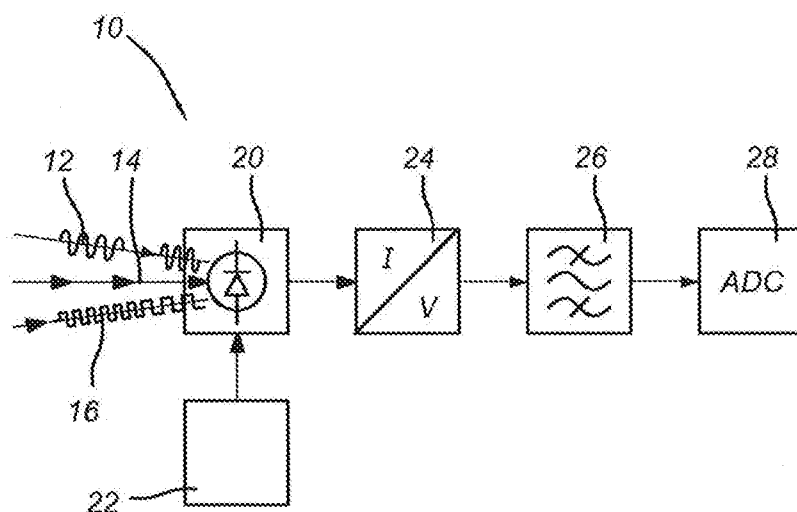


Fig. 2



27

Fig. 3A

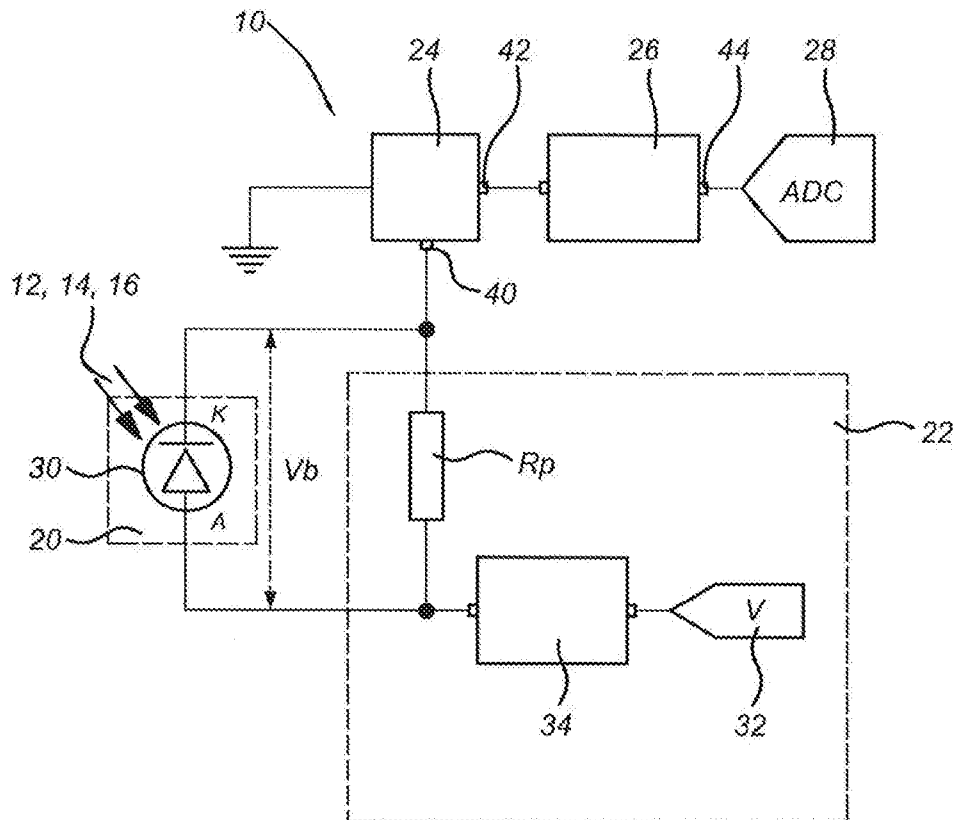
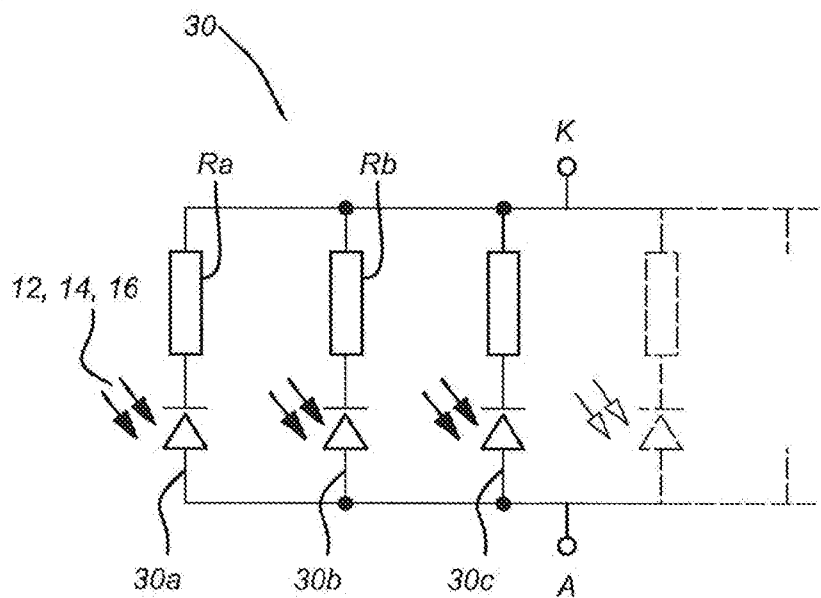
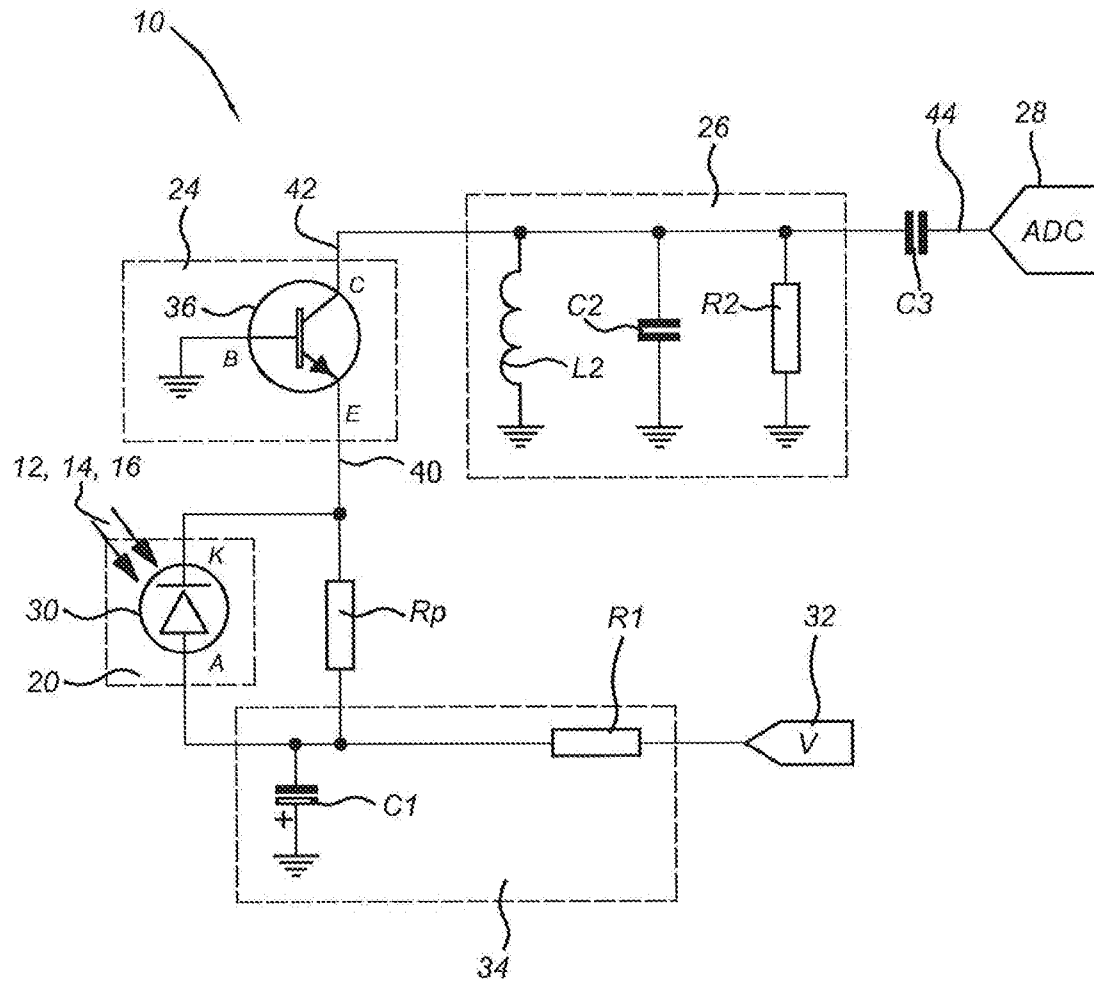


Fig. 3B



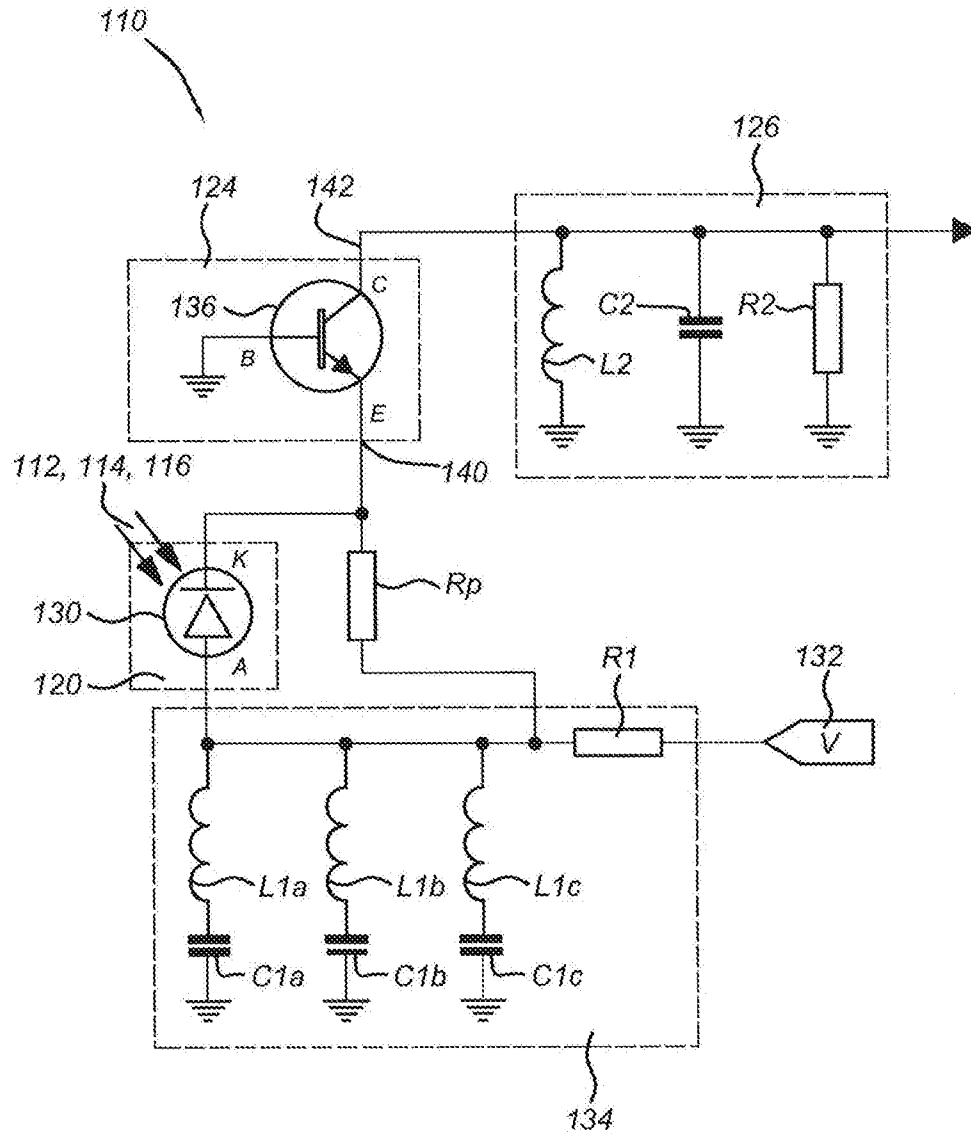
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Fig. 4



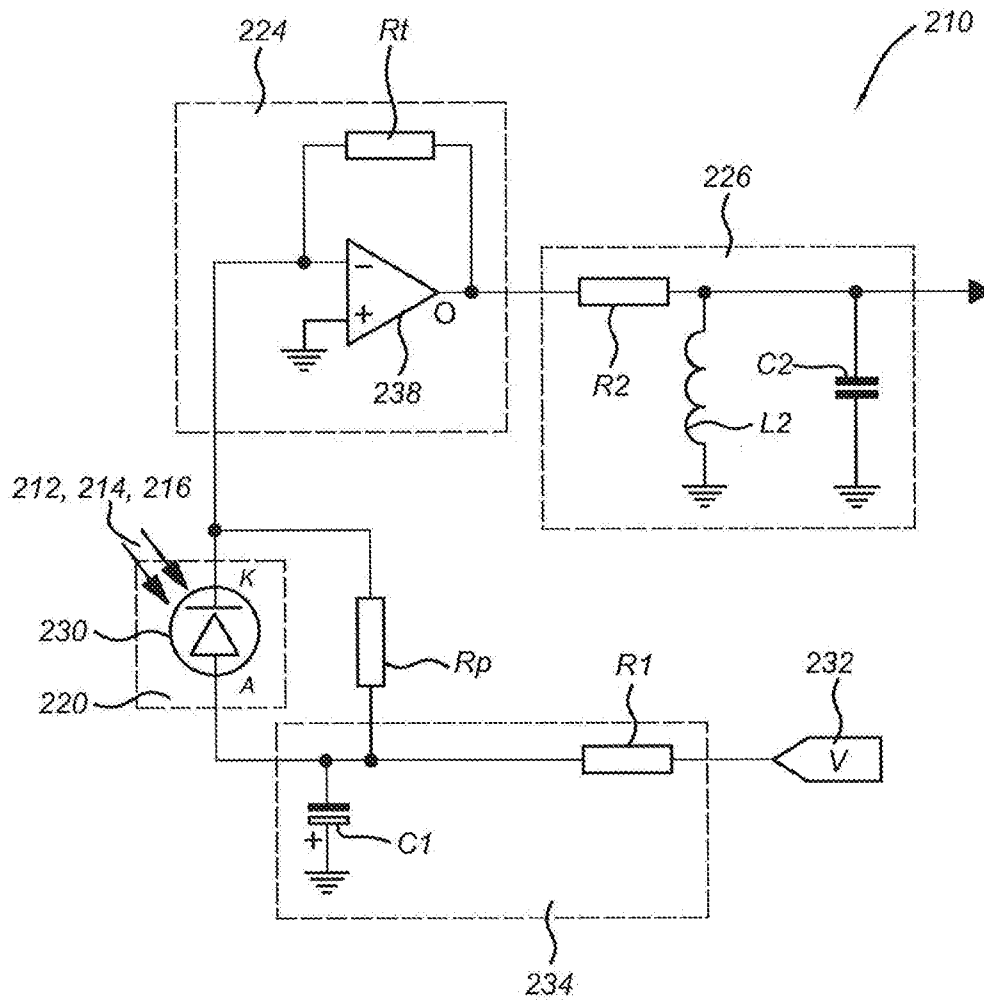
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Fig. 5

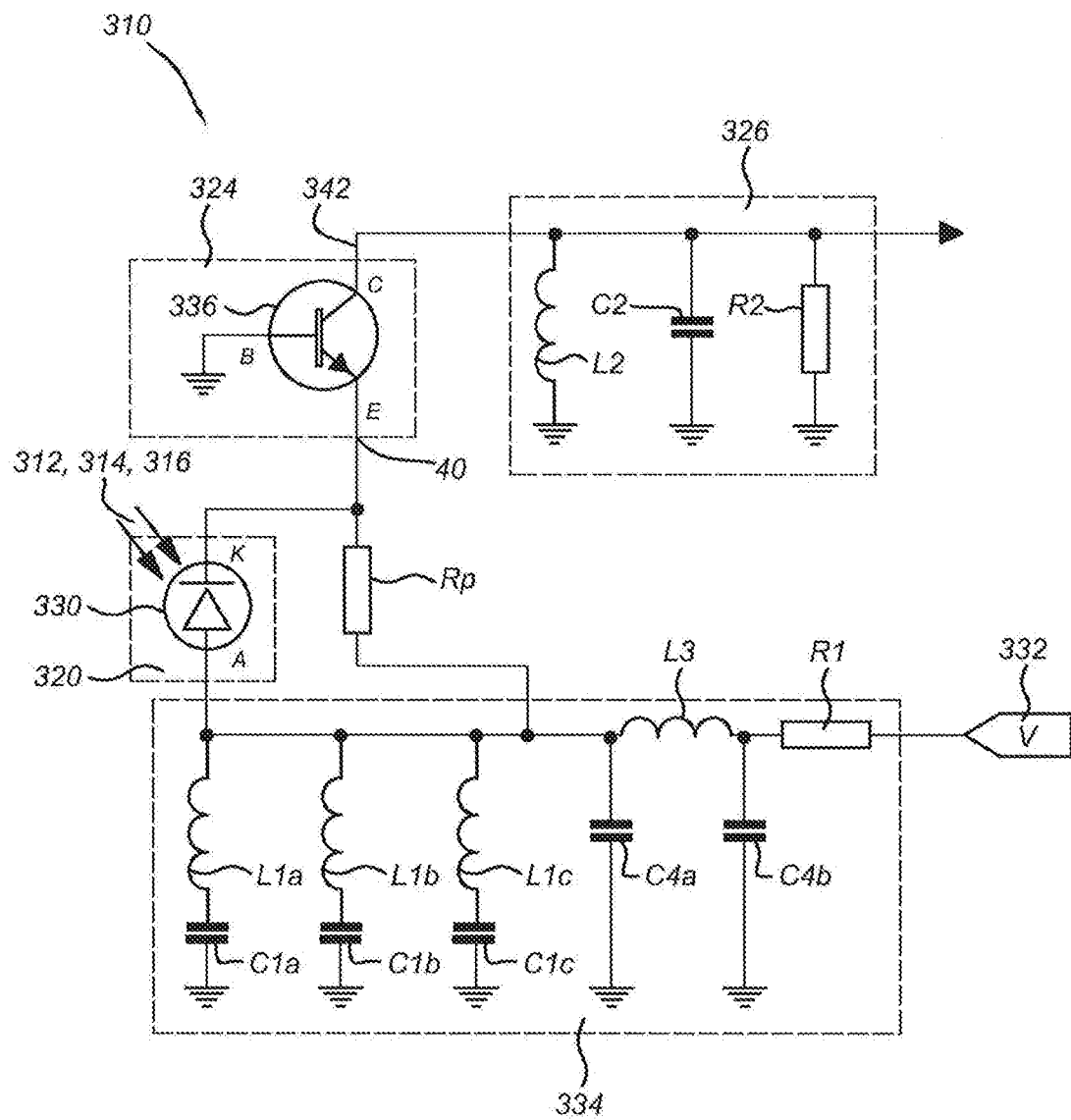


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Fig. 6



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Fig. 7

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Fig. 8

