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(71) Applicant *(for all designated States except US)*: **FULTEC PTY LTD** [AU/AU]; Building 76A, University of Queensland Campus, St Lucia, QLD 4072 (AU).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **HARRIS, Richard, Allen** [AU/AU]; 10 Carinya Crescent, Kawana Downs, QLD 4306 (AU).

(74) Agent: **EAGAR NEWCOMB & BUCK PATENT AND TRADE MARK ATTORNEYS**; PO Box 509, Spring Hill, QLD 4004 (AU).

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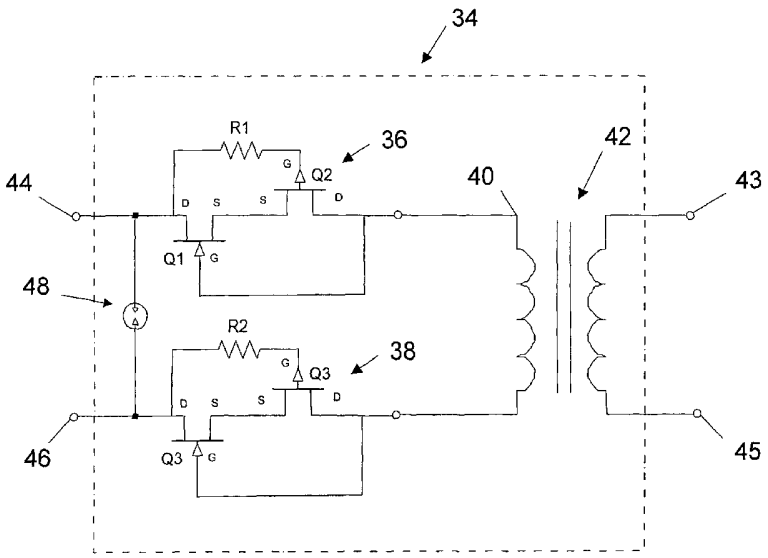
(54) Title: A PROTECTION DEVICE FOR PREVENTING THE FLOW OF UNDESIRABLE DIFFERENTIAL MODE TRANSIENTS



(57) Abstract: A differential mode surge protection apparatus (34) includes first (36) and second (38) solid state protection device in series between respective input and output connection points. The apparatus may be provided in conjunction with a common mode protection apparatus such as an isolation transformer (42). Alternatively, the apparatus may be provided integrated into a single miniaturised protection package. In a preferred embodiment the apparatus includes a surge arrestor (48) arranged to supplement protection conferred by the first (36) and second (38) solid state protection device and selected so that in use it triggers prior to breakdown of either the first or second solid state protection devices. The apparatus may be incorporated into digital processing cards such as LAN cards and also into cables to conveniently provide differential mode protection.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A PROTECTION DEVICE FOR PREVENTING THE FLOW OF UNDESIRABLE DIFFERENTIAL MODE TRANSIENTS

Field of the Invention

The present invention relates to electrical surge protection devices.

Background to the Invention

Wherever electronic circuitry is coupled to an external cable run, a risk of damage to the circuitry, due to the transmission of transient overvoltages by the cable run, may occur. Such overvoltages may be due to any one of several factors. For example, lightning, electrostatic discharge or malfunction of equipment at a remote end of the cable may be responsible. Several techniques exist for isolating circuitry from potentially damaging surges. These include, inductive coupling as shown in Figure 1, capacitive coupling, and opto-isolation as shown in Figure 2. Isolation transformers are usually used to implement inductive coupling.

Figure 1 is a schematic diagram of a typical arrangement whereby a cable including a pair of conductors 2, 4 terminate on an isolation transformer 6 which is connected to a load 12. In the event of a common mode voltage surge the potential on both conductors 2 and 4 will vary virtually identically thereby causing substantially zero net current to flow through the primary coil 8 of transformer 6. As a result, the common mode transient does not induce a fault current in secondary coil 10 and so isolation transformer 6 provides common mode protection to load 12.

However, in the event that a voltage transient affects one of conductors 2 and 4 substantially more than the other then a surge current will flow through primary coil 8 and induce a transient voltage across the output terminals of secondary coil 10. The surge current may damage the isolation device and may also damage the equipment that is intended to be protected. Consequently, it will be realised that while an isolation transformer provides a good measure of protection from common mode transients it does not provide protection from differential mode surges.

One area where isolation transformers are used significantly is in the implementation of local area computer data networks (LANs). With reference to

Figure 3, a digital processing card in the form of a network interface card (NIC), or as it is often called a "LAN card", couples to J8-45 plug 22 of LAN cable 16 by means of J8-45 socket 18. LAN card 14 includes an isolation transformer module 20 that couples socket 18 to a data processing chip 24 which in turn communicates with the central processor 26 of a workstation by means of PCI slot connectors 28 that are received into a PCI connector 30 which is in turn mounted on a mainboard 32 of the workstation.

Figure 4 is a schematic diagram of the prior art card of Figure 3 wherein like indicia are used to refer to like components. The card receives and transmits data pulses by means of respective balanced twisted pair wires that are enclosed in LAN cable 16 and which terminate on the RX+ and RX- pins and TX+ and TX- pins of J8-45 socket 18.

Isolation module 20 includes a pair of transformers 20A and 20B which respectively provide isolation for processing chip 24 from transients on the transmit and receive twisted pairs. As previously explained, isolation transformers 20A and 20B provide considerable immunity from damaging common mode transients but not from differential mode transients. For example, in the event of a voltage transient occurring at the RX+ pin but not on the RX- pin then that transient will be transmitted across the isolation transformer and may damage processing chip 24.

It is an object of the present invention to provide a convenient means for addressing the problems posed by differential mode transients as discussed above.

Summary of the Invention

According to a first aspect of the present invention there is provided a differential mode surge protection apparatus including:

a pair of input connection points and a corresponding pair of output connection points;

a first solid state protection device in series between a first one of the pair of input connection points and a first one of the corresponding pair of output connection points; and

a second solid state protection device in series between a second one of the pair of input connection points and a second one of the corresponding pair of output connection points.

The first and second solid state protection devices may be integrated into a single miniaturised protection package.

Preferably a surge arrestor is arranged to supplement protection conferred by the first and second solid state protection devices and selected so that in use it triggers prior to breakdown of either the first or second solid state protection devices.

The surge arrestor may be connected across the input connection points.

Preferably the first and second solid state protection devices comprise a matched pair of unipolar transient blocking units (TBUs), each unipolar transient blocking unit including two series connected field effect transistors.

The differential mode protection device may be provided in combination with a digital signal processing card such as a LAN card.

Preferably the solid state protection devices are disposed between a common mode isolation device of the digital signal processing card and external connection points of the digital signal processing card. Alternatively, it is possible that the solid state protection devices be disposed between an output side of the isolation device and a digital signal processing chip of the card.

Where the apparatus is not provided in combination with a digital processing card, it may be provided further including a common mode isolation device disposed between the first solid state protection device and the second solid state device and the output connection points.

The common mode isolation device may comprise an isolation transformer.

Alternatively, the common mode isolation device could comprise another suitable device such as an opto-isolator.

According to a further aspect of the present invention a cable may be provided that includes one or more of the differential mode surge protection apparatus. In that case the pair of input connection points may terminate upon a first connector of the cable and the output connection points may terminate upon a second connector of the cable.

The first connector may comprise a socket and the second connector a plug. Alternatively the first connector may comprises a plug and the second connector may comprise a plug.

Typically the cable comprises a LAN cable and the first and second connectors comprise LAN cable connectors.

Further preferred features of the various aspects of the invention will be apparent from the following description of preferred embodiments which will be made with reference to a number of figures.

Brief Description of the Figures

Figure 1 is a schematic diagram of a prior art common mode protection circuit.

Figure 2 is a schematic diagram of a further prior art common mode protection circuit.

Figure 3 depicts the external appearance of a prior art network interface card.

Figure 4 is a schematic diagram of the network interface card of Figure 3.

Figure 5 is a schematic diagram of surge protection module according to an embodiment of the present invention.

Figure 6 is a schematic diagram of a differential mode protection device package according to an embodiment of the invention.

Figure 7 is a schematic diagram of a circuit of the differential mode protection device package of Figure 6.

Figure 8 is a schematic diagram of a variation to the circuit of the differential mode protection device package of Figure 7.

Figure 9 is a schematic diagram of a network interface card according to an embodiment of the present invention.

Figure 10 depicts the external appearance of a differential mode surge protection apparatus according to a further embodiment of the present invention.

Figure 11 is a schematic diagram of the protection apparatus of Figure 7.

Figure 12 depicts the external appearance of a differential mode surge protection apparatus according to a further embodiment of the invention.

Detailed Description of Preferred Embodiment

Referring now to Figure 5, an isolation module 34 according to an embodiment of the present invention is depicted. Isolation module 34 includes a common mode isolation device 42 which in the present embodiment comprises a transformer although it will be realised that it could instead be some other common mode isolation device such as an opto-isolator. Isolation module 34 includes two identical series connected unipolar transient blocking units (TBUs) 36 and 38 connected at respective sides of primary coil 40 of transformer 42.

A TBU is a transistor device configured to open-circuit once the current through it reaches a certain predetermined trigger level. TBU 36 consists of two depletion mode FETs being N-channel FET Q1 and P-channel FET Q2. Q1 and Q2 are connected with their conduction paths in series. The gate electrode of transistor Q1 is coupled to the drain electrode of transistor Q2. The source electrodes of Q1 and Q2 are coupled to each other and the drain electrode of transistor Q1 is coupled to a first terminal 44. Resistor R1 extends between the drain electrode of Q1 and the gate electrode of Q2. The drain of Q2 is connected to a first side of primary coil 40. In effect, TBU 36 functions as a fuse for positive current flowing from terminal 44 through to the primary coil. The structure of TBU 38 is identical to that of TBU 36 so that TBU 38 acts as a fuse for positive current flowing from terminal 46 towards primary coil 40. TBU 38 and TBU 36 are selected so that they have as close as possible insertion loss in order that the balance of the circuit is maintained.

TBUs 36 and 38 protect a load connected across terminals 43 and 45 from differential surge currents by triggering to an open circuit when the current through the load reaches the preset trigger level. If the differential current into terminal 44 attains the trigger level then TBU 36 will open-circuit. Alternatively if the differential current flowing out of terminal 44 attains the trigger level then TBU 38 will trigger. Of course, the TBUs could be reverse-orientated relative to the configuration depicted in Figure 4.

In that case if the differential current into terminal 44 attains the trigger level then TBU 38 would open circuit and conversely if the differential current flowing out of terminal 44 attained the trigger level then TBU 36 would trigger.

In the event that the voltage across a triggered TBU continues to rise then eventually a breakdown voltage will be reached at which the TBU conducts again. At present TBUs with breakdown voltages up to 800V are available. In order to provide protection from surges that exceed the breakdown voltage, surge arrestor 48 may be included. A gas arrestor, as depicted at item 48 is typically used. However, any suitable surge arrestor could be used as an alternative. Surge arrestor 48 is connected line-to-line across terminals 44 and 46 and is selected so that it will trigger at 90% of the TBUs' breakdown voltage. Consequently, in the event of a differential mode surge approaching the breakdown voltage of the TBUs the surge arrestor will trigger and short the surge before it can cause breakdown of the triggered TBU and subsequently be transmitted across isolation transformer 42 to potentially damage any load connected between output terminals 43 and 45.

Suitable TBU's may be purchased from Fultec Pty Ltd of,Building 76A, University of Queensland Campus, St Lucia, Brisbane, Queensland, Australia. Circuits for implementing suitable TBUs are described in granted United States patent No. 5,742,463 and in international patent application No. PCT/AU03/00175, both by the present inventor. The descriptions of both US 5,742,463 and PCT/AU03/00175 are hereby both incorporated in their entireties by cross-reference.

With reference to Figure 6, according to a further embodiment of the invention a differential mode protection device 43 is conveniently provided in a single package having four connectors A, B, C, D as shown. The device may be provided with or without a surge arrestor as desired. A schematic diagram of the internal circuit of device 43 without surge arrestor is shown in Figure 7 whereas a schematic for a further version with surge arrestor is shown in Figure 8. Further variations of the device are possible. For example an eight terminal version of the device might be provided including two of the circuits of Figure 7 or Figure 8.

A schematic diagram of a digital processing card, in the present example a LAN card, according to a preferred embodiment of the invention is shown in Figure 9. It will be noted that the LAN card of Figure 9 incorporates two

pairs of TBUs 51A, 51B and 52A, 52B placed in series with the TX+, TX-, and RX+, RX- terminals of socket 18 respectively.

(The TBUs are each identical to TBUs 36 and 38 of Figure 5 and might be provided in an eight terminal version of device 43 of Figure 6.) Surge arrestors 19 and 21 are connected across the TX+, TX- and RX+, RX- pins respectively. The surge arrestors are selected so that they will trigger at 90% of the TBUs' breakdown voltage. As previously explained, in the event of a differential mode surge approaching the breakdown voltage of the TBUs the surge arrestors will trigger and short the surge before it can cause breakdown of the TBUs and subsequently be transmitted across isolation transformer to potentially damage logic circuitry 24.

Figure 10 depicts the external appearance of a differential mode surge protector 50 according to a further embodiment of the present invention while Figure 11 is a corresponding schematic diagram. Surge protector 50 includes a J8-45 plug 52 for connection to a socket of a LAN card. The J8-45 plug is coupled to a differential mode protection module 54 which includes TBU's and surge arrestors as shown in Figure 11. The surge protector further includes a J8-45 socket 58 which is coupled to circuitry in module 54 and which is intended to receive a LAN cable.

Figure 12 is a variation of the differential mode surge protector of Figures 10 and 11 being a cable 63 incorporating differential mode protection according to the present invention. Cable 63 includes a connector 52 for connection to a digital processing card. In the present example it is intended that cable 63 be a LAN cable and so connectors 52 and 59 are J8-45 plugs although obviously other connectors might be used for other applications. A differential mode protection module 54, identical to the one in Figure 10 and containing the circuitry depicted in Figure 11 is coupled to connector 52. A relatively long run of cable 61 connects protection module 54, which includes TBU's and surge arrestors as shown in Figure 11, to remote connector 59. In use it is intended that connector 52 be plugged into a digital processing card such as a LAN card whereas connector 59 is plugged into a remote device such as a network hub. If desired, a second module may be incorporated proximal to plug 59. Variations to the cable shown in Figure 12 are of course possible.

For example, the circuitry that is provided inside housing 54 might be integrated into one or the other of connectors 52 and 59.

Although the present invention has been described in terms of preferred embodiments, it is not intended that the invention be limited to these embodiments. Equivalent methods, structures, arrangements, processes, steps and other modifications apparent to those skilled in the art will fall within the scope of the following claims.

Claims:

1. A differential mode surge protection apparatus including:

a pair of input connection points and a corresponding pair of output connection points;

a first solid state protection device in series between a first one of the pair of input connection points and a first one of the corresponding pair of output connection points; and

a second solid state protection device in series between a second one of the pair of input connection points and a second one of the corresponding pair of output connection points.

2. An apparatus according to claim 1, wherein the first and second solid state protection devices are integrated into a single miniaturised protection package.

3. An apparatus according to claim 1 or claim 2, further including a surge arrestor arranged to supplement protection conferred by the first and second solid state protection devices and selected so that in use it triggers prior to breakdown of either the first or second solid state protection devices.

4. An apparatus according to claim 3, wherein the surge arrestor is connected across the input connection points.

5. An apparatus according to claim 1, wherein the first and second solid state protection devices comprise a matched pair of unipolar transient blocking units (TBUs), each unipolar transient blocking unit including two series connected field effect transistors.

6. An apparatus according to claim 1 in combination with a digital signal processing card.

7. An apparatus according to claim 6, further including a surge arrestor arranged to supplement protection conferred by the first and second solid state protection devices and selected so that in use it triggers prior to breakdown of either the first or second solid state protection devices.

8. An apparatus according to claim 7, wherein the solid state protection devices are connected between a common mode isolation device of the digital signal processing card and external connection points of the digital signal processing card.

9. An apparatus according to claim 6, wherein the digital signal processing card comprises a LAN card.

10. An apparatus according to claim 1, further including a common mode isolation device disposed between the first solid state protection device and the second solid state device and the output connection points.

11. An apparatus according to claim 2 or claim 3, further including a common mode isolation device disposed between the first solid state protection device and the second solid state device and the output connection points.

12. An apparatus according to claim 10, wherein the common mode isolation device comprises an isolation transformer.

13. An apparatus according to claim 10, wherein the common mode isolation device comprises an opto-isolation device.

14. A cable including one or more apparatus according to claim 1, wherein the pair of input connection points terminate upon a first connector of the cable and wherein the output connection points terminate upon a second connector of the cable.

15. A cable according to claim 14, wherein the first connector comprises a socket and the second connector comprises a plug.

16. A cable according to claim 14, wherein the first connector comprises a plug and second connector comprises a plug.

17. A cable according to claim 14, wherein the cable comprises a LAN cable and the first and second connectors comprise LAN cable connectors.

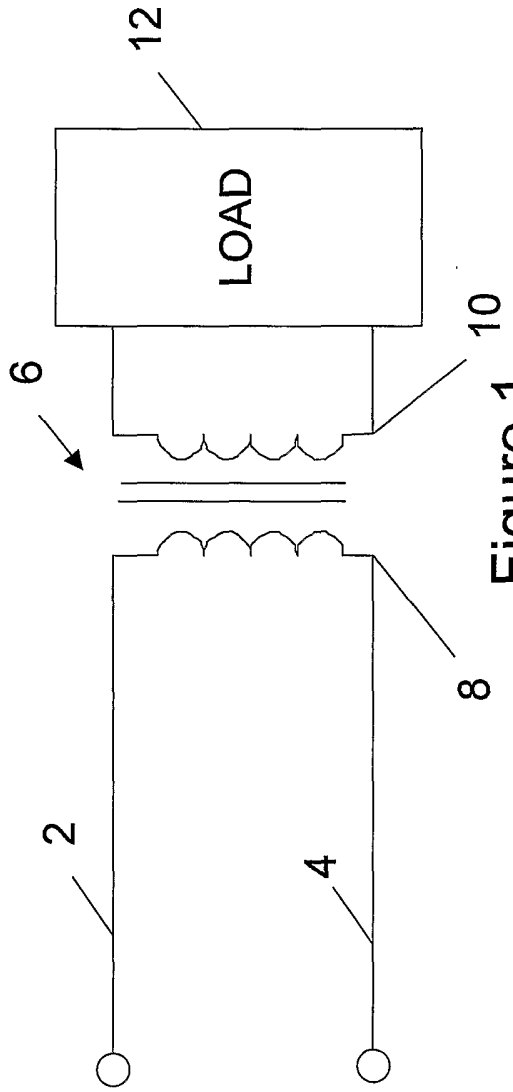


Figure 1
(Prior Art)

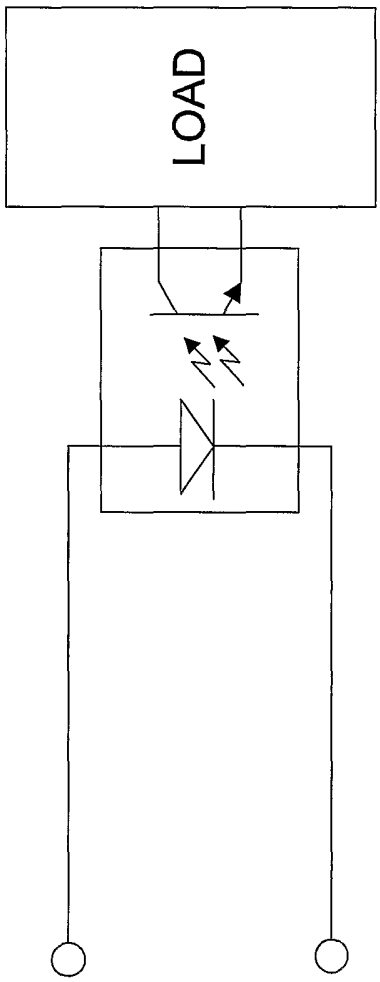


Figure 2
(Prior Art)

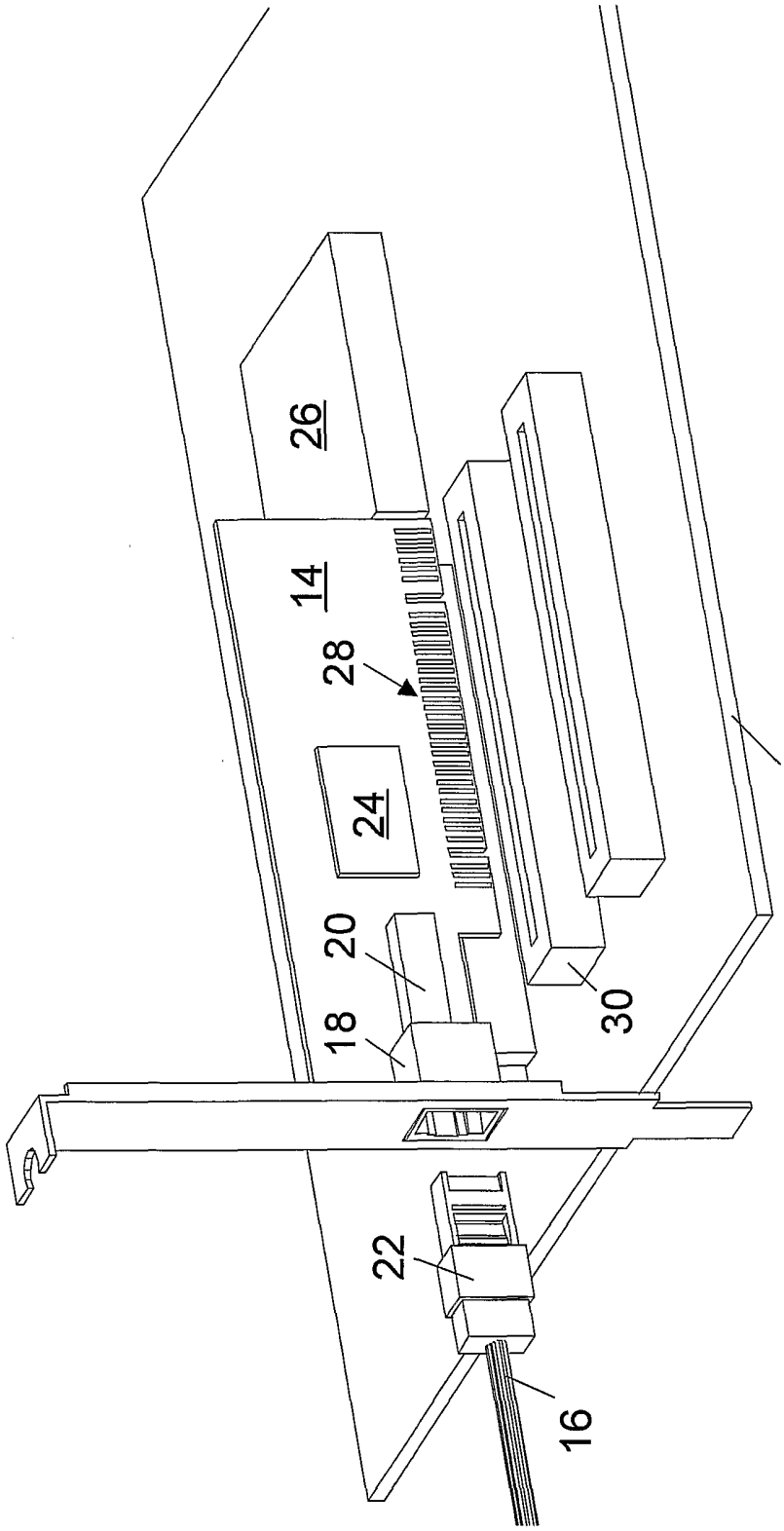


Figure 3
(Prior Art)

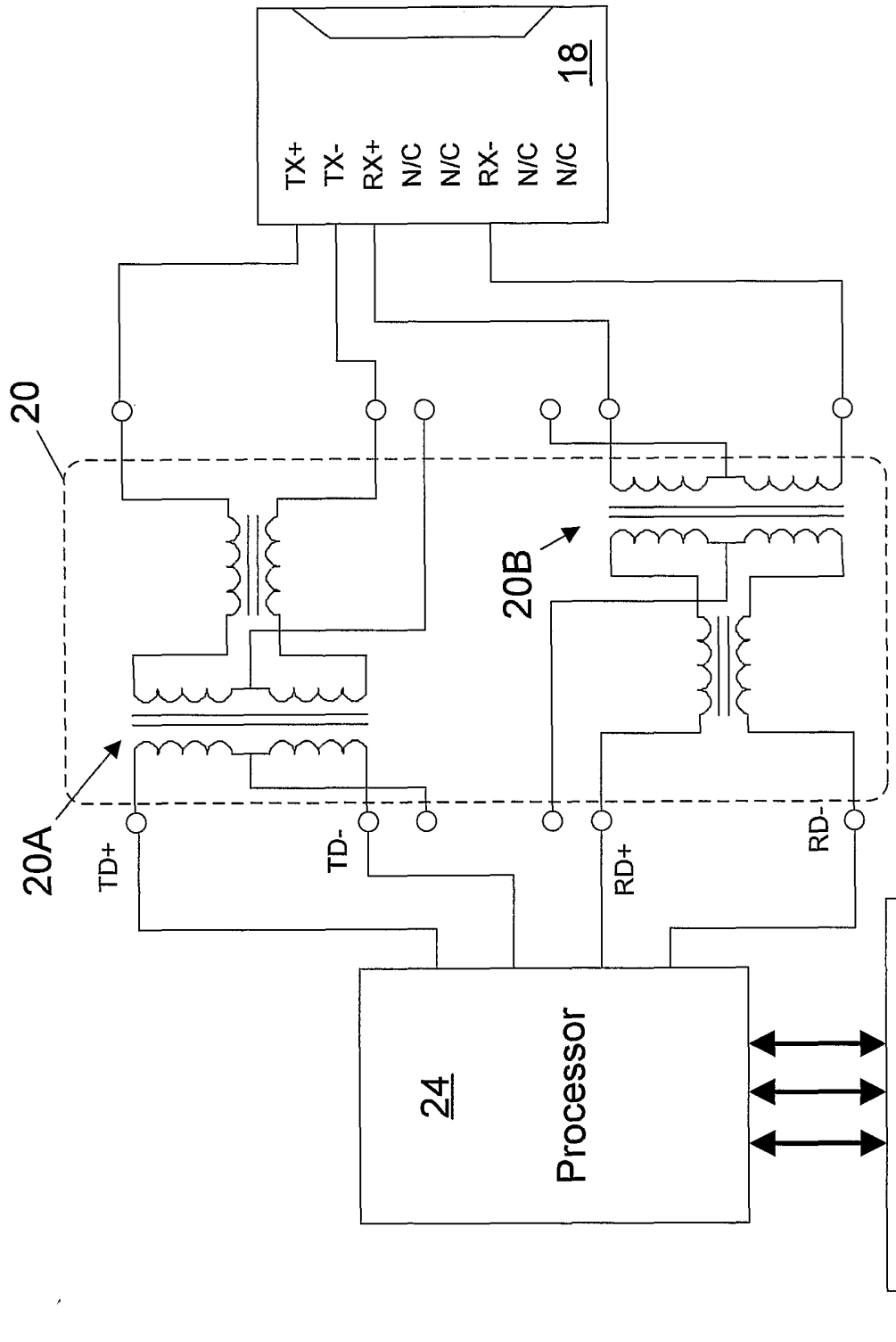


Figure 4
(Prior Art)

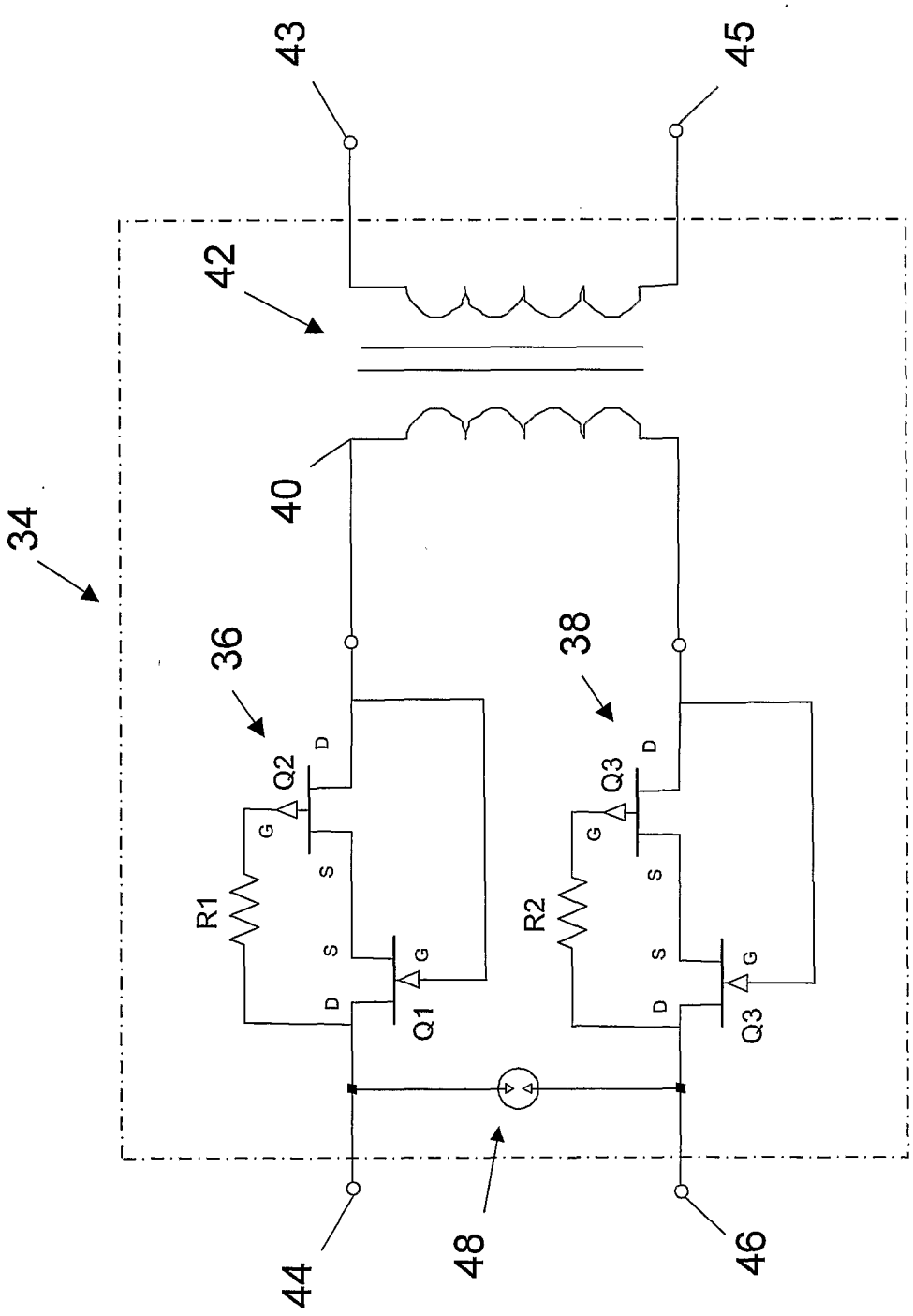


Figure 5

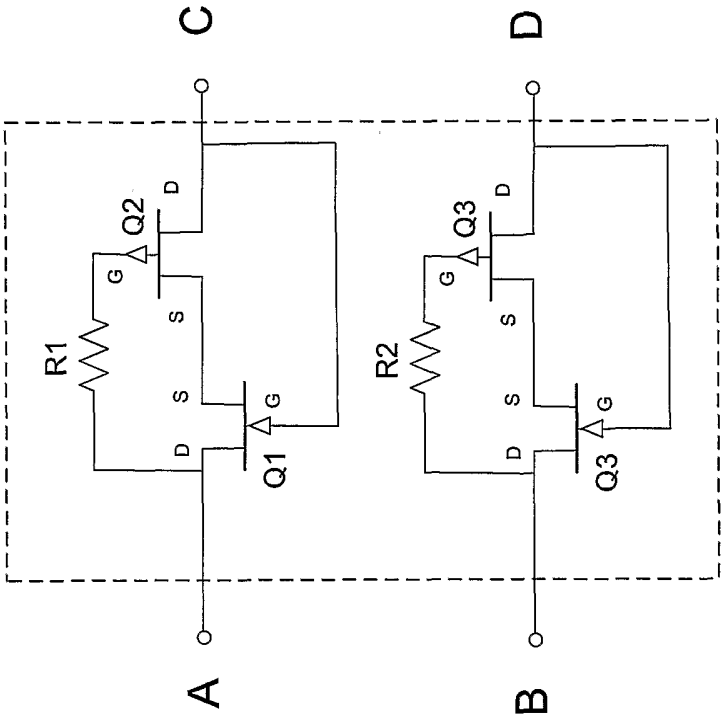


Figure 7

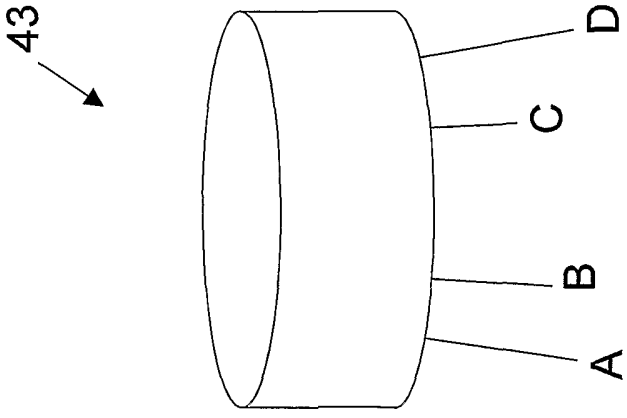


Figure 6

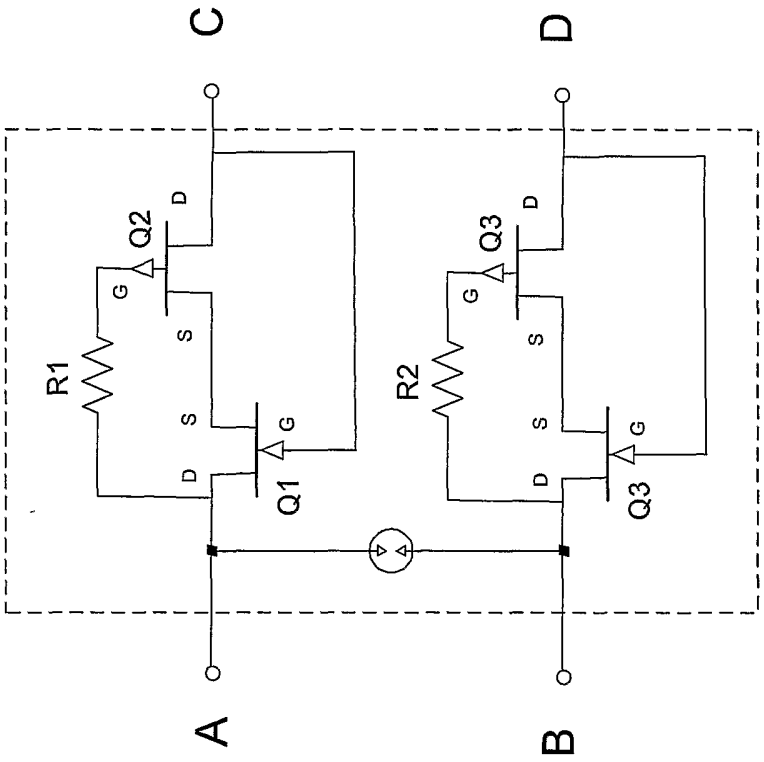
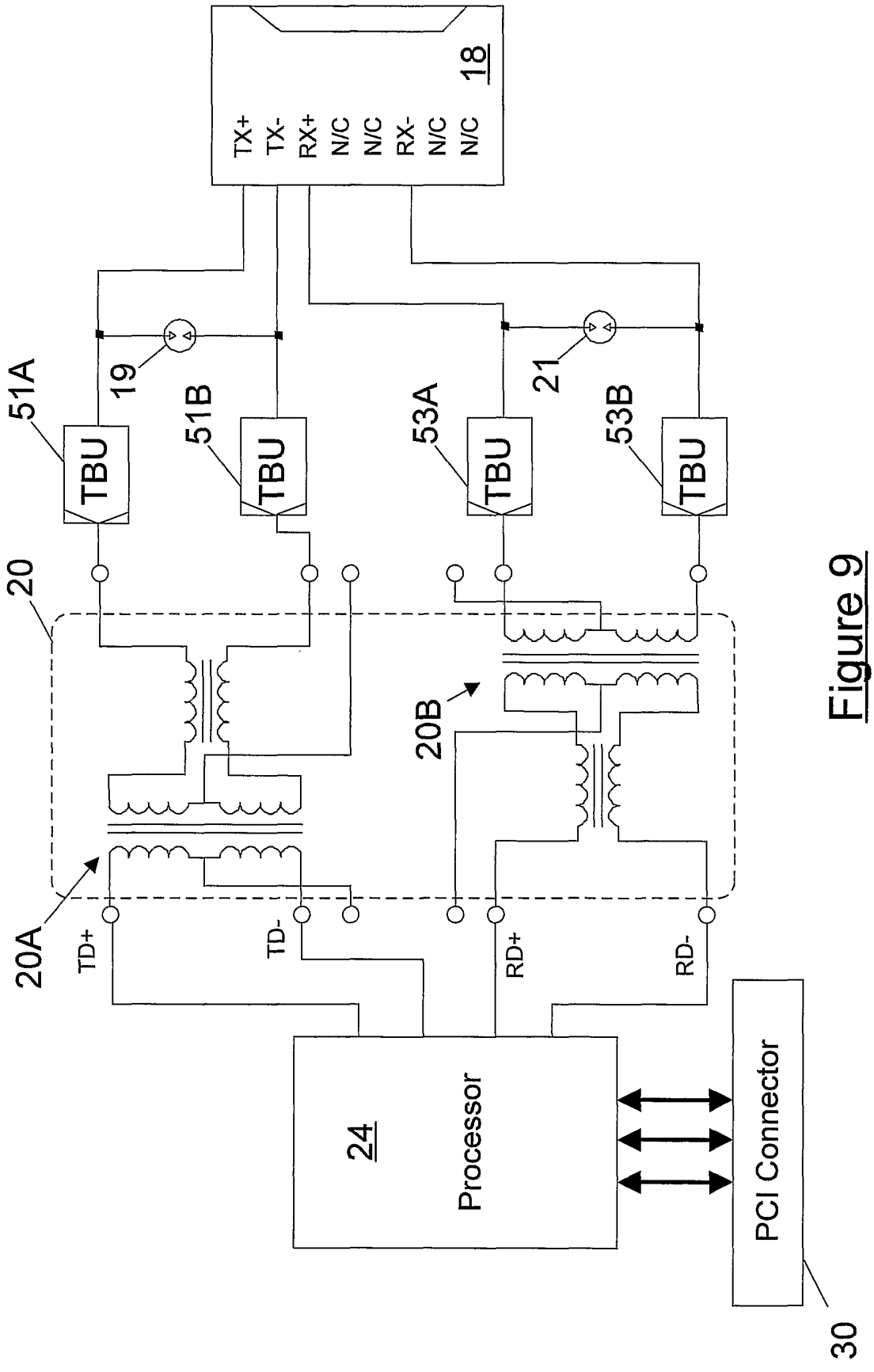


Figure 8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TX+
TX-
RX+
N/C
N/C
RX-
N/C
N/C
19
21
51A
51B
53A
53B
TBU
TBU
TBU
TBU
20
20A
20B
TD+
TD-
RD+
RD-
24
Processor
PCI Connector
30

Figure 9

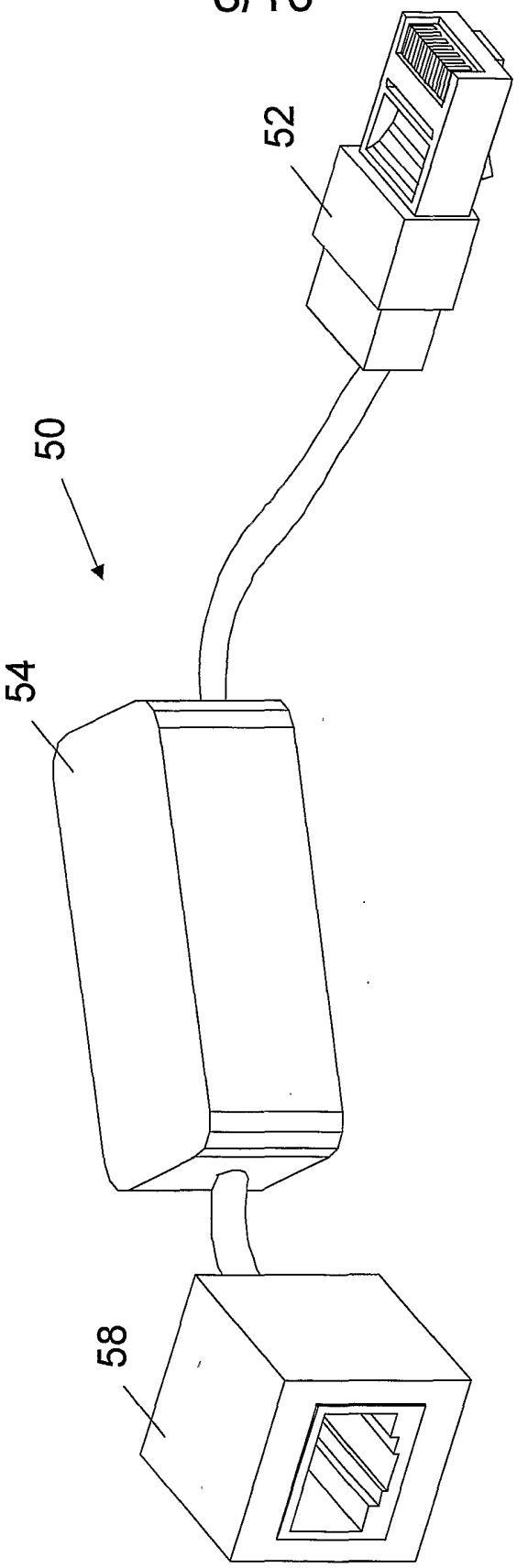
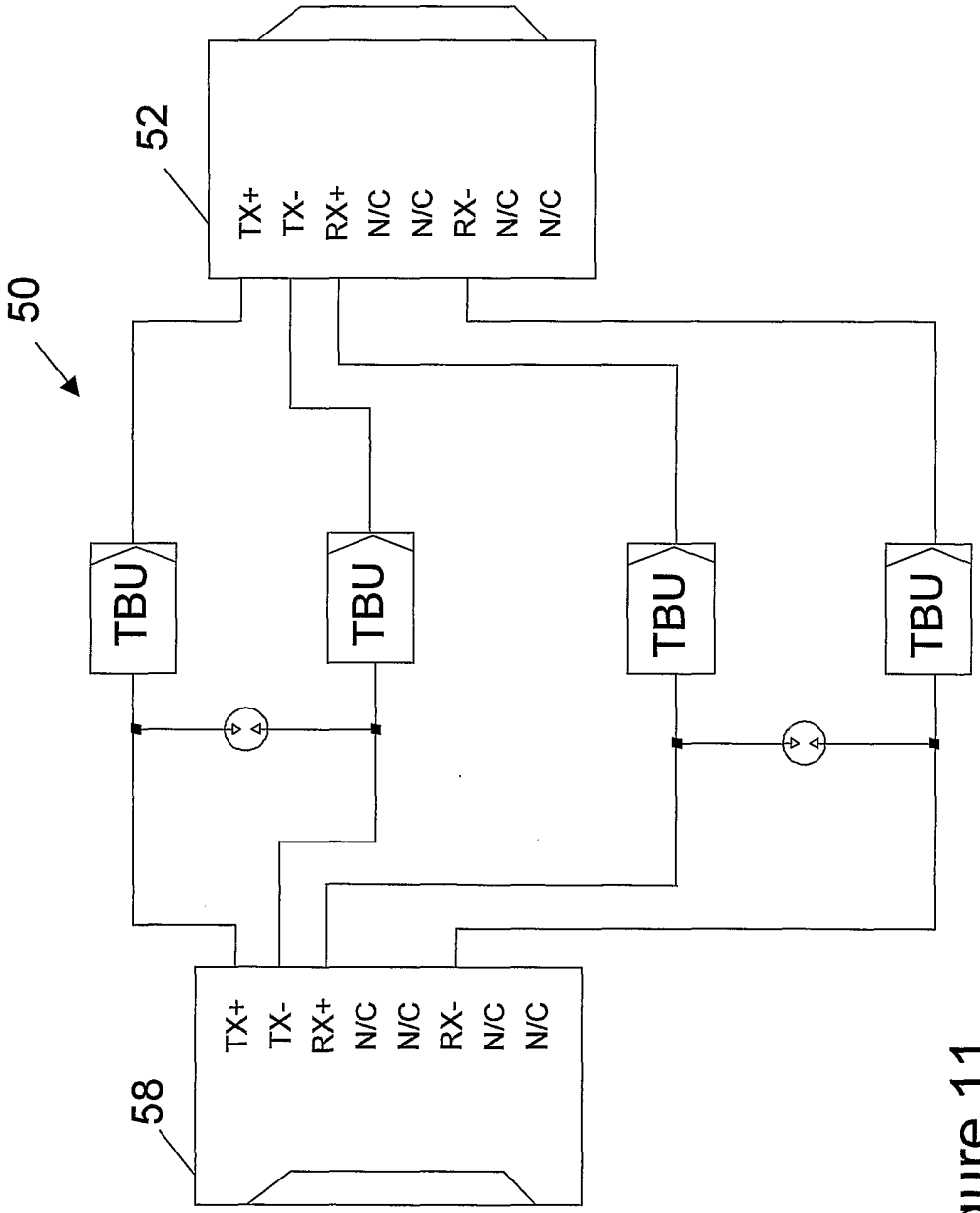


Figure 10


50
52
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TX-
RX+
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N/C
RX-
N/C
N/C
TBU
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TX-
RX+
N/C
N/C
RX-
N/C
N/C
58

Figure 11

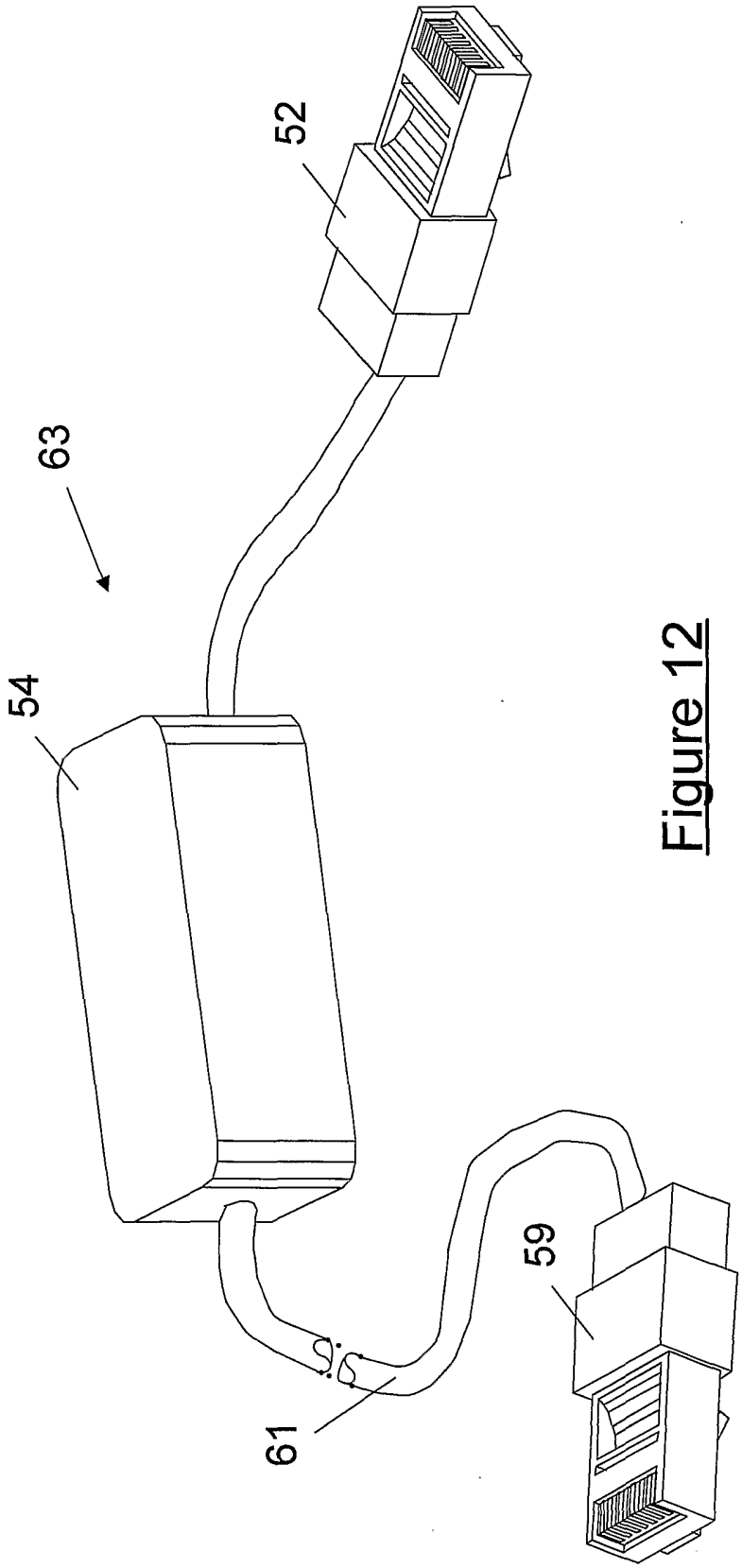

Figure 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU03/01326

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H02H 9/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
REFER ELECTRONIC DATA BASE CONSULTED BELOW

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI: IPC H02H 3/-, H02H 9/-, H01L 29/-, G05F 1/- & keywords: SURGE, SUPRESS+, DIFFERENTIAL, TBU, TWISTED PAIR and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 01/01539 A1 (TYCO ELECTRONICS CORPORATION) 4 January 2001 See: whole document, especially Fig.2 and page 1 line 10 - page 6 line 25	1-4, 6-17
A	US6252754 B1 (CHAUDHRY) 26 Jun 2001 See whole document	1-17

[-] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 October 2003	29 OCT 2003
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **BAYER MITROVIC** Telephone No : (02) 6283 2164

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/AU03/01326

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	01/01539	AU	58989/00	BR	0012458	CA	2377456
		EU	1192696	US	6266223		
US	6252754	AU	12251/00	US	6188557	WO	0038152
							END OF ANNEX