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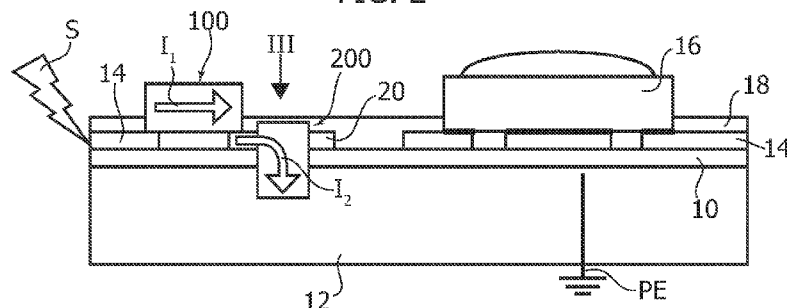
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(54) Title: A LIGHTING DEVICE AND A METHOD OF PRODUCING A LIGHTING DEVICE

FIG. 2



(57) Abstract: A lighting device includes: - an insulated metal substrate (10, 12, 14) with an electrically insulating layer (10) having first and second opposed faces, electrically conductive lines (14) on the first face of the electrically insulating layer and a base metal layer (12) coupled with the second face of the electrically insulating layer, at least one electrically powered light radiation source (16), e.g. a LED source, mounted on the electrically conductive lines (14), - an electrical overstress protection. The protection includes: a first surge clamp (100) between the electrically conductive lines (14) and an electrically conductive pad (20) on the electrically insulating layer (10), and a second surge clamp (200) between the electrically conductive pad (20) and the base metal layer (12), whereby overstresses on the electrically conductive lines (14) are discharged to said base metal layer (12) by the first (100) and the second (200) surge clamps.

A LIGHTING DEVICE AND A METHOD OF PRODUCING A LIGHTING DEVICE

Technical field

The present description relates to lighting
5 devices.

One or more embodiments may refer to lighting devices employing LED sources as light radiation sources.

Technological background

10 Lighting devices such as LED modules may meet requirements such as:

- high luminous flux (e.g. > 10,000 lm) in hot conditions (e.g. with a housing temperature higher than 70° C);
- 15 - high power efficiency (e.g. > 110 lm/W), in hot conditions (e.g. with a housing temperature higher than 70° C);
- high electrical insulation (e.g. > 2 kV AC) due to the dielectric breakdown of the PCB (Printed Circuit
20 Board) and to creepage and clearance (CR & CL) distance;
- high reliability in terms of high rated lumen maintenance life (e.g. > 50.000 hours) and low catastrophic failure rate;
- 25 - low cost.

In order to meet such specifications a trade-off may be pursued among thermal management (e.g. thermal resistance), breakdown voltage and cost of the lighting module.

30 Moreover, the overall LED luminaire (including the Electronic Control Gear (ECG) and the lighting module, e.g. LED module) may need to be robust against Electrical OverStress (EOS), possibly also including lightning surges.

On the market level a trend is to be seen towards an ever-increasing degree of robustness, e.g. with values of 10 kV for Line and Neutral to Protective Earth (L+N-PE) stress.

5 The ECG may not be able to offer a surge protection to the overall luminaire without involving high costs; moreover, it is desirable for the lighting device to be robust against stress without jeopardizing other features, which makes it difficult to meet all
10 the previously described needs.

The robustness of a lighting device, e.g. a LED lighting device, against EOS events, e.g. against surge events, may depend on various facts such as:

- robustness against current overstresses,
- 15 - the so called CR & CL (creepage and clearance) distance,
- the overall parasitic capacitance of the lighting sources with respect to the PE (Protective Earth) plane, which may consist e.g. in a housing or
20 heatsink of a metal material, e.g. aluminium.

Figure 1 is a schematic representation of a LED lighting module including:

- an Insulated Metal Substrate (IMS) board, adapted to include an electrically insulating
25 dielectric layer 10 arranged on the base metal layer 12, with electrically conductive lines or tracks 14, and
- one or more electrically powered light radiation sources 16, e.g. LED sources, applied on the
30 electrically conductive lines 14 e.g. through a solder mask 18.

Such an assembly is adapted to be mounted on a thermally dissipative support, such as for example a housing or heatsink (not visible in the Figures).

In general terms the described structure must be considered as known in itself in different various embodiments, which makes it unnecessary to provide a more detailed description herein.

5 Figure 1 shows the behaviour of such a lighting device in the presence of an electrical overvoltage (schematically represented by the broken arrow S) at the supply lines (positive line - LED⁺ and/or negative line - LED⁻).

10 Between lighting source(s) 16 and the PE plane of the support (e.g. housing or heatsink) which may be considered as practically short-circuited with respect to the base metal layer 12) a parasitic capacitance C may appear. Because of such a parasitic capacitance C,
15 an overvoltage S may generate a displacement current (schematically shown with arrows I₁ and I₂) which may pass first through source(s) 16 and then through the dielectric layer 10 of the IMS board. This involves the risk of inducing a failure of source 16 and/or of
20 dielectric 10.

A possibility to deal with this problem may consist in the choice of light radiation sources with a high robustness against current overstresses.

This solution however may involve some problems.

25 For example, the robustness data may not be available for certain sources.

In addition, a different source type may cause substantial changes in performances (e.g. in luminous flux and power efficiency), in long-term reliability
30 (e.g. lumen maintenance, catastrophic failure rate, solder-joint reliability) and in cost.

Another way to face the previously outlined problem may consist in choosing boards having a low parasitic capacitance (C_{par}). In the case of IMS boards,
35 a low parasitic capacitance may be achieved by using

thick dielectrics, which however may lead to a worse thermal management, or low-k dielectric materials.

It is also possible to use ceramic or FR-4 single or double layers having a thick dielectric layer.

5 These ceramic boards have good performance in thermal management and electrical insulation, but their use may be limited by considerations of cost and by a high sensitivity to vibrations.

10 Moreover, such boards as FR-4 may have high thermal resistance, which drastically reduces the performances of the lighting module.

Another possibility may involve the use of Thermal Interface Materials (TIMs) with electrical insulation properties.

15 By using a TIM layer the parasitic capacitance may be reduced dramatically.

20 This solution, however, requires an ad-hoc system to fix the lighting module to the support (housing/heatsink, e.g. of aluminium), because the use of screws may make TIMs ineffective.

25 This solution, moreover, may involve higher costs, because the materials for TIM interfaces must have good electrical insulation properties and a low thermal resistance, in order to avoid an increase of the overall thermal resistance.

A further possibility may involve the use of Surge Protection Devices (SPDs) arranged at the ECG or between the ECG and the light radiation sources.

30 This solution, however, involves higher costs, because the integration of the SPD into the lighting device and its connection to PE may present difficulties.

Object and Summary

35 One or more embodiments aim at overcoming the previously outlined drawbacks.

According to one or more embodiments, said object is achieved thanks to a device having the features specifically set forth in the claims that follow.

One or more embodiments may also refer to a
5 corresponding method.

The claims are an integral part of the technical teaching provided herein with reference to the invention.

In one or more embodiments, overstresses (e.g. EOS
10 events) on the electrically conductive lines may be discharged towards the base metal layer of the IMS substrate through a first and a second surge clamp, without risking the generation of displacement currents, which may traverse the light radiation
15 source(s) and the dielectric material of the substrate and damage them.

One or more embodiments may lead to the achievement of one or more of the following advantages:

- improved EOS robustness,
- 20 - very low, practically negligible BOM increase,
- design simplification and easy implementation,
- no significant consequent alterations of the other characteristics of the lighting device, such as thermal resistance, electrical insulation, etc.

25 Brief description of the Figures

One or more embodiments will now be described, by way of non-limiting example only, with reference to the enclosed figures, wherein:

- Figure 1 has already been described in the
30 foregoing,

- Figure 2 shows, according to modes substantially corresponding to Figure 1, examples of embodiments;

- Figure 3 is a detail substantially along arrow III of Figure 2, and

35 - Figures 4 to 9 show various possible

embodiments.

It will be appreciated that, for a better clarity of illustration, the parts visible in the Figures are not necessarily drawn to scale.

5 Detailed Description

In the following description, numerous specific details are given to provide a thorough understanding of one or more exemplary embodiments. The embodiments may be practiced without one or several specific
10 details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the embodiments. Reference throughout this specification to "an
15 embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the possible appearances of the phrases "in one embodiment" or "in an embodiment" in various places
20 throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

25 The headings provided herein are for convenience only and therefore do not interpret the scope or meaning of the embodiments.

Moreover, in Figures 2 to 9, parts and elements similar or equivalent to others already introduced in
30 the description of Figure 1 have been denoted with the same reference numbers. A corresponding description, therefore, will not be repeated for Figures 2 to 9. On the other hand, the use of the same reference number for parts or elements in the various Figures does not
35 necessarily mean that they must be implemented in the

same way in one or more embodiments as exemplified therein.

In short, the Figures refer to devices comprising:

- an Insulated Metal Substrate (IMS) with an electrically insulating layer 10 having a first and a second opposed faces, with electrically conductive lines 14 on the first face of the electrically insulating layer and a base metal layer 12 coupled with the second face of the electrically insulating layer,
- one or more electrically powered light radiation sources 16, e.g. LED sources, mounted on the electrically conductive lines 14, e.g. through a solder mask 18.

One or more embodiments may be based on the idea of integrating (embedding) a protection structure against electrical overstresses (e.g. EOS events) directly into a lighting module (e.g. a LED module) based on an IMS board structure, as previously described, in order to guarantee a protection against surges between the LED⁺/LED⁻ terminals and PE, while ensuring the necessary electrical insulation.

In one or more embodiments, the related protection structure may include two surge "clamps" 100 and 200.

The term "clamp" denotes in general an electrical device for protecting circuits against electrical overstresses, such as overvoltages.

In one or more embodiments it is an arrangement which (by operating according to modes exemplified in the following) enables to absorb surges, therefore avoiding the generation of a displacement current which may damage the radiation source(s), e.g. LED sources, and/or the dielectric of the lighting device board.

Referring to the schematic representation of Figure 2, a first clamp 100 may be connected between electrically conductive lines 14 (positive, LED⁺,

negative, LED⁻), e.g. copper lines, and a conductive pad 20 (e.g. a copper pad) arranged for example on the electrically insulating layer 10, so as to be electrically insulated from lines 14.

5 In one or more embodiments, first surge clamp 100 may have, during the normal operation of the device, a high resistance (substantially behaving as an open circuit), its (AC and CC) trigger voltage being adapted to be higher than the electrical insulation value
10 required for the lighting device.

 In the presence of an electrical overstress, clamp 100 is adapted to act as a low-resistive path (practically a short circuit), by discharging for example an EOS event towards second clamp 200.

15 In one or more embodiments, the second clamp 200 may be connected between said pad 20 and the base metal layer 12 (e.g. of aluminium) of the IMS structure, which, as previously stated, may actually be considered, especially during the discharge, as short-
20 circuited to PE.

 In one or more embodiments, the second clamp 200 may actually be implemented so as to behave as a short circuit between its terminals, both during the normal operation of the device and in the presence of an
25 overstress such as for example an EOS event.

 In one or more embodiments, the overstress discharged from the first clamp 100 may be caused to be discharged to PE through the second clamp 200.

 Figures 3 to 9 exemplify various possible
30 embodiments of the general principle of operation schematically shown in Figure 2.

 In one or more embodiments, features that are shown herein separately, with reference to any one of the Figures 2 to 9, may be present both in combination
35 and in swap arrangements: for example, a feature that

has been illustrated herein with reference to a certain Figure may be applied to one or more embodiments exemplified in another Figure.

Figures 3 to 5 exemplify one or more embodiments
5 wherein the first clamp 100 may be implemented as a spark gap, i.e. may be adapted to generate electrical sparks in the air, while the second clamp 200 is simply implemented as an electrically conductive path or "via" 22 which traverses the dielectric layer 10 (see for
10 instance Figure 4) starting from pad 20 to the base metal layer 12.

Figure 3 is an ideal top view roughly corresponding to the view point shown by arrow III of Figure 2, wherein the first clamp 10 is obtained by a
15 spark gap 24 having e.g. the shape of a star, such as a star with eight points arranged in four pairs regularly spaced by 90° around the periphery.

The representation of Figure 3 is deliberately schematic, because the geometry of gap 24 and of the
20 parts which define it may be modified in many different ways. In Figure 3, the external portion 14 may be seen as representative of a portion of conductive tracks 14 (which may be chosen as close as possible to the connection to source(s) 16), while the internal portion
25 represents pad 20 connected to the base metal layer 12 through the conductive connection or via 22, the contour of which is schematically represented by dashed lines.

In one or more embodiments, the separation gap 24
30 between the terminals of clamp 100 (lines 14 and pad 20) may be large enough to guarantee the CR&CL (creepage and clearance) distance adapted to ensure the necessary electrical insulation, both in CC and in AC normal operation of the device, even after several
35 surge pulses.

In one or more embodiments, it is possible to control the discharge voltage and reduce the possible damage of solder mask 18 and of dielectric 10 of the PCB board during the discharges, because the EOS event
5 is discharged in air. In one or more embodiments, as exemplified in Figures 3 and 4, this result is obtained if gap 24 defines, between the two metal terminals (e.g. of copper, both for lines 14 and for pad 20) an air path where the solder mask 18 is absent.

10 In one or more embodiments, the possible oxidation of metal, e.g. copper, parts which are not covered by the solder mask may be contrasted by a surface finish, e.g. through an LF HASL (Lead Free Hot Air Solder Leveling).

15 As previously stated, in one or more embodiments the second clamp 200 may simply include a conductive path or "via" 22 through the dielectric layer, which may be implemented in an IMS board with known technologies, e.g. by SinkPAD LLC of Placentia CA
20 92870, USA.

Figure 5 exemplifies the behaviour of the exemplified arrangement during an EOS event, shown by arrow S and adapted to be discharged initially through the first clamp 100 (e.g. with the star-shaped spark
25 gap) and then towards PE through path or via 22.

In one or more embodiments, as exemplified in Figure 6, the first clamp 100 may be implemented according to the examples of Figures 3 to 5, while the second clamp 200 may envisage the presence of an
30 inserted element, possibly through press-fitting and subsequent soldering, of a soldered metal.

In one or more embodiments, said element may have a mushroom-like shape, with a head part 26 and a stem part 28, the stem part 28 being inserted into a hole
35 120 in the metal layer 12 and the head part 26 being

supported against pad 20. As these parts are of an electrically conductive material (e.g. soldered material), there is provided an electrical connection between the terminal of first clamp 100, consisting in
5 the pad 20 (see for example Figure 3) and PE.

One or more embodiments as exemplified in Figure 6 may be less costly compared with the embodiments exemplified in Figures 4 and 5, because they avoid forming a path or via 22 through the IMS board.

10 Figures 7 and 8 exemplify one or more embodiments wherein the second clamp 200 is substantially similar to the clamp shown in Figures 4 and 5, while the first clamp 100 may be implemented in different ways.

As previously stated in the introduction to the
15 present detailed description, elements and features exemplified with reference to any one of the annexed Figures may be freely applied to embodiments shown in other Figures.

In one or more embodiments as exemplified in
20 Figure 9, the second clamp 200 may thus substantially correspond to the one exemplified in Figure 6, while the first clamp 100 may correspond to the one shown in Figures 7 and 8.

In one or more embodiments as exemplified in
25 Figures 7 to 9, the first clamp 200 may consist in a proper spark gap, such as an air discharged tube as available from various manufacturers, such as Bourns, Inc. of Riverside, CA (USA) or Vishay Intertechnology, Inc. of Malvern, PA (USA), or by a varistor (e.g. a
30 ceramic varistor) as supplied by various manufacturers, such as EPCOS AG of Munich (Germany), Murata Manufacturing Co., Ltd of Nagaokakyo, Kyoto (Japan) and previously quoted Vishay.

In comparison with the star-shaped solution
35 exemplified in Figure 3, one or more embodiments of the

first clamp 100, as exemplified in Figures 7 to 9, may contribute to guaranteeing the desired trigger voltage during the EOS events, and the AC and DC electrical insulation after several EOS events.

5 In one or more embodiments as exemplified in Figures 7 and 8, the second clamp 200 may be of the kind exemplified in Figure 6: the related components have actually been denoted with the same reference numbers, while keeping in mind that the attribution of
10 the same reference number does not necessarily imply that the related solutions must be implemented in the same way.

Figure 8 exemplifies the behaviour of the structure shown in Figure 7 during an EOS event, which
15 is discharged through the first clamp 100 (see arrow I_1) towards PE through path 22 of the second clamp 200 (see arrow I_2).

As previously stated, Figure 9 exemplifies one or more embodiments combining the possibility of
20 implementing the first clamp 100 as exemplified in Figures 7 and 8 with the possibility to form the second clamp 200 as exemplified in Figure 6.

Of course, without prejudice to the principle of the invention, the details and the embodiments may
25 vary, even appreciably, with respect to what has been described herein by way of non-limiting example only, without departing from the extent of protection.

Said extent is defined by the annexed claims.

CLAIMS

1. A lighting device, including:

- an insulated metal substrate (10, 12, 14) with an electrically insulating layer (10) having first and second opposed faces, electrically conductive lines (14) on the first face of the electrically insulating layer and a base metal layer (12) coupled with a second face of the electrically insulating layer,
- at least one electrically powered light radiation source (16) mounted on said electrically conductive lines (14),
- an electrical overstress protection including:
 - a first surge clamp (100) between the electrically conductive lines (14) and an electrically conductive pad (20) on said electrically insulating layer (10), and
 - a second surge clamp (200) between said electrically conductive pad (20) and said base metal layer (12), whereby electrical overstresses on said electrically conductive lines (14) are discharged to said base metal layer (12) by said first (100) and second (200) surge clamps.

2. The lighting device of claim 1, wherein said first surge clamp (100) includes an air gap (24) between said electrically conductive lines (14) and said electrically conductive pad (20).

3. The lighting device of claim 1 or claim 2, wherein said first surge clamp (100) includes a star-like spark gap (24) between said electrically conductive lines (14) and said electrically conductive pad (20).

4. The lighting device of any of the previous claims, wherein said first surge clamp (100) includes an air discharge tube.

5. The lighting device of any of claims 1 to 3,

wherein said first surge clamp (100) includes a varistor, preferably a ceramic varistor.

6. The lighting device of any of the previous claims, wherein said second surge clamp (200) includes
5 at least one electrically conductive via (22) through said insulating layer (10).

7. The lighting device of any of claims 1 to 5, wherein said second surge clamp (200) includes an electrically conductive member (26, 28) in said metal
10 base layer (12), preferably press fitted and soldered therein.

8. A method of producing a lighting device including:

- providing an insulated metal substrate (10, 12,
15 14) with an electrically insulating layer (10) having first and second opposed faces, electrically conductive lines (14) on the first face of the electrically insulating layer and a base metal layer (12) coupled with a second face of the electrically insulating
20 layer,

- mounting at least one electrically powered light radiation source (16) on said electrically conductive lines (14),

- providing an electrical overstress protection
25 including:

- a first surge clamp (100) between the electrically conductive lines (14) and an electrically conductive pad (20) on said electrically insulating layer (10), and

30 - a second surge clamp (200) between said electrically conductive pad (20) and said base metal layer (12), whereby electrical overstresses on said electrically conductive lines (14) are discharged to said base metal layer (12) by said first (100) and
35 second (200) surge clamps.

FIG. 1

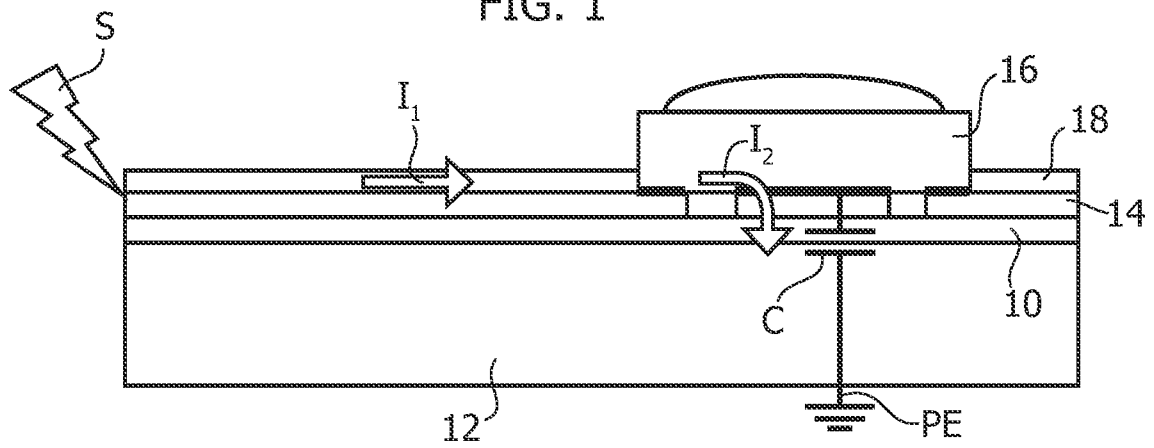


FIG. 2

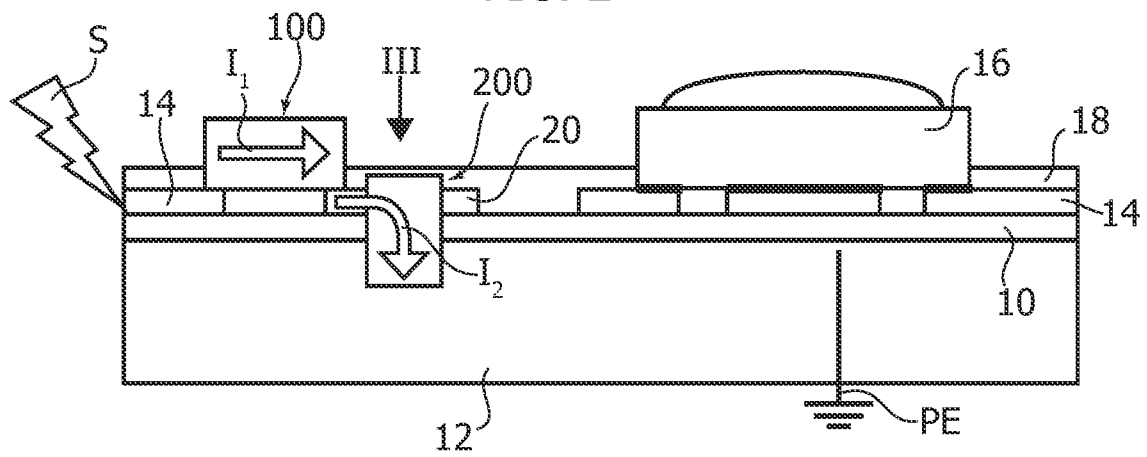


FIG. 3

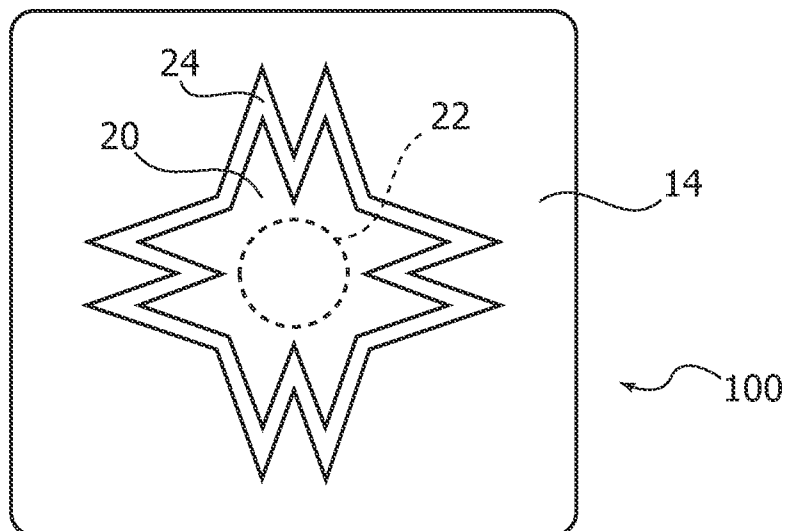


FIG. 4

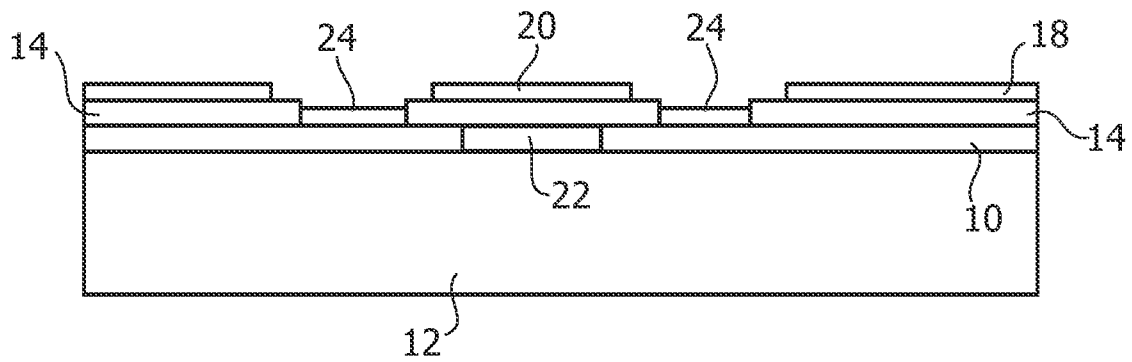


FIG. 5

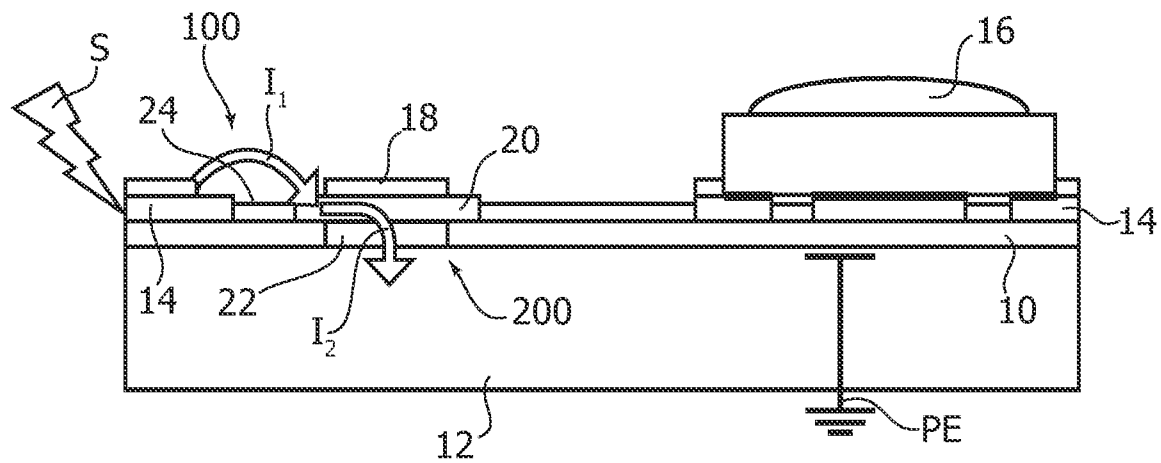


FIG. 6

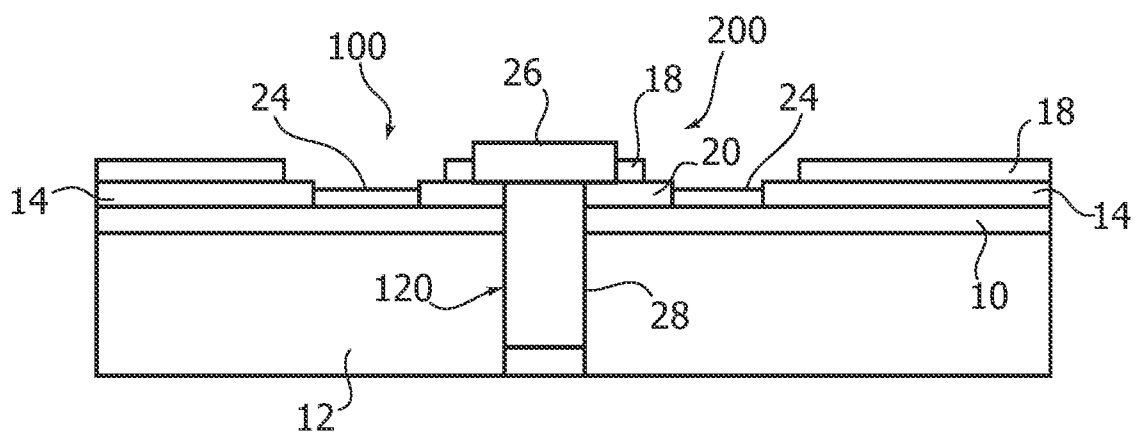


FIG. 7

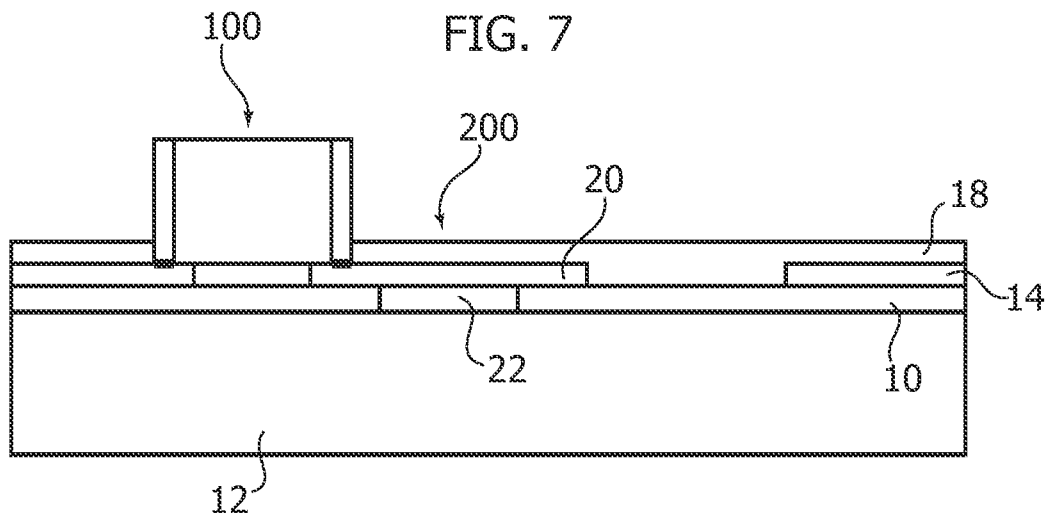


FIG. 8

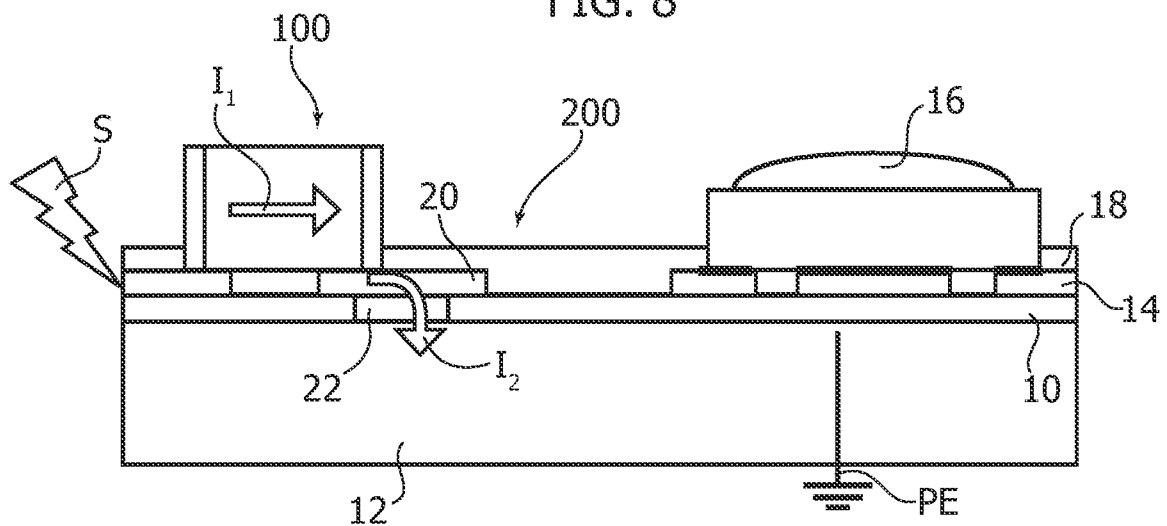
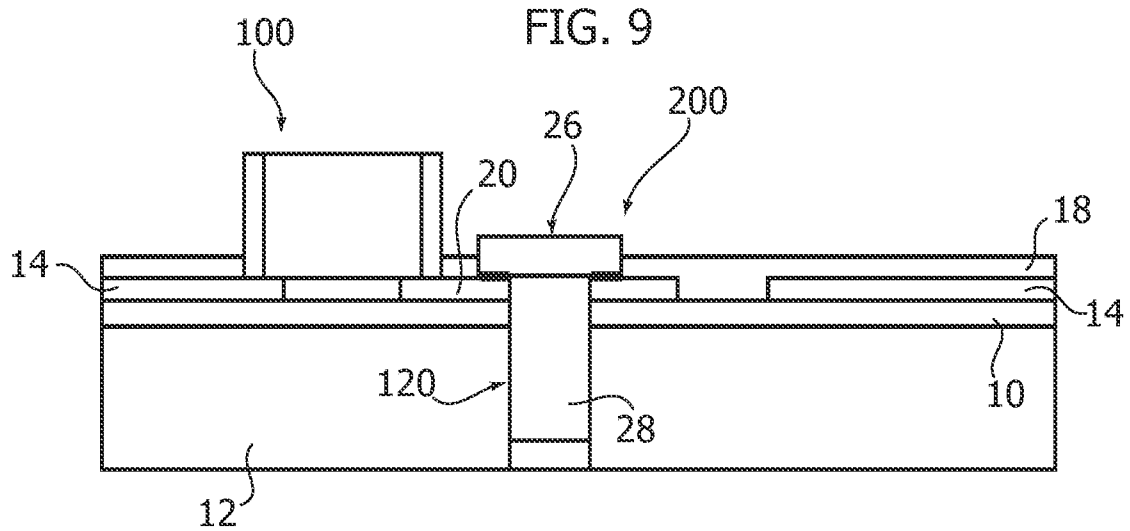


FIG. 9



INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2015/052189

A. CLASSIFICATION OF SUBJECT MATTER

INV. H05K1/02 H02H9/06
ADD. H05K1/05 H01T4/00 H01C7/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05K H01T H02H H01C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/246247 A1 (OOYABU YASUNARI [JP] ET AL) 25 October 2007 (2007-10-25)	1,4-6,8
Y	paragraphs [0013], [0014], [0033] - [0049]; figures 1, 2	2,3,7
Y	----- US 2010/053961 A1 (MO CI-JIN [CN] ET AL) 4 March 2010 (2010-03-04)	7
Y	paragraphs [0015] - [0021]; figures	
Y	----- US 2013/194708 A1 (LOEVSKOG THOMAS [SE] ET AL) 1 August 2013 (2013-08-01)	2,3
Y	paragraphs [0032] - [0042]; figures 1, 2C	
A	----- US 2010/270546 A1 (KOSOWSKY LEX [US]) 28 October 2010 (2010-10-28)	1-8
	paragraphs [0064] - [0080]; figure 8	
	----- -/--	



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

9 June 2015

Date of mailing of the international search report

16/06/2015

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Authorized officer

Batev, Petio

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2015/052189

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012/211773 A1 (FLEMING ROBERT [US] ET AL) 23 August 2012 (2012-08-23) paragraphs [0066], [0067], [0071], [0018]; figures 2A, 3A, 4C -----	1-8

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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