United States Patent

[11] 3,573,572

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[21] Appl. No. **761,587**
[22] Filed **Sept. 23, 1968**
[45] Patented **Apr. 6, 1971**
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[54] **CONTROLLED RECTIFIER HAVING HIGH RATE-OF-RISE-OF-CURRENT CAPABILITY AND LOW FIRING GATE CURRENT**
3 Claims, 8 Drawing Figs.

[52] U.S. Cl. **317/235,** 307/305
[51] Int. Cl. **H01l 11/10**
[50] Field of Search 317/235/41.1; 317/235/28, 235/44

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ABSTRACT: A semiconductor controlled rectifier having an auxiliary cathode region and a main cathode region with a main control gate lead disposed adjacent to the auxiliary cathode region. The controlled rectifier including the auxiliary cathode region can be fired by a relatively low gate current. The output current of the auxiliary cathode region is connected to auxiliary gates disposed in proximity to the main cathode and supplies necessary current for turning on the main portion of the controlled rectifier.

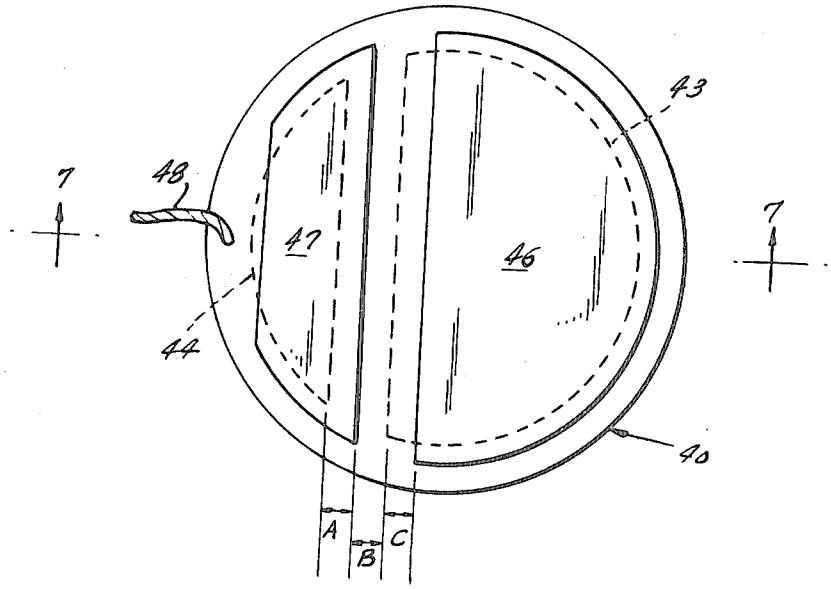

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FIG. 1.

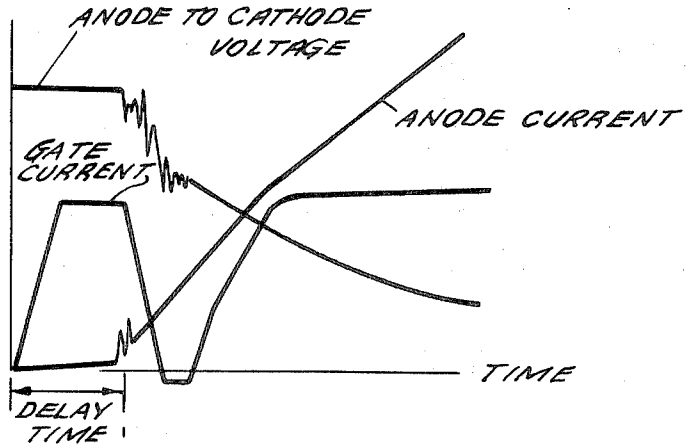

FIG. 2.

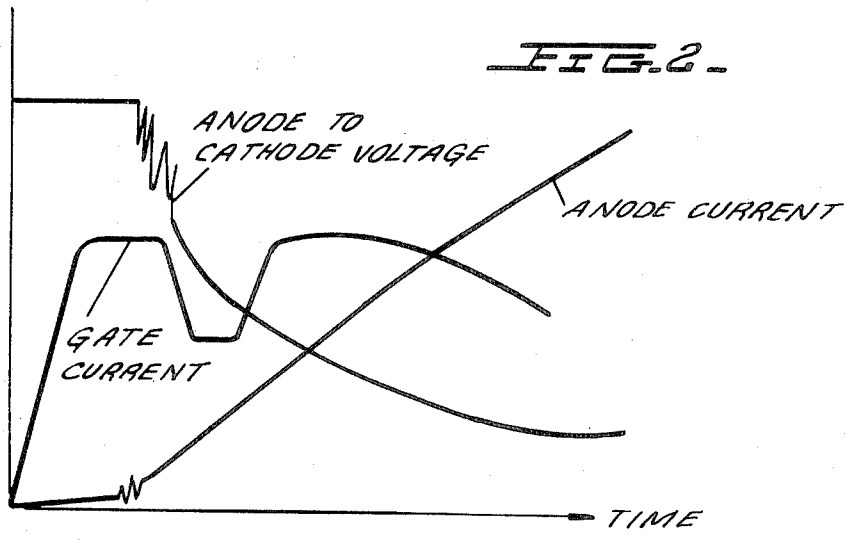

FIG. 3.

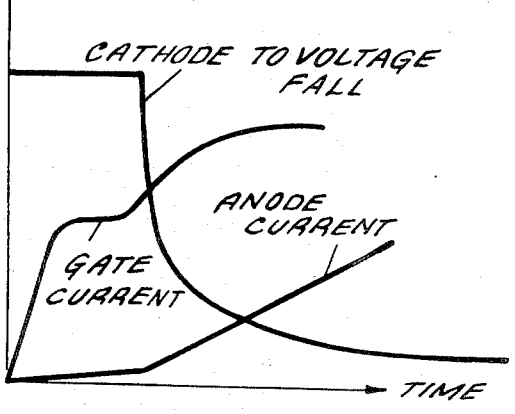

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FIG. 4.

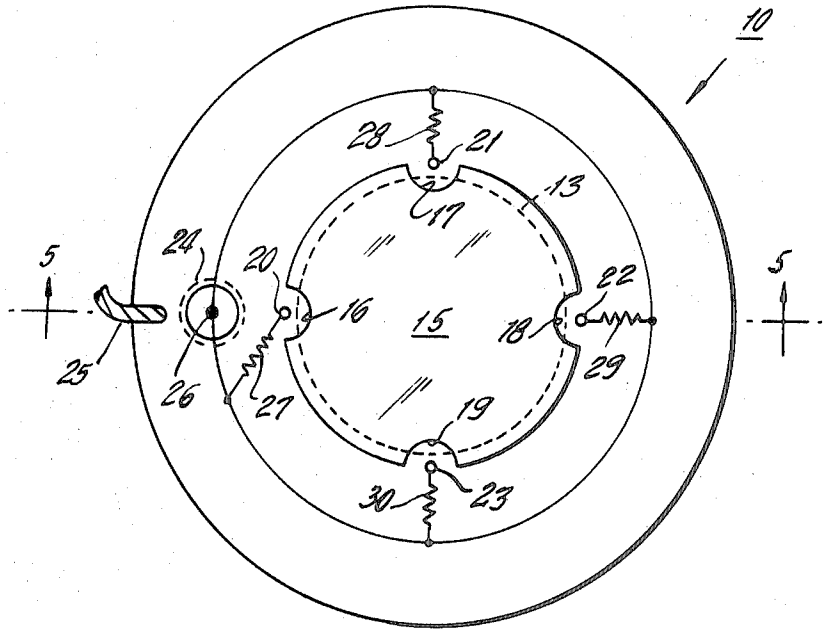

FIG. 5.

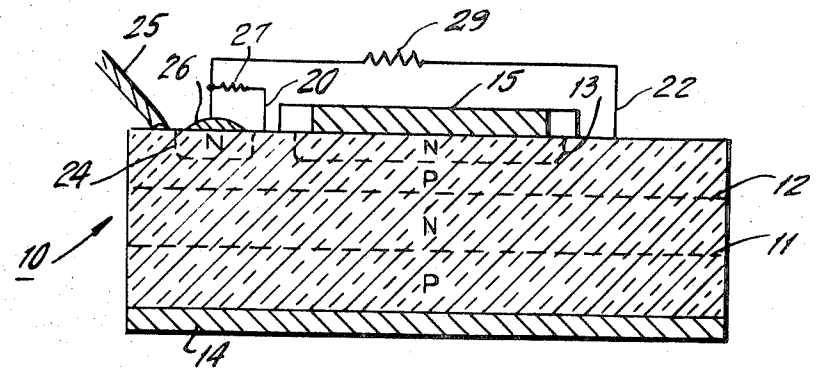

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FIG. 7

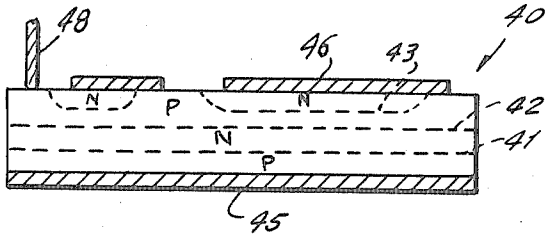


FIG. 6

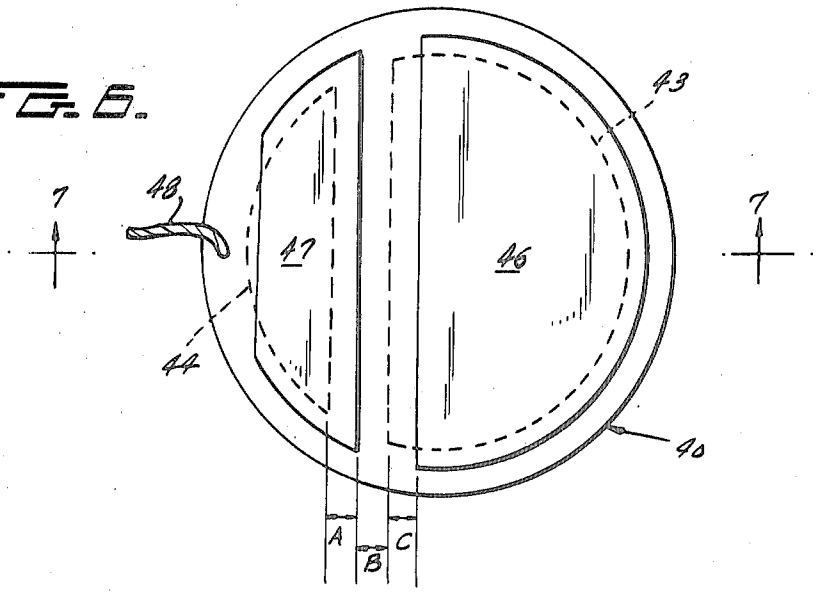
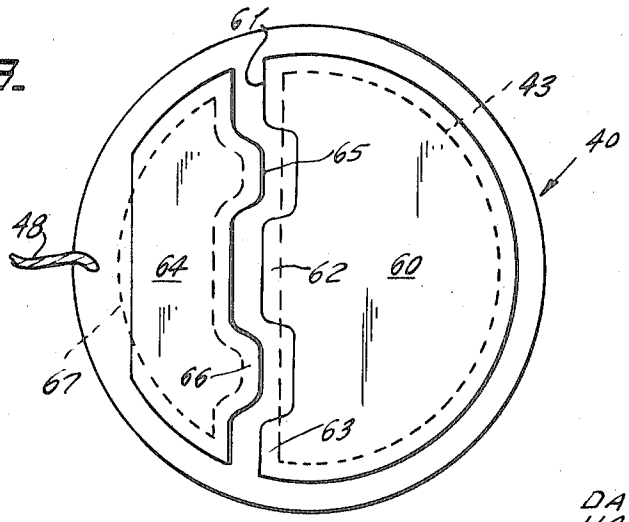


FIG. 8



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CONTROLLED RECTIFIER HAVING HIGH RATE-OF-RISE-OF-CURRENT CAPABILITY AND LOW FIRING GATE CURRENT

This invention relates to controlled rectifiers, and more particularly relates to a controlled rectifier having an auxiliary cathode region which is connected to at least one auxiliary gate electrode adjacent to the main cathode region, whereby a small gate signal causes the auxiliary cathode to conduct, thereby supplying current to the auxiliary gate electrodes which fire the main portion of the device.

Many applications require a controlled rectifier to have a relatively high rate-of-rise-of-current capability, and also to be capable of being fired with a low gate current. These have been considered to be inconsistent requirements for controlled rectifier design, since heretofore high gate currents have had to be utilized to obtain high rate-of-rise-of-current characteristic. In order to increase the rate-of-rise-of-current characteristics in a controlled rectifier, it has been common practice to provide a plurality of gate connections for the device so that a corresponding number of initial conducting plasmas will be created over a considerable area between the anode and cathode of the controlled rectifier. In such arrangements, the gate firing circuit must have sufficient current capability to supply the gate current required by each gate connection. It was also required to inject such supply current extremely rapidly, for example, in the order of 1 amp in 0.1 seconds. Therefore, a source of high gate current is normally required.

Another characteristic noted in prior art devices, heretofore unexplained, is a tendency for irregular wave patterns in anode-cathode voltage to appear shortly after device turn on. This represented an attempt of the device, through back e.m.f., to impede turn on action. Since the initial current injection wave over a very small area, the induced voltage irregularities tended to cause localized carrier injection to cease, which could be observed by gate current dropping to zero or below, concurrently in time with the observed voltage irregularity. This in turn caused an even smaller initial area to be turned on. Any anode current flowing at this time would thus be forced to flow through such constricted area, causing high current densities and high localized temperatures which led to device failure.

In accordance with the present invention, a controlled rectifier semiconductor wafer has an auxiliary cathode region adjacent to the main cathode region. A main gate lead is also connected adjacent to the auxiliary cathode. The main cathode region is provided with one or more gate connections in order to form the desired initial conducting plasmas necessary to a high rate-of-rise-of-current device. A low gate firing the auxiliary cathode will then cause the main cathode to conduct.

The high current from the auxiliary cathode is provided by the internally generated e.m.f. caused by device turn on. The magnitude of such auxiliary current is a function of the rate-of-rise-of-anode current. Thus, with more rapid current increase, the main cathode injection correspondingly becomes more rapid. Consequently, the gate current will not tend to dip and irregularities in anode-cathode voltage will be diminished. Moreover, since the initial current flow will not be confined to a small area, inrush current capability of the device is greatly improved as a further result of a wider current path, and localized burnout leading to device failure is reduced.

Accordingly, a primary object of this invention is to provide a novel controlled rectifier device having a high rate-of-rise-of-current capability which is internally induced by a low external gate current.

Another object of this invention is to provide a novel controlled rectifier structure in which a relatively low gate current, such as the output of an integrated circuit, can fire a controlled rectifier without amplification.

Another object of this invention is to improve the stability and decrease failure rate of high rate-of-rise-of-current controlled rectifiers.

Still another object of this invention is to provide a novel high rate-of-rise-of-current capability controlled rectifier having internal gate means driven from an auxiliary cathode which in turn is excited by a lower current than would be required to turn on the main gate from an external supply.

These and other objects and advantages of the present invention will become apparent from the following description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a graph which shows the gate current, cathode current and anode to cathode voltage characteristics of standard controlled rectifier having a single gate for a high rate-of-rise-of-anode current.

FIG. 2 displays the same parameters as in FIG. 1, for a standard controlled rectifier having a plurality of gates.

FIG. 3 shows the improved electrical characteristics obtained with a controlled rectifier constructed in accordance with this invention.

FIG. 4 is a top view of a controlled rectifier semiconductor wafer constructed in accordance with the present invention.

FIG. 5 is a cross-sectional view taken across the section line 5–5 in FIG. 4.

FIG. 6 shows a top view of a second embodiment of a structure incorporating the invention.

FIG. 7 is a cross-sectional view taken across the section line 7–7 in FIG. 6.

FIG. 8 is a top view of a third embodiment of the invention.

Referring now first to FIG. 1, there are shown wave shapes of the anode current, gate current, and anode to cathode voltage during turn on conditions, for a typical controlled rectifier having a single gate.

After a short initial delay time, considerable noise (i.e., oscillations) appears in the anode to cathode voltage, and sometimes in the anode current rise characteristic. More significantly, the gate current is forced toward zero after the delay time by internally-generated back voltage. This internal voltage is due to the high internal sheet resistance of the semiconductor material (such as silicon) in the gate-cathode region. It has been found that when the gate current is forced to zero, or below zero as shown in FIG, 1, the device may fail in the mode known as *di/dt* failure due to the small turn on area, as discussed above.

To overcome this type of failure, many devices are built with more than one gate electrode. Such devices have the somewhat improved gate current characteristics shown in FIG. 2. Deep gate starvation nonetheless occurs so that such devices have limited usefulness in high *di/dt* applications. Moreover, the use of multiple gates requires the injection of a considerable gate current, usually of from 1 to 5 amperes with a very fast rise time.

In accordance with this invention, a novel controlled rectifier structure is provided which eliminates the gate-starvation conditions shown in FIGS. 1 and 2, and produces the superior characteristics shown in FIG. 3 which will be described later. One embodiment of this novel structure is shown in FIGS. 4 and 5 whose size, especially in thickness, is exaggerated for purposes of clarity.

A semiconductor wafer 10 is illustrated, which may be of monocrystalline silicon. Wafer 10 may have a diameter, for example, of three-fourths inch and a thickness of about 10 mils, it being understood that these dimensions can vary depending on the desired power rating of the device. The wafer 10 has P–N junctions 11, 12 and 13 therein, in a manner typical for any controlled rectifier structure, which separate the various P and N layers identified in FIG. 5. These layers may be formed by any of the well-known junction-forming techniques such as diffusion, alloying, epitaxial deposition, or the like.

An anode contact electrode 14 is then suitably affixed to the bottom of P-layer of wafter 10, and an upper cathode electrode 15 is secured above junction 13, in a well-known manner. Note that cathode electrode 15 overlaps planar junction 13 to form a so-called "shorted emitter" connection.

Electrode 15 has a plurality of notches 16 to 19 symmetrically disposed about its periphery, and a plurality of auxiliary gate leads 20 to 23 are disposed adjacent notches 16 to 19, respectively. Gate leads 20 to 23 can be made in any desired manner and could, for example, be formed of aluminum lead wires which are ultrasonically bonded to the upper P-type surface of wafer 10 and in surrounding relationship to cathode 15.

As previously described, in one prior art-type configuration, the various gates 20 to 23 are connected to a common source of firing current such that, when anode 14 is positive and cathode 15 is negative so that junction 12 is reverse-biased, the application of a positive potential to the gate leads with respect to cathode 15 will cause firing of the device. By using a plurality of gate leads, a plurality of initial conducting plasmas will be created from anode 14 to cathode 15, so that the device can turn on with a relatively high rate-of-rise-of-current. However, this heretofore required a relatively high gate current source, since the source must provide the gate currents required for each of gates 20 to 23.

In accordance with the present invention, the standard wafer configuration, which has been described to this point, is changed by the addition of an auxiliary cathode region defined by the N-type region above an additional P–N junction 24 and by the addition of an adjacent main gate lead 25 which cooperates therewith. An auxiliary conductive cathode electrode 26 is then connected atop the N-type region above junction 24, and electrode 26 is then connected to each of the auxiliary gates 20 to 23 which surround the main cathode 15 by suitable leads. Gate lead 25 may again be of an aluminum wire which is ultrasonically bonded to the upper P-type region of wafer 10 adjacent junction 24. In order to insure proper current-sharing of the various gates 20 to 23, the leads to the gates 20 to 23 may be provided with parallel connected resistors 27 to 30, respectively. If gate sensitivity were properly balanced, the balancing resistors 27 to 30 could be eliminated.

The device shown in FIGS. 4 and 5 operates in the following manner. Assuming that anode 14 is positive with respect to cathode 15, the N-type region above junction 24 will inject electrons into the lower P-type region, thereby causing an initial conduction plasma on the left-hand side of the device in FIG. 5 from cathode 26 to auxiliary cathode electrode 15. This initial firing, obtained by a relatively low current from cathode 26 (which is internally generated by the initial anode current causing back e.m.f. due to silicon sheet resistance), is then directed through the various balancing resistors to the individual gates 20 to 23, thereby firing the main portion of the controlled rectifier with a high rate-of-rise-of-current.

The electrical characteristics of the device of FIGS. 4 and 5 are shown in FIG. 3 where it is seen that, at the end of the delay period, and as the anode to cathode voltage begins to decrease, there is a continuing rise in gate current, rather than a decrease as in FIGS. 1 and 2. This rise in gate current is a function of the accompanying rise in anode current which in turn generates the voltage which excites the auxiliary cathode. This enhances the *di/dt* characteristics of the main cathode and reduces the danger of *di/dt* failure of the device. Moreover, the magnitude and rise time of current into the main gate lead 25 no longer determine the *di/dt* capability of the device.

It will be apparent to those skilled in the art that the wafer of FIGS. 4 and 5 can be contained within any suitable type of housing. Similarly, it will be understood that the specific conductivity-type sequences shown in FIGS. 4 and 5 could be reversed.

FIGS. 6 and 7 show a second embodiment of the invention, wherein the individual gates 20 and 23 of FIGS. 4 and 5 are replaced by a single electrode plate which extends over the edge of the additional junction 24 in FIGS. 4 and 5.

Referring to FIGS. 6 and 7, a silicon wafer 40 contains the usual junctions 41, 42 and 43, where, however junction 43 has the generally semicircular shape shown in FIG. 6. An auxiliary junction 44 having the shape shown in FIG. 6 replaces the junction 24 of FIGS. 4 and 5. An anode electrode 45 is affixed to the bottom of wafer 40 and semicircular aluminum contact 46 is connected to the top of wafer 40, overlapping the right-hand portion of junction 43 which terminates on the surface of wafer 40. An aluminum bar 47 is then applied across the junction 44 to serve as the auxiliary cathode contact and as a continuous auxiliary gate electrode for the main cathode region underlying cathode contact 46. A main gate 48, which is similar to gate 25 of FIGS. 4 and 5 is then placed adjacent junction 44. A suitable spacing of the adjacent sides of contacts 46 and 47 and the left edge of junction 43 is such that dimensions A, B, and C of FIG. 6 are each about 0.015 inch for a wafer having the size of the wafer described in connection with FIGS. 4 and 5.

A device of the type shown in FIGS. 6 and 7 was tested in a standard *di/dt* switching test with a case temperature of about 65° C., an anode to cathode voltage of about 700 volts and at frequencies which varied from 400 to 5,000 cycles per second. The device was also tested at a repetition rate of 75 Hz. under higher *di/dt* conditions. It withstood rates of rise of current up to 1400 amperes per microsecond.

FIG. 8 shows a modification of the arrangement of FIGS. 6 and 7 where components similar to those of FIGS. 6 and 7 have identical identifying numerals. In FIG. 8, the main cathode 60 has a greater area than cathode 46 of FIG. 6 by use of projecting fingers 61, 62 and 63 for cathode electrode 60. Electrode 64, which replaces electrode 47 of FIG. 6 then has extending fingers 65 and 66 which are interleaved with fingers 61, 62 and 63. Note that junction 67 which replaces junction 44 of FIG. 6 has a shape which follows the periphery of the right-hand side of electrode 64. As shown in FIG. 8, the interleaving arrangement permits the use of more cathode area for a given size of silicon wafer than the design of FIGS. 6 and 7. Thus the device can have a higher current rating.

Although this invention has been described with respect to particular embodiments, it should be understood that many variations and modifications will now be obvious to those skilled in the art. Therefore, the scope of this invention is limited not by the specific disclosure herein, but only by the appended claims.

We claim:

1. A controllably conductive semiconductor device having a high rate-of-rise-of-current capability and which can be fired with a relatively low gate current, comprising: a wafer of monocrystalline semiconductor material having first and second parallel surfaces; first, second and third spaced P–N junctions sequentially disposed therein; at least a portion of said third P–N junction terminating along said first surface of said wafer and dividing said first surface into a first surface region extending atop said third P–N junction and into a second surface region; a first main electrode connected to said first surface region of said first surface; a second main electrode connected to said second surface of said wafer; a fourth P–N junction disposed beneath said second surface region of said first surface and above said second P–N junction and being laterally displaced from said third P–N junction solely at one side thereof; an auxiliary electrode connected to said second surface region atop said fourth junction; said auxiliary electrode having a surface area smaller than the surface area of said first main electrode; a main gate electrode connected to said second surface region adjacent said auxiliary electrode; and an auxiliary gate electrode connected to said auxiliary electrode and to said second surface region of said wafer and adjacent to said first main electrode; said auxiliary electrode and said auxiliary gate electrode comprising a common conductive electrode extending across said fourth P–N junction; said auxiliary electrode being disposed between said main gate electrode and said first main electrode; the confronting edges of said first main electrode and said common conductive electrode being substantially coextensive; said common conductive electrode and said first main electrode consisting of spaced segments of a common metallic disc.

2. The device of claim 1 wherein said confronting edges of said common conductive electrode and of said first main electrode have respective extending fingers which are interleaved.

3. The device of claim 1 wherein said first main electrode extends from said first surface region and across said third junction and to a portion of said second surface region.