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(71) Applicant: INTEL IP CORPORATION [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).

(72) Inventors: YOUSEF, Amr; Forstenrieder Allee 259, 81476 Muenchen (DE). KHODIER, Moustafa; Gruenauer Allee 14, 82008 Unterhaching (DE). NICKISCH, Dirk; Kirchweg 11, 85667 Oberpfaffenhofen (DE). IT-JESHORST, Ralf; Schulstr. 10, 85469 Walpertskirchen (DE).

(74) Agent: LAMBSDORFF & LANGE, PATENTAN-WAELTE; Dingolfinger Str. 6, 81673 Muenchen (DE).

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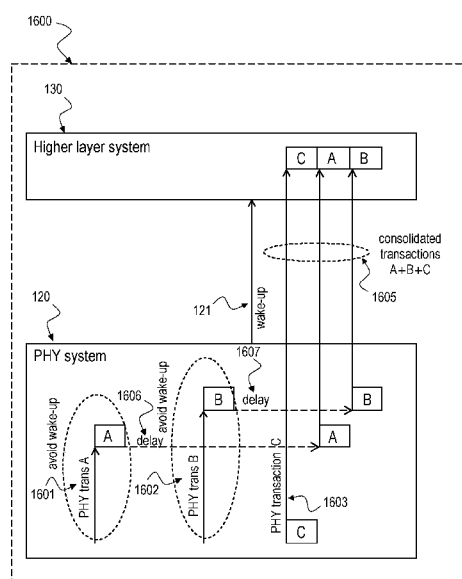


Fig. 16

(57) Abstract: This disclosure relates to a mobile device, comprising: a physical layer (PHY) system configured to process physical layer related operations; a higher layer system configured to process operations related to layers above the physical layer; and a communication channel established between the PHY system and the higher layer system for reporting a plurality of transactions to the higher layer system, wherein the PHY system is configured to consolidate the plurality of transactions based on a single wake-up message directed to the higher layer system.

MOBILE DEVICE USING CONSOLIDATED TRANSACTIONS**FIELD**

[0001] The disclosure relates to a mobile device and a method for operating a mobile device using consolidated transactions between a physical layer (PHY) system processing physical layer related operations and a higher layer system such as a cellular protocol stack (CPS) system processing operations related to layers above the physical layer. The disclosure particularly relates to low throughput use cases CPS activities consolidation through PHY.

BACKGROUND

[0002] In Wireless Networks connected mode low throughput use cases (like VoLTE, web-browsing, social media applications like Facebook, chatting applications), CPS "Cellular/wireless Protocol Stack" CP "Control Plane" and DP "Data Plane" activities are occurring with low frequency. Figure 1 shows a mobile device connected to a wireless network to perform a variety of different activities 101, 102, 103, 104. Table 1 shows statistics for frequency of activities triggered for VoLTE calls in field testing in different locations.

Activity Name	Activity Frequency per millisecond
DL Data Handling	17.48
UL Grant Handling	17.94
Serving cell measurement report	34.70
EUTRA measurements report	50.80

Table 1: LTE VoLTE Use Cases PHY-CPS Transactions Frequency

[0003] To start these activities, transactions from PHY system 120 to CPS system 130 is needed. Based on the CPS System 120 state, a wake up 121 may be needed to initiate transaction and provide corresponding information/message. The CPS System 130 can include CPS cores, external memory, HW accelerators and other HW modules serving cores, etc.

[0004] Due to low frequency of PHY-CPS transactions in mobile networks low throughput use cases, the probability of having these activities aligned (i.e. being triggered by PHY in same subframe) is low, which results in many cases to dedicated wake ups 121 and active time for CPS system 130 per activity. Since in low throughput use cases expectations are to have low rate of DP & CP activities and these are most common use cases for mobile terminals users, these use cases are always having aggressive low power consumption targets. However, having dedicated CPS system wake ups and active time per activity will have considerable impact on power consumption. Hence, there is a need to provide a concept for reducing power in mobile devices, in particular in low throughput use cases as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The accompanying drawings are included to provide a further understanding of embodiments and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments and together with the description serve to explain principles of embodiments. Other embodiments and many of the intended advantages of embodiments will be readily appreciated as they become better understood by reference to the following detailed description.

[0006] Fig. 1 is a schematic diagram illustrating a mobile device 110 connected to a wireless network to perform a variety of different activities 101, 102, 103, 104.

[0007] Fig. 2 is a block diagram illustrating the high level architecture 200 for CPS 130 and PHY 120 system.

[0008] Fig. 3 is a message sequence chart 300 for transaction sequence between PHY 120 and CPS 130 systems.

[0009] Fig. 4 is a schematic diagram of an example message sequence 400 for not aligned PHY-CPS CP/DP transactions.

[0010] Fig. 5 is a schematic diagram 500 illustrating consolidation of PHY latency non-critical to latency critical transactions according to the disclosure.

[0011] Fig. 6 is a schematic diagram 600 illustrating parallel processing for consolidated PHY transactions to latency critical transactions according to the disclosure.

[0012] Fig. 7 is a message sequence diagram 700 illustrating CPS system enabling/disabling delay for CP transaction according to the disclosure.

[0013] Fig. 8 is a schematic diagram 800 illustrating a sequence of actions for PHY-CPS transactions delaying according to the disclosure.

[0014] Fig. 9 is a schematic diagram illustrating a PHY algorithm (or method) 900 for delaying DL data transactions to CPS according to the disclosure.

[0015] Fig. 10 is a schematic diagram 1000 illustrating an Example for aligning DL data transaction with UL transaction assuming single core CPS system according to the disclosure.

[0016] Fig. 11 is a schematic diagram 1100 illustrating an exemplary DL data transaction having delay timer expiry without occurrence of latency critical transaction according to the disclosure.

[0017] Fig. 12 is a histogram 1200 illustrating an analysis of PHY-CPS DL data transactions.

[0018] Fig. 13 is a schematic diagram 1300 illustrating an exemplary Consolidation of CP transaction to DP transaction according to the disclosure.

[0019] Fig. 14 is a schematic diagram 1400 illustrating an exemplary latency non-critical CP transaction delay time elapse according to the disclosure.

[0020] Fig. 15 is a histogram 1500 illustrating an analysis of PHY-CPS CP transactions.

[0021] Fig. 16 is a schematic diagram illustrating a mobile device 1600 according to the disclosure consolidating transactions between PHY system and higher layer system based on a single wake-up message.

[0022] Fig. 17 is a schematic diagram illustrating a method 1700 for operating a mobile device according to the disclosure.

DETAILED DESCRIPTION

[0023] In the following detailed description, reference is made to the accompanying drawings, which form a part thereof, and in which is shown by way of illustration specific aspects in which the invention may be practiced. It is understood that other aspects may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

[0024] The following terms, abbreviations and notations will be used herein:

UE:	User Equipment, cellular handset
LTE:	Long Term Evolution
VoLTE:	Voice over LTE
PHY:	Physical Layer
CPS:	Cellular Protocol Stack
CP:	Control Plane
DP:	Data Plane
UL:	Uplink
DL:	Downlink
FW:	Firmware
HW:	Hardware
SW:	Software

[0025] It is understood that comments made in connection with a described method may also hold true for a corresponding device configured to perform the method and vice versa. For example, if a specific method step is described, a corresponding device may include a unit to perform the

described method step, even if such a unit is not explicitly described or illustrated in the figures. Further, it is understood that the features of the various exemplary aspects described herein may be combined with each other, unless specifically noted otherwise.

[0026] The techniques described herein may be implemented in wireless communication networks, in particular communication networks based on high speed communication standards from the 802.11 family according to the WiFi alliance, e.g. 802.11ad and successor standards. The methods are also applicable for mobile communication standards such as LTE, in particular LTE-A and/or OFDM and successor standards such as 5G. The methods and devices described below may be implemented in electronic devices such as cellular handsets, mobile or wireless devices (or mobile stations or User Equipments (UE)). The described devices may include integrated circuits and/or passives and may be manufactured according to various technologies. For example, the circuits may be designed as logic integrated circuits, analog integrated circuits, mixed signal integrated circuits, optical circuits, memory circuits and/or integrated passives.

[0027] In the following, embodiments are described with reference to the drawings, wherein like reference numerals are generally utilized to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of one or more aspects of embodiments. However, it may be evident to a person skilled in the art that one or more aspects of the embodiments may be practiced with a lesser degree of these specific details. The following description is therefore not to be taken in a limiting sense.

[0028] The various aspects summarized may be embodied in various forms. The following description shows by way of illustration various combinations and configurations in which the aspects may be practiced. It is understood that the described aspects and/or embodiments are merely examples, and that other aspects and/or embodiments may be utilized and structural and functional modifications may be made without departing from the scope of the present disclosure.

[0029] Fig. 2 is a block diagram illustrating the high level architecture 200 for CPS 130 and PHY 120 system.

[0030] The PHY system 120 can process layer 1 operations, i.e. on the physical layer while the CPS system processes higher layer operations, for example operations related to layers 2 (data link layer), 3 (network layer) and above of the OSI (open system interconnection) model. The cellular protocol stack (CPS) system is an implementation of a cellular networking *protocol suite*. The terms are often used interchangeably. Strictly speaking, the suite is the definition of the protocols of the cellular network, and the stack is the software implementation of them.

[0031] The CPS system 130 includes a CPS core 231, an external memory 232, a hardware (HW) accelerator 233 and other HW modules 234 serving cores. The communication channel 222 between PHY system 120, also referred to as PHY Firmware system hereinafter, is used to transport transactions between PHY system 120 and CPS system 130. The communication channel 222 may be a bidirectional channel. A wake-up message 121 can wake-up the CPS system for processing the messages transported from PHY system 120 to CPS system. 130.

[0032] Fig. 3 is a message sequence chart 300 for transaction sequence between PHY 120 and CPS 130 systems. For starting activities between PHY system 120 and CPS system 130, as described above with respect to Fig. 1, transaction from PHY system 120 to CPS system 130 needs to be initiated 301. Based on CPS System state 310, 320, wake up 121 may be needed to initiate transaction 304 and provide corresponding information/message.

[0033] When a FW transaction needs to be initiated 301 to CPS system that is in inactive state 310, a wake-up 121 is sent from PHY system 120 to CPS system 130 to bring CPS system 130 in active state 320. The wake-up 121 may be acknowledged 303 by CPS system 130 before CPS system 130 changes to active state 320. When processing is complete 305, PHY system 130 may change again to inactive state 310.

[0034] Fig. 4 is a schematic diagram of an example message sequence 400 for not aligned PHY-CPS CP/DP transactions.

[0035] A CP transaction 410 is initiated by the FW, i.e. the PHY system 120 at time N ms. This CP transaction 410 is transferred to CPS system 130 resulting in a wake-up of CPS system 130 (change from state inactive 310 to state active 230) and CPS CP activity to process the CP transaction 410. After processing of the CP transaction 410 the CPS system 130 returns to state inactive 310. The same procedure is repeated for a DP_DL data transaction 420 at time N+2 ms and for a DP_UL Grant transaction 430 at time N+6 ms.

[0036] Since in low throughput use cases as depicted in Fig. 4 expectations are to have low rate of DP & CP

activities and these are most common use cases for mobile terminals users, these use cases are always having aggressive low power consumption targets. However, having dedicated CPS system wake ups and active time per activity will have considerable impact on power consumption.

[0037] To reduce power consumption, a framework as described in the following is applied for wireless systems connected mode operations (i.e. connection is established) through which PHY transactions to CPS across multiple frames can be consolidated in single CPS system activation/wake up.

[0038] For such a framework, the following definitions may apply: The PHY System includes all modules involved in wireless systems physical layer related operations. The CPS System includes Cellular/Wireless protocol stack system performing L2 and above operations for wireless system. PHY-CPS Transactions include all transactions initiated from PHY to CPS system. PHY-CPS Transaction Types are related to the following: In wireless systems, transactions from PHY to CPS in connected mode can be classified into the two categories: Latency Critical Transactions and Non-latency Critical Transactions. Latency Critical Transactions are type of PHY-CPS transactions that have hard processing latency requirements on CPS, one example for such transactions is processing of UL grants received from networks where processing by CPS in most of wireless systems needs to be done as soon as possible to meet timing requirements for sending data on air by physical layer. Non-latency Critical Transactions are type of PHY-CPS transactions that have no hard latency requirements on CPS and slight delay in processing of such transactions by CPS shouldn't

impact wireless system behavior, one example for such transactions is measurement reports. The PHY-CPS Transaction Delay is the maximum allowed delay to start CPS processing for PHY-CPS transaction.

[0039] The target of such a framework is to delay reporting of non-latency critical PHY-CPS transactions by PHY until next latency critical PHY-CPS transaction to have single activation/wake up for CPS system handling both non-latency and latency critical transaction from PHY as shown in Figure 5.

[0040] Fig. 5 is a schematic diagram 500 illustrating consolidation of PHY latency non-critical to latency critical transactions according to the disclosure.

[0041] A non-latency critical PHY transaction A, 510 is initiated by the PHY system 120 at time N ms. This non-latency critical transaction A, 510 is delayed until time N+m ms. A wake-up message is avoided 513. The same procedure is repeated for a non-latency critical PHY transaction B, 520 which is also delayed unit time N+m ms and for which transmitting a wake-up is avoided 523. At time N+m a latency critical PHY transaction C, 530 is initiated by the PHY system 120. For this transaction C, 530 a wake-up message is transmitted to CPS system 130 resulting in a wake-up of CPS system 130 (change from state inactive 310 to state active 230) and CPS CP activity to process the CP transactions. The two non-latency critical transactions A, 510 and B, 520 are consolidated with the latency critical transaction C, 530 and transmitted as a consolidated transaction 530, 510, 520 to the CPS system 130. After processing these consolidated transaction 530, 510, 520 the CPS system 130 returns to state

inactive 310. Thus, only a single activation or wake-up is required for handling all PHY-CPS transactions 501.

[0042] In multi core or SW/HW partitioned CPS systems, this framework reduces CPS system overall active time by increasing CPS system resources utilization through parallelizing PHY-CPS transactions activities processing, e.g. as described in the example below with respect to Fig. 6.

[0043] Fig. 6 is a schematic diagram 600 illustrating parallel processing for consolidated PHY transactions to latency critical transactions according to the disclosure.

[0044] In the Example depicted in Fig. 6, it is assumed that Transaction C, 530 on CPS 130 needs software (SW) operations on Core0 (processing core no. 0) for 100 microseconds and hardware (HW) operations (e.g. data ciphering on HW accelerator) for 100 microseconds. Transaction B, 520 may be executed on Core 0 for 100 microseconds. Transaction A, 510 may be executed on Core 1 (processing core no. 1) for 100 microseconds.

[0045] Thus, the CPS overall active time without PHY-CPS transactions consolidation would be 400 microseconds. By applying the disclosed PHY-CPS transactions consolidation framework, the overall CPS active time can be reduced to 200 microseconds which is a 50% reduction in active time and accordingly CPS system power consumption.

[0046] The above described framework may further define the further items: PHY-CPS transactions can be classified into latency critical and non-critical transactions based

on timing response requirements. For each latency non-critical transaction type (e.g. serving cell measurement report), an allowed max PHY-CPS Transaction Delay that may be applied by the PHY can be defined. The PHY-CPS Transaction Delay value can be changed in run-time based on different factors (e.g. serving cell power value) either directly by PHY or through CPS. A value of zero may be the default value which means that delay shall be disabled. An example for an algorithm that can be applied to define a maximum allowed delay value for a specific transaction type is described below with respect to Fig. 7.

[0047] Fig. 7 is a message sequence diagram 700 illustrating CPS system enabling/disabling delay for CP transaction according to the disclosure. This figure provides an example for a use case where CPS is enabling and disabling the delay on PHY-CPS transaction.

[0048] If at CPS domain 130 the condition to enable delay for certain transaction type is satisfied 701, an "enable_delay" message 702 is transferred from CPS domain 130 to PHY FW system 120 indicating the PHY system 120 to enable delay with a specific transaction type and a specific delay value as included in the "enable_delay" message 702. Responsive to this message 703 the PHY system 120 activates delay with the specific delay value on the specific transaction type 703.

[0049] If at CPS domain 130 the condition to disable delay for certain transaction type is satisfied 704, a "disable_delay" message 705 is transferred from CPS domain 130 to PHY FW system 120 indicating the PHY system 120 to disable delay with the specific transaction type as included

in the "disable_delay" message 705. Responsive to this message 705 the PHY system 120 deactivates delay on the specific transaction type 706.

[0050] Fig. 8 is a schematic diagram 800 illustrating a sequence of actions for PHY-CPS transactions delaying according to the disclosure.

[0051] Once PHY-CPS transaction required to be initiated and for which delay is enabled and delay conditions are satisfied, PHY shall cache/save transaction internally until any of stop delaying conditions are satisfied. Examples for stop delay conditions are the following: Any of delayed CPS-PHY transactions delay time elapse; Latency critical transaction required to be initiated to CPS system; PHY system needs to be powered down. Once any of stop delay conditions is satisfied, PHY shall trigger wake up for CPS system and then provide all pending PHY-CPS transactions to CPS system. Fig. 8 provides an example how such a framework can be realized.

[0052] The PHY system 120 may include a PHY internal transactions queue 820 to queue the various delayed transactions 821, 822, 823. When a flush cache queue event 811 is triggered, for example by the following events 810: time critical transaction needs to be provided to CPS system; or cached transaction delay elapsed, a wake up signal 824 is transferred to CPS system 130 and the cached transactions 821, 822, 823 are moved 824 to CPS system, e.g. to an external memory PHY_CPS transactions queue 831 included in the CPS system 130. After moving is complete, a move complete 826 message is transferred from CPS system 130 to PHY system

120 and the PHY system 120 may trigger an interrupt 827 to the CPS system 130.

[0053] Applying this framework will decrease the number of dedicated CPS system wake ups for PHY-CPS transactions and reduce the overall active time needed by CPS system for handling these transactions which accordingly will result in considerable reduction on power consumption by CPS system.

[0054] The following section addresses LTE low throughput use cases as an example on how this framework can be realized and gains that can be achieved. The following section addresses in details two types of consolidation to be applied: 1) Consolidating DL Data latency non-critical transactions; and 2) Consolidating periodic Control Plane latency non-critical transactions. The algorithms described in this section for defining maximum allowed delay values on transactions are generic and can be applied on any other wireless protocols (e.g. 3G) with consideration of adjustment on conditions.

[0055] The first type of 1) Consolidating DL Data latency non-critical transactions is described in the following.

[0056] PHY-CPS LTE UL grant transactions (i.e. LTE UL grant handling) may have high latency requirements which can't be delayed but LTE DL data transactions may have more relaxed latency requirements based on radio bearers QoS "Quality of Service" configuration. As described above, the idea is to avoid having dedicated CPS wake ups for DL data transactions by applying configurable delay on these transactions to be consolidated with next latency

critical transaction (e.g. UL Grant transaction). An exemplary algorithm by which such a delay can be applied is described below.

[0057] CPS shall configure PHY with list of Logical channel IDs having latency non-critical requirements and max allowed delay value per each. CPS-PHY interface to provide such configuration can be as follows:
 cps_phy_dl_data_delay_config(list of latency non-critical logical channel IDs, list of non-critical logical channel IDs allowed delay). Note that logical channel IDs are identities for LTE radio bearers on MAC level. Maximum allowed delay value per logical channel ID shall be adjusted based on packet delay values defined for corresponding data bearer QCI "QoS class of identifier". Table 2 lists possible QCIs packet delay values for LTE EPS Bearers:

QCI	Bearer Type	Priority	Packet Delay	Packet Loss	Example
1	GBR	2	100 ms	0,01	VoIP call
2	GBR	4	150 ms	0,001	Video call
3	GBR	3	50 ms	0,001	Online gaming (real time)
4	GBR	5	300 ms	0,000001	Video streaming
5	Non-GBR	1	100 ms	0,000001	IMS signaling
6	Non-GBR	6	300 ms	0,000001	Video, TCP based services, e.g. email, chat, ftp, etc.
7	Non-GBR	7	100 ms	0,001	Voice, video,

					interactive gaming
8	Non-GBR	8	300 ms	0,000001	Video, TCP based services, e.g. email, chat, ftp, etc.
9	Non-GBR	9	300 ms	0,000001	Video, TCP based services, e.g. email, chat, ftp, etc.

Table 2: List of LTE EPS bearers configuration

[0058] Both SRBs "Signaling Radio Bearers" and DRBs "Data Radio Bearers" with packet delay less than or equal 50ms (i.e. QCI3), delay SHALL NOT be applied on corresponding DL Data Transactions/TBs which have data on these bearers to avoid impacting there low packet delay requirements.

[0059] For other radio bearers, default delay value 4ms shall be applied, as based on statistics from field testing for LTE low throughput use cases the following was identified: More than 40% of DL data transactions is always followed by UL grant transaction within 4 ms and increasing more delay doesn't help much in consolidating more DL Data transactions. 4 ms shall be acceptable delay for most of latency non-critical radio bearers. Maximum allowed delay per QCI value, shall be possible to be re-adjusted by AP "Application Processor"/Higher Layers to CPS through NVRAM configuration or Configuration Interface. This shall provide high layers flexibility to readjust delay value per QCI value based on device needs.

Once LTE DL TB "Transport Block"/PDU is received by PHY, based on logical channel IDs identified in TB MAC sub-headers, FW shall decide if delay on DL Data transaction shall be applied or not.

[0060] Fig. 9 is a schematic diagram illustrating a PHY algorithm (or method) 900 for delaying DL data transactions to CPS according to the disclosure.

[0061] The algorithm 900 includes the following blocks and functionalities: In a first block 901 PHY receives DL transport block. In a subsequent second block 902 PHY decodes DL TB MAC Sub-Header. In a subsequent third block 903 a check is performed if any of MAC Sub-Headers logical channel IDs is considered as latency critical data based on CPS configuration. If the answer is no, in a subsequent fourth block 904 DL TB transaction is cached and delay value is applied equal to minimum of CPS configured delay for logical channels received in TB and the algorithm goes to an end block 906. If the answer is yes, in a subsequent fifth block 905 DL TB transaction to CPS is triggered as soon as possible and the algorithm goes to the end block 906.

[0062] For DL Data transactions considered to be delayed, PHY shall delay these transactions until one of two scenarios occurs: Scenario#1 (depicted in Fig. 10): Latency critical transaction (e.g. UL Grant transaction) needs to be indicated to CPS. Scenario#2 (depicted in Fig. 11): Delay applied on DL Data transaction or other latency non-critical transaction expires (i.e. maximum allowed delay elapsed without occurrence of latency critical transaction)

[0063] Fig. 10 is a schematic diagram 1000 illustrating an Example for aligning DL data transaction with UL transaction assuming single core CPS system according to the disclosure.

[0064] After enabling delay configuration 1011 by CPS system 130, a DL transaction 1010 is cached 1012 until a latency critical UL transaction 1020 is ready. Both transactions 1010, 1020 are consolidated and transmitted together to CPS system 130 after waking up 1021 CPS system 130.

[0065] Fig. 11 is a schematic diagram 1100 illustrating an exemplary DL data transaction having delay timer expiry without occurrence of latency critical transaction according to the disclosure.

[0066] After enabling delay configuration 1011 by CPS system 130, a DL transaction 1110 is cached 1112 until an expiration of the delay value configured by message 1011 occurs. In response to an expiry of delay value the DL transaction 1110 is transmitted to CPS system 130 after waking up CPS system 130.

[0067] Fig. 12 is a histogram 1200 illustrating an analysis of PHY-CPS DL data transactions. The left two bars 1201 and 1202 illustrate results without applying the disclosed framework, where bar 1201 indicates consolidated transactions in % and bar 1202 indicates un-consolidated transactions in %. The right two bars 1203 and 1204 illustrate results with applying the disclosed framework, where bar 1203 indicates consolidated transactions in % and bar 1204 indicates un-consolidated transactions in %.

[0068] Based on a large number of LTE low throughput traces collected from field testing in different locations, the following results can be concluded. DL data transactions represents up to 38% of overall transactions to CPS. UL Grant transaction is most frequent latency critical transaction from PHY to CPS in such use cases: Only 16% of DL data transactions were aligned with UL Grant transactions (i.e. happening in same 1ms slot), all other DL data transactions (84%) required dedicated CPS system wake ups. 38% of these DL data transactions followed by UL grant transaction within time difference ranges between 1-4 ms.

[0069] Accordingly if 4 ms delay is applied, 38% of DL data transactions won't need a dedicated wake up for CPS system and accordingly expected CPS wake ups reduction can be up to 14%. I.e., 38% of CPS system wake ups of 38% DL data transactions can be avoided.

[0070] The second type of 2) Consolidating Control Plane non-critical transactions is described in the following.

[0071] As described above, PHY-CPS CP "Control Plane" transactions in low throughput use cases can have considerable frequency compared to DP "Data Plane" transactions which accordingly can have considerable contribution in CPS power consumption by having dedicated wake ups and active time for CPS system resources. As described above, the idea is to avoid having dedicated CPS wake ups and active time for CP latency non-critical transactions by applying configurable delay on these transactions to be consolidated with next latency critical PHY-CPS transaction (e.g. UL Grant transaction).

[0072] The following CP Transactions are Considered for Applying Delay: 1) EUTRA serving cell measurement report: PHY-CPS transaction through which PHY indicates CPS regarding serving cell(s) power values. 2) EUTRA intra and inter neighbor cells measurement report: PHY-CPS transaction through which PHY indicates CPS regarding EUTRA cells measurements (intra and inter measurements). 3) Measurements gaps: PHY-CPS transaction through which gaps (either MEAS Gap or DRX Gap) indicated by PHY to perform inter frequency or IRAT measurements by other PHYs.

[0073] An exemplary algorithm by which such a delay can be applied is described in the following.

[0074] Measurements Gaps Transactions: Maximum allowed delay for these transactions shall be applied directly by PHY based on gap start time. Once measurement gap transaction is ready in PHY to be reported to CPS, PHY shall adjust max possible delay value can be applied on transaction based on the following inputs: 1) Time remaining for gaps start; 2) CPS time needed to process transaction. This time processing value shall be configured by CPS; 3) Type of active measurements (e.g inter Frequency, IRAT) to consider other RAT PHY gap processing time needed. This time processing value shall be configured by CPS.

[0075] EUTRA serving cell, intra and inter neighbor cells measurement reports transactions: Decision of delaying these transactions will be based on serving cell power. CPS shall configure PHY with serving cell power thresholds

and corresponding allowed max delay value. Once any of these transactions is ready to be reported to CPS, PHY shall check serving cell power value and based on which corresponding max allowed delay value shall be applied. Zero delay value means no delay is allowed to be applied on this transaction.

[0076] One implementation for delay configuration setting by CPS is as follows: Good Cell Quality Threshold: as long as serving cell power is equal to or greater than this threshold, 12 ms delay value shall be applied. As based on statistics from field testing for LTE low throughput use cases the following was identified: 1) Around 52% of these CP transactions are always followed by latency critical transaction (e.g. UL Grant Transaction) within 12 ms and increasing more delay doesn't consolidate much transactions. 2) Within good cell quality conditions, average periodicity of reporting serving and neighbor cell measurements is around 120 ms so introducing 12 ms delay (~10% of periodicity) shouldn't causing any impact on system behavior. Below this threshold (i.e. serving cell quality is less than "Good Cell Quality Threshold"), no delay shall be applied on these CP transactions.

[0077] Once any of measurement reports transactions (serving or EUTRA measurements) shall be reported by PHY, PHY shall check serving cell quality and compare it to delay configured threshold from CPS. If serving cell power is better than or equal delay configured threshold then delay on transaction shall be applied.

[0078] Transactions Reporting Conditions: For CP latency non-critical transactions considered to be delayed, PHY

shall delay these transactions until one of two scenarios occurs:

[0079] Scenario#1 (depicted in Fig. 13): Latency critical transaction (e.g. UL Grant transaction) needs to be indicated to CPS: Step#1: CPS enable CP_Transaction(Serving Cell Report) delay; Step#2: PHY in frame X requires to report serving cell measurement report, but since delay is enabled, PHY shall apply delay on transaction; Step#3: In frame X+2, DP transaction required to be triggered to CPS and accordingly FW wake up CPS system and provide DP transaction; Step#4: Since CPS system wake up triggered, FW shall provide any pending delayed transactions (i.e. CP Serving Cell Report transaction in this example) to CPS.

[0080] Figure 13 illustrating Scenario#1 shows CP transaction 1310 and accordingly corresponding CPS activity was delayed till next DP transaction 1320 to CPS 130 and was executed in parallel to DP HW activity which is accordingly: Avoid dedicated wake up for CP transaction; Decreasing CPS overall active time by increasing CPS System resources utilization by performing CP transaction in parallel to DP HW activity as highlighted in Figure 13 by dotted oval 1330.

[0081] Scenario#2 (depicted in Fig. 14): Delay applied on CP transaction 1410 or other latency non-critical transaction elapses (i.e. max allowed delay elapsed without occurrence of latency critical transaction): Same as previous example (Scenario#1) shown in Fig. 13 without DP transaction triggered until 12 frames have elapsed and

accordingly FW triggers CPS wake up to provide delayed CP transaction.

[0082] Fig. 15 is a histogram 1500 illustrating an analysis of PHY-CPS CP transactions. The left two bars 1501 and 1502 illustrate results without applying the disclosed framework, where bar 1501 indicates consolidated transactions in % and bar 1502 indicates un-consolidated transactions in %. The right two bars 1503 and 1504 illustrate results with applying the disclosed framework, where bar 1503 indicates consolidated transactions in % and bar 1504 indicates un-consolidated transactions in %.

[0083] Based on large number of LTE low throughput traces collected from field testing in different locations, the following results can be concluded. CP transactions represents up to 23% of overall transactions. Only 14% of these transactions were aligned with DP transactions. All other CP transactions (86%) required dedicated CPS system wake ups. 52% of these CP transactions followed by DP transactions within time 12 ms.

[0084] Accordingly in good cell conditions, if 12ms delay applied, 52% of CP transactions won't need dedicated wake up for CPS system and accordingly expected CPS system wake ups reduction can be up to 12%. I.e. 52% of CPS system wake ups of 23% CP transactions can be avoided.

[0085] Applying PHY-CPS transactions consolidation the disclosed framework on PHY-CPS periodic latency non-critical transactions, especially in low throughput use cases, which are one of most common use cases for mobile terminals, has considerable reduction in CPS system power

consumption by either: 1) Reducing CPS System Wake Ups up to 26% (12% from CP transactions consolidation and 14% from DP DL data transactions consolidation) as described in details in the analysis above or 2) Reducing CPS System Active Time with also considerable percentage by considering parallel possible processing for consolidated transactions with latency critical transaction as highlighted in previous sections and shown in Fig. 6.

[0086] Fig. 16 is a schematic diagram illustrating a mobile device 1600 according to the disclosure consolidating transactions between PHY system 120 and higher layer system 130 based on a single wake-up message 121.

[0087] The mobile device 1600 includes a physical layer (PHY) system 120 for processing physical layer related operations; a higher layer system 130 for processing operations related to layers above the physical layer, e.g. operations of data link layer (layer 2), network layer (layer 3), transport layer (layer 4), session layer (layer 5); presentation layer (layer 6), application layer (layer 7) according to the OSI model; and a communication channel established between the PHY system 120 and the higher layer system 130 for reporting a plurality of transactions 1601, 1602, 1603 to the higher layer system 130. The PHY system 120 is configured to consolidate 1605 the plurality of transactions 1601, 1602, 1603 based on a single wake-up message 121 directed to the higher layer system 130.

[0088] This higher layer system 130 may include a cellular protocol stack (CPS) system as described above with respect to Figures 1 to 15. The wake-up message 121 is configured to

wake-up the higher layer system 130 for processing the consolidated plurality of transactions 1605.

[0089] For example, the plurality of transactions 1601, 1602, 1603 may include at least one first type of latency critical transaction (in Figure 16 the PHY transaction C 1603) and at least one second type of non-latency critical transaction (in Figure 16 the PHY transaction A 1601 and the PHY transaction B 1602), e.g. as described above with respect to Figures 5 to 15. A timing response requirement for the latency-critical transaction 1603 may be for example more strict than a timing response requirement for the non-latency critical transaction 1601, 1602. The PHY system 120 may delay 1606, 1607 reporting a non-latency critical transaction 1601, 1602 until reporting a latency critical transaction 1603.

[0090] The higher layer system 130 may control the PHY system 120 enabling or disabling consolidation of the plurality of transactions 1601, 1602, 1603), e.g. as described above with respect to Figures 5 to 15.

[0091] The higher layer system 130 may enable the PHY system 120 consolidating transactions 1605 of a specific transaction type. The higher layer system 130 may be configured to indicate a delay value applicable for the specific transaction type to the PHY system 120, e.g. as described above with respect to Fig. 7. The PHY system 120 may be configured to activate consolidation 1605 of transactions 1601, 1602, 1603 of the specific transaction type based on the delay value indicated by the higher layer system 130, e.g. as described above with respect to Fig. 7. The delay value may be changeable in run-time either by the PHY system 120 or by the higher layer system 130.

[0092] The PHY system 120 may cache the transactions of the specific transaction type in a cache (memory) until a delaying condition is satisfied. Such delaying condition may be for example: an elapse of a delay time specified by the delay value for the specific transaction type, a latency critical transaction required to be reported to the higher layer system, and/or a power down requirement for the PHY system, e.g. as described above with respect to Fig. 9. The PHY system 120 may report the cached transactions of the specific transaction type to the higher layer system 130 when the delaying condition is fulfilled.

[0093] The concept presented in this disclosure can be applied to all Wireless Protocols (e.g., 2G/3G/4G/CDMA/Wifi) low throughput use cases, like VoLTE, web-browsing, voice calls, chatting apps, etc.

[0094] Power consumption is one of key KPIs (Key Performance Indicators) for UE having special user attention. Applying the framework as described in this disclosure will improve CPS power consumption values especially in low throughput use cases which are most common use cases for UE (like VoLTE, web-browsing, chatting applications like WhatsApp, social media applications like Facebook). Improving power consumption in these use cases will give advantage versus other mobile devices not applying this framework for power consumption.

[0095] Fig. 17 is a schematic diagram illustrating a method 1700 for operating a mobile device, e.g. a mobile device 1600 as depicted in Fig. 16, according to the disclosure.

The method 1700 may be processed by a mobile device 1600 as described above with respect to Fig. 16.

[0096] The method 1700 includes initiating 1701 a physical layer (PHY) system for processing physical layer related operations. The method 1700 further includes initiating 1702 a higher layer system for processing operations related to layers above the physical layer. The method 1700 further includes establishing 1703 a communication channel between the PHY system and the higher layer system for reporting a plurality of transactions from the PHY system to the higher layer system. The method 1700 further includes consolidating 1704 the plurality of transactions based on a single wake-up message directed to the higher layer system, e.g. as described above with respect to Figures 5 to 16.

[0097] The higher layer system may include a cellular protocol stack (CPS) system, e.g. as described above with respect to Figures 1 to 18. The wake-up message may be configured to wake-up the higher layer system for processing the consolidated plurality of transactions, e.g. as described above with respect to Figures 5 to 16.

[0098] The plurality of transactions may include at least one first type of latency critical transaction and at least one second type of non-latency critical transaction. A timing response requirement for the latency-critical transaction may be more strict than a timing response requirement for the non-latency critical transaction.

[0099] The method 1700 may include delaying reporting a non-latency critical transaction until reporting a latency critical transaction, e.g. as described above with respect to

Figures 5 to 16. The method 1700 may include controlling an enabling or disabling of the consolidation of the plurality of transactions, e.g. as described above with respect to Figures 5 to 16.

[0100] The method 1700 may include enabling the consolidation of transactions of a specific transaction type, e.g. as described above with respect to Figures 5 to 16. The method 1700 may include indicating a delay value applicable for the specific transaction type to the PHY system. The method 1700 may include activating consolidation of transactions of the specific transaction type based on the indicated delay value. The delay value can be changed in run-time.

[0101] The method 1700 may include caching the transactions of the specific transaction type until a delaying condition is satisfied. The delaying condition may include an elapse of a delay time specified by the delay value for the specific transaction type, a latency critical transaction required to be reported to the higher layer system, and/or a power down requirement for the PHY system, e.g. as described above with respect to Figures 5 to 16. The method 1700 may further include reporting the cached transactions of the specific transaction type to the higher layer system when the delaying condition is fulfilled.

[0102] The devices and systems described in this disclosure may be implemented as Digital Signal Processors (DSP), micro-controllers or any other side-processor or hardware circuit on a chip or an application specific integrated circuit (ASIC).

[0103] Embodiments described in this disclosure can be implemented in digital electronic circuitry, or in computer hardware, firmware, software, or in combinations thereof, e.g. in available hardware of mobile devices or in new hardware dedicated for processing the methods described herein.

[0104] The present disclosure also supports a computer program product including computer executable code or computer executable instructions that, when executed, causes at least one computer to execute the performing and computing blocks described herein, in particular the method 1700 described above with respect to Fig. 17 and the computing blocks described above with respect to Figures 5 and 16. Such a computer program product may include a non-transient readable storage medium storing program code thereon for use by a processor, the program code comprising instructions for performing the methods or the computing blocks as described above.

EXAMPLES

[0105] The following examples pertain to further embodiments. Example 1 is a mobile device, comprising: a physical layer (PHY) system configured to process physical layer related operations; a higher layer system configured to process operations related to layers above the physical layer; and a communication channel established between the PHY system and the higher layer system for reporting a plurality of transactions to the higher layer system, wherein the PHY system is configured to consolidate the plurality of transactions based on a single wake-up message directed to the higher layer system.

[0106] In Example 2, the subject matter of Example 1 can optionally include that the higher layer system comprises a cellular protocol stack (CPS) system.

[0107] In Example 3, the subject matter of any one of Examples 1-2 can optionally include that the wake-up message is configured to wake-up the higher layer system for processing the consolidated plurality of transactions.

[0108] In Example 4, the subject matter of any one of Examples 1-3 can optionally include that the plurality of transactions comprise at least one first type of latency critical transaction and at least one second type of non-latency critical transaction.

[0109] In Example 5, the subject matter of Example 4 can optionally include that a timing response requirement for the latency-critical transaction is more strict than a timing response requirement for the non-latency critical transaction.

[0110] In Example 6, the subject matter of any one of Examples 4-5 can optionally include that the PHY system is configured to delay reporting a non-latency critical transaction until reporting a latency critical transaction.

[0111] In Example 7, the subject matter of any one of Examples 1-6 can optionally include that the higher layer system is configured to control the PHY system enabling or disabling consolidation of the plurality of transactions.

[0112] In Example 8, the subject matter of any one of Examples 1-7 can optionally include that the higher layer

system is configured to enable the PHY system consolidating transactions of a specific transaction type.

[0113] In Example 9, the subject matter of Example 8 can optionally include that the higher layer system is configured to indicate a delay value applicable for the specific transaction type to the PHY system.

[0114] In Example 10, the subject matter of Example 9 can optionally include that the PHY system is configured to activate consolidation of transactions of the specific transaction type based on the delay value indicated by the higher layer system.

[0115] In Example 11, the subject matter of any one of Examples 9-10 can optionally include that the delay value is changeable in run-time either by the PHY system or by the higher layer system.

[0116] In Example 12, the subject matter of any one of Examples 8-11 can optionally include that the PHY system is configured to cache the transactions of the specific transaction type until a delaying condition is satisfied.

[0117] In Example 13, the subject matter of Example 12 can optionally include that the delaying condition comprises at least one of the following: an elapse of a delay time specified by the delay value for the specific transaction type, a latency critical transaction required to be reported to the higher layer system, a power down requirement for the PHY system.

[0118] In Example 14, the subject matter of any one of Examples 12-13 can optionally include that the PHY system is configured to report the cached transactions of the specific transaction type to the higher layer system when the delaying condition is fulfilled.

[0119] Example 15 is a method for operating a mobile device, the method comprising: initiating a physical layer (PHY) system for processing physical layer related operations; initiating a higher layer system for processing operations related to layers above the physical layer; establishing a communication channel between the PHY system and the higher layer system for reporting a plurality of transactions from the PHY system to the higher layer system; and consolidating the plurality of transactions based on a single wake-up message directed to the higher layer system.

[0120] In Example 16, the subject matter of Example 15 can optionally include that the higher layer system comprises a cellular protocol stack (CPS) system.

[0121] In Example 17, the subject matter of any one of Examples 15-16 can optionally include that the wake-up message is configured to wake-up the higher layer system for processing the consolidated plurality of transactions.

[0122] In Example 18, the subject matter of any one of Examples 15-17 can optionally include that the plurality of transactions comprise at least one first type of latency critical transaction and at least one second type of non-latency critical transaction.

[0123] In Example 19, the subject matter of Example 18 can optionally include that a timing response requirement for the latency-critical transaction is more strict than a timing response requirement for the non-latency critical transaction.

[0124] In Example 20, the subject matter of any one of Examples 18-19 can optionally include: delaying reporting a non-latency critical transaction until reporting a latency critical transaction.

[0125] In Example 21, the subject matter of any one of Examples 15-20 can optionally include: controlling an enabling or disabling of the consolidation of the plurality of transactions.

[0126] In Example 22, the subject matter of any one of Examples 15-21 can optionally include: enabling the consolidation of transactions of a specific transaction type.

[0127] In Example 23, the subject matter of Example 22 can optionally include: indicating a delay value applicable for the specific transaction type to the PHY system.

[0128] In Example 24, the subject matter of Example 23 can optionally include: activating consolidation of transactions of the specific transaction type based on the indicated delay value.

[0129] In Example 25, the subject matter of any one of Examples 23-24 can optionally include that the delay value is changeable in run-time.

[0130] In Example 26, the subject matter of any one of Examples 22-25 can optionally include: caching the transactions of the specific transaction type until a delaying condition is satisfied.

[0131] In Example 27, the subject matter of Example 26 can optionally include that the delaying condition comprises at least one of the following: an elapse of a delay time specified by the delay value for the specific transaction type, a latency critical transaction required to be reported to the higher layer system, a power down requirement for the PHY system.

[0132] In Example 28, the subject matter of any one of Examples 26-27 can optionally include: reporting the cached transactions of the specific transaction type to the higher layer system when the delaying condition is fulfilled.

[0133] Example 29 is a circuit arrangement for a mobile device, the circuit arrangement comprising: a first circuit configured to process physical layer related operations; a second circuit configured to process operations related to layers above the physical layer; and a communication channel established between the first circuit and the second circuit for reporting a latency critical transaction and at least one non latency critical transaction from the first circuit to the second circuit, wherein the first circuit is configured to delay reporting the at least one non-latency critical transaction until reporting the latency critical transaction.

[0134] In Example 30, the subject matter of Example 29 can optionally include that the first circuit comprises a

physical layer (PHY) circuit; and that the second circuit comprises a cellular protocol stack (CPS) circuit.

[0135] In Example 31, the subject matter of any one of Examples 29-30 can optionally include that the first circuit is configured to consolidate the at least one non-latency critical transaction with the latency critical transaction based on a single wake-up message directed to the higher layer system.

[0136] In Example 32, the subject matter of Example 31 can optionally include that the wake-up message is configured to wake-up the second circuit for processing the consolidated transactions.

[0137] In Example 33, the subject matter of any one of Examples 29-32 can optionally include that a timing response requirement for the latency-critical transaction is more strict than a timing response requirement for the at least one non-latency critical transaction.

[0138] Example 34 is a mobile device, comprising: means for initiating a physical layer (PHY) system for processing physical layer related operations; means for initiating a higher layer system for processing operations related to layers above the physical layer; means for establishing a communication channel between the PHY system and the higher layer system for reporting a plurality of transactions from the PHY system to the higher layer system; and means for consolidating the plurality of transactions based on a single wake-up message directed to the higher layer system.

[0139] In Example 35, the subject matter of Example 34 can optionally include that the higher layer system comprises a cellular protocol stack (CPS) system.

[0140] In Example 36, the subject matter of any one of Examples 34-35 can optionally include that the wake-up message is configured to wake-up the higher layer system for processing the consolidated plurality of transactions.

[0141] Example 37 is a wireless system, comprising: a physical layer (PHY) system configured to process physical layer related operations; a higher layer system configured to process operations related to layers above the physical layer; and a communication channel established between the PHY system and the higher layer system for reporting a plurality of transactions to the higher layer system, wherein the PHY system is configured to consolidate the plurality of transactions based on a single wake-up message directed to the higher layer system.

[0142] In Example 38, the subject matter of Example 37 can optionally include that the higher layer system comprises a cellular protocol stack (CPS) system.

[0143] In Example 39, the subject matter of any one of Examples 37-38 can optionally include that the wake-up message is configured to wake-up the higher layer system for processing the consolidated plurality of transactions.

[0144] Example 40 is a wireless communication circuit, comprising: a physical layer (PHY) circuit configured to process physical layer related operations; a higher layer circuit configured to process operations related to layers

above the physical layer; and a communication channel established between the PHY circuit and the higher layer circuit for reporting a plurality of transactions to the higher layer circuit, wherein the PHY circuit is configured to consolidate the plurality of transactions based on a single wake-up message directed to the higher layer circuit.

[0145] In Example 41, the subject matter of Example 40 can optionally include that the higher layer circuit comprises a cellular protocol stack (CPS) circuit.

[0146] In Example 42, the subject matter of any one of Examples 40-41 can optionally include that the wake-up message is configured to wake-up the higher layer circuit for processing the consolidated plurality of transactions.

[0147] Example 43 is a computer readable non-transitory medium on which computer instructions are stored which when executed by a computer cause the computer to perform the method of any one of Examples 15 to 28.

[0148] In addition, while a particular feature or aspect of the disclosure may have been disclosed with respect to only one of several implementations, such feature or aspect may be combined with one or more other features or aspects of the other implementations as may be desired and advantageous for any given or particular application. Furthermore, to the extent that the terms "include", "have", "with", or other variants thereof are used in either the detailed description or the claims, such terms are intended to be inclusive in a manner similar to the term "comprise". Furthermore, it is understood that aspects of the disclosure may be implemented in discrete circuits, partially integrated circuits or fully

integrated circuits or programming means. Also, the terms "exemplary", "for example" and "e.g." are merely meant as an example, rather than the best or optimal.

[0149] Although specific aspects have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific aspects shown and described without departing from the scope of the present disclosure. This application is intended to cover any adaptations or variations of the specific aspects discussed herein.

[0150] Although the elements in the following claims are recited in a particular sequence with corresponding labeling, unless the claim recitations otherwise imply a particular sequence for implementing some or all of those elements, those elements are not necessarily intended to be limited to being implemented in that particular sequence.

CLAIMS

1. A mobile device, comprising:
 - a physical layer (PHY) system configured to process physical layer related operations;
 - a higher layer system configured to process operations related to layers above the physical layer; and
 - a communication channel established between the PHY system and the higher layer system for reporting a plurality of transactions to the higher layer system,wherein the PHY system is configured to consolidate the plurality of transactions based on a single wake-up message directed to the higher layer system.
2. The mobile device of claim 1,
 - wherein the higher layer system comprises a cellular protocol stack (CPS) system.
3. The mobile device of claim 1 or 2,
 - wherein the wake-up message is configured to wake-up the higher layer system for processing the consolidated plurality of transactions.
4. The mobile device of claim 1 or 2,
 - wherein the plurality of transactions comprise at least one first type of latency critical transaction and at least one second type of non-latency critical transaction.
5. The mobile device of claim 4,
 - wherein a timing response requirement for the latency-critical transaction is more strict than a timing response requirement for the non-latency critical transaction.

6. The mobile device of claim 4,
wherein the PHY system is configured to delay reporting a non-latency critical transaction until reporting a latency critical transaction.
7. The mobile device of claim 1 or 2,
wherein the higher layer system is configured to control the PHY system enabling or disabling consolidation of the plurality of transactions.
8. The mobile device of claim 1 or 2,
wherein the higher layer system is configured to enable the PHY system consolidating transactions of a specific transaction type.
9. The mobile device of claim 8,
wherein the higher layer system is configured to indicate a delay value applicable for the specific transaction type to the PHY system.
10. The mobile device of claim 9,
wherein the PHY system is configured to activate consolidation of transactions of the specific transaction type based on the delay value indicated by the higher layer system.
11. The mobile device of claim 9,
wherein the delay value is changeable in run-time either by the PHY system or by the higher layer system.
12. The mobile device of claim 8,

wherein the PHY system is configured to cache the transactions of the specific transaction type until a delaying condition is satisfied.

13. The mobile device of claim 12,

wherein the delaying condition comprises at least one of the following:

an elapse of a delay time specified by the delay value for the specific transaction type,

a latency critical transaction required to be reported to the higher layer system,

a power down requirement for the PHY system.

14. The mobile device of claim 12,

wherein the PHY system is configured to report the cached transactions of the specific transaction type to the higher layer system when the delaying condition is fulfilled.

15. A method for operating a mobile device, the method comprising:

initiating a physical layer (PHY) system for processing physical layer related operations;

initiating a higher layer system for processing operations related to layers above the physical layer;

establishing a communication channel between the PHY system and the higher layer system for reporting a plurality of transactions from the PHY system to the higher layer system; and

consolidating the plurality of transactions based on a single wake-up message directed to the higher layer system.

16. The method of claim 15,

wherein the higher layer system comprises a cellular protocol stack (CPS) system.

17. A circuit arrangement for a mobile device, the circuit arrangement comprising:

a first circuit configured to process physical layer related operations;

a second circuit configured to process operations related to layers above the physical layer; and

a communication channel established between the first circuit and the second circuit for reporting a latency critical transaction and at least one non latency critical transaction from the first circuit to the second circuit,

wherein the first circuit is configured to delay reporting the at least one non-latency critical transaction until reporting the latency critical transaction.

18. The circuit arrangement of claim 17,

wherein the first circuit comprises a physical layer (PHY) circuit; and

wherein the second circuit comprises a cellular protocol stack (CPS) circuit.

19. A mobile device, comprising:

means for initiating a physical layer (PHY) system for processing physical layer related operations;

means for initiating a higher layer system for processing operations related to layers above the physical layer;

means for establishing a communication channel between the PHY system and the higher layer system for reporting a plurality of transactions from the PHY system to the higher layer system; and

means for consolidating the plurality of transactions based on a single wake-up message directed to the higher layer system.

20. The mobile device of claim 19,

wherein the higher layer system comprises a cellular protocol stack (CPS) system.

21. A wireless system, comprising:

a physical layer (PHY) system configured to process physical layer related operations;

a higher layer system configured to process operations related to layers above the physical layer; and

a communication channel established between the PHY system and the higher layer system for reporting a plurality of transactions to the higher layer system,

wherein the PHY system is configured to consolidate the plurality of transactions based on a single wake-up message directed to the higher layer system.

22. The wireless system of claim 21,

wherein the higher layer system comprises a cellular protocol stack (CPS) system.

23. A wireless communication circuit, comprising:

a physical layer (PHY) circuit configured to process physical layer related operations;

a higher layer circuit configured to process operations related to layers above the physical layer; and

a communication channel established between the PHY circuit and the higher layer circuit for reporting a plurality of transactions to the higher layer circuit,

wherein the PHY circuit is configured to consolidate the plurality of transactions based on a single wake-up message directed to the higher layer circuit.

24. The wireless communication circuit of claim 23,
wherein the higher layer circuit comprises a cellular protocol stack (CPS) circuit.

25. A computer readable non-transitory medium on which computer instructions are stored which when executed by a computer cause the computer to perform the method of claim 15 or 16.

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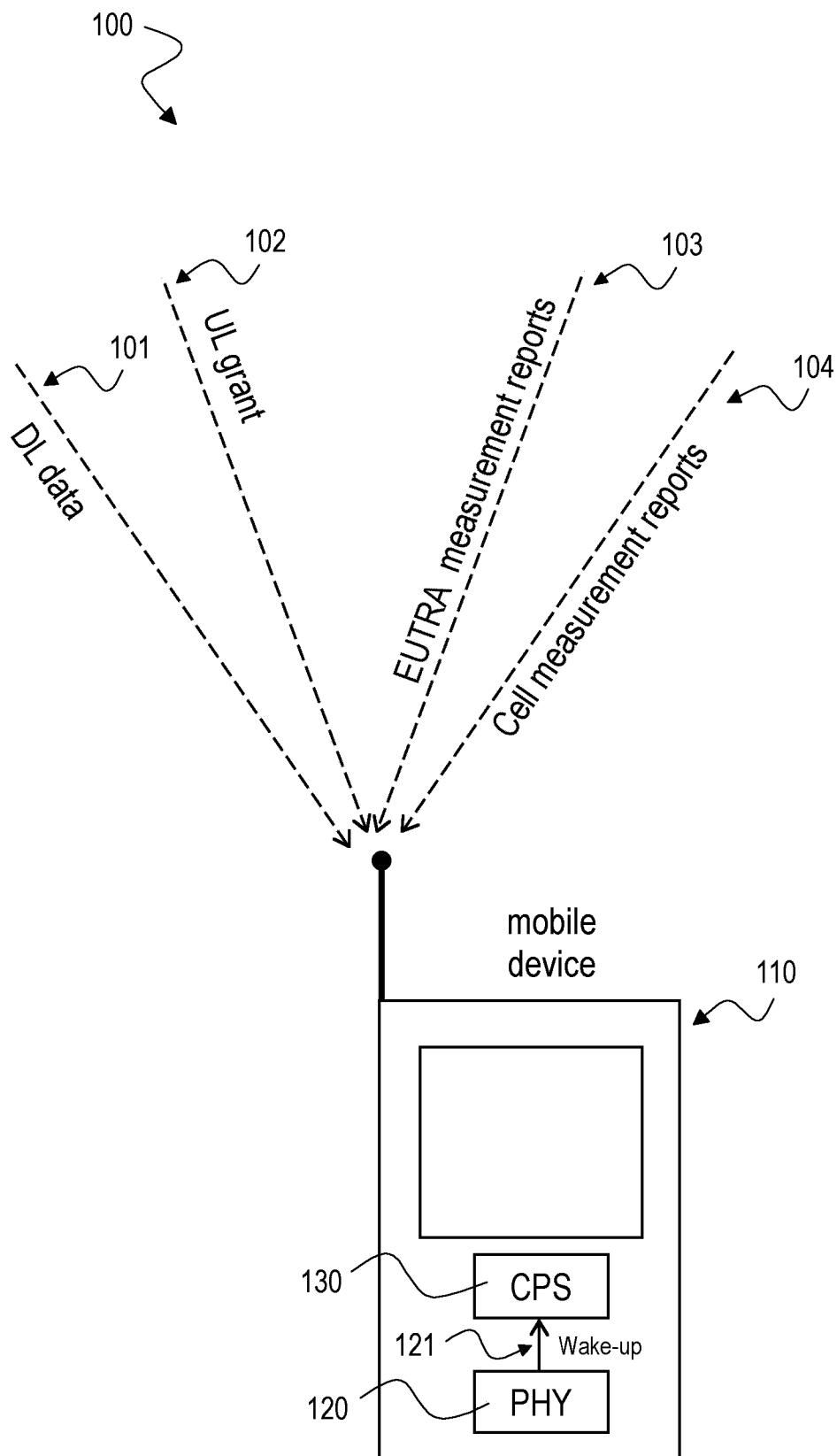
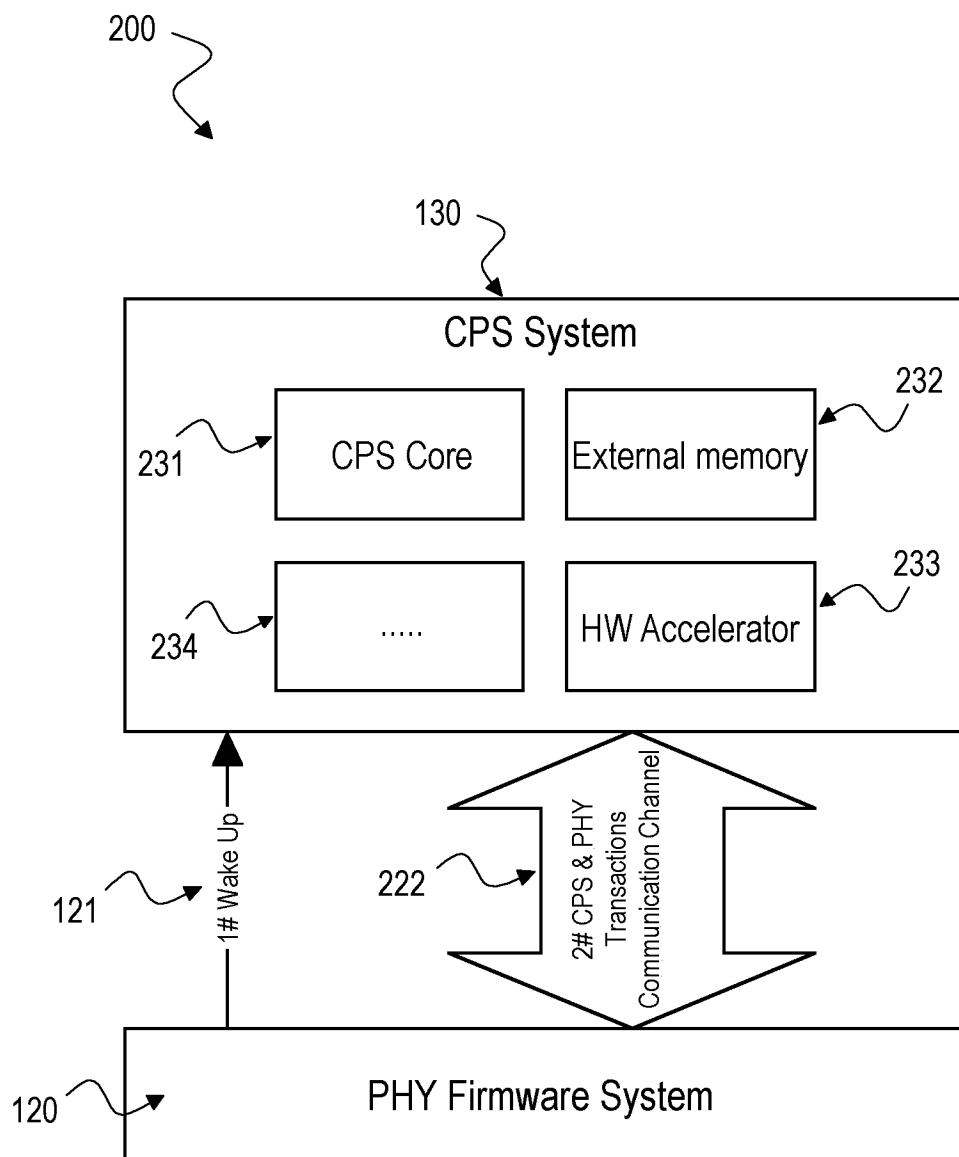
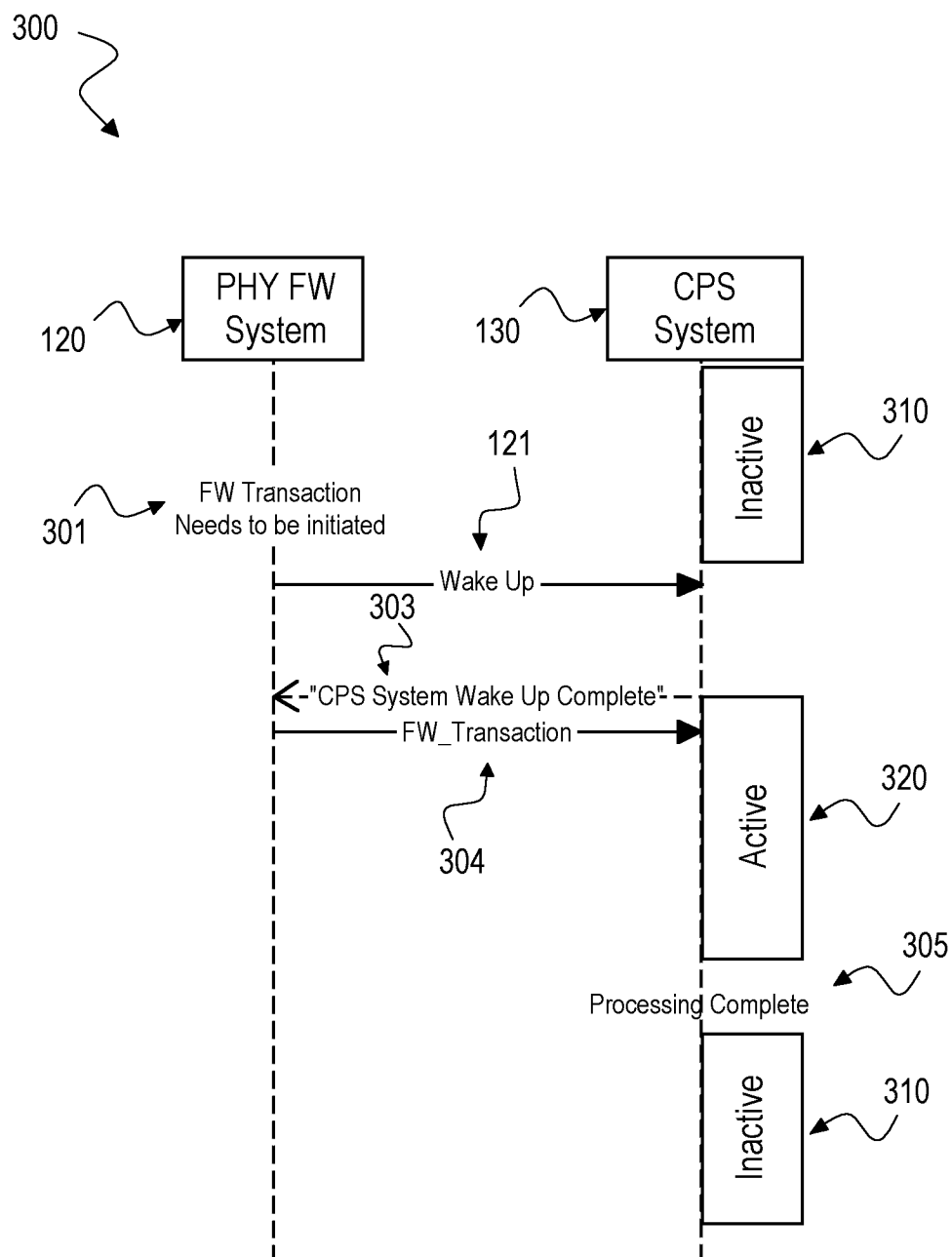


Fig. 1

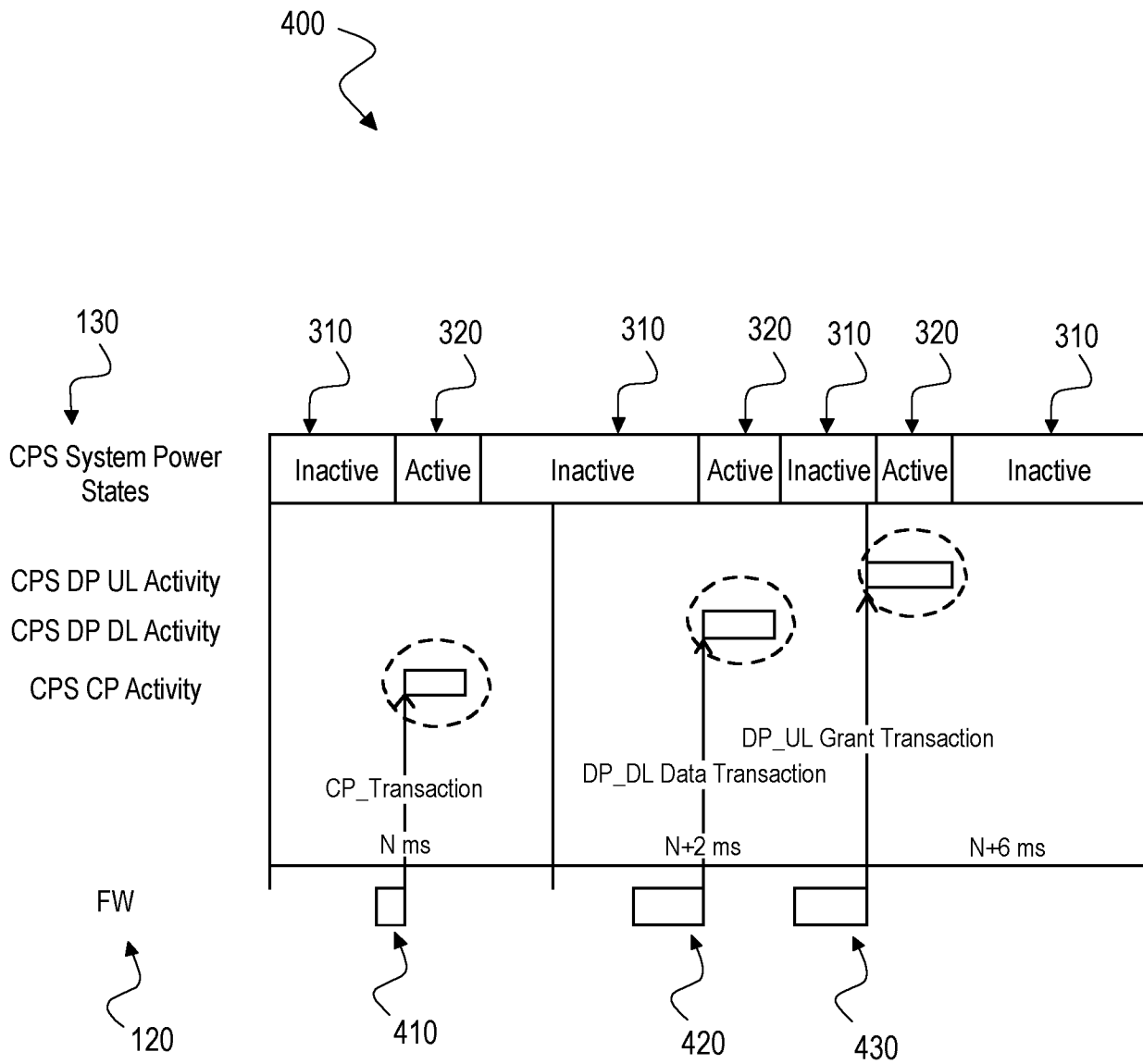
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**Fig. 2**

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**Fig. 3**

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**Fig. 4**

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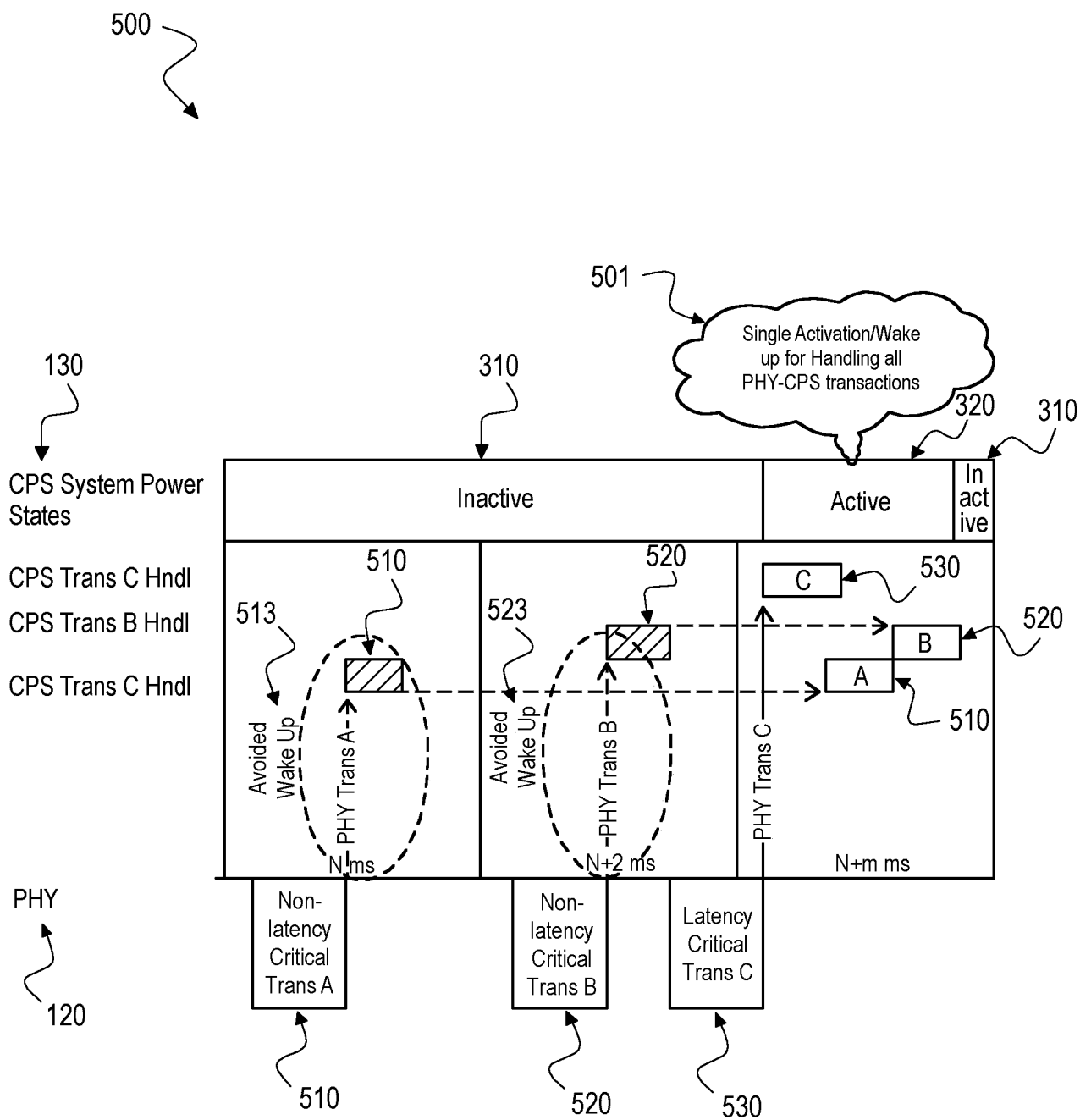


Fig. 5

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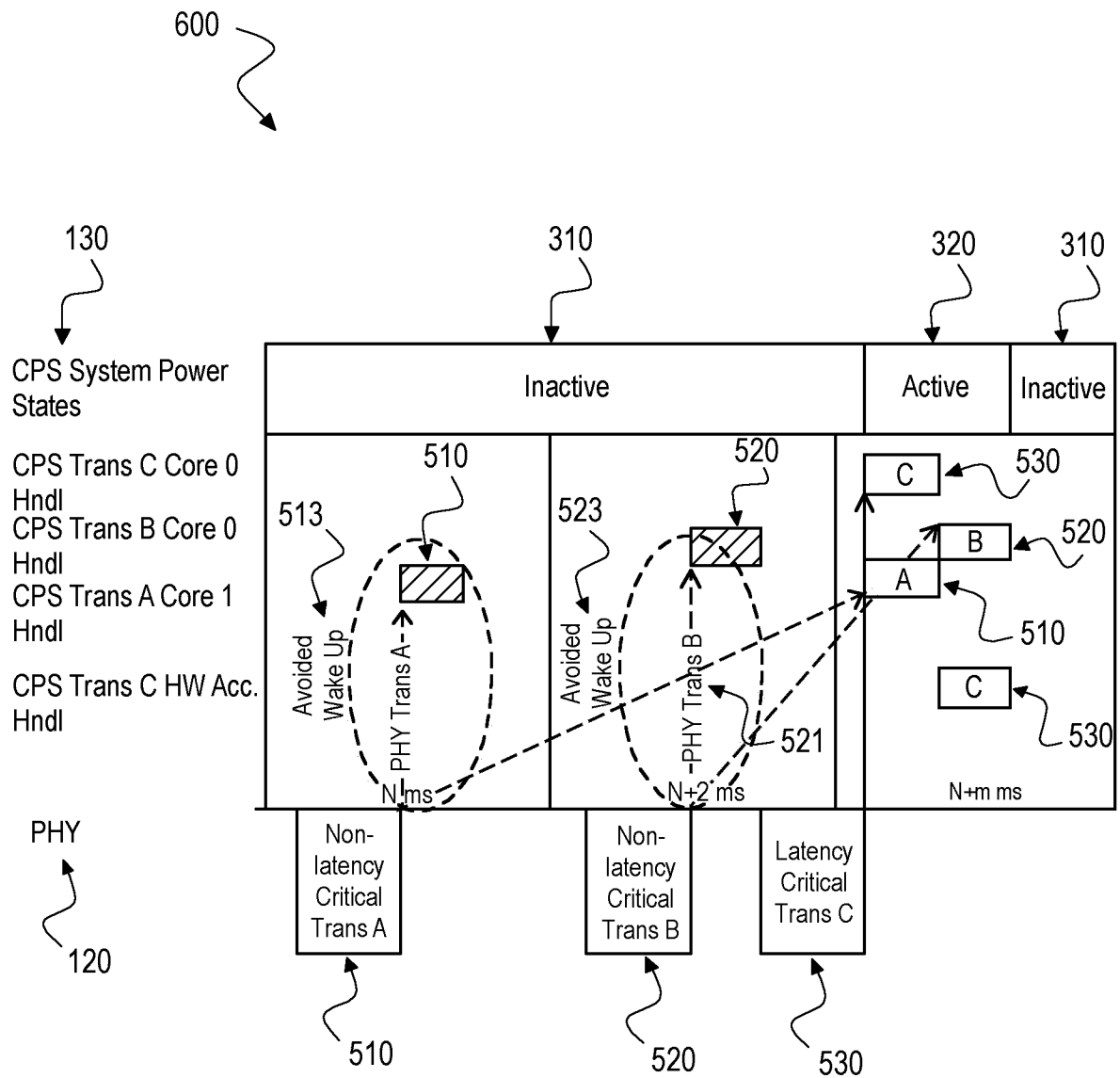
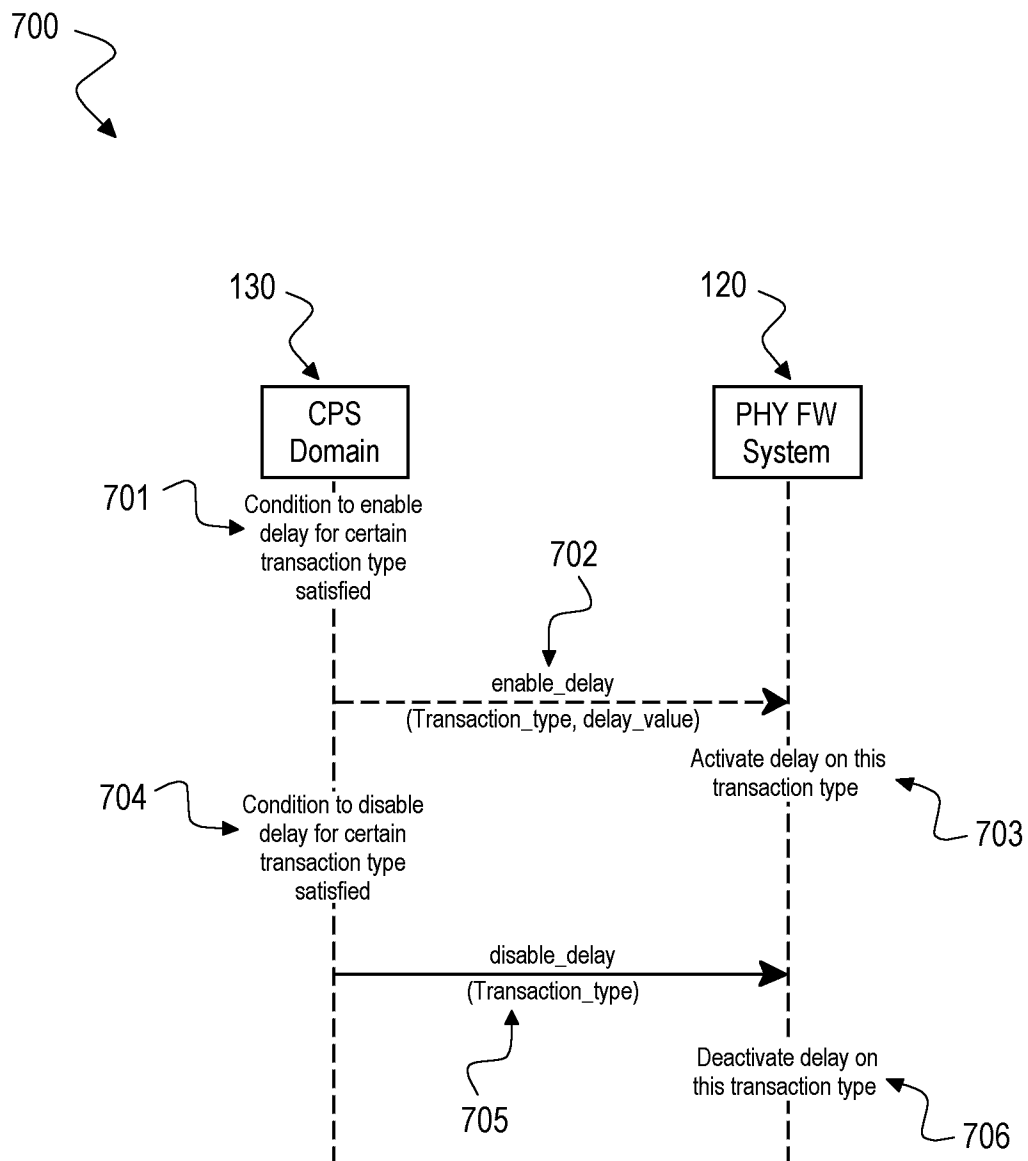


Fig. 6

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**Fig. 7**

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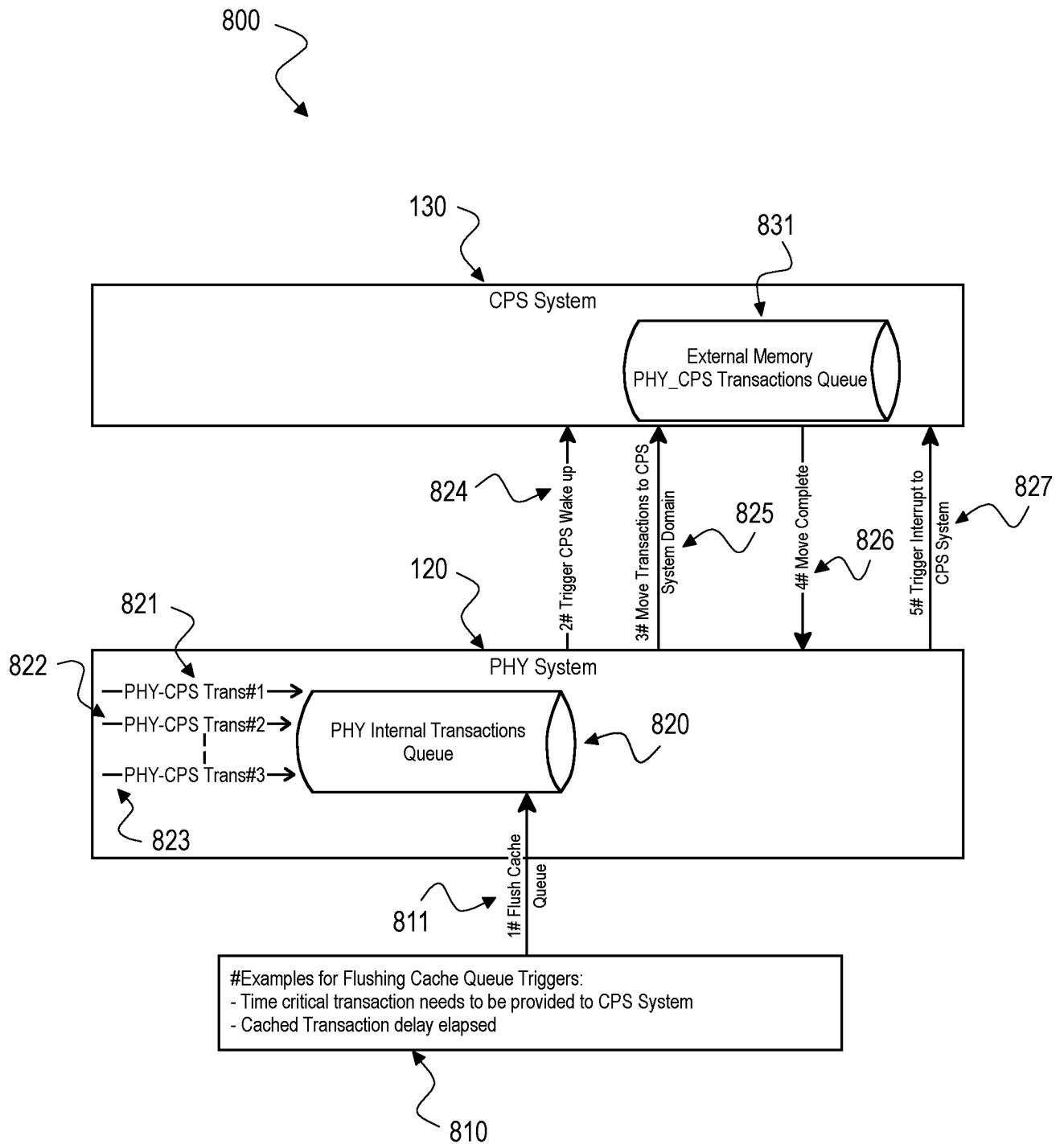


Fig. 8

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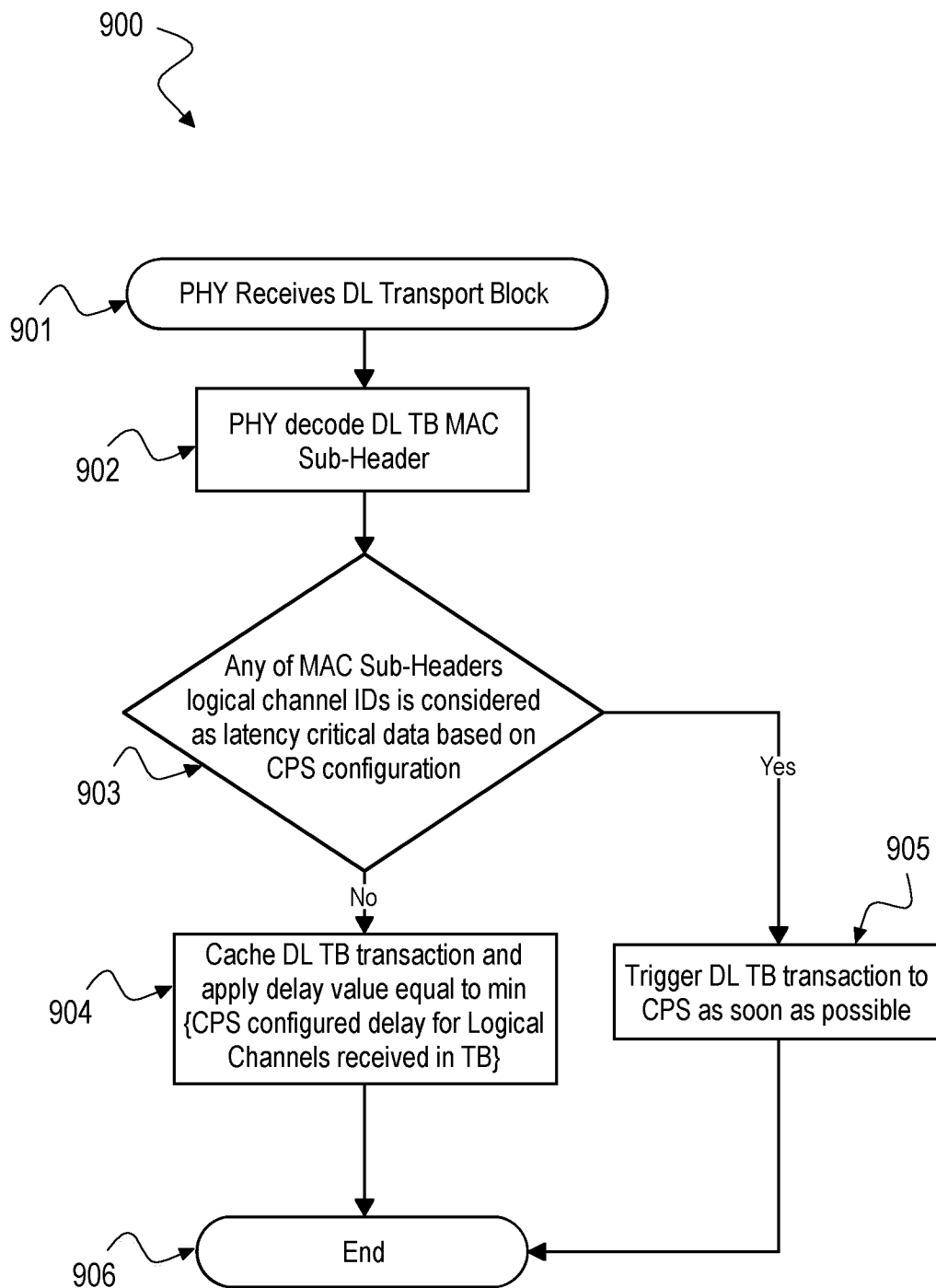


Fig. 9

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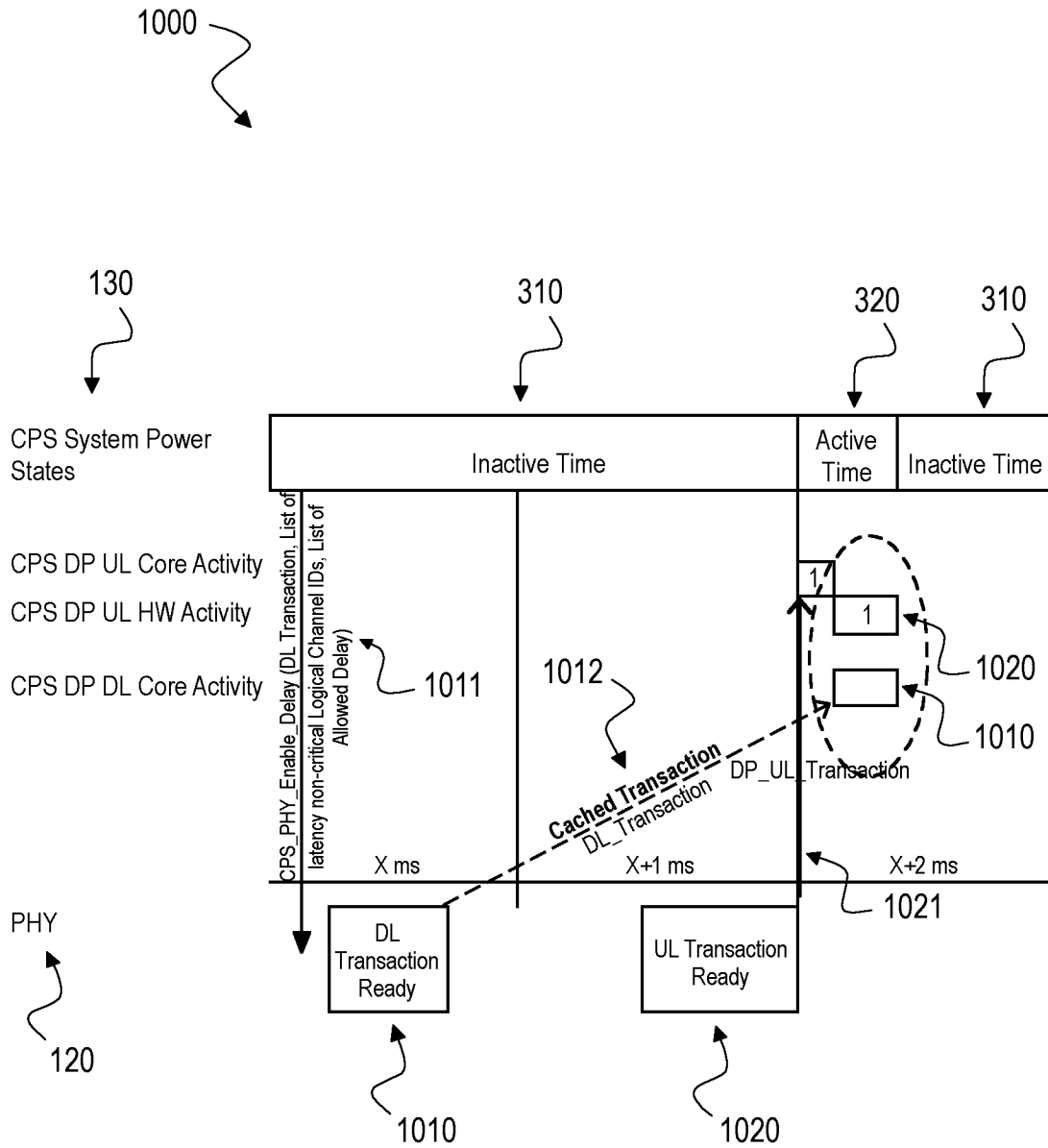


Fig. 10

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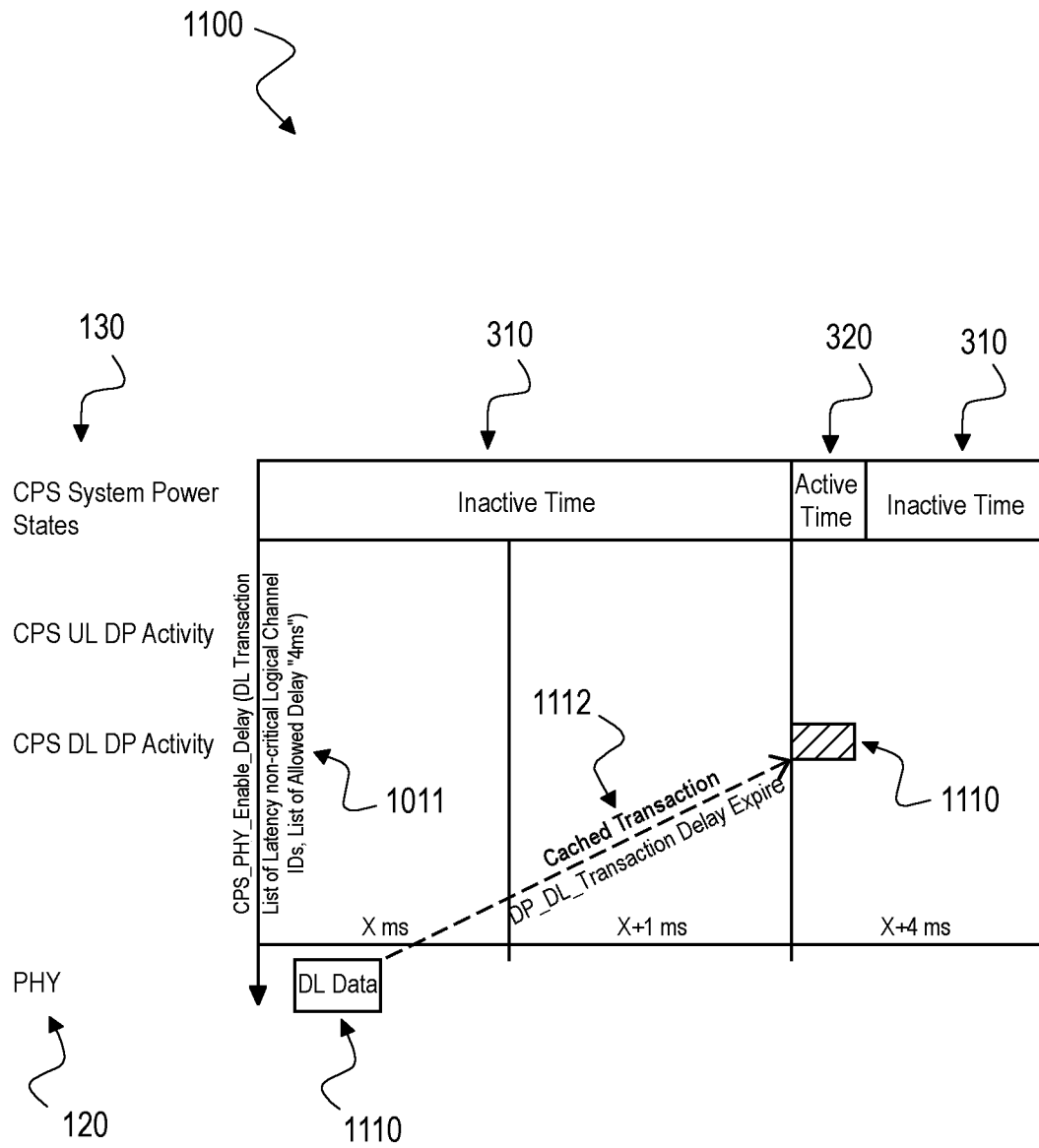
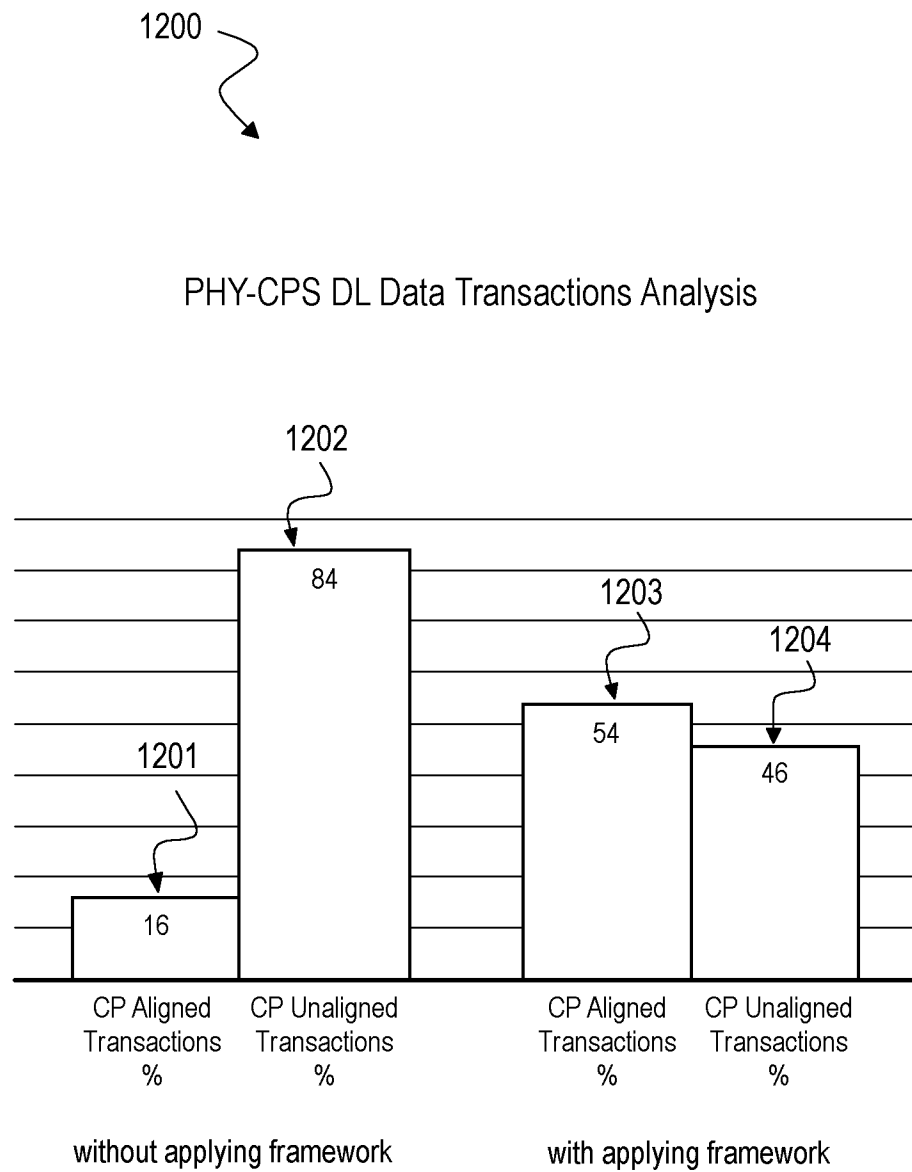


Fig. 11

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**Fig. 12**

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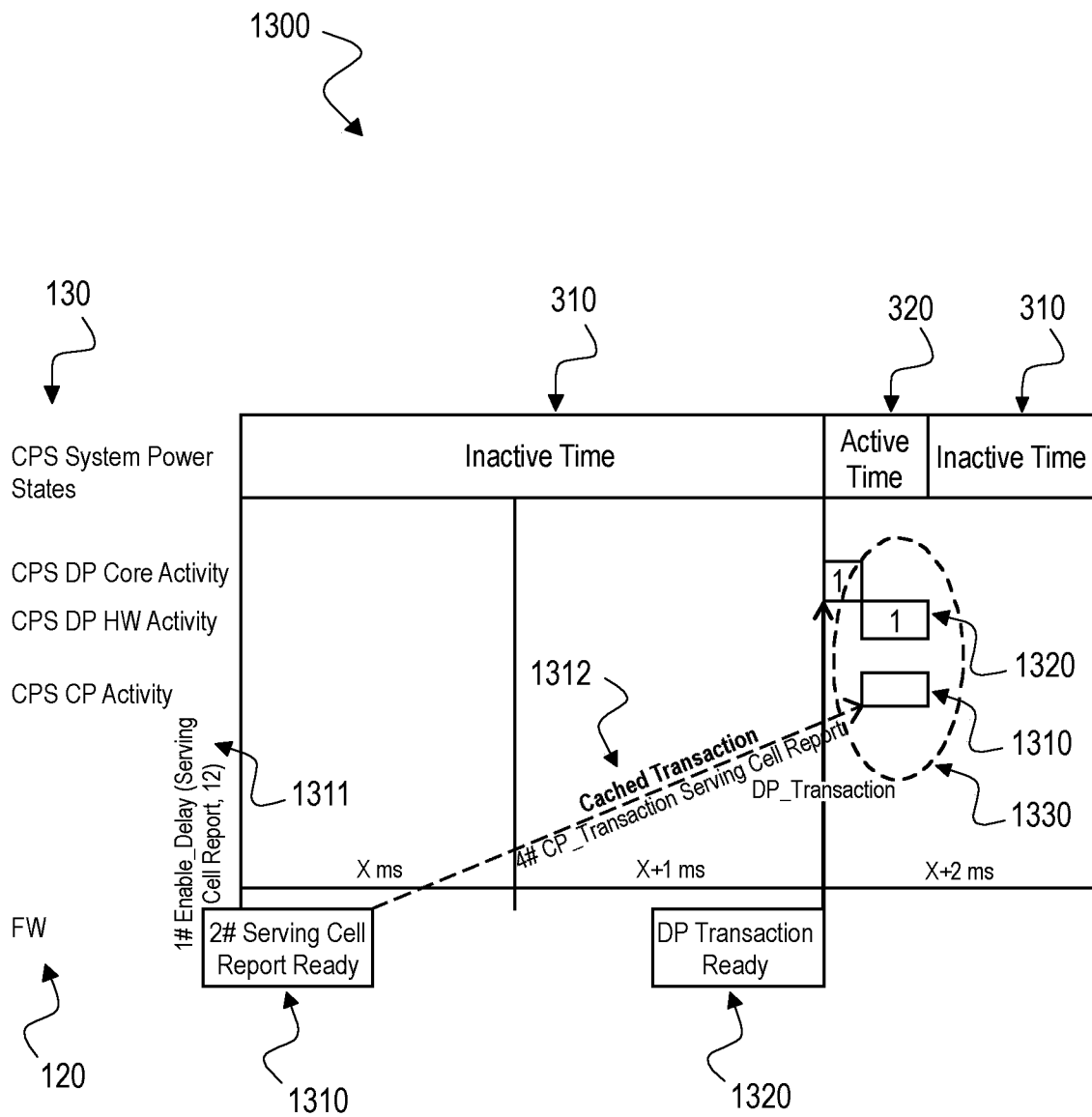


Fig. 13

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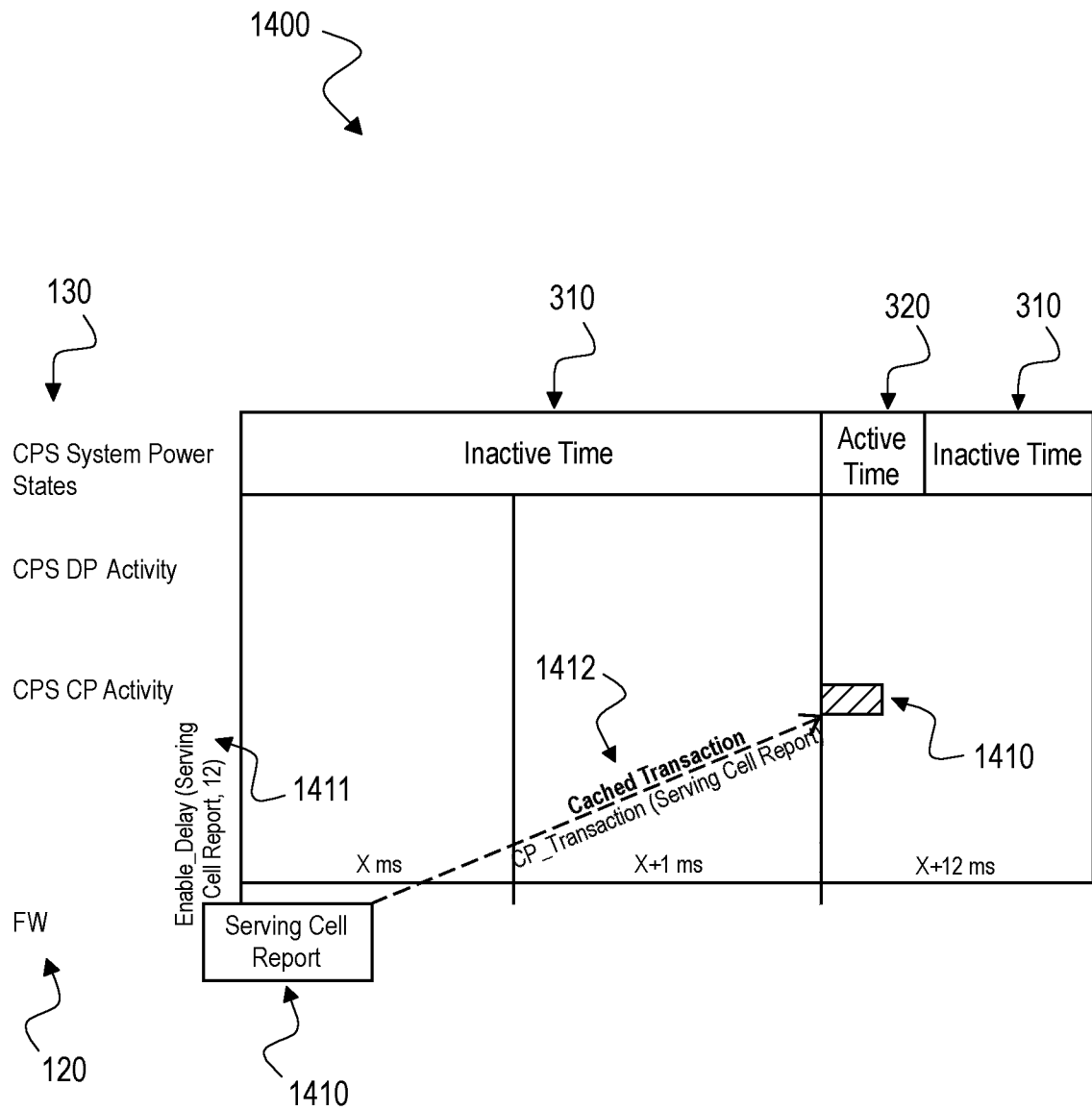
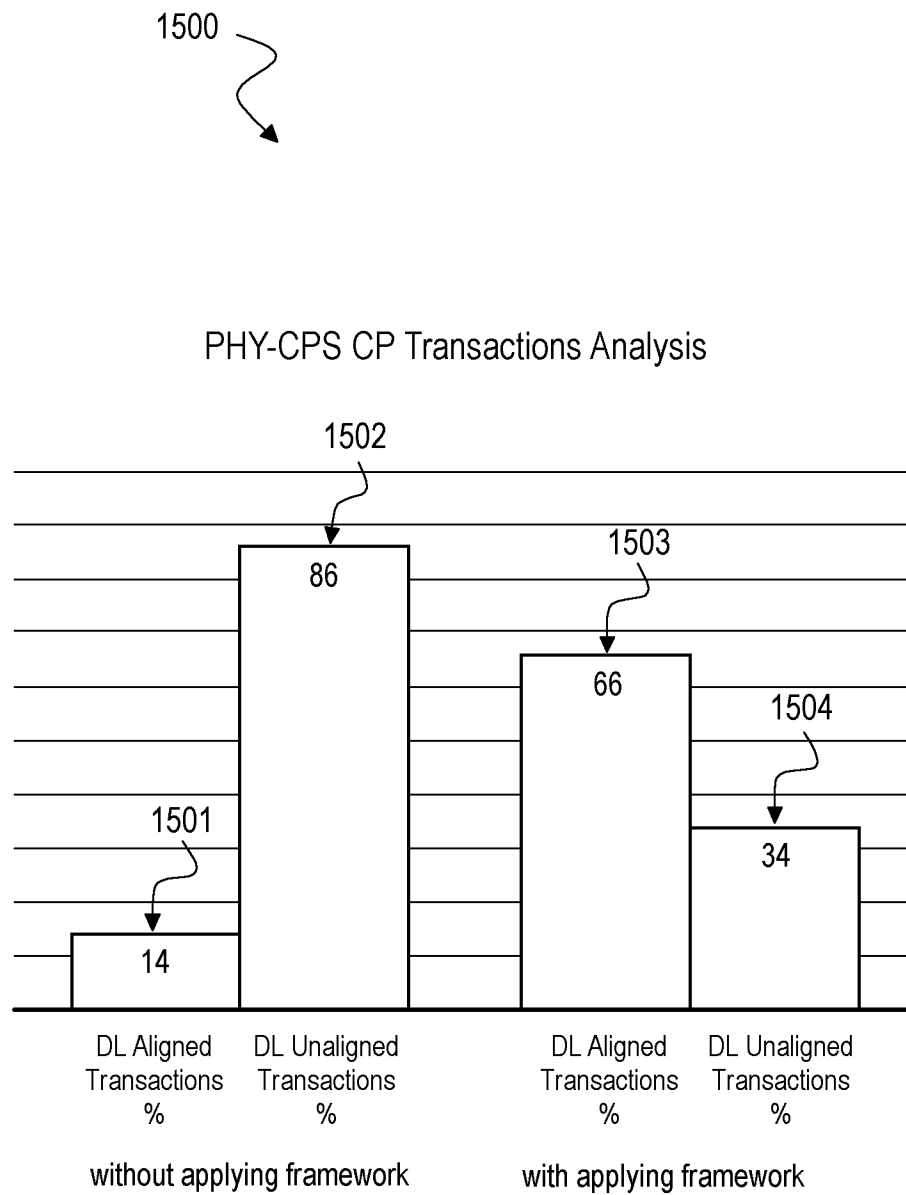


Fig. 14

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**Fig. 15**

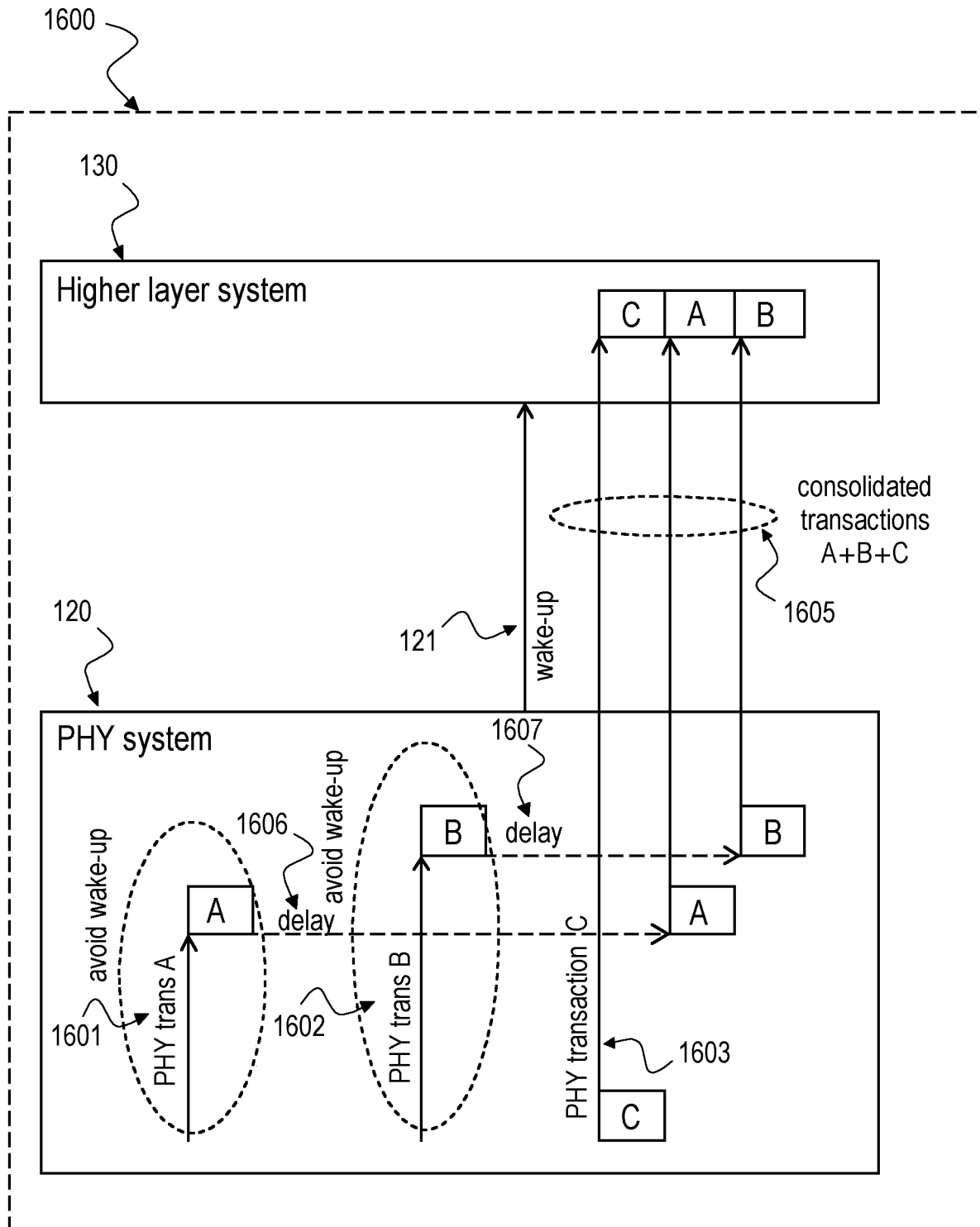
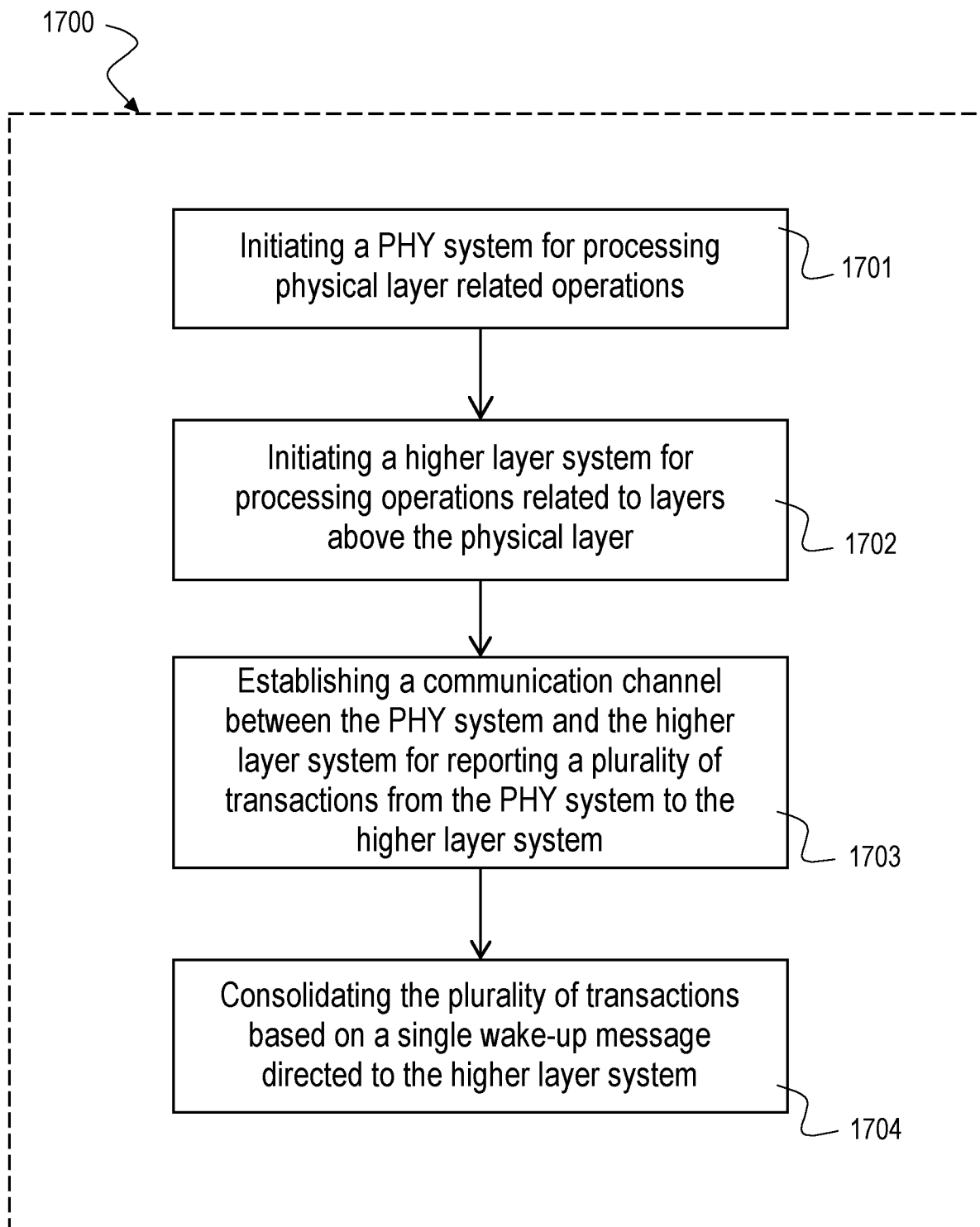


Fig. 16

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**Fig. 17**

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/080781

A. CLASSIFICATION OF SUBJECT MATTER INV. G06F13/14 H04W24/10 H04W52/02 ADD. H04W28/06 H04W80/02		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) G06F H04W		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 2011/022699 A1 (POWELL SCOTT [US] ET AL) 27 January 2011 (2011-01-27) paragraphs [0013], [0014], [0025] - [0028] -----	1-5, 15-25 6-14
Y A	US 2009/140844 A1 (ROYCHOWDHURY DIGANTA [FI]) 4 June 2009 (2009-06-04) paragraphs [0002], [0003], [0004], [0031], [0043], [0067], [0071], [0072] -----	1-5, 15-25 6-14
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents :		
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 19 March 2018		Date of mailing of the international search report 28/03/2018
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Weinmiller, Jost

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011022699	A1	27-01-2011	NONE

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