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(54) Title: REFERENCE VOLTAGE OPTIMIZATION FOR FLASH MEMORY

(57) Abstract: A system includes a voltage generator and a reference voltage setting module. The voltage generator is configured to generate K voltages to be applied to memory cells. The K voltages are used to determine a reference voltage used to read the memory cells, where K is an integer greater than 1. The reference voltage setting module is configured to selectively set the reference voltage to a value between two adjacent ones of the K voltages or one of the two adjacent ones of the K voltages.



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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C16/26 G11C16/30
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/169621 A1 (KAWAMURA SHOICHI [JP]) 11 September 2003 (2003-09-11) the whole document	1-18
A	US 2007/159891 A1 (TU LOC [US] ET AL) 12 July 2007 (2007-07-12) the whole document	1-18



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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003169621	A1	11-09-2003	JP 4068863 B2 26-03-2008
		JP 2003263897 A	19-09-2003
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