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Sorensen

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[54] SYNCHRONIZED COUNTING SYSTEM FOR COUNTING SYMMETRICAL SIGNALS DURING A TIME BASE

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[52] **U.S. Cl.** .....**328/41,** 307/220 R, 307/225 R, 307/269, 328/48, 328/63, 328/72

[51] **Int. Cl.** **H03k 21/00,** H03k 23/06

[58] **Field of Search** .....307/208, 220 R, 225 R, 269, 307/247 R; 328/41, 48, 63, 72–74

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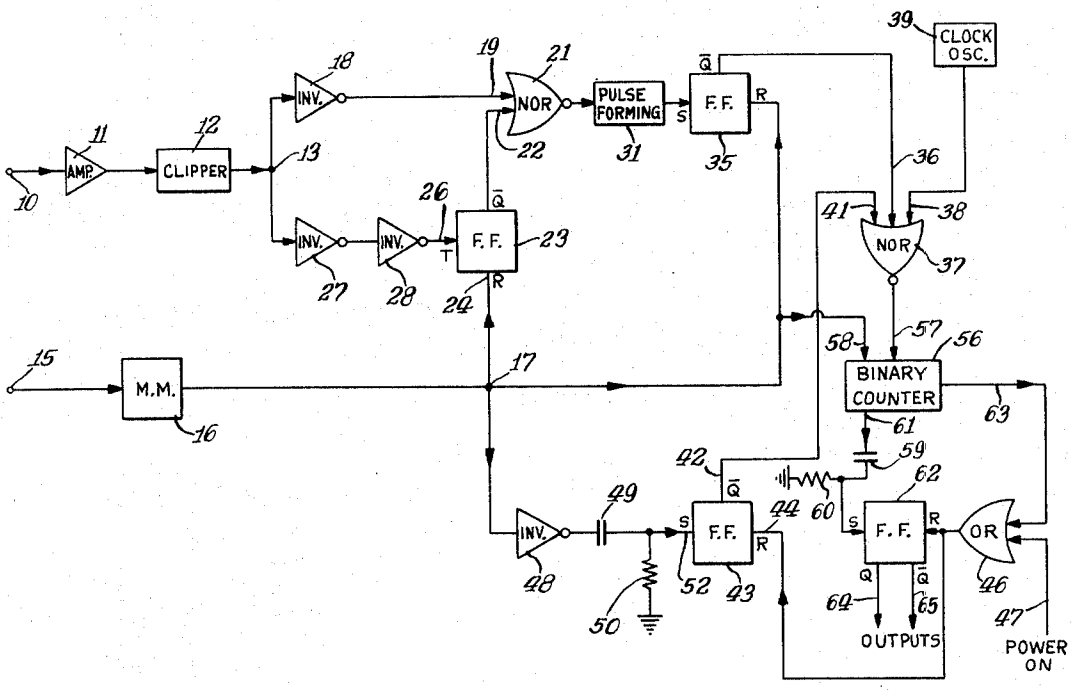
Primary Examiner—Stanley D. Miller, Jr.

Attorney—Lowell C. Noyes et al.

[57] **ABSTRACT**

This disclosure deals with a system for counting the number of cycles of a symmetrical signal, occurring within a time base. The time base is initiated essentially in synchronism with a point in a cycle of the signal and it is terminated a predetermined time thereafter. A counter counts the cycles occurring during the time base and a count is registered at a second point in each cycle, the second point being displaced one-half cycle from the first point, thus providing an advantageous round-off feature.

20 Claims, 3 Drawing Figures



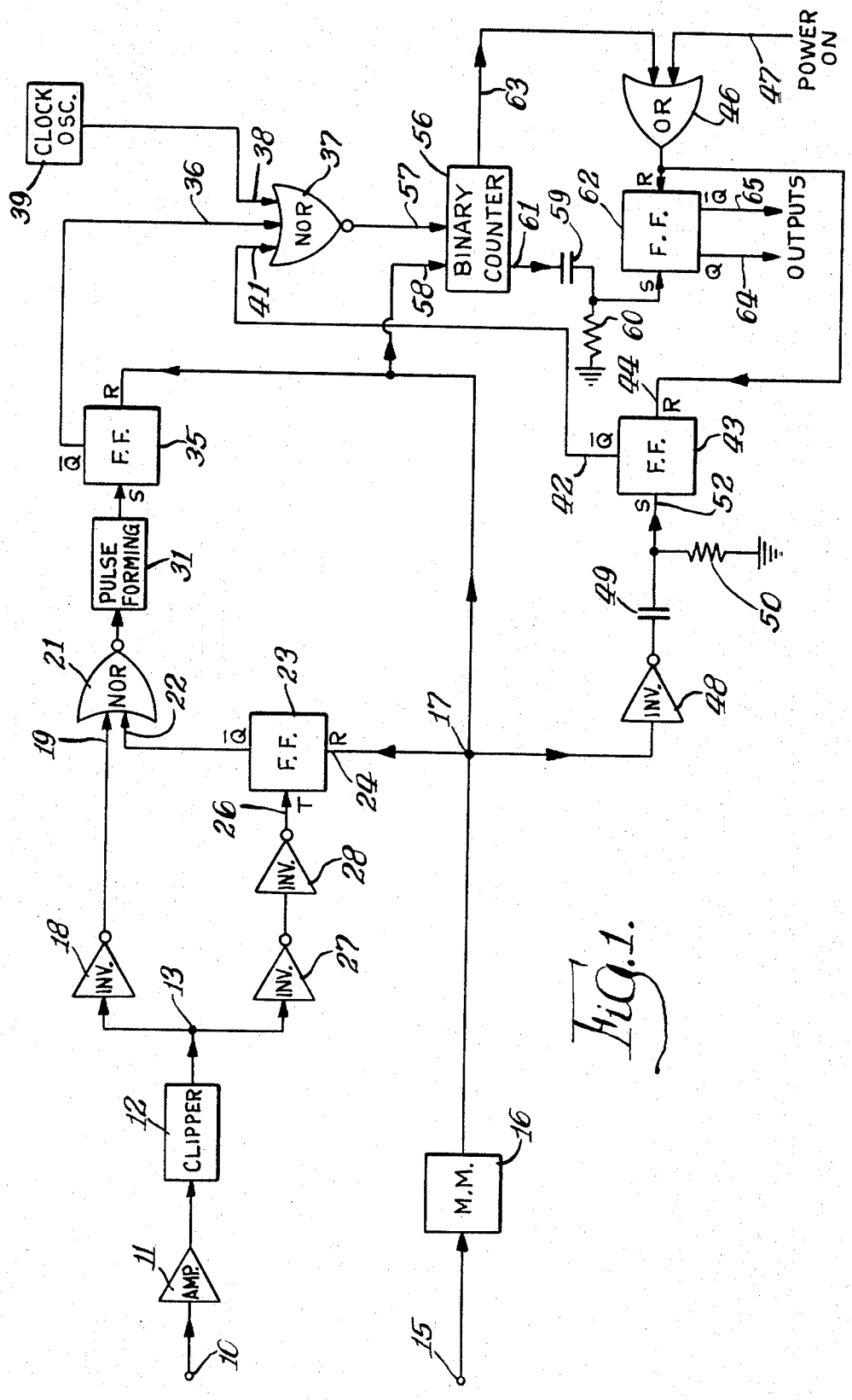

CLOCK OSC.
39
38
37
NOR
36
41
57
56
BINARY COUNTER
58
61
59
62
63
OR
46
47
POWER ON
R
F.F.
65
OUTPUTS
64
S
60
44
R
F.F.
43
42
52
S
49
50
INV.
48
17
PULSE FORMING
31
F.F.
35
R
S
21
NOR
22
19
F.F.
23
24
T
26
INV.
28
INV.
27
INV.
18
13
CLIPPER
12
AMP.
11
10
M.M.
16
15

Fig. 1.

Fig. 2.

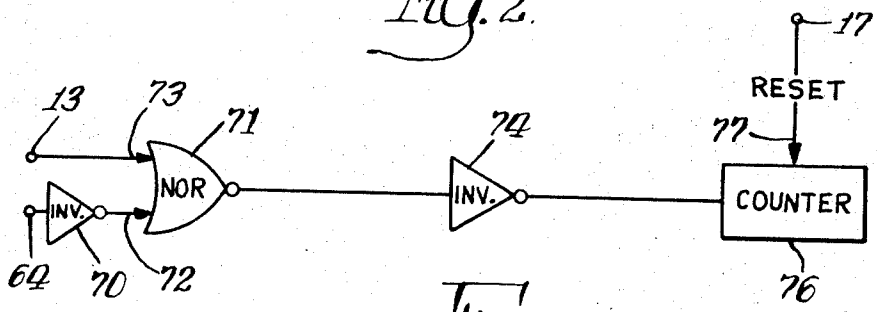
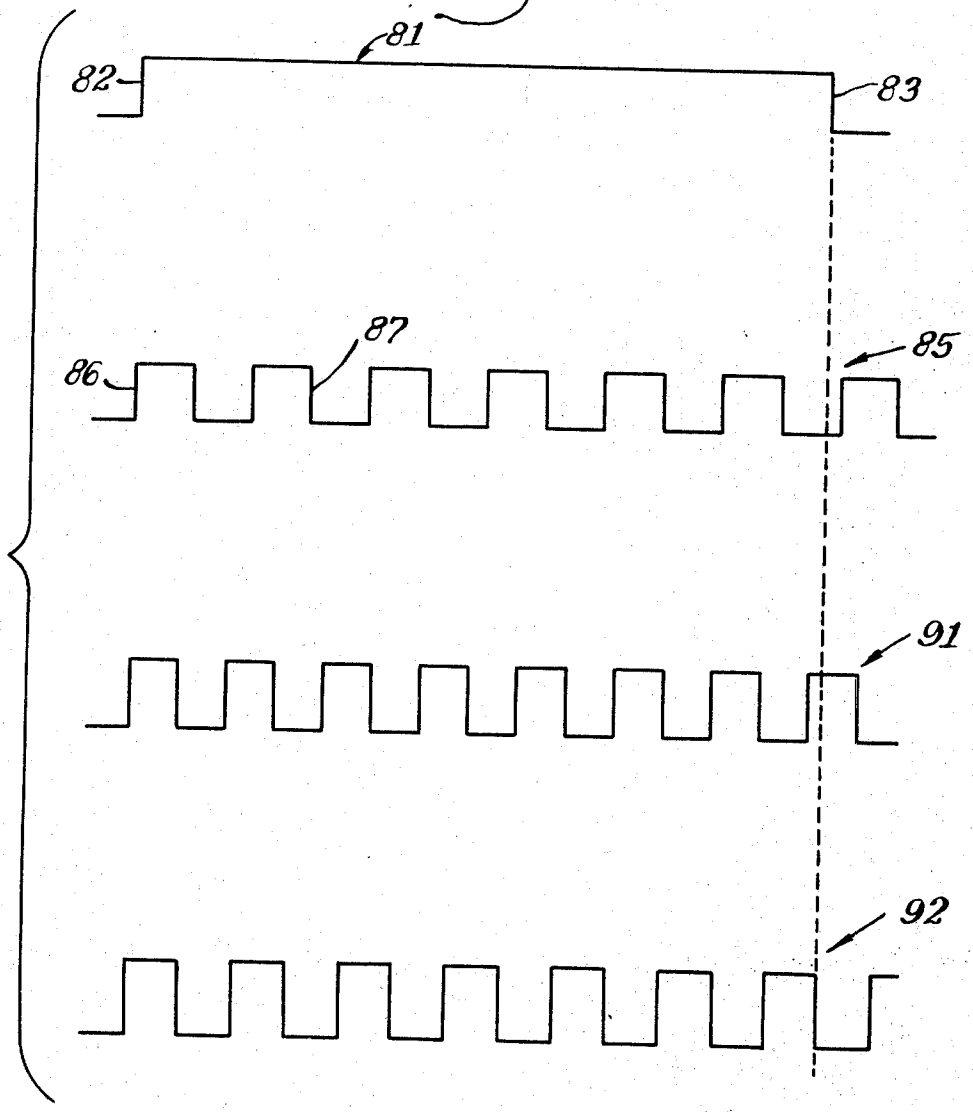

17
RESET
13
73
71
74
77
NOR
INV.
INV.
COUNTER
64
70
72
76

Fig. 3.


81
82
83
87
86
85
91
92

SYNCHRONIZED COUNTING SYSTEM FOR COUNTING SYMMETRICAL SIGNALS DURING A TIME BASE

Numerous circuits are known in the computer art for initiating a signal in response to and substantially in synchronization with another signal. However, there are no known circuits for initiating a desired or base signal in response to first and second signals which may or may not be in time coincidence, the base signal starting essentially in synchronism with the first signal and terminating a predetermined time thereafter. Further, there is no known counting system utilizing such a base signal to count cycles of the first signal during the base signal to obtain an advantageous round-off feature.

It is therefore an object of this invention to provide a counting system for counting the number of cycles of a substantially symmetrical regularly varying signal, occurring during a time base signal, comprising circuit means responsive to said varying signal for initiating a time base signal in synchronism with a certain point in a cycle of said varying signal, gating means having inputs connected to receive said varying signal and said time base signal, and counting means connected to receive the output of said gating means and to count another point in each cycle, which is displaced substantially ½ cycle from said certain point.

It is a further object to provide a circuit for use in the foregoing system for generating a base signal essentially in synchronism with said certain point.

Other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying figures of the drawings wherein:

FIG. 1. is a block diagram of a synchronization circuit in accordance with the present invention;

FIG. 2 is a block diagram of a circuit for use with the circuit shown in FIG. 1; and

FIG. 3 is a timing chart illustrating the operation of the circuits shown in FIGS. 1 and 2.

The circuit shown in FIG. 1 includes a terminal 10 for connecting the circuit to receive a regularly varying signal such as a sine wave. The sine wave signal received at the terminal 10 passes through an amplifier and a clipper circuit 12 which convert the sine wave to a square wave appearing at a junction 13 connected to the output of the clipper 12.

When the circuit shown in FIG. 1 is used in conjunction with a counting system as described hereinafter, to obtain a round-off feature, it is essential that the signal received at the junction 13 be approximately a symmetrical or 50 percent duty cycle wave. In other words, the time duration of the high portion of the wave should be approximately equal to the time duration of the low portion of the wave. In the present illustration, the sine wave received at the terminal 10 is a symmetrical wave. However, if the incoming signal is not symmetrical but is regularly varying, any conventional circuit may be utilized to convert it to a symmetrical wave. If the circuit of FIG. 1 is not utilized in a counting system and only the synchronization feature is important, the wave received at the junction 13 need not be symmetrical.

Regarding the square wave at the junction 13, the high portion of the wave is considered logic "one" and the low portion is considered logic "zero".

The signal received at the terminal 10 may be generated by a transducer which produces a signal having a frequency representative of a parameter being measured. The counting system thus serves as a frequency measuring arrangement for determining the value of the parameter.

In addition to the signal received at the terminal 10, the circuit further receives a second or start signal at a terminal 15 connected to the input of a pulse shaping circuit 16 which, in the present instance, consists of a monostable multivibrator. The signal at the terminal 15 may be manually initiated as by closing a switch or it may be automatically initiated by an associated circuit (not shown). The output of the multivibrator 16 is connected to a junction 17, and a square reset pulse, generated by the multivibrator 16, having a fixed width and amplitude, appears at the junction 17 for each start pulse received at the terminal 15. Again, the high portion of the reset pulse is considered logic one and the low portion is considered logic zero.

The square wave received at the junction 13 passes through an inverter 18 connected between the junction 13 and an input 19 of a NOR gate 21. The NOR gate 21 has a second input 22 which is connected to the $\overline{Q}$ output of a bistable device which in the present instance is a J-K flip-flop 23. The flip-flop 23 includes a reset input 24 which is connected to the junction 17 to receive the reset pulses appearing thereon, and a T input 26 which is connected to the junction 13 through a series connection of two inverters 27 and 28.

Briefly, a reset pulse appearing at the junction 17 resets the flip-flop 23, and the signal appearing at the $\overline{Q}$ output, which is high or at logic one, in the reset state of the flip-flop 23, inhibits or disables the NOR gate 21. With an inhibit signal at the input 22, the output of the gate 21 is low, or at logic zero, regardless of the signal at the input 19. After the termination of the reset pulse, the falling edge of the next square wave at the junction 13, after a short time delay introduced by the two inverters 27 and 28, toggles the flip-flop 23 to its set state. The $\overline{Q}$ output becomes low and thus enables or turns on the NOR gate 21. The square wave at the junction 13 then passes through the inverter 18 to the gate 21, and after the next falling edge of the square wave at the input 19, the output of the gate 21 corresponds to the inverted form of the square wave at the input 19. Due to the double inversions in the components 18 and 21, the signal out of the gate 21 corresponds to the square wave at the junction 13. The time delay introduced by the components 18 and 21 is sufficiently small to be neglected. A pulse forming circuit 31 receives the square wave and forms a relatively sharp positive pulse in response to the rising edge of each square wave which edge is considered herein as being the beginning of each cycle of the square wave.

The two inverters 27 and 28 mentioned above are utilized to introduce a small time delay and thereby ensure that the output of the gate 21 cannot shift to logic one until the next rising edge, or positive going transition, in the next square wave appearing at the junction 13 occuring after a falling edge, or negative going transition, of the reset pulse.

The output of the pulse forming circuit 31 is connected to the set input of a flip-flop 35 which has its reset input connected to receive the reset pulse appear-

ing at the junction 17. The $\overline{Q}$ output of the flip-flop 35 is connected to an input 36 of another NOR gate 37 which also includes an input 38 connected to receive a train of pulses from a clock oscillator 39.

During operation of the system, the flip-flop 35 is reset by each reset pulse appearing at the terminal 17, and the reset state of the flip-flop 35 causes a logic one of inhibit signal to appear at the input 36 of the gate 37.

The NOR gate 37 has another input 41 which is connected to the $\overline{Q}$ output 42 of another flip-flop 43. The reset input 44 of the flip-flop 43 is connected to receive a power-on signal through an OR gate 46, the power-on signal appearing on a conductor 47. The reset pulse appearing at the junction 17 passes through an inverter 48 and through an RC pulse shaping circuit, including a capacitor 49 and a resistor 50, to the set input 52 of the flip-flop 43. The rising edge of the pulse out of the inverter 48, which corresponds to the falling edge of a reset pulse at the junction 17, causes a relatively sharp positive pulse to appear at the set input 52 of the flip-flop 43 and thereby toggle the flip-flop 43 to its set state. As mentioned above, when the flip-flop 43 is in its reset state, an inhibit or logic one signal appears at the input 41 of the NOR gate 37, and when the flip-flop 43 is in its set state, an enable or logic zero signal appears at the input 41.

The alternating current output of the oscillator 39 alternates between logic zero and logic one and when both inputs 36 and 41 are at logic zero, the output of the gate 37 follows the complement of the oscillator 39 output. The NOR gate 37 output is connected to an input 57 of a binary counter 56. The binary counter 56 also has a reset input 58 connected to receive the reset pulse appearing at the junction 17, whereby the counter 56 is reset or cleared at the appearance of each reset pulse. The binary counter 56 includes a series of flip-flops which are connected to form a binary up counter. After the counter 56 has been cleared by a reset pulse at the input 58 and the two signals at the inputs 36 and 41 of the NOR gate 37 are at zero, the pulses through the gate 37 cause the flip-flops in the counter 56 to count up until the last flip-flop in the series is set and the counter output 63 is at logic one.

The first flip-flop in the counter 56 to be toggled by a pulse from the oscillator 39 is connected by the output 61 to the set input of a flip-flop 62, and the last flip-flop in the counter 56 is connected by another output 63 to the reset input of the flip-flop 62 through the OR gate 46. A capacitor 59 and a resistor 60 are connected in the line between the output 61 and the set input of the flip-flop 62, and produce a sharp positive pulse to set the flip-flop 62 when the output 61 has a transition from logic zero to logic one. Thus, the flip-flop 62 is reset either by a power-on signal appearing on the conductor 47 or by the signal appearing at the output 63 of the counter 56. The outputs from the circuit are taken from the Q and $\overline{Q}$ outputs 64 and 65 of the flip-flop 62, one of course being the complement of the other.

Considering the operation of the circuit as a whole, when the power is initially turned on, a power-on signal appearing on the conductor 47 passes through the OR gate 46 and resets the flip-flops 43 and 62. Thereafter, a start pulse received at the terminal 15 causes a reset pulse to appear on the junction 17 which clears the binary counter 56 or presets the counter to any desired number. When the flip-flop 62 is in its reset state, the Q output 64 is at logic zero and the $\overline{Q}$ output 65 is at logic one. When the flip-flop 43 is reset, a high or logic one signal appears at the input 41 of the gate 37 and inhibits the gate 37. The reset pulse appearing at the junction 17 also passes through the inverter 48 and through the capacitor 49, and the trailing edge of the reset pulse sets the flip-flop 43, removing the inhibit signal from the input 41 of the NOR gate 37.

The reset pulse at the junction 17 also resets the flip-flop 23 and thus causes an inhibit signal to appear at the input 22 of the NOR gate 21. The falling edge of the next square wave appearing at the junction 13 sets the flip-flop 23 and removes the inhibit signal from the input 22 of the gate 21. Subsequent square waves appearing at the junction 13 then pass through the inverter 18 and the NOR gate 21, and the leading or rising edge of the next subsequent square wave causes a positive pulse to appear at the set input of the flip-flop 35 which sets this flip-flop. When the flip-flop 35 is set, the inhibit signal appearing on the input 36 of the NOR gate 37 is also removed, and the signal from the clock oscillator 39 flows through the NOR gate 37 to the input 57 of the binary counter 56. Thus, the gate 37 is enabled or turned on and pulses begin to flow to the binary counter 56 substantially in synchronism with the leading or rising edge of the first square wave appearing at the terminal 13 and occurring after a reset pulse.

Actually, the binary counter 56 begins counting a short time after the leading edge of this square wave because of the inherent time delays in the circuit components and because the signal from the oscillator 39 may not become zero as soon as the NOR gate 37 is turned on. The first factor mentioned above is negligible, and the second factor may be made negligible by making the frequency of the oscillator 39 far higher than that of the signal at the terminal 10. The oscillator signal may, for example, be around 100 KHz, and the signal at the terminal 10 may be in the range of 125 Hz.

Counting of the first pulse by the binary counter 56 causes a signal to appear at its output 61 which sets the flip-flop 62, causing the signal at the Q output 64 to shift to logic one and the signal at the $\overline{Q}$ output 65 to shift to logic zero. These signals may be referred to as timed signals, or base signals. The binary counter 56 continues counting until the last flip-flop in the series in the binary counter is set, at which time a signal appears on the output 63. This signal passes through the OR gate 46 and resets the flip-flop 62, thus terminating its output signals. The signal at the output 63 also resets the flip-flop 43, causing an inhibit signal to again appear at the input 41 of the NOR gate 37. This of course stops the flow of pulses to the binary counter 56. The circuit then remains in this state until the next start pulse appears at the terminal 15 in order to repeat the foregoing cycle of operation.

It will be apparent from the foregoing that the time duration of the signals of the flip-flop 62 is determined both by the frequency of the oscillator 39 and by the number to which the binary counter 56 counts, and either the frequency or the number may be varied to obtain the desired time duration. Preferably, the counter 56 is provided with circuitry for presetting it to a certain number in response to each reset pulse, so that a desired time duration may be obtained simply by

changing the wiring to obtain a different preset number. The system described above is highly advantageous both because the flip-flop **62** signals are always initiated essentially in synchronism with the leading edge of a square wave and because the time duration of the signals may be readily adjusted to obtain a predetermined value.

While the pulse synchronization circuit illustrated in FIG. **1** is useful in other circumstances, it is particularly advantageous when used in a counting system because of a round-off feature obtainable with it. With reference to FIG. **2**, a NOR gate **71** has an input **72** connected through an inverter **70** to receive the signal appearing on the Q output **64** of the flip-flop **62**, and an input **73** connected to receive the square wave appearing at the junction **13**. The inverter **70** may of course be dispensed with if the input **72** is connected to the $\overline{Q}$ output **65** of the flip-flop **62**. The output of the NOR gate **71** is connected through an inverter **74** to a counter **76**. A reset or clear input **77** of the counter **76** is connected to receive the reset pulse appearing at the junction **17** in order to clear the counter **76** prior to a counting operation.

When the flip-flop **62** (FIG. **1**) is reset, the output **64** is at zero and the inverter **70** produces the complement logic one at the input **72**, thus inhibiting the NOR gate **71** and blocking the flow of the square wave through the gate **71**. As soon as the flip-flop **62** is set, this inhibit is removed from the NOR gate **71** and the square wave flows through the inverter **74** to the counter **76**.

With reference to FIG. **3**, the reference numeral **81** represents the output **64** signal which has a leading edge **82** and a trailing edge **83**. The reference numeral **85** represents a square wave to be counted, each cycle having a leading or rising edge **86** and a trailing or falling edge **87**. As previously mentioned, the leading edge **82** of the signal **81** essentially coincides with the leading edge **86** of a cycle. The edge **82** turns the gate **71** on and, in effect, the square wave **85** flows through the gate **71**. The inverter **74** again inverts the square wave and the falling edges of the square wave at the counter **76** input actuate the counter. Due to the two inversions in the components **71** and **74**, the square wave to the counter **76** corresponds to the wave **85**. Thus, the counter **76** counts the number of falling edges of the wave **85** occurring within the duration of the signal **81**. In the case of the square wave **85**, approximately 5⅞ cycles occur within the signal **81**. Since falling edges of the wave are counted and a total of six falling edges occur within the signal **81**, a total count of six is registered in the binary counter **76**. It will be apparent, therefore, that the count in the counter **76** is rounded to the nearest full number.

With reference to the square wave indicated by the reference numeral **91**, the wave **91** has a slightly higher frequency than the wave **85** and a total of 7⅝ cycles occur within the signal **81**. Again, the falling edges of the wave are counted and a total of seven falling edges occur within the duration of the time base signal **81**. Consequently, the count in the counter **76** is again rounded to the nearest full number. With reference to the square wave indicated by the reference numeral **92**, the frequency of the wave **92** is intermediate of the frequencies of the trains **85** and **91**. Approximately 6½ cycles of the wave **92** occur within signal **81**. In the wave **92**, the seventh falling edge substantially coincides with the edge **83** of the signal **81**, and the count indicated by the counter **76** could be either six or seven with equal probability, but again the count is rounded to the nearest full number.

It will be apparent from the foregoing that the counter **76** always indicates the number of cycles falling within the base signal **81** rounded to the nearest full number, thus ensuring that any rounding error cannot be greater than ½ cycle. For the system to provide this round-off feature, the signal **81** preferably is initiated essentially in synchronism with the leading edge of a cycle of a square wave to be counted, the counter **76** preferably counts the falling edges of the wave, and the square wave to be counted preferably is symmetrical.

It should be understood that the foregoing circuits may be composed of either electronic circuit components or fluidic circuit components.

While operation of the circuit has been described wherein a time base has been initiated on the rising edge of a square wave and counts are taken on the falling edges, it will be obvious that a time base could be initiated on a falling edge and the counts could be taken on the rising edges. Further, while the assignment of logic levels described herein for illustration purposes is the case where logic one is high and logic zero is low, it should be realized that an opposite assignment could be made where logic one is low and logic zero is high. In a system of the latter character, the NOR gates disclosed herein would be replaced by NAND components and the OR gates would be replaced by AND components.

It will be apparent from the foregoing description that a novel and useful pulse synchronization circuit and counting system have been provided. The circuit provides a timed or base signal which is always initiated essentially in synchronism with a certain point, preferably the leading edge, of a square wave. When used in a counting system, it is highly advantageous in that it provides a round-off feature which ensures that the total count is never in error by more than one-half a cycle. Where the time duration of the signal **81** is known, the counting system as described may be used to determine the frequency of the square wave rounded to the nearest full number.

I claim:

1. A counting system for counting the number of cycles occurring during a time base signal of a substantially symmetrical signal, comprising circuit means responsive to said symmetrical signal for initiating a time base signal in synchronism with a predetermined point in a cycle of said symmetrical signal, gating means having inputs connected to receive said symmetrical signal and said time base signal, and counting means connected to receive the output of said gating means and to count in each cycle at another point which is displaced substantially one-half cycle from said predetermined point.

2. A system as in claim **1**, wherein said predetermined point comprises the beginning of a cycle, and said other point is midway in a cycle.

3. A counting system as in claim **1**, wherein said circuit means generates a time base signal having a fixed time duration.

4. A counting system as in claim 1, wherein said circuit means comprises second counting means, oscillator means, and second gating means for connecting the output of said oscillator means to the input of said second counting means essentially in synchronism with said predetermined point in a cycle of said symmetrical signal.

5. A counting system as in claim 4, wherein the frequency of said oscillator means is substantially greater than the frequency of said symmetrical signal.

6. A counting system as in claim 1, wherein said circuit means is adapted to respond to a positive transition of a square wave and said counting means is adapted to respond to a negative transition of a square wave.

7. A signal synchronization circuit for providing a base signal in response to a start signal and to a regularly varying signal, comprising first circuit means for generating said base signal, said first circuit means including an enabling circuit which initiates said base signal in response to an enabling signal, and second circuit means responsive to said start signal and to said regularly varying signal for providing said enabling signal at a predetermined point in the first cycle of said varying signal occurring after a start signal.

8. A circuit as in claim 7, wherein said first circuit means provides a base signal having a preselected time duration.

9. A circuit as in claim 8, wherein said first circuit means includes an oscillator, and a counter for counting cycles of said oscillator, said time duration being dependent upon the count of said counter and the frequency of said oscillator.

10. A circuit as in claim 9, wherein said first circuit means further includes a flip-flop connected to said counter and set by the first count of said counter and reset by the last count of said counter, said flip-flop providing said base signal while in said reset state.

11. A circuit as in claim 9, wherein said enabling circuit includes a gate connected between said oscillator and said counter, said enabling signal turning said gate on.

12. A circuit as in claim 11, wherein said first circuit means further comprises bistable means having an input connected to said counter and being toggled upon said counter reaching said last count, said bistable means further including an output connected to said enabling circuit for inhibiting said enabling circuit upon said toggling of said bistable means.

13. A circuit as in claim 7, wherein said second circuit means includes gate means connected to respond to said start signal and to said regularly varying signal, said gate means initiating said enabling signal.

14. A circuit as in claim 13, wherein said second circuit means further includes bistable means connected between said gate means and said enabling circuit, said bistable means being toggled to a first state by the beginning of the first cycle of said varying signal which occurs after said start signal, said bistable means forming said enabling signal when in said first state.

15. A circuit as in claim 14, wherein said bistable means is connected to be toggled to a second state by a start signal.

16. A circuit as in claim 13, wherein said second circuit further includes bistable means forming said connection between said start signal and said gate means, said bistable means being toggled to a first state by a start signal and thereby inhibiting said gate means, said bistable means being further connected to receive said varying signal and being toggled to a second state and thereby enabling said gate means.

17. A circuit as in claim 8, further including counting means, and gate means having its output connected to said counting means and two inputs respectively connected to said varying signal and to said output signal, said counting means counting the number of the other of said edges occurring within said time duration.

18. A circuit for counting to the nearest whole cycle the number of cycles of a regularly varying signal occurring during a base signal having a predetermined time duration, each of said cycles including a first point and a second point which is one-half cycle removed from said first point, said circuit comprising counter means adapted to receive said base signal and to initiate a counting operation in synchronism with one of said first points, and said counter means being connected to receive said varying signal and counting during said base signal the number of said second points.

19. A circuit for counting to the nearest whole cycle the number of cycles of a regularly varying signal occurring during a predetermined time, each of said cycles including a first point and a second point which is ½ cycle removed from said first point, said circuit comprising time base means for generating a base signal having a time duration equal to said predetermined time, means responsive to said varying signal and connected to said time base means for initiating a base signal in synchronism with one of said first points, and counter means connected to receive both said base signal and said varying signal for counting during said base signal the number of said second points.

20. A circuit for counting to the nearest whole cycle the number of cycles of a regularly varying signal occurring during a predetermined time, each of said cycles including a first point and a second point which is one-half cycle removed from said first point, said circuit comprising means responsive to said varying signal for generating a time base initiation signal coincident with said first point in a cycle of said varying signal, means for generating a base signal having a predetermined time duration in response to said initiation signal, and counter means connected to receive both said base signal and said varying signal for counting during said base signal the number of said second points.

* * * * *

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,710,262 Dated 1/9/73

Inventor(s) Peter F. Sorensen

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the first page of the patent, application No. "159,986" should read--194,986--; column 3, line 8, "of" should read --or--; column 5, line 58, "7 5/8" should read --7 1/8--.

Signed and sealed this 29th day of May 1973.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents