



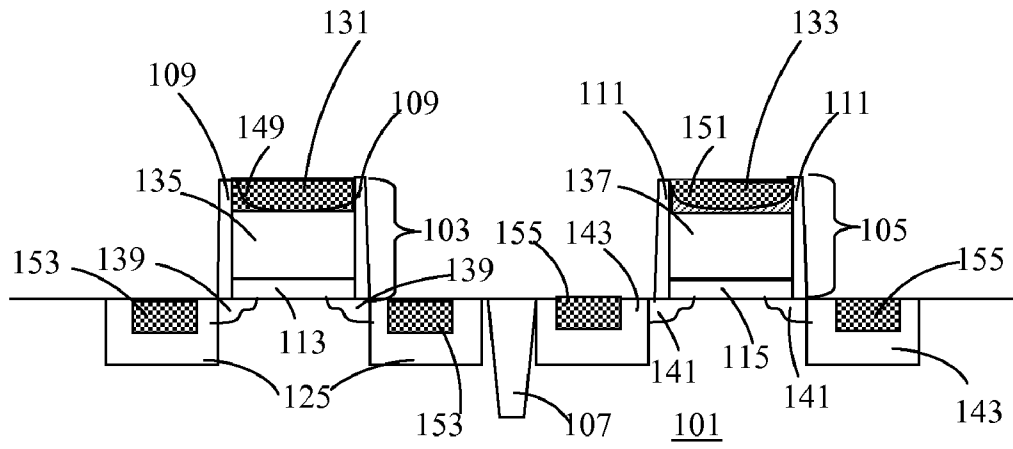
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(19) **United States**(12) **Patent Application Publication**
JAVORKA et al.(10) **Pub. No.: US 2014/0167110 A1**(43) **Pub. Date: Jun. 19, 2014**(54) **PARTIAL POLY AMORPHIZATION FOR
CHANNELING PREVENTION****Publication Classification**(71) Applicant: **GLOBAL FOUNDRIES Inc.**, Grand
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Cayman (KY)(21) Appl. No.: **14/188,022**(22) Filed: **Feb. 24, 2014****Related U.S. Application Data**(62) Division of application No. 13/190,566, filed on Jul.
26, 2011, now Pat. No. 8,704,229.(51) **Int. Cl.****H01L 29/78** (2006.01)**H01L 27/092** (2006.01)**H01L 29/49** (2006.01)(52) **U.S. Cl.**CPC **H01L 29/7848** (2013.01); **H01L 29/4933**
(2013.01); **H01L 27/092** (2013.01)USPC **257/192**

(57)

ABSTRACT

Semiconductor devices are formed without zipper defects or channeling and through-implantation and with different silicide thicknesses in the gates and source/drain regions. Embodiments include forming a gate on a substrate, forming a nitride cap on the gate, forming a source/drain region in the substrate on each side of the gate, forming a wet cap fill layer on the source/drain region on each side of the gate, removing the nitride cap from the gate, and forming an amorphized layer in a top portion of the gate. Embodiments include forming the amorphized layer by implanting low energy ions.



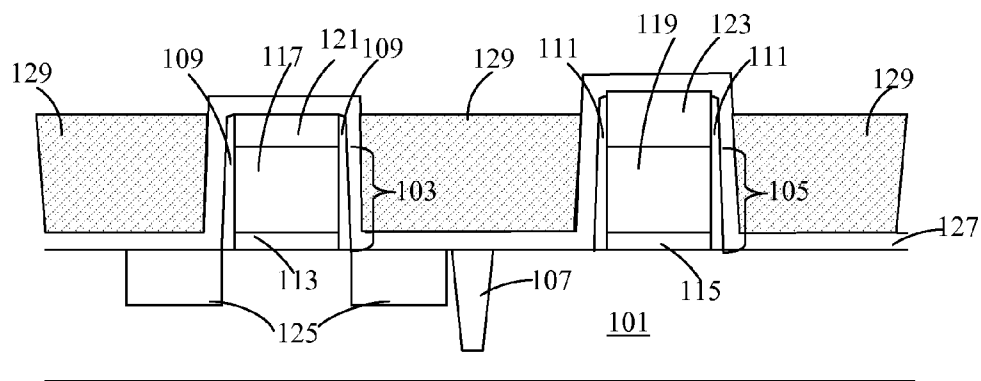


FIG. 1A

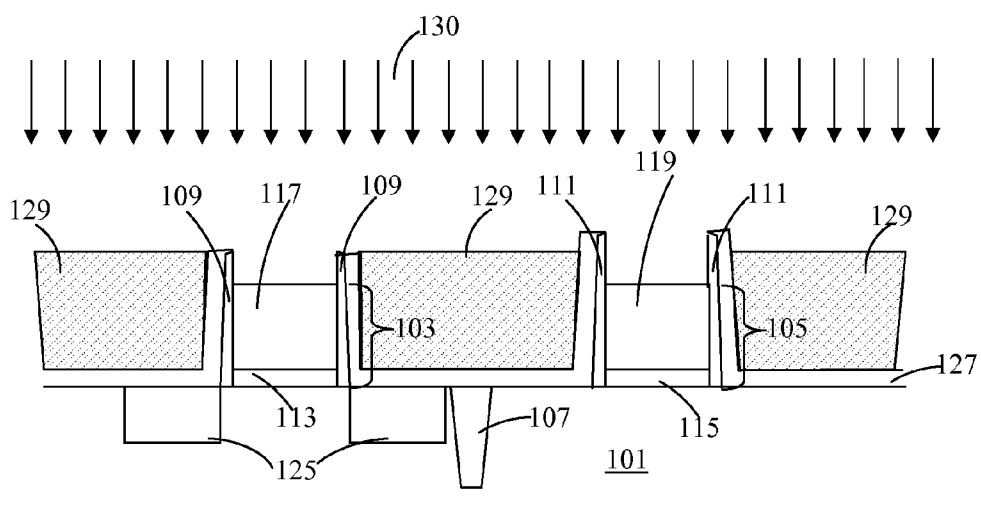


FIG. 1B

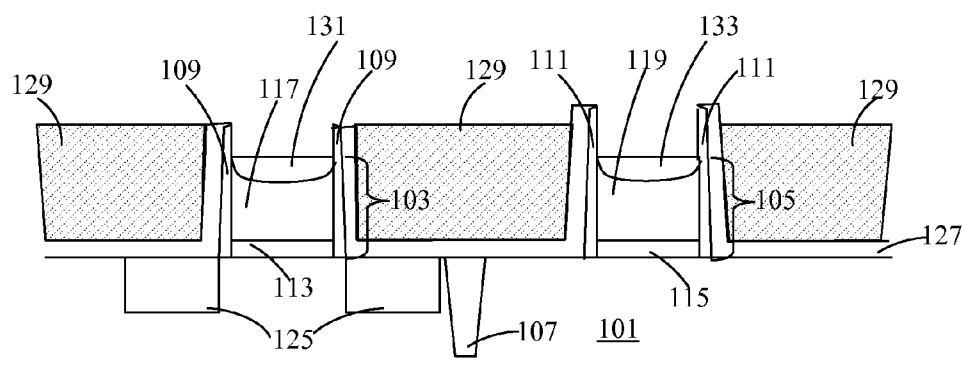


FIG. 1C

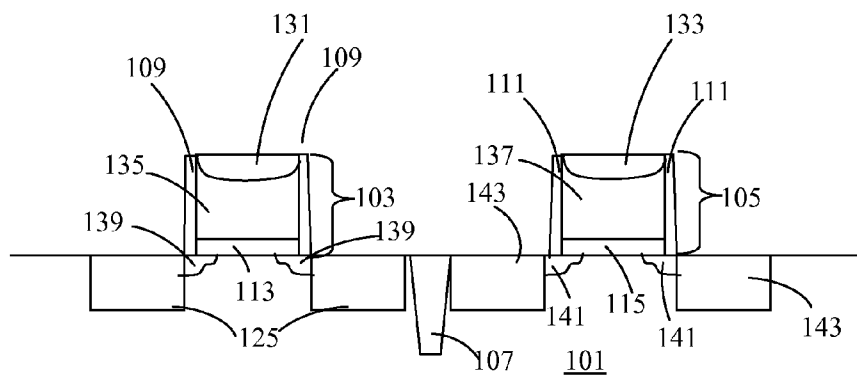


FIG. 1D

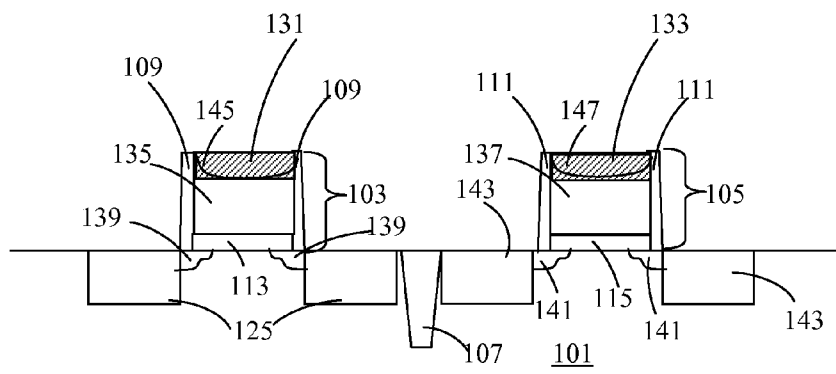


FIG. 1E

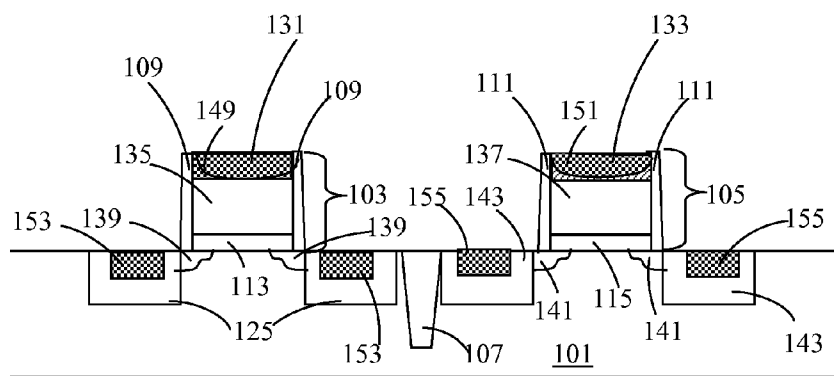


FIG. 1F

PARTIAL POLY AMORPHIZATION FOR CHANNELING PREVENTION

CROSS REFERENCED APPLICATION

[0001] This application is a division of U.S. application Ser. No. 13/190,566 filed Jul. 26, 2011, the entirety of which is incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to amorphization of semiconductor gates. The present disclosure is particularly applicable to semiconductor devices in 32 nanometer (nm) bulk and SOI, 22 nm bulk and SOI technology nodes, and beyond.

BACKGROUND

[0003] Currently, polycrystalline silicon having a thickness of 500 angstroms (Å) to 600 Å is being used for transistor gate electrodes. Since the gates are so thin, channeling and through-implantation during further implantation steps, for example, during halo/extension and source/drain regions implantation occur, further causing transistor leakage and lack of gate control. Although such through implantation may be blocked at the sides of the gate, the top of the gate remains vulnerable.

[0004] To reduce the channeling effect, a pre-amorphization implant (PAI) of the gate is employed. In standard gate amorphization, blanket PAI is performed after polycrystalline silicon deposition. This approach, as it is conducted prior to the gate etch, may lead to non-homogenous etching of the gate and may thus cause a bottle-shaped gate profile. Further, as the PAI is performed prior to halo/extension implantation, the amorphous extension regions re-crystallize after thermal anneal, which creates a so-called "zipper defect," thereby negatively affecting the transistor's performance and yield. Additionally, the amorphization implant may cause destruction/relaxation of embedded silicon germanium (eSiGe) source/drain regions, and, therefore, cannot be used for p-channel metal-oxide semiconductor (PMOS) transistors with eSiGe integration.

[0005] In addition, silicidation of gates and of source/drain regions are typically performed simultaneously such that the resulting silicides have the same thicknesses. However, for performance reasons it is beneficial for the gate silicide to extend closer to the gate dielectric, and for the silicide in the source/drain regions to be shallower. Current technology lacks sufficient control over the volume of silicide in the gates with respect to the volume of silicide in the source/drain regions.

[0006] A need therefore exists for methodology enabling amorphization of gates, after the gate etch, while protecting the surrounding areas and for independent silicidation of gates and source/drain regions, and the resulting devices.

SUMMARY

[0007] An aspect of the present disclosure is a method of fabricating a semiconductor device, by forming a wet gap fill layer prior to polycrystalline silicon amorphization, thereby protecting the gate's surrounding areas from implants during amorphization.

[0008] Another aspect of the present disclosure is a semiconductor device including a silicide layer in the gate having a greater thickness than the thickness of a silicide layer in the source/drain regions.

[0009] Additional aspects and other features of the present disclosure will be set forth in the description which follows and in part will be apparent to those having ordinary skill in the art upon examination of the following or may be learned from the practice of the present disclosure. The advantages of the present disclosure may be realized and obtained as particularly pointed out in the appended claims.

[0010] According to the present disclosure, some technical effects may be achieved in part by a method comprising: forming a gate on a substrate; forming a nitride cap on the gate; forming a source/drain region in the substrate on each side of the gate; forming a wet gap fill layer on the source/drain region on each side of the gate; removing the nitride cap from the gate; and forming an amorphized layer in a top portion of the gate.

[0011] Aspects of the present disclosure include forming the amorphized layer by implanting low energy ions in the gate. Further aspects include forming a liner on the nitride cap, on the sides of the gate, and on the source/drain region on each side of the gate, prior to forming the wet gap fill layer; and removing the liner from the nitride cap subsequent to forming the wet gap fill layer. Other aspects include removing the wet gap fill layer and the remaining liner, subsequent to implanting the low energy ions in the gate. Another aspect includes implanting germanium (Ge) or xenon (Xe) as the low energy ions. Further aspects include implanting Ge ions with an energy of 15 kiloelectron volts (keV) to 20 keV or Xe ions with an energy of 30 keV to 35 keV. Other aspects include implanting Ge or Xe ions in the upper $\frac{1}{3}$ portion of the gate. Another aspect includes implanting Ge or Xe ions in the upper 100 Å to 200 Å of the gate. Further aspects include forming the wet gap fill layer of an organic planarizing layer (OPL) and forming the liner of an oxide. Other aspects include implanting a silicide promoter in the amorphized layer. Another aspect includes implanting a first silicide promoter in the gate prior to implanting Ge or Xe ions in the gate and a second silicide promoter in each source/drain region, the first silicide promoter having higher energy than the second silicide promoter. Further aspects include implanting a silicide promoter in the gate at a first energy; thermally diffusing the silicide promoter toward the substrate; and implanting each source/drain region with a silicide promoter at a second energy less than the first energy. Other aspects include forming halo/extensions regions in the substrate on each side of the gate subsequent to forming the amorphized layer.

[0012] Another aspect of the present disclosure is a device including: a substrate, a gate formed on the substrate, the gate including a polycrystalline silicon layer formed in the lower two thirds of the gate; a source/drain region in the substrate on each side of the gate; a first silicide formed in the upper one third of the gate; and a second silicide on each source/drain region, wherein the first silicide has a thickness greater than the second silicide.

[0013] Aspects include a device having a polycrystalline silicon layer with a thickness of 100 Å to 200 Å. Other aspects include a device wherein the thickness of the first silicide is 20% to 30% greater than the thickness of the second silicide.

[0014] Another aspect of the present disclosure is a method including: forming a polysilicon gate on a substrate; forming

a nitride cap on the gate; forming an embedded silicon germanium (eSiGe) source/drain region in the substrate on each side of the gate; forming an oxide liner on the nitride cap on each side of the gate, and on each source/drain region; forming an organic planarizing wet gap fill layer on the oxide liner on each side of the gate to a thickness greater than a thickness of the gate; removing the oxide liner from the nitride cap; removing the nitride cap from the gate; implanting Ge ions with the energy of 15 keV to 20 keV or Xe ions with the energy of 30 keV to 35 keV in the upper $\frac{1}{3}$ portion of the gate to amorphize the upper portion of the gate; removing the organic planarizing wet gap fill layer and remaining oxide liner; forming halo/extension regions in the substrate on each side of the gate; and forming a first silicide on the gate and a second silicide on each source/drain region, wherein the first silicide has a thickness greater than a thickness of the second silicide.

[0015] Aspects include forming the first silicide by implanting a silicide promoter in the amorphized portion of the gate. Further aspects include implanting a first silicide promoter in the gate prior to implanting the Ge or Xe ions in the gate and a second silicide promoter in each source/drain region, the first silicide promoter having a higher energy than the second silicide promoter. Another aspect includes implanting a silicide promoter in the gate at a first energy, thermally diffusing the silicide promoter toward the substrate, and implanting each source/drain region with a silicide promoter at a second energy less than the first energy.

[0016] Additional aspects and technical effects of the present disclosure will become readily apparent to those skilled in the art from the following detailed description wherein embodiments of the present disclosure are described simply by way of illustration of the best mode contemplated to carry out the present disclosure. As will be realized, the present disclosure is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, all without departing from the present disclosure. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The present disclosure is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawing and in which like reference numerals refer to similar elements and in which:

[0018] FIGS. 1A Through 1F schematically illustrate a process flow for a semiconductor device, in accordance with an exemplary embodiment.

DETAILED DESCRIPTION

[0019] In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of exemplary embodiments. It should be apparent, however, that exemplary embodiments may be practiced without these specific details or with an equivalent arrangement. In other instances, well-known structures and devices are shown in block diagram form in order to avoid unnecessarily obscuring exemplary embodiments. In addition, unless otherwise indicated, all numbers expressing quantities, ratios, and numerical properties of ingredients, reaction conditions, and so forth used in

the specification and claims are to be understood as being modified in all instances by the term “about.”

[0020] The present disclosure addresses and solves the current problems of non-homogenous etching of the gate, formation of a zipper defect in extension regions, destruction/relaxation of eSiGe source/drain regions in PMOS transistors, and channeling and through-implantation during further implantation steps, attendant upon blanket PAI after polycrystalline silicon deposition for semiconductor gates. In accordance with embodiments of the present disclosure, the gates are etched prior to amorphization and a wet gap fill layer around the gates enables amorphization of only the gates, thereby avoiding the “zipper defect,” destruction/relaxation of PMOS eSiGe source/drain regions, and non-homogenous etching of the gate, as well as channeling and through-implantation during further implantation steps. Amorphization of the top portion of the gate can be used to define the volume of the modified material in the gate that is different from the volume of the material in the source/drain regions, for example, to control the relative silicide thicknesses in the gate and in the source/drain regions.

[0021] Methodology in accordance with embodiments of the present disclosure includes forming a gate on a substrate, forming a nitride cap on the gate, forming a source/drain region in the substrate on each side of the gate, forming a wet gap fill layer on the source/drain region on each side of the gate, removing the nitride cap from the gate, and forming an amorphized layer in a top portion of the gate.

[0022] Still other aspects, features, and technical effects will be readily apparent to those skilled in this art from the following detailed description, wherein preferred embodiments are shown and described, simply by way of illustration of the best mode contemplated. The disclosure is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

[0023] FIGS. 1A through 1F schematically illustrate a process flow for the amorphization of polycrystalline silicon in a gate, and further, a formation in the gate of a silicide layer of a controlled thickness, in accordance with an exemplary embodiment. Adverting to FIG. 1A, gates **103** and **105**, of a p-type and an n-type transistor, respectively, are formed by conventional methods on a substrate **101**. Shallow trench isolation (STI) region **107** is formed in the substrate, to electrically isolate the p-type transistor from the n-type transistor. After gates **103** and **105** are etched, differential spacers **109** and **111** are formed on both sides of gates **103** and **105**, respectively. Spacers may comprise nitride, for example silicon nitride (SiN), and are formed by conventional methods to a width of 30 Å to 200 Å.

[0024] Gates **103** and **105** may include gate dielectric layers **113** and **115**, respectively, at the gate to substrate interface. Gate dielectric layers **113** and **115** may include an oxide, for example hafnium oxide. Gates **103** and **105** may further include polycrystalline silicon layers **117** and **119**, respectively formed on dielectric layers **113** and **115**, to a thickness of 500 Å to 600 Å. Nitride caps **121** and **123**, for example of SiN, are formed on top of polycrystalline silicon layers **117** and **119**, respectively. Source/drain regions **125**, which may include eSiGe, are formed in the substrate on each side of gate **103**, by conventional methods. A sacrificial liner **127** is formed on nitride caps **121** and **123**, on each side of gates **103** and **105**, and on source/drain regions **125**. Liner **127** may be

formed of an oxide, for example silicon oxide (SiO_2), and may be formed by thermal oxidation to the thickness of 10 Å to 50 Å. A wet gap fill layer 129 is formed on liner 127, on each side of gates 103 and 105, to a thickness that is greater than the thickness of polycrystalline silicon layers 117 and 119, for example, 400 Å to 600 Å. Wet gap fill layer 129 may be an organic planarizing layer, and may be formed by photo-sensitive organic polymer.

[0025] As illustrated in FIG. 1B, gates 103 and 105 are exposed by removal of liner 127 by, for example, polishing, e.g., chemical mechanical polishing (CMP), followed by removal of nitride caps 121 and 123, for example by etching, e.g., using hot phosphoric acid (H_3PO_4), or hydrofluoric acid (HF). Low energy ions 130 are implanted in gates 103 and 105 to amorphize the upper portion of polycrystalline silicon layers 117 and 119, respectively. Ions 130 may be, for example, germanium (Ge) or xenon (Xe). Ge implantation energy may be 15 keV to 20 keV, while Xe implantation energy may be 30 keV to 35 keV.

[0026] Adverting to FIG. 1C, amorphized layers 131 and 133 are illustrated, having a thickness that is one third the thickness of original polycrystalline silicon layers 117 and 119, respectively. The remaining polycrystalline silicon layers 135 and 137 have a thickness that is, for example, 300 Å to 500 Å, e.g., 400 Å.

[0027] Wet gap fill layer 129 and remaining liner 127 are then removed, as illustrated in FIG. 1D. This may be performed by resist strip followed by HF etch. Halo/extension regions 139 and 141 may then be formed in substrate 101 on each side of gates 103 and 105, respectively, by arsenic (As) or boron (B) implantation. In addition, source/drain regions 143 may be formed on each side of gate 105, for example by implantation of As or B. Amorphized layers 131 and 133 prevent channeling and through-implantation during the halo/extension and source/drain implantations.

[0028] Amorphized layers 131 and 133 may also be used to control the volume of material in gates 103 and 105 that becomes silicided, to form a silicide in the gates to a different thickness than a silicide in the source/drain regions, as the gates benefit from a thicker silicide which extends closer to the dielectric layer, while it is beneficial for silicide in source/drain regions to be shallower, with less lateral spread under the gates. To accomplish silicidation, amorphized layers 131 and 133 may be implanted with a silicide promoter, for example selenium (Se) or sulfur (S), as illustrated in FIG. 1E, forming silicide promoter implanted layers 145 and 147. A silicide promoter may likewise be introduced into source/drain regions 125 and 143 (not shown for illustrative convenience). Alternatively, the silicide promoter may be implanted in gates 103 and 105 after gate etch and prior to implanting Ge or Xe ions in gates 103 and 105, with a higher energy than the silicide promoter implanted in source/drain regions 125 and 143. Gates 103 and 105 may, for example, be implanted with a silicide promoter with the energy of 10 keV to 50 keV, while source/drain regions 125 and 143 may be implanted with a silicide promoter with an energy of 2 keV to 20 keV. As another alternative, gates 103 and 105 may be implanted with a silicide promoter which is then thermally diffused (for example at temperatures of 600° C. to 800° C.) in the direction of substrate 101 until it reaches a required depth. Subsequent source/drain implants may then be at a lower energy, for example 2 keV to 10 keV.

[0029] A metal layer, e.g., nickel or nickel alloy, is formed over gates 103 and 105 and source/drain regions 125 and 143

and is annealed to form the gate and source/drain silicides. FIG. 1F illustrates formation of gate silicides 149 and 151 in gates 103 and 105, respectively, and source/drain silicides 153 and 155 in source/drain regions 125 and 143, respectively. The thickness of gate silicides 149 and 151 is greater than the thickness of source/drain silicides, for example by 20% to 30%. Spacers 157 and 159 may be formed on both sides of gates 103 and 105, respectively, prior to silicide formation in source/drain regions 125 and 143.

[0030] The embodiments of the present disclosure can achieve several technical effects, including elimination of deformed bottle-shaped gates, prevention of the zipper defect in halo/extension regions, reduced destruction/relaxation of eSiGe source/drain regions in PMOS transistors, prevention of channeling and through-implantation during implantation of halo/extension regions and source/drain regions, thereby reducing transistor leakage and improving gate control, as well as independent control of the silicide volume in the gates and source/drain regions. The present disclosure enjoys industrial applicability in any of various types of highly integrated semiconductor technologies, particularly in 32 nm bulk, 32 nm SOI, 22 nm bulk, and 22 nm SOI technology nodes and beyond.

[0031] In the preceding description, the present disclosure is described with reference to specifically exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present disclosure, as set forth in the claims. The specification and drawings are, accordingly, to be regarded as illustrative and not as restrictive. It is understood that the present disclosure is capable of using various other combinations and embodiments and is capable of any changes or modifications within the scope of the inventive concept as expressed herein.

What is claimed is:

1. A device comprising:

- a substrate,
- a gate formed on the substrate, the gate comprising a polycrystalline silicon layer formed in a lower two thirds of the gate; and
- a source/drain region in the substrate on each side of the gate;
- a first silicide formed in an upper one third of the gate; and
- a second silicide on each source/drain region, wherein the first silicide has a thickness greater than the second silicide.

2. The device according to claim 1, wherein the upper one third of the gate comprises amorphized silicon.

3. The device according to claim 1, wherein a thickness of the polycrystalline silicon layer is 300 Å to 500 Å.

4. The device according to claim 1, wherein the thickness of the first silicide is 20% to 30% greater than the thickness of the second silicide.

5. The device according to claim 1, further comprising halo/extension regions in the substrate on each side of the gate.

6. The device according to claim 1, further comprising spacers on each side of the gate.

7. The device according to claim 1, wherein the source/drain regions ions implanted in the substrate.

8. The device according to claim 1, wherein the source/drain regions comprise embedded silicon germanium (eSiGe) source/drain regions in the substrate.

9. A device comprising:

a substrate,

at least one gate formed on the substrate, the gate comprising a polycrystalline silicon layer having a thickness of 300 Å to 500 Å formed in a lower two thirds of each gate and an amorphized silicon layer formed in an upper one third of each gate; and

a source/drain region in the substrate on each side of each gate;

a first silicide formed in the amorphized silicon layer of each gate; and

a second silicide on each source/drain region, wherein the first silicide has a thickness greater than the second silicide.

10. The device according to claim **9**, comprising two gates wherein a source/drain region on each side of the first gate comprises embedded silicon germanium (eSiGe) source/drain regions in the substrate and a source/drain region on each side of the second gate comprises ions implanted in the substrate.

11. The device according to claim **9**, wherein the thickness of the first silicide is 20% to 30% greater than the thickness of the second silicide.

12. The device according to claim **9**, further comprising halo/extension regions in the substrate on each side of each gate.

13. The device according to claim **9**, further comprising spacers on both sides of each gate.

14. A device comprising:

a substrate,

an n-type and a p-type gate formed on the substrate, each gate comprising a polycrystalline silicon layer formed in a lower two thirds of the gate;

a shallow trench isolation (STI) region formed in the substrate between the n-type and the p-type gates; and

an embedded silicon germanium (eSiGe) source/drain region in the substrate on each side of the p-type gate;

an ion implanted source/drain region in the substrate on each side of the n-type gate;

a first silicide formed in an upper one third of each of the p-type and n-type gates; and

a second silicide on each eSiGe and each ion implanted source/drain region, wherein the first silicide has a thickness greater than the second silicide.

15. The device according to claim **14**, wherein the upper one third of each of the p-type and n-type gates comprises amorphized silicon.

16. The device according to claim **14**, wherein a thickness of the polycrystalline silicon layer is 300 Å to 500 Å.

17. The device according to claim **14**, wherein the thickness of the first silicide is 20% to 30% greater than the thickness of the second silicide.

18. The device according to claim **14**, wherein the ion implanted source/drain regions comprise arsenic (As) or boron (B) ions implanted in the substrate.

19. The device according to claim **14**, further comprising halo/extension regions in the substrate on each side of each of the p-type and n-type gates.

20. The device according to claim **14**, further comprising spacers on both sides of each of the p-type and n-type gates.

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