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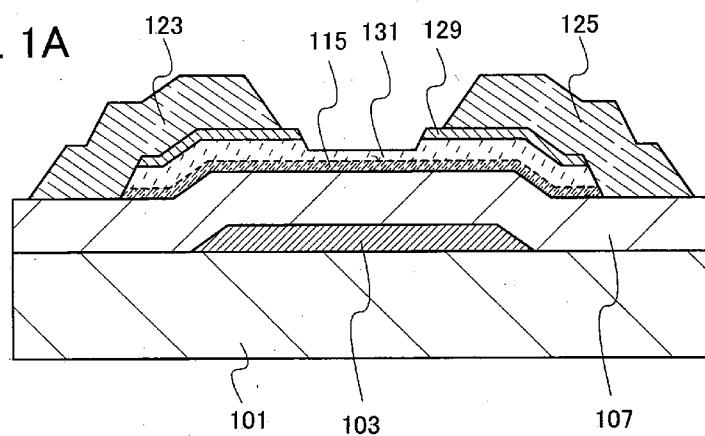
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(54) Title: THIN FILM TRANSISTOR, SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE

FIG. 1A



(57) Abstract: A thin film transistor includes, as a buffer layer, an amorphous semiconductor layer having nitrogen or an NH group between a gate insulating layer and source and drain regions and at least on the source and drain regions side. As compared to a thin film transistor in which an amorphous semiconductor is included in a channel formation region, on-current of a thin film transistor can be increased. In addition, as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region, off-current of a thin film transistor can be reduced.

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## DESCRIPTION

### THIN FILM TRANSISTOR, SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE

5

#### TECHNICAL FIELD

[0001]

The present invention relates to a thin film transistor and a method for manufacturing the thin film transistor, and a semiconductor device and a display device  
10 using the thin film transistor.

#### BACKGROUND ART

[0002]

As a kind of field-effect transistor, a thin-film transistor in which a channel  
15 region is formed in a semiconductor layer formed over a substrate having an insulating surface is known. Techniques in which amorphous silicon, microcrystalline silicon, or polycrystalline silicon is used for the semiconductor layer used in the thin-film transistor have been disclosed (see Patent Documents 1 to 5). A typical application of  
20 a thin-film transistor is a liquid crystal television device, and the thin film transistor has been put to the practical use as a switching transistor for each pixel included in a display screen.

[Reference]

[Patent Document]

[0003]

[Patent Document 1] Japanese Published Patent Application No. 2001-053283

[Patent Document 2] Japanese Published Patent Application No. Hei05-129608

[Patent Document 3] Japanese Published Patent Application No. 2005-049832

[Patent Document 4] Japanese Published Patent Application No. Hei07-131030

5 [Patent Document 5] Japanese Published Patent Application No. 2005-191546

## DISCLOSURE OF INVENTION

[0004]

A thin film transistor in which a channel is formed using an amorphous silicon layer has problems such as low field-effect mobility and low on-current. On the other hand, a thin film transistor in which a channel is formed using a microcrystalline silicon layer has a problem in that, whereas the field-effect mobility is higher than that of the thin film transistor in which a channel is formed using an amorphous silicon layer, the off-current is high, and thus sufficient switching characteristics cannot be obtained.

15 [0005]

The thin-film transistor in which a polycrystalline silicon layer is used for the channel formation region has characteristics in that the field-effect mobility is far higher than those of the above-described two kinds of thin-film transistors and high on-current can be obtained. Because of such characteristics, this thin film transistor can be used 20 not only as a switching transistor provided in a pixel but also in a driver circuit for which high-speed operation is required.

[0006]

However, a thin film transistor formed using a polycrystalline silicon layer requires a crystallization step for a semiconductor layer and has a problem of higher

manufacturing cost as compared to a thin film transistor formed using an amorphous silicon layer. For example, with laser annealing technique involved in the process for manufacturing a polycrystalline silicon layer has a problem in that large liquid crystal panels cannot be produced efficiently because the laser beam irradiation area is small.

5 [0007]

A mother glass for manufacturing display panels has been grown in size from year to year as follows: the 3rd generation (550 mm × 650 mm), the 3.5th generation (600 mm × 720 mm or 620 mm × 750 mm), the 4th generation (680 mm × 880 mm or 730 mm × 920 mm), the 5th generation (1100 mm × 1300 mm), the 6th generation 10 (1500 mm × 1850 mm), the 7th generation (1870 mm × 2200 mm), and the 8th generation (2200 mm × 2400 mm). From now on, the size of mother glasses is expected to grow to the 9th generation (2400 mm × 2800 mm or 2450 mm × 3050 mm) and the 10th generation (2950 mm × 3400 mm). Increase in size of mother glasses is based on the minimum-cost design concept.

15 [0008]

However, the technique that thin-film transistors capable of high-speed operation can be manufactured over a large-area mother glass such as a 10th generation (2950 mm × 3400 mm) mother glass with high productivity has not been established yet, which is a problem in industry.

20 [0009]

In view of the foregoing, it is an object of the present invention to solve the aforementioned problems related to on-current and off-current of a thin film transistor. It is another object of the present invention to provide a thin film transistor capable of high-speed operation.

## [0010]

In the present invention, a thin film transistor includes, as a buffer layer, an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group between a gate insulating layer and source and drain regions and at least on the source and drain regions side. The buffer layer is provided on a so-called back channel side. In addition, in the present invention, in a thin film transistor, an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group is formed between a gate insulating layer and source and drain regions.

## [0011]

An amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group is formed using, as a reactive gas, a gas in which a semiconductor source gas (e.g. a silicon hydride gas, a silicon fluoride gas, a silicon chloride gas, a germanium hydride gas, a germanium fluoride gas, or a germanium chloride gas) and a dilution gas are mixed at a mixture ratio at which an amorphous semiconductor can be generated. The reactive gas is introduced into an ultrahigh vacuum reaction chamber where an oxygen concentration is reduced, and a predetermined pressure is maintained therein to generate glow discharge plasma. Accordingly, a film is deposited over a substrate which is placed in the reaction chamber. At the early stage of deposition or during deposition, a nitrogen element and a hydrogen element, or an NH group are/is included in the reaction chamber to start deposition of a film, and dangling bonds in the film are cross-linked with an NH group, whereby an amorphous semiconductor layer in which the defect levels are reduced is formed. Alternatively, at the early stage of deposition or during deposition, a nitrogen element and a hydrogen element or an NH<sub>2</sub> group are/is included in the reaction chamber to start deposition of a film, and dangling bonds in the

film are terminated with an NH group, whereby an amorphous semiconductor layer in which the defect levels are reduced is formed.

[0012]

The concentration of nitrogen contained in the amorphous semiconductor layer 5 is preferably a concentration at which semiconductor characteristics are kept, the defect levels are reduced, and carrier mobility is increased.

[0013]

By including nitrogen, typically an NH group in a semiconductor layer and cross-linking dangling bonds of Si atoms with nitrogen, typically, an NH group, the 10 bonding becomes a carrier path at the crystal grain boundary, whereby carrier transfer is facilitated. Accordingly, in a thin film transistor, an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group is provided as a buffer layer between a channel formation region and source and drain regions, whereby the resistance in a thickness direction of the buffer layer when a voltage is applied to the source region or the drain 15 region can be reduced. In particular, an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group is provided as a buffer layer directly under the source and drain regions, whereby on-current can be increased. Therefore, as compared to a thin film transistor in which an amorphous semiconductor layer is provided between a gate insulating layer and source and drain regions, on-current of a thin film transistor can be 20 increased.

[0014]

Dangling bonds in a semiconductor layer are defect levels. However, dangling bonds of a semiconductor element are cross-linked with an NH group, whereby the defect levels are eliminated. Further, the dangling bonds of the

semiconductor element are terminated with an NH<sub>2</sub> group, whereby the defect levels are eliminated. An amorphous semiconductor layer has short-range order and no constant repeated patterns like a crystal lattice in a structure. Therefore, many dangling bonds are included, and the dangling bonds become defect levels where carriers are trapped.

5     However, the dangling bonds in the amorphous semiconductor layer are cross-linked with an NH group, whereby the defect levels can be eliminated. Further, the dangling bonds in the amorphous semiconductor layer are terminated with an NH<sub>2</sub> group, whereby the defect levels in the amorphous semiconductor layer can be reduced. When there are defect levels, at the defect levels, electrons and holes are generated and 10    recombined by thermal excitation and Shockley-Read-Hall current flows. However, when defect levels are eliminated, the current can be reduced. Accordingly, an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group is provided as a buffer layer in a region where off-current flows, whereby off-current can be reduced as compared to a thin film transistor in which a microcrystalline semiconductor is provided 15    between a gate insulating layer and source and drain regions.

[0015]

Accordingly, on-current and field-effect mobility can be increased as compared to a thin film transistor in which an amorphous semiconductor layer is provided between a gate insulating layer and source and drain regions, and off-current can be 20    reduced as compared to a thin film transistor in which a microcrystalline semiconductor layer is provided between a gate insulating layer and source and drain regions.

[0016]

Note that the concentration of an impurity element in silicon which reduces the coordination number of silicon and generates dangling bonds, such as oxygen, is

reduced. That is, it is preferable that the oxygen concentration which is measured by secondary ion mass spectrometry be less than or equal to  $5 \times 10^{18} \text{ cm}^{-3}$ .

[0017]

Note that here, a concentration without mention of a measuring method is a concentration measured by secondary ion mass spectrometry.

[0018]

Note that on-current refers to current which flows between a source electrode and a drain electrode when a transistor is on. For example, in the case of an n-channel transistor, the on current refers to current which flows between the source electrode and the drain electrode when a gate voltage of the transistor is higher than a threshold voltage thereof.

[0019]

Further, off-state current is current which flows between a source electrode and a drain electrode when a transistor is off. For example, in the case of an n-channel transistor, the off-state current is current which flows between the source electrode and the drain electrode when a gate voltage of the transistor is lower than a threshold voltage thereof.

[0020]

According to the present invention, as compared to a thin film transistor in which an amorphous semiconductor is included in a channel formation region, on-current of a thin film transistor can be increased. In addition, as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region, off-current of a thin film transistor can be reduced.

## BRIEF DESCRIPTION OF DRAWINGS

[0021]

In the accompanying drawings:

FIGS. 1A and 1B are views illustrating an example of a thin film transistor

5 according to an embodiment of the present invention;

FIGS. 2A to 2C are views each illustrating a semiconductor layer included in a thin film transistor according to an embodiment of the present invention;

FIG. 3 is a view illustrating a semiconductor layer included in a thin film transistor according to an embodiment of the present invention;

10 FIG. 4 is a view illustrating a semiconductor layer included in a thin film transistor according to an embodiment of the present invention;

FIG. 5 is a view illustrating a semiconductor layer included in a thin film transistor according to an embodiment of the present invention;

15 FIG. 6 is a view illustrating a semiconductor layer included in a thin film transistor according to an embodiment of the present invention;

FIGS. 7A and 7B are views illustrating an example of a thin film transistor according to an embodiment of the present invention;

FIGS. 8A and 8B are views each illustrating a semiconductor layer included in a thin film transistor according to an embodiment of the present invention;

20 FIGS. 9A and 9B are views illustrating an example of a thin film transistor according to an embodiment of the present invention;

FIGS. 10A to 10C are views illustrating an example of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

FIGS. 11A to 11C are views illustrating an example of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

5 FIGS. 12A and 12B are views illustrating an example of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

FIGS. 13A and 13B are views illustrating an example of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

10 FIG. 14 is a view illustrating a device which can be applied to a method for manufacturing a thin film transistor according to an embodiment of the present invention;

15 FIG. 15 is a diagram showing an example of a timing chart of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

FIG. 16 is a diagram showing an example of a timing chart of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

20 FIG. 17 is a diagram showing an example of a timing chart of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

FIG. 18 is a diagram showing an example of a timing chart of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

FIG. 19 is a diagram showing an example of a timing chart of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

FIGS. 20A and 20B are views illustrating an example of a method for 5 manufacturing a thin film transistor according to an embodiment of the present invention;

FIGS. 21A to 21C are views illustrating an example of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

10 FIGS. 22A to 22C are views illustrating an example of a method for manufacturing a thin film transistor according to an embodiment of the present invention;

FIGS. 23A and 23B are views illustrating an example of a method for manufacturing a thin film transistor according to an embodiment of the present 15 invention;

FIGS. 24(A-1), 24(A-2), 24(B-1), and 24(B-2) are views showing multi-tone masks which can be applied to the present invention;

FIGS. 25A to 25C are views each illustrating an electronic device to which a thin film transistor according to an embodiment of the present invention can be applied;

20 FIGS. 26A to 26D are views each illustrating an electronic device to which a thin film transistor according to an embodiment of the present invention can be applied;

FIG. 27 is a view illustrating an electronic device to which a thin film transistor according to an embodiment of the present invention can be applied;

FIGS. 28A to 28C are views illustrating an electronic device to which a thin

film transistor according to an embodiment of the present invention can be applied; and

FIGS. 29A and 29B are views each illustrating a structure of a thin film transistor according to an embodiment of the present invention.

5

## BEST MODE FOR CARRYING OUT THE INVENTION

[0022]

Hereinafter, embodiments are described with reference to the drawings. Note that the present invention disclosed is not limited to the following description. It is easily understood by those skilled in the art that the mode and detail can be variously changed unless departing from the scope and spirit of the invention disclosed. Therefore, the invention should not be interpreted as being limited to the description of the embodiments to be given below. Note that as structures of the present invention are described with reference to the drawings, like portions are denoted by common reference numerals in different drawings. The same hatching pattern is applied to like portions, and the like portions are not especially denoted by reference numerals in some cases.

[0023]

(Embodiment 1)

In this embodiment, an example of a mode of a thin film transistor will be described with reference to the drawings.

[0024]

FIGS. 1A and 1B are cross-sectional views of a thin film transistor according to this embodiment. A thin film transistor illustrated in FIG. 1A includes a gate electrode layer 103 over a substrate 101; a gate insulating layer 107 which covers the gate

electrode layer 103; a semiconductor layer 115 which is provided over and in contact with the gate insulating layer 107 and serves as a channel formation region; a buffer layer 131 over the semiconductor layer 115; and source and drain regions 129 which are in contact with part of the buffer layer 131. In addition, the thin film transistor 5 includes a wiring layer 123 and a wiring layer 125 which are provided over and in contact with the source and drain regions 129. The wiring layer 123 and the wiring layer 125 form a source electrode and a drain electrode. Further, each layer has been patterned into a desired shape. Here, the buffer layer 131 is formed using an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group (hereinafter, 10 referred to as an amorphous semiconductor layer having an NH group).

[0025]

As illustrated in FIG. 1B, in the semiconductor layer 115, a region 171 which overlaps with the gate electrode layer 103 and is provided on the gate insulating layer 107 side serves as a channel. Further, in the buffer layer 131, a region 172 which is 15 provided on a side opposite to the gate insulating layer 107 and is not in contact with the source and drain regions 129 serves as a back channel. Further, in the buffer layer 131, a region 173 on a side which is in contact with the drain region becomes a depletion layer. Further, a region 174 where the buffer layer 131 and the source region or the drain region are in contact with each other is a bond region.

20 [0026]

As the substrate 101, in addition to a glass substrate and a ceramic substrate, a plastic substrate or the like with heat resistance which can withstand a process temperature in this manufacturing process can be used. In the case where a substrate does not need a light-transmitting property, a substrate obtained by providing an

insulating layer on a surface of a substrate of a metal such as a stainless steel alloy may be used. As a glass substrate, an alkali-free glass substrate formed using barium borosilicate glass, aluminoborosilicate glass, aluminosilicate glass, or the like may be used.

5 [0027]

The gate electrode layer 103 can be formed as a single layer or a stacked layer using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium or an alloy material which includes any of these materials as a main component. Alternatively, a semiconductor layer typified by 10 polycrystalline silicon doped with an impurity element such as phosphorus, or an AgPdCu alloy may be used.

[0028]

For example, as a two-layer structure of the gate electrode layer 103, a two-layer structure in which a molybdenum layer is stacked over an aluminum layer, a 15 two-layer structure in which a molybdenum layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer or a tantalum nitride layer is stacked over a copper layer, or a two-layer structure in which a titanium nitride layer and a molybdenum layer are stacked is preferable. As a three-layer structure, a structure in which a tungsten layer or a tungsten nitride layer, a layer of an alloy of 20 aluminum and silicon or an alloy of aluminum and titanium, and titanium nitride or a titanium layer are stacked is preferable. When a metal layer serving as a barrier layer is stacked over a layer with low electric resistance, electric resistance of the gate electrode layer can be reduced and a metal element from the metal layer can be prevented from diffusing into the semiconductor layer.

[0029]

The gate insulating layer 107 can be formed as a single layer or a stacked layer of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, or a silicon nitride oxide layer by a CVD method, a sputtering method, or the like. Further, the 5 gate insulating layer 107 is formed using a silicon oxynitride layer, whereby, in the case of forming a microcrystalline semiconductor layer as the semiconductor layer 115, fluctuation in the threshold voltage of the thin film transistor can be suppressed.

[0030]

Note that in this specification, silicon oxynitride contains more oxygen than 10 nitrogen, and in the case where measurements are conducted using Rutherford backscattering spectrometry (RBS) and hydrogen forward scattering (HFS), silicon oxynitride preferably contains oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from 50 to 70 at.%, 0.5 to 15 at.%, 25 to 35 at.%, and 0.1 to 10 at.%, respectively. Further, silicon nitride oxide contains more nitrogen than oxygen, and in 15 the case where measurements are conducted using RBS and HFS, silicon nitride oxide preferably contains oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from 5 to 30 at.%, 20 to 55 at.%, 25 to 35 at.%, and 10 to 30 at.%, respectively. Note that percentages of nitrogen, oxygen, silicon, and hydrogen fall within the ranges given 20 above, where the total number of atoms contained in the silicon oxynitride or the silicon nitride oxide is defined as 100 at.%.

[0031]

The semiconductor layer 115 is formed using a microcrystalline semiconductor layer, an amorphous semiconductor layer, or an amorphous semiconductor layer having an NH group. As a microcrystalline semiconductor layer, an amorphous

semiconductor layer, or an amorphous semiconductor layer having an NH group, silicon, germanium, or silicon germanium can be used. Note that phosphorus imparting n-type conductivity or boron imparting p-type conductivity may be added into the semiconductor layer 115. A metal element which reacts with silicon to form a silicide, 5 such as titanium, zirconium, hafnium, vanadium, niobium, tantalum, chromium, molybdenum, tungsten, cobalt, nickel, or platinum, may be added into the semiconductor layer 115. Phosphorus imparting n-type conductivity, boron imparting p-type conductivity, a metal element which reacts with silicon to form a silicide, or the like is added into the semiconductor layer 115, whereby the carrier mobility of the 10 semiconductor layer can be increased. Thus, the field-effect mobility of the thin film transistor in which the semiconductor layer serves as a channel formation region can be increased.

[0032]

A microcrystalline semiconductor layer is a layer including a semiconductor 15 having an intermediate structure between amorphous and crystalline (including single crystal and polycrystal) structures. A microcrystalline semiconductor is a semiconductor having a third state that is stable in terms of free energy and a crystalline semiconductor having short-range order and lattice distortion, in which columnar or needle-like crystals 115a having a crystal grain size of greater than or equal to 2 nm and 20 less than or equal to 200 nm, preferably greater than or equal to 10 nm and less than or equal to 80 nm, more preferably greater than or equal to 20 nm and less than or equal to 50 nm have grown in a direction normal to the substrate surface. Therefore, a crystal grain boundary 115b is formed at the interface between the columnar or needle-like crystals 115a. Further, an amorphous structure 115c exists between the columnar or

needle-like crystals 115a (see FIG. 2A).

[0033]

Further, the concentrations of oxygen and nitrogen included in the microcrystalline semiconductor layer, which are measured by secondary ion mass spectrometry, are preferably less than  $1 \times 10^{18}$  atoms/cm<sup>3</sup>.

[0034]

Alternatively, in the microcrystalline semiconductor layer, an amorphous layer 115d may be formed at an interface with the gate insulating layer 107 and the columnar or needle-like crystals 115a may be formed thereover (see FIG. 2B).

10 [0035]

Further alternatively, as illustrated in FIG. 2C, the columnar or needle-like crystals 115a may be formed on a surface of the gate insulating layer 107 without an amorphous structure at an interface between the gate insulating layer 107 and the semiconductor layer 115. When an amorphous structure does not exist at the interface 15 between the gate insulating layer 107 and the semiconductor layer 115 as described above, carriers flow in the columnar or needle-like crystals 115a with high crystallinity; therefore, on-current and field-effect mobility of the thin film transistor can be increased.

[0036]

20 Microcrystalline silicon, which is a typical example of a microcrystalline semiconductor, has a Raman spectrum which is shifted to a lower wavenumber side than 520 cm<sup>-1</sup> that represents single crystal silicon. That is, the peak of the Raman spectrum of the microcrystalline silicon exists between 520 cm<sup>-1</sup> which represents single crystal silicon and 480 cm<sup>-1</sup> which represents amorphous silicon. The semiconductor

includes hydrogen or halogen of at least 1 at.% to terminate a dangling bond. Moreover, a rare gas element such as helium, argon, krypton, or neon may be contained to further promote lattice distortion, so that stability is enhanced and a favorable microcrystalline semiconductor layer can be obtained. Such a microcrystalline 5 semiconductor layer is disclosed in, for example, United States Patent No. 4,409,134.

[0037]

Here, a structure of the buffer layer 131 which is one of main features of the present invention will be described. As the buffer layer 131, an amorphous semiconductor layer having an NH group with which dangling bonds of a Si atom are 10 cross-linked is used. Alternatively, an amorphous semiconductor layer having an NH<sub>2</sub> group with which dangling bonds of a Si atom are terminated is used. An amorphous semiconductor layer has no constant repeated patterns like a crystal lattice. Therefore, many dangling bonds are included and regions of the dangling bonds become defect levels, and thus the regions are portions where carriers are trapped, thereby reducing the 15 carrier mobility. However, in the buffer layer 131 of the present invention, the dangling bonds are cross-linked with an NH group, or dangling bonds of a Si atom are terminated with an NH<sub>2</sub> group, so that the number of dangling bonds is reduced. That is, defect levels in the buffer layer 131 are reduced. Further, dangling bonds are 20 cross-linked with an NH group, whereby the bond portion can be a carrier path, and thus carrier mobility is increased as compared to a conventional amorphous semiconductor layer. As a result, in the case of using the buffer layer of the present invention as a buffer layer of a thin film transistor, on-current and field-effect mobility of the thin film transistor can be increased and off-current thereof can be reduced.

[0038]

Note that “dangling bonds of a Si atom in an amorphous semiconductor layer are cross-linked with an NH group” means that different bonds of the NH group are used for bonds with different semiconductor elements in the amorphous semiconductor layer. Therefore, a first bond of a N atom is used for a bond with a H atom, a second bond of the N atom is used for a bond with a first semiconductor atom, and a third bond of the N atom is used for a bond with a second semiconductor atom. In addition, “dangling bonds of a Si atom in an amorphous semiconductor layer are terminated with an NH<sub>2</sub> group” means that an NH<sub>2</sub> group is bonded with the Si atom in the amorphous semiconductor layer. Therefore, the first and second different bonds of the N atom are used for bonds with its different H atoms and the third bond of the N atom is used for a bond with a Si atom.

[0039]

Note that as an impurity element which suppresses generation of crystal nuclei, oxygen and nitrogen can be given and an impurity element (e.g. nitrogen) in silicon which does not trap carriers is selected. On the other hand, the concentration of an impurity element (e.g. oxygen) which reduces the coordination number of silicon and generates dangling bonds is reduced. Therefore, it is preferable to reduce the oxygen concentration without reducing the nitrogen concentration. Specifically, it is preferable that the oxygen concentration which is measured by secondary ion mass spectrometry be less than or equal to  $5 \times 10^{18} \text{ cm}^{-3}$ .

[0040]

Further, it is preferable that the nitrogen concentration be a concentration at which an amorphous semiconductor layer maintains a semiconductor property, dangling bonds are reduced, and carrier mobility is increased. When the nitrogen concentration

is too high, a semiconductor property is lowered, resulting in high insulating property, and thus on-current is reduced. In addition, when the nitrogen concentration is too low, the carrier mobility is not increased and the defect levels are increased similarly to a conventional amorphous semiconductor layer.

5 [0041]

Next, a model will be described below in which carriers flow easily when a plurality of dangling bonds included in the amorphous semiconductor layer as described above are cross-linked with nitrogen, typically, an NH group.

[0042]

10 Here, simulation of LUMO (lowest unoccupied molecular orbital) which is a level contributing to n-type-carriers transfer (that is, the lowest level in a conduction band) is performed on each of amorphous silicon layers of a model (model 1) in which one pair of dangling bonds are cross-linked with an O atom 193 in a silicon layer having a defect 192 where dangling bonds of a Si atom are terminated with H atoms 191a as 15 illustrated in FIG. 3, and a model (model 2) in which one pair of dangling bonds are cross-linked with an NH group 194 in a silicon layer having a defect 192 where dangling bonds of a Si atom are terminated with H atoms 191a as illustrated in FIG. 4. As software for the simulation, first principle calculation software employing density 20 functional theory is used. Note that the NH group 194 indicates a nitrogen atom 195 and a hydrogen atom 191b in FIG. 4. Further, an intersection of lines indicates a silicon atom and the line indicates a bond or a dangling bond of the silicon atom. Further, in order to evaluate effectiveness of the oxygen atom and the NH group, the 25 dangling bonds other than the dangling bond cross-linked with the oxygen atom or the NH group are all terminated with the hydrogen atoms.

[0043]

FIG. 5 illustrates a calculation result obtained by using the model 1 and FIG. 6 illustrates a calculation result obtained by using the model 2.

[0044]

5 FIG. 5 illustrates a shape of a wave function in a region where the Si atoms are cross-linked with the O atom and in the periphery of the region. A region 196 and a region 197 indicate regions whose phases are positive and negative, respectively (or negative and positive, respectively) and whose absolute value are the same. FIG. 6 illustrates a shape of a wave function in a region where the Si atoms are cross-linked  
10 with the NH group and in the periphery of the region. A region 198 and a region 199 are regions whose phases are positive and negative respectively (or negative and positive, respectively) and whose absolute values are the same.

[0045]

15 FIG. 5 shows that in the case where the dangling bonds of the Si atom are cross-linked with the O atom, since regions which have the same absolute values and the same phases of a wave function (for example, regions 196a and 196b) are separated, carriers do not easily flow. That is, when the amorphous silicon layer includes oxygen, a bond which interrupts carrier transfer is formed, whereby the carrier mobility of the amorphous silicon layer is reduced.

20 [0046]

On the other hand, FIG. 6 shows that in the case where the dangling bonds of the Si atom are cross-linked with the NH group, since the region 198 which has the same absolute value and the same phase of the wave function among different Si atoms is connected to both the adjacent dangling bonds, carriers are likely to flow. That is,

when the amorphous silicon layer includes the NH group, a bond which facilitates the carrier transfer in the dangling bonds is formed, whereby the carrier mobility of the amorphous silicon layer is increased. Further, it is considered that the mobility of the thin film transistor is increased.

5 [0047]

As is seen from the above, in the amorphous semiconductor layer, the dangling bonds of the Si atom are cross-linked with the NH group, whereby the bond with which carriers can transfer is formed. Further, the carrier mobility of the amorphous semiconductor layer can be increased. Furthermore, the oxygen concentration in the 10 amorphous semiconductor layer is reduced, whereby the bond which interrupts the carrier transfer in the defect can be reduced in the defect.

[0048]

In the amorphous semiconductor layer, by reducing the oxygen concentration, controlling the nitrogen concentration, and further inclusion of the NH group or the NH<sub>2</sub> group, the defect levels of the amorphous semiconductor layer can be reduced, the carrier mobility can be increased, and Shockley-Read-Hall current can be reduced. Therefore, the amorphous semiconductor layer is used for a buffer layer, whereby the off-current of the thin film transistor can be reduced and the on-current thereof can be increased.

20 [0049]

In addition, since the drain withstand voltage of the thin film transistor is relieved by using the amorphous semiconductor layer having the NH group for the buffer layer, deterioration of the thin film transistor can be reduced. Further, in the case of forming, using a microcrystalline semiconductor layer, the semiconductor layer

which is in contact with the gate insulating layer, an amorphous semiconductor layer having an NH group is used for the buffer layer and the microcrystalline semiconductor layer and an amorphous semiconductor layer having an NH group are formed successively, whereby the interface of the microcrystalline semiconductor and the 5 amorphous structure in the microcrystalline semiconductor layer can be prevented from being oxidized, and thus the carrier mobility of the microcrystalline semiconductor layer can be increased.

[0050]

A structure of an interface between the microcrystalline semiconductor layer 10 and the buffer layer will be described with reference to FIGS. 29A and 29B.

[0051]

As illustrated in FIG. 29A, the interface between the semiconductor layer 115 and the buffer layer 131 can be almost planar. The nitrogen concentration at the interface having such a shape may be set to be high when the buffer layer is deposited 15 over the semiconductor layer 115 to form the amorphous semiconductor layer. As a result, the amorphous semiconductor layer having an NH group can be formed on the surface of the semiconductor layer 115 as the buffer layer 131.

[0052]

Further, as illustrated in FIG. 29B, the interface between the semiconductor 20 layer 115 and the buffer layer 131 can have projections and depressions. In particular, when the semiconductor layer 115 is a microcrystalline semiconductor layer, the surface of the crystal grain has projections and depressions. However, the projection of the semiconductor layer 115 has an obtuse angle, so that height difference between the top of the projection and the bottom of the depression is small.

[0053]

As the source and drain regions 129, a semiconductor layer into which an impurity element imparting one conductivity type is added (hereinafter, referred to as an impurity semiconductor layer) is formed. In the case of forming an n-channel thin film transistor, phosphorus may be used as an impurity element imparting one conductivity type, and the thin film transistor is formed typically using amorphous silicon or microcrystalline silicon which contains phosphorus. In the case of forming a p-channel thin film transistor, boron may be used as an impurity element imparting one conductivity type, and the thin film transistor is formed typically using amorphous silicon or microcrystalline silicon which contains boron.

[0054]

By setting a concentration of an impurity element imparting one conductivity type, here, phosphorus or boron, to  $1 \times 10^{19} \text{ cm}^{-3}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ , an ohmic contact with the wiring layers 123 and 125 can be obtained, and the impurity semiconductor layer serves as the source and drain regions.

[0055]

The source and drain regions 129 are formed to have a thickness of greater than or equal to 10 nm and less than or equal to 100 nm, preferably, greater than or equal to 30 nm and less than or equal to 50 nm. When the thickness of the source and drain regions 129 is made small, throughput can be increased.

[0056]

The wiring layers 123 and 125 can be formed as a single layer or stacked layers using any of aluminum, copper, titanium, neodymium, scandium, molybdenum, chromium, tantalum, tungsten, and the like. An aluminum alloy to which an element

to prevent a hillock is added (e.g., an Al-Nd alloy which can be used for the gate electrode layer 103) may be used. Alternatively, crystalline silicon to which an impurity element serving as a donor is added may be used. The wiring layers 123 and 125 may have a stacked-layer structure where a layer on the side which is in contact with the crystalline silicon to which an impurity element serving as a donor is added is formed using titanium, tantalum, molybdenum, tungsten, or nitride of any of these elements and aluminum or an aluminum alloy is formed thereover. Alternatively, top and bottom surfaces of aluminum or an aluminum alloy may be each covered with titanium, tantalum, molybdenum, tungsten, or nitride thereof to form a stacked-layer structure. For example, the wiring layers 123 and 125 preferably have a three-layer structure in which an aluminum layer is sandwiched between molybdenum layers.

[0057]

According to this embodiment, as compared to a thin film transistor in which an amorphous semiconductor is included in a channel formation region, on-current of a thin film transistor can be increased. In addition, as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region, off-current of a thin film transistor can be reduced.

[0058]

(Embodiment 2)

In this embodiment, modes which can be used for the semiconductor layer 115 in the thin film transistor described in Embodiment 1 will be described with reference to FIGS. 7A and 7B and FIGS. 8A and 8B. FIG. 7A is a cross-sectional view of a thin film transistor and FIG. 7B is an enlarged view of a region in which the gate insulating layer 107, a microcrystalline semiconductor 118, and the buffer layer 131 are in contact

with each other.

[0059]

As illustrated in FIGS. 7A and 7B, in a thin film transistor described in this embodiment, dispersed microcrystalline semiconductor particles or a net-like microcrystalline semiconductor 118 are formed over the gate insulating layer 107.

[0060]

Dispersed microcrystalline semiconductor particles 118a can be formed using silicon, silicon germanium ( $Si_xGe_{1-x}$ ,  $0.5 < x < 1$ ) that contains more silicon than germanium, or the like. As viewed from above, each of the dispersed microcrystalline semiconductor particles has a circular shape as illustrated in FIG. 8A and a cross section thereof has a hemispherical shape as illustrated in FIGS. 7A and 7B. When the diameter of the dispersed microcrystalline semiconductor particle seen from above is set at 1 nm to 30 nm and the density thereof is set at less than  $1 \times 10^{13}/cm^3$ , preferably less than  $1 \times 10^{10}/cm^3$ , the dispersed microcrystalline semiconductor particles can be formed by only deposition.

[0061]

The diameter of the dispersed microcrystalline semiconductor particle is not limited to the above and may be larger.

[0062]

Further, a net-like microcrystalline semiconductor 118b, as illustrated in FIG. 8B, has a shape in which microcrystalline semiconductors are partially continuous and a portion where a microcrystalline semiconductor is continuously formed may be arranged regularly (e.g. lattice-shaped or zigzag) or irregularly. FIG. 8B illustrates a shape viewed from above in which microcrystalline semiconductors are continuous

irregularly.

[0063]

Such a net-like microcrystalline semiconductor 118b in which microcrystalline semiconductors are partially continuous can be formed in such a manner that an 5 amorphous semiconductor or a microcrystalline semiconductor is formed over the gate insulating layer 107, irradiated with a laser beam having energy with such a level that the amorphous semiconductor or the microcrystalline semiconductor is melted, melted, and solidified.

[0064]

10 The dispersed microcrystalline semiconductor particle or the net-like microcrystalline semiconductor 118 is formed between the gate insulating layer 107 and the buffer layer 131, whereby adhesion between the buffer layer 131 and the gate insulating layer 107 can be increased. Therefore, a yield of thin film transistors can be enhanced. Further, since the buffer layer 131 is formed using an amorphous 15 semiconductor layer having an NH group, dangling bonds at an interface between the dispersed microcrystalline semiconductor particle or the net-like microcrystalline semiconductor 118 and the buffer layer are cross-linked with the NH group, so that the defect levels at the interface can be reduced. Alternatively, dangling bonds at the interface between the dispersed microcrystalline semiconductor or the net-like 20 microcrystalline semiconductor 118 and the buffer layer are terminated with an NH<sub>2</sub> group, so that the defect levels at the interface can be reduced.

[0065]

According to this embodiment, as compared to a thin film transistor in which an amorphous semiconductor is included in a channel formation region, on-current of a

thin film transistor can be increased. In addition, as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region, off-current of a thin film transistor can be reduced. Further, the dispersed microcrystalline semiconductor particle or the net-like microcrystalline semiconductor 5 is formed over the gate insulating layer, whereby adhesion between the gate insulating layer and the buffer layer is improved, so that yield can be enhanced.

[0066]

(Embodiment 3)

In this embodiment, a mode of a thin film transistor which is different from that 10 described in Embodiment 1 will be described with reference to FIGS. 9A and 9B.

[0067]

FIG. 9A is a cross-sectional view taken along a line A-B of FIG. 9B illustrating a thin film transistor of this embodiment. A thin film transistor illustrated in FIG. 9A includes a gate electrode layer 103 over a substrate 101; a gate insulating layer 107 which covers the gate electrode layer 103; a semiconductor layer 143 which is provided 15 over and in contact with the gate insulating layer 107 and serves as a channel formation region; a buffer layer 159 over the semiconductor layer 143; and source and drain regions 157 which are in contact with part of the buffer layer 159. In addition, the thin film transistor includes a wiring layer 153 and a wiring layer 155 which are provided 20 over and in contact with the source and drain regions 157. The wiring layer 153 and the wiring layer 155 form a source electrode and a drain electrode. Further, each layer has been patterned into a desired shape. Here, the buffer layer 159 is formed using an amorphous semiconductor layer having an NH group.

[0068]

Further, as illustrated in FIG. 9B, in the shape viewed from above of the thin film transistor of this embodiment, the source and drain regions 157 are exposed at outer edges of the wiring layer 153 and the wiring layer 155. Such a structure is formed by a photolithography process using a multi-tone mask.

5 [0069]

The semiconductor layer 143, the buffer layer 159, the source and drain regions 157, and the wiring layers 153 and 155 can be formed using, as appropriate, materials similar to those of the semiconductor layer 115, the buffer layer 131, the source and drain regions 129, and the wiring layers 123 and 125 in Embodiment 1, respectively.

10 [0070]

In this embodiment, one of the source electrode and the drain electrode is formed so as to have a U shape (a reversed C shape or a horseshoe shape), and partially surrounds the other of the source electrode and the drain electrode. The distance between the source and drain electrodes is kept almost constant (see FIG. 9B).

15 [0071]

One of the source electrode and the drain electrode has the above-described shape, whereby a channel width of the thin film transistor can be increased, and thus the amount of current of when the thin film transistor is turn on is increased. In addition, variation in electric characteristics can be reduced. Further, decrease in reliability due 20 to misalignment of a mask pattern in a manufacturing process can be suppressed. However, the present invention is not limited thereto. One of the source electrode and the drain electrode does not necessarily have a U shape, and the source electrode and the drain electrode may face each other in a linear manner. Further, the shapes of the thin film transistors viewed from above in Embodiments 1 and 2 can be the same as that in

this embodiment.

[0072]

According to this embodiment, as compared to a thin film transistor in which an amorphous semiconductor is included in a channel formation region, on-current of a thin film transistor can be increased. In addition, as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region, off-current of a thin film transistor can be reduced.

[0073]

(Embodiment 4)

10 In this embodiment, a method for manufacturing a thin film transistor and a pixel portion of a display device will be described below. Here, a liquid crystal display device is used as a display device. An n-channel thin film transistor has higher carrier mobility than a p-channel thin film transistor. It is preferable that all thin film transistors formed over the same substrate have the same polarity because the number of 15 manufacturing steps can be reduced. Therefore, in this embodiment, a method for manufacturing an n-channel thin film transistor will be described.

[0074]

First, a gate electrode layer 103 and a capacitor wiring 105 are formed over a substrate 101 (see FIG. 10A).

20 [0075]

As the substrate 101, the substrate 101 described in Embodiment 1 can be used as appropriate.

[0076]

The gate electrode layer 103 and the capacitor wiring 105 are formed using a

material used for the gate electrode layer 103 described in Embodiment 1 as appropriate.

The gate electrode layer 103 and the capacitor wiring 105 can be formed in such a manner that a conductive layer is formed over the substrate 101, using the above material by a sputtering method or a vacuum evaporation method, a mask is formed over the conductive layer by a photolithography method, an inkjet method, or the like, and the conductive layer is etched using the mask. Alternatively, the gate electrode layer 103 can be formed by discharging a conductive nanopaste of silver, gold, copper, or the like over the substrate by an inkjet method and baking the conductive nanopaste.

Note that a nitride layer of any of the above metal materials may be provided between

the substrate 101 and the gate electrode layer 103 and the capacitor wiring 105. Here, the conductive layer is formed over the substrate 101 and etched using a resist mask which is formed using a photomask.

#### [0077]

Note that it is preferable that side surfaces of the gate electrode layer 103 and

the capacitor wiring 105 have a tapered shape. This is in order to prevent disconnection at a step portion because the semiconductor layer and the wiring layer are to be formed over the gate electrode layer 103 in a later step. In order that the side surfaces of the gate electrode layer 103 and the capacitor wiring 105 have a tapered shape, etching may be performed while the resist mask is made to recede. For example, by using an etching gas containing an oxygen gas, etching can be performed while the resist mask is made to recede.

#### [0078]

Through the step of forming the gate electrode layer 103, a gate wiring (a scanning line) can also be formed at the same time. Note that a “scanning line” means

a wiring which selects a pixel, while a “capacitor wiring” means a wiring which is connected to one of electrodes of a storage capacitor in a pixel. However, without limitation thereto, the gate electrode layer 103 and one or both of a gate wiring and a capacitor wiring may be formed separately.

5 [0079]

Next, a gate insulating layer 107, a semiconductor layer 109, a buffer layer 111, and an impurity semiconductor layer 113 are formed so as to cover the gate electrode layer 103.

[0080]

10 The gate insulating layer 107 can be formed using any of the materials for the gate insulating layer 107 which are described in Embodiment 1 as appropriate. Furthermore, the gate insulating layer 107 can be formed by a CVD method, a sputtering method, or the like. The gate insulating layer 107 can be formed by a plasma CVD method with a frequency of 1 MHz to 20 MHz, typically a high frequency 15 of 13.56 MHz; or a high frequency of higher than 20 MHz and lower than or equal to 120 MHz approximately, typically 27.12 MHz or 60 MHz. Further, the gate insulating layer 107 may be formed using a microwave plasma CVD apparatus with a high frequency (greater than or equal to 1 GHz). When the gate insulating layer 107 is formed by a microwave plasma CVD apparatus, the withstand voltage between a gate 20 electrode and a drain electrode or a source electrode can be improved; therefore, a highly reliable thin film transistor can be obtained.

[0081]

Here, as an example of the gate insulating layer 107, a silicon oxynitride layer with a thickness of about 110 nm is formed in such a manner that the source gases are

introduced into a treatment chamber and stabilized, where the flow rate of SiH<sub>4</sub> is 30 sccm and the flow rate of N<sub>2</sub>O is 1200 sccm; and plasma discharge of 50W is performed, where the pressure in the treatment chamber is 40 Pa and the temperature of the substrate is 280 °C. After that, similarly to the formation of the silicon nitride layer, 5 only the introduction of SiH<sub>4</sub> is stopped, and after several seconds, the plasma discharge is stopped.

[0082]

It is preferable that the semiconductor layer 109 be formed to have a thickness of greater than or equal to 2 nm and less than or equal to 60 nm, preferably greater than 10 or equal to 10 nm and less than or equal to 30 nm.

[0083]

A microcrystalline semiconductor layer as the semiconductor layer 109 is formed by glow discharge plasma generated by mixing a deposition gas including silicon or germanium with hydrogen in a reaction chamber of the plasma CVD apparatus. A microcrystalline semiconductor layer is formed using mixture of the deposition gas including silicon or germanium and hydrogen, which is obtained by diluting the deposition gas with hydrogen whose flow rate is 10 times to 2000 times, 15 preferably 50 times to 200 times that of the deposition gas.

[0084]

20 As a typical example of the deposition gas including silicon or germanium, SiH<sub>4</sub>, Si<sub>2</sub>H<sub>6</sub>, GeH<sub>4</sub>, Ge<sub>2</sub>H<sub>6</sub>, or the like can be given.

[0085]

Here, as an example of the semiconductor layer 109, a microcrystalline silicon layer with a thickness of about 50 nm can be formed in such a manner that the source

gases are introduced in a treatment chamber and stabilized, where the flow rate of SiH<sub>4</sub> is 10 sccm and the flow rate of H<sub>2</sub> is 1500 sccm, and plasma discharge of 50W is performed, where the pressure in the treatment chamber is 280 Pa and the temperature of the substrate is 280 °C. After that, similarly to the formation of the silicon oxynitride layer, only the introduction of SiH<sub>4</sub> is stopped, and after several seconds, the plasma discharge is stopped.

[0086]

Next, a method for forming the buffer layer 111 will be described.

[0087]

10 The buffer layer 111 is formed using an amorphous semiconductor layer having an NH group. Dangling bonds in the amorphous semiconductor layer are preferably cross-linked with an NH group. The dangling bonds are cross-linked with an NH group in such a manner that an oxygen concentration is made low and a nitrogen concentration is made higher than the oxygen concentration, for example, and thus the 15 buffer layer 111 can be formed. Here, it is preferable that the nitrogen concentration be one or more digits higher than the oxygen concentration. More specifically, the oxygen concentration which is measured by secondary ion mass spectroscopy is less than or equal to  $5 \times 10^{18} \text{ cm}^{-3}$ . Further, the nitrogen concentration is greater than or equal to  $1 \times 10^{20} \text{ cm}^{-3}$  and less than or equal to  $1 \times 10^{21} \text{ cm}^{-3}$ , preferably greater than or 20 equal to  $2 \times 10^{20} \text{ cm}^{-3}$  and less than or equal to  $1 \times 10^{21} \text{ cm}^{-3}$ .

[0088]

In this embodiment, the gate insulating layer 107 has a stacked-layer structure in which a silicon oxynitride layer is formed over a silicon nitride layer, and as the semiconductor layer 109, a microcrystalline silicon layer is formed and the

microcrystalline semiconductor layer is exposed to ammonia, whereby nitrogen, preferably an NH group, is supplied to the surface of the semiconductor layer 109 to control the nitrogen concentration of the buffer layer.

[0089]

5       Here, an example of forming the gate insulating layer 107, the semiconductor layer 109, the buffer layer 111, and the impurity semiconductor layer 113 will be described in detail. These layers are formed by a CVD method or the like. Further, the gate insulating layer 107 has a stacked-layer structure in which a silicon oxynitride layer is formed over a silicon nitride layer. By employing such a structure, the silicon 10 nitride layer can prevent an element included in the substrate which adversely affects electric characteristics (an element such as sodium in the case where the substrate is a glass substrate) from entering the semiconductor layer 109 or the like. FIG. 14 is a schematic view illustrating a CVD apparatus which is used for forming these layers.

[0090]

15       A plasma CVD apparatus 261 illustrated in FIG. 14 is connected to a gas supply means 250 and an exhaust means 251.

[0091]

20       The plasma CVD apparatus 261 illustrated in FIG. 14 includes a treatment chamber 241, a stage 242, a gas supply portion 243, a shower plate 244, an exhaust port 245, an upper electrode 246, a lower electrode 247, an alternate-current power source 248, and a temperature control portion 249.

[0092]

25       The treatment chamber 241 is formed using a material having rigidity and the inside thereof can be evacuated to vacuum. The treatment chamber 241 is provided

with an upper electrode 246 and a lower electrode 247. Note that in FIG. 14, a structure of a capacitive coupling type (a parallel plate type) is illustrated; however, another structure such as that of an inductive coupling type can be used, as long as plasma can be generated in the treatment chamber 241 by applying two or more

5 different high-frequency powers.

[0093]

When treatment is performed with the plasma CVD apparatus illustrated in FIG. 14, a given gas is supplied from the gas supply portion 243. The supplied gas is introduced into the treatment chamber 241 through the shower plate 244.

10 High-frequency power is applied with the alternate-current power source 248 connected to the upper electrode 246 and the lower electrode 247 to excite the gas in the treatment chamber 241, whereby plasma is generated. Further, the gas in the treatment chamber 241 is exhausted through the exhaust port 245 which is connected to a vacuum pump.

15 Further, the temperature control portion 249 makes it possible to perform plasma treatment while an object to be processed is being heated.

[0094]

The gas supply means 250 includes a cylinder 252 which is filled with a reactive gas, a pressure adjusting valve 253, a stop valve 254, a mass flow controller 255, and the like. The treatment chamber 241 includes a shower plate which is 20 processed in a plate-like shape and provided with a plurality of pores, between the upper electrode 246 and the substrate 101. A reactive gas supplied to the upper electrode 246 is supplied to the treatment chamber 241 from the pores in the upper electrode 246 having a hollow structure.

[0095]

The exhaust means 251 which is connected to the treatment chamber 241 has a function of vacuum evacuation and a function of controlling the pressure inside the treatment chamber 241 to be maintained at a predetermined level when a reactive gas is made to flow. The exhaust means 251 includes in its structure a butterfly valve 256, a 5 conductance valve 257, a turbo molecular pump 258, a dry pump 259, and the like. In the case of arranging the butterfly valve 256 and the conductance valve 257 in parallel, the butterfly valve 256 is closed and the conductance valve 257 is operated, so that the evacuation speed of the reactive gas is controlled and thus the pressure in the treatment chamber 241 can be kept in a predetermined range. Moreover, the butterfly valve 256 10 having higher conductance is opened, so that high-vacuum evacuation can be performed.

[0096]

In the case of performing ultra-high vacuum evacuation up to a pressure lower than  $10^{-5}$  Pa on the treatment chamber 241, a cryopump 260 is preferably used together. 15 Alternatively, when exhaust is performed up to ultra-high vacuum as ultimate vacuum, the inner wall of the treatment chamber 241 may be polished into a mirror surface, and the treatment chamber 141 may be provided with a heater for baking in order to reduce deflation from the inner wall.

[0097]

20 Note that as illustrated in FIG. 14, when precoating treatment is performed so that a layer is formed (deposited) so as to cover the entire treatment chamber 241, it is possible to prevent an impurity element attached to the inner wall of the treatment chamber or an impurity element for forming the inner wall of the treatment chamber from mixing into an element. In this embodiment, as precoating treatment, a layer

containing silicon as its main component may be formed. For example, an amorphous silicon layer or the like may be formed. Note that it is preferable that this layer does not include oxygen.

[0098]

5 A series of steps from a step of forming the gate insulating layer 107 to a step of forming the impurity semiconductor layer will be described with reference to FIG. 15. Note that the gate insulating layer 107 is formed in such a manner that a silicon oxynitride layer is stacked over a silicon nitride layer.

[0099]

10 First, the substrate over which the gate electrode layer 103 is formed is heated in the treatment chamber 241 of the CVD apparatus, and in order to form a silicon nitride layer, source gases used for depositing a silicon nitride layer are introduced into the treatment chamber 241 (pretreatment 201 in FIG. 15). Here, as an example, a silicon nitride layer with a thickness of about 110 nm is formed in such a manner that  
15 the source gases are introduced and stabilized, where the flow rate of SiH<sub>4</sub> is 40 sccm, the flow rate of H<sub>2</sub> is 500 sccm, the flow rate of N<sub>2</sub> is 550 sccm, and the flow rate of NH<sub>3</sub> is 140 sccm, and plasma discharge of 370 W is performed, where the pressure in the treatment chamber is 100 Pa and the temperature of the substrate is 280 °C. After that, only the introduction of SiH<sub>4</sub> is stopped, and after several seconds, the plasma  
20 discharge is stopped (formation of SiN 203 in FIG. 15). This is because if plasma discharge is stopped in a state where SiH<sub>4</sub> is present in the treatment chamber 141, grains or powders containing silicon as its main component are formed, which causes reduction in yield.

[0100]

Next, the source gases used for depositing the silicon nitride layer are exhausted and source gases used for depositing a silicon oxynitride layer are introduced into the treatment chamber 241 (replacement of gases 205 in FIG. 15). Here, as an example, a silicon oxynitride layer with a thickness of about 110 nm is formed in such a 5 manner that the source gases are introduced and stabilized, where the flow rate of SiH<sub>4</sub> is 30 sccm and the flow rate of N<sub>2</sub>O is 1200 sccm, and plasma discharge of 50W is performed, where the pressure in the treatment chamber is 40 Pa and the temperature of the substrate is 280 °C. After that, in a manner similar to that of the silicon nitride layer, only the introduction of SiH<sub>4</sub> is stopped, and after several seconds, the plasma 10 discharge is stopped (formation of SiON 207 in FIG. 15).

10 [0101]

Through the above steps, the gate insulating layer 107 can be formed. After the gate insulating layer 107 is formed, the substrate 101 is carried out of the treatment chamber 241 (unloading 225 in FIG. 15).

15 [0102]

After the substrate 101 is carried out of the treatment chamber 241, for example, a NF<sub>3</sub> gas is introduced into the treatment chamber 241 and the inside of the treatment chamber 241 is cleaned (cleaning treatment 227 in FIG. 15). After that, treatment for forming an amorphous silicon layer in the treatment chamber 241 is performed 20 (precoating treatment 229 in FIG. 15). Although the amorphous silicon layer is formed in a manner similar to that of a buffer layer 111, which will be described later, hydrogen may be introduced into the treatment chamber 241 as indicated by a dashed line 234 or may not be introduced into the treatment chamber 241. By this treatment, the amorphous silicon layer is formed on the inner wall of the treatment chamber 241.

After that, the substrate 101 is carried into the treatment chamber 241 (loading 231 in FIG. 15).

[0103]

Next, source gases used for depositing the semiconductor layer 109 are 5 introduced into the treatment chamber 241 (replacement of gases 209 in FIG. 15).

Next, the semiconductor layer 109 is formed over an entire surface of the gate insulating layer 107. In a later step, the semiconductor layer 109 is patterned into the semiconductor layer 115. First, source gases used for depositing the semiconductor layer 109 are introduced into the treatment chamber. Here, as an example, a 10 microcrystalline silicon layer with a thickness of about 50 nm can be formed in such a manner that the source gases are introduced into a treatment chamber and stabilized, where the flow rate of SiH<sub>4</sub> is 10 sccm and the flow rate of H<sub>2</sub> is 1500 sccm, and plasma discharge of 50W is performed, where the pressure in the treatment chamber is 280 Pa and the temperature of the substrate is 280 °C. After that, in a manner similar to that 15 of the silicon nitride layer or the like described above, only the introduction of SiH<sub>4</sub> is stopped, and after several seconds, the plasma discharge is stopped (formation of a semiconductor layer 211 in FIG. 15).

[0104]

Next, nitrogen is supplied to the surface of the semiconductor layer 109. Here, 20 by exposing the surface of the semiconductor layer 109 to an ammonia gas, nitrogen is supplied (here, such treatment is referred to as “flushing treatment”) (flushing treatment 213 in FIG. 15). Further, hydrogen may be contained in the ammonia gas as indicated by a dashed line 236a. Instead of an ammonia gas, a nitrogen gas may be used as indicated by a dashed line 236b or a hydrogen gas may be used as indicated by a dashed

line 236a. Alternatively, an ammonia gas and a nitrogen gas may be used. Here, for example, the treatment may be performed under such conditions that the pressure in the treatment chamber 241 is about 20 Pa to 30 Pa, the substrate temperature is 280 °C, and the treatment time is 60 seconds. Further alternatively, after the flushing treatment, the 5 pressure in the treatment chamber is reduced or increased to be controlled, so that the amount of nitrogen in the treatment chamber 141 may be controlled. Note that in the treatment of this step, the substrate 101 is only exposed to an ammonia gas; however, plasma treatment may be performed. After that, these gases are exhausted and gases used for depositing the buffer layer 111 are introduced (replacement of gases 215 in FIG. 10 15).

[0105]

Next, the buffer layer 111 is formed over an entire surface of the semiconductor layer 109. In a later step, the buffer layer 111 is patterned into the buffer layer 131. Here, the buffer layer is formed using an amorphous semiconductor layer having an NH 15 group. Here, as an example, an amorphous semiconductor layer 105a with a thickness of about 50 nm, here, an amorphous silicon layer can be formed in such a manner that the source gases are introduced and stabilized, where the flow rate of SiH<sub>4</sub> is 280 sccm and the flow rate of H<sub>2</sub> is 300 sccm; the pressure in the treatment chamber is 280 Pa; the temperature of the substrate is 280 °C; and plasma discharge is performed with the RF 20 power source frequency of 13.56 MHz; and the power of the RF power source of 60W. In this step, the ammonia gas introduced into the reaction chamber by the flushing treatment is decomposed by plasma discharge, so that an NH group or an NH<sub>2</sub> group is generated. Further, when the amorphous semiconductor layer is deposited, different dangling bonds included in the amorphous semiconductor layer can be cross-linked to

each other. Further, different dangling bonds included in the amorphous semiconductor layer can be terminated. Note that in the case of introducing a nitrogen gas as a gas containing nitrogen into the reaction chamber, a hydrogen gas which is a source gas of the amorphous semiconductor layer and the nitrogen gas are reacted with 5 each other by plasma discharge, so that an NH group or an NH<sub>2</sub> group is generated. Further, different dangling bonds in the amorphous semiconductor layer are cross-linked with the NH group. Further, dangling bonds included in the amorphous semiconductor layer can be terminated with the NH group. After that, in a manner similar to that of the silicon nitride layer or the like described above, only the introduction of SiH<sub>4</sub> is 10 stopped, and after several seconds, the plasma discharge is stopped (formation of a buffer layer 217 in FIG. 15). After that, these gases are exhausted and gases used for depositing the impurity semiconductor layer 113 are introduced (replacement of gases 219 in FIG. 15).

[0106]

15 A gas containing nitrogen is supplied to a reaction chamber in which the buffer layer of this embodiment is formed. The gas containing nitrogen is subjected to plasma discharge, so that an NH group or an NH<sub>2</sub> group is generated. Further, as described above, dangling bonds included in the amorphous silicon layer are cross-linked with an NH group. Further, dangling bonds included in the amorphous 20 silicon layer can be terminated with an NH group. Therefore, in the reaction chamber where a gas containing nitrogen is supplied, the buffer layer 111 is formed over the semiconductor layer 109, whereby an amorphous semiconductor layer having an NH group with which dangling bonds are cross-linked can be formed. Further, an amorphous semiconductor layer having an NH<sub>2</sub> group with which dangling bonds are

terminated can be formed.

[0107]

In the buffer layer 111 formed by such a method, the nitrogen concentration which is measured by secondary ion mass spectrometry has a peak at an interface 5 between the semiconductor layer 109 and the buffer layer 111 and is gradually reduced in a direction in which the semiconductor layer 109 is deposited.

[0108]

Note that as indicated by a dashed line 235a in FIG. 15, in formation of a buffer layer 217, an ammonia gas may be made to flow in the reaction chamber. Instead of 10 an ammonia gas, as indicated by a dashed line 235b, a nitrogen gas may be made to flow. Further, an ammonia gas and a nitrogen gas may be made to flow. As a result, the nitrogen concentration of the buffer layer 111 is increased, so that dangling bonds included in the amorphous silicon layer are cross-linked or terminated, leading to reduction in the defect levels.

15 [0109]

In the buffer layer 111 formed by such a method, the nitrogen concentration which is measured by secondary ion mass spectrometry has a peak at an interface between the semiconductor layer 109 and the buffer layer 111 and is constant in the direction in which the semiconductor layer 109 is deposited.

20 [0110]

Next, the impurity semiconductor layer 113 is formed over an entire surface of the buffer layer 111. In a later step, the impurity semiconductor layer 113 is patterned into the source and drain regions 129. First, source gases used for depositing the impurity semiconductor layer 113 are introduced into the treatment chamber 241.

Here, as an example, a semiconductor layer with a thickness of about 50 nm can be formed in such a manner that the source gases are introduced and stabilized, where the flow rate of SiH<sub>4</sub> is 100 sccm and the flow rate of a mixed gas in which PH<sub>3</sub> is diluted with H<sub>2</sub> to 0.5 vol% is 170 sccm, and plasma discharge of 60W is performed, where the 5 pressure in the treatment chamber 241 is 280 Pa and the temperature of the substrate is 280 °C. After that, in a manner similar to that of the silicon nitride layer, only the introduction of SiH<sub>4</sub> is stopped, and after several seconds, the plasma discharge is stopped (formation of an impurity semiconductor layer 221 in FIG. 15). After that, these gases are exhausted (exhaust 223 in FIG. 15).

10 [0111]

As described above, steps of forming components up to the impurity semiconductor layer 113 can be performed (see FIG. 10A).

[0112]

Next, with use of a resist mask formed by a second photolithography step, the 15 semiconductor layer 109, the buffer layer 111, and the impurity semiconductor layer 113 are etched to form the semiconductor layer 115, a buffer layer 117, and an impurity semiconductor layer 119 (see FIG. 10B). After that, the resist mask is removed.

[0113]

Next, conductive layer 121 is formed so as to cover the semiconductor layer 20 115, the buffer layer 117, and the impurity semiconductor layer 119 (see FIG. 10C).

[0114]

The conductive layer 121 can be formed using a material and a stacked-layer structure of the conductive layer 121 described in Embodiment 1 as appropriate. The conductive layer 121 is formed by a CVD method, a sputtering method, or a vacuum

evaporation method. Alternatively, the conductive layer 121 may be formed by discharging a conductive nanopaste of silver, gold, copper, or the like by a screen printing method or an inkjet method and baking the conductive nanopaste. After that, a resist mask is formed over the conductive layer 121.

5 [0115]

Next, with use of a resist mask formed by a third photolithography step, the conductive layer 121 is etched to form a wiring layer 123 and a wiring layer 125 (see FIG. 11A). The wiring layer 123 and the wiring layer 125 form the source electrode and the drain electrode. The conductive layer 121 is preferably etched by wet etching.

10 By wet etching, the conductive layer is etched isotropically. As a result, the edges of the conductive layer recede to an inner side than the edges of the resist mask, and thus the wiring layer 123 and the wiring layer 125 are formed. Accordingly, the side surfaces of the wiring layer 123 and the wiring layer 125 are not aligned with the side surfaces of the etched source and drain regions 129, and the side surfaces of the source 15 and drain regions are located outside of the side surfaces of the wiring layer 123 and the wiring layer 125. The wiring layer 123 and the wiring layer 125 serve not only as a source electrode and a drain electrode but also as a signal line. However, without limitation thereto, a signal line may be provided separately from the wiring layer 123 and the wiring layer 125.

20 [0116]

Next, with use of a resist mask formed by a third photolithography step, the impurity semiconductor layer 119 and part of the buffer layer 117 are etched (see FIG. 11B). The semiconductor layer 115, the buffer layer 131, and the source and drain regions 129 are formed through the process up to this step. After that, the resist mask

is removed. FIG. 13A is a top view of FIG. 11B.

[0117]

Next, dry etching is preferably performed. A condition of dry etching is set so that the exposed region of the buffer layer 131 is not damaged and the etching rate with respect to the buffer layer 131 is low. In other words, a condition which gives almost no damages to the exposed surface of the buffer layer 131 and hardly reduces the thickness of the exposed region of the buffer layer 131 is applied. As an etching gas, a chlorine-based gas is used; typically, a Cl<sub>2</sub> gas is used. There is no particular limitation on an etching method and an inductively coupled plasma (ICP) method, a 10 capacitively coupled plasma (CCP) method, an electron cyclotron resonance (ECR) method, or a reactive ion etching (RIE) method, or the like can be used.

[0118]

An example of a condition of dry etching which can be used here is as follows: the flow rate of Cl<sub>2</sub> gas is 100 sccm; the pressure in a chamber is 0.67 Pa; the 15 temperature of the lower electrode is -10 °C; an RF power (13.56 MHz) of 2000 W is applied to the coil of the upper electrode to generate plasma; no power (i.e. non-biased 0 W) is applied to the substrate 101 side; and thus etching is performed for 30 seconds. The temperature of the inner wall of the chamber is preferably approximately 80 °C.

[0119]

20 Next, the surface of the buffer layer 131 may be irradiated with water plasma, ammonia plasma, nitrogen plasma, or the like.

[0120]

Water plasma treatment can be performed in such a manner that a gas containing water typified by water vapor (H<sub>2</sub>O vapor) as its main component is

introduced into a reaction space to generate plasma.

[0121]

As described above, after the pair of source and drain regions 129 are formed, dry etching is further performed under such a condition that the buffer layer 131 is not damaged, whereby an impurity element such as a residue existing on the exposed region 5 of the buffer layer 131 can be removed. Further, after the dry etching, water plasma treatment is performed, whereby a residue of the resist mask can also be removed. By water plasma treatment, insulation between the source region and the drain region can be secured, and thus, in a thin film transistor which is completed, the off-current can be 10 reduced, the on-current can be increased, and variation in the electric characteristics can be reduced.

[0122]

Note that the order of the steps of plasma treatment and the like are not limited to the above. Before the resist mask is removed, etching with non-bias applied or 15 plasma treatment may be performed.

[0123]

Through the steps described above, a thin film transistor according to this embodiment can be manufactured. Like the thin film transistor described in Embodiment 1, the thin film transistor according to this embodiment can also be applied 20 to a switching transistor in a pixel of a display device typified by a liquid crystal display device. Therefore, an insulating layer 133 is formed so as to cover this thin film transistor.

[0124]

Next, an opening 134 and an opening 136 are formed in the insulating layer

133 so as to reach the source electrode and the drain electrode formed using the wiring layer 212. The opening 134 and the opening 136 can be formed by a fourth photolithography step. Note that when the insulating layer 133 is formed using a photosensitive resin, the insulating layer 133 can be formed by the fourth photolithography step. After that, a pixel electrode layer 135 is provided over the insulating layer 133 so that connection through the opening 134 and the opening 136 is obtained. In such a manner, a switching transistor in a pixel of a display device which is illustrated in FIG. 12A can be manufactured.

[0125]

10 Note that the insulating layer 133 can be formed in a manner similar to that of the gate insulating layer 107. Further, a dense silicon nitride layer is preferably used as the insulating layer 133 such that entry of a contaminant impurity element such as an organic substance, a metal, or moisture floating in the atmosphere can be prevented.

[0126]

15 Note that the pixel electrode layer 135 can be formed using a conductive composition including a conductive macromolecule (also referred to as a conductive polymer) having a light-transmitting property. The pixel electrode layer 135 preferably has a sheet resistance of less than or equal to  $10000 \Omega/\text{cm}^2$  and a light transmittance of greater than or equal to 70 % at a wavelength of 550 nm. Further, the 20 resistance of the conductive macromolecule included in the conductive composition is preferably less than or equal to  $0.1 \Omega\cdot\text{cm}$ .

[0127]

As a conductive macromolecule, a so-called  $\pi$  electron conjugated conductive macromolecule can be used. For example, polyaniline and/or a derivative thereof,

polypyrrole and/or a derivative thereof, polythiophene and/or a derivative thereof, and a copolymer of two or more kinds of those materials can be given.

[0128]

The pixel electrode layer 135 can be formed using, for example, indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide (hereinafter also referred to as ITO), indium zinc oxide, indium tin oxide to which silicon oxide is added, or the like.

[0129]

The pixel electrode layer 135 may be etched by a photolithography method to be patterned in a manner similar to that of the wiring layers 123, 125 or the like.

[0130]

Note that although not illustrated, an insulating layer formed using an organic resin by a spin coating method or the like may be formed between the insulating layer 133 and the pixel electrode layer 135. The insulating layer formed using an organic resin is formed using a photosensitive resin, whereby the number of steps can be reduced.

[0131]

After that, in a vertical alignment (VA) liquid crystal display device, in the case 20 of employing a multi-domain vertical alignment mode (so-called MVA mode) in which pixels are divided into a plurality of portions and the alignment of liquid crystal molecules in pixels of in the divided portions is made different for viewing angle expansion, a protrusion 137 having a predetermined shape is preferably formed over the pixel electrode layer 135. The protrusion 137 is formed using an insulating layer.

FIG. 13B is a top view of FIG. 12B.

[0132]

Here, after a composition containing a photosensitive acrylic is applied to form a composition layer with a thickness of 0.9  $\mu\text{m}$  to 1.0  $\mu\text{m}$ , heating is performed at 90 °C for 120 seconds, so that the composition layer is dried. Next, the composition layer is exposed to light with a photomask and developed to have a predetermined shape. Next, heating is performed at 230 °C for one hour to form an acrylic resin layer.

[0133]

When the protrusion 137 is formed over the pixel electrode layer, in the case where the voltage of the pixel electrode is an off-state, liquid crystal molecules are aligned perpendicularly to a surface of an alignment film; however, liquid crystal molecules in the vicinity of the protrusion are aligned to be inclined slightly to the substrate surface. When the voltage is applied to of the pixel electrode layer, first, the liquid crystal molecules in the vicinity of the protrusion which are aligned to be inclined slightly are inclined. Further, the liquid crystal molecules other than those in the vicinity of the protrusion are also affected by the liquid crystal molecules in the vicinity of the protrusion to be sequentially aligned in the same direction. As a result, stable alignment can be obtained in all the pixels. That is, alignment of the liquid crystal molecules in the entire display portion is controlled from the protrusion.

20 [0134]

Instead of the protrusion provided over the pixel electrode layer, a slit may also be provided for the pixel electrode. In this case, when a voltage is applied to the pixel electrode layer, electric field distortion is generated near the slit and electric field distribution and alignment of the liquid crystal molecules can be controlled similarly to

the case where the protrusion is provided over the pixel electrode layer.

[0135]

Through the steps described above, an element substrate can be manufactured which can be used for a liquid crystal display device and which has a thin film transistor with high on-current as compared to a thin film transistor in which an amorphous semiconductor is included in a channel formation region and with low off-current as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region.

[0136]

10 (Embodiment 5)

In this embodiment, a formation process of a buffer layer which can be applied to Embodiment 4 will be described.

[0137]

In this embodiment, the inside of a treatment chamber is cleaned before the 15 buffer layer 111 is deposited, and after that, the inner wall of the chamber is covered with a silicon nitride layer, whereby nitrogen is included in the buffer layer 111, the oxygen concentration is suppressed low, and the nitrogen concentration is made higher than the oxygen concentration. Since a series of steps from a step of forming the gate insulating layer 107 to a step of forming the semiconductor layer 109 can be performed 20 in a manner similar to that of Embodiment 4, here, a series of steps from a step of forming of the semiconductor layer 109 to a step of forming the impurity semiconductor layer 113 will be described with reference to FIG. 16.

[0138]

Next, the semiconductor layer 109 is formed over an entire surface of the gate

insulating layer 107. In a later step, the semiconductor layer 109 is patterned into the semiconductor layer 115. First, source gases used for depositing the semiconductor layer 109 are introduced into the treatment chamber. Here, as an example, in a manner similar to that of Embodiment 4, a microcrystalline semiconductor layer with a thickness of about 50 nm is formed as the semiconductor layer 109. After that, the plasma discharge is stopped (formation of a semiconductor layer 211 in FIG. 16). After that, the substrate 101 is carried out of the treatment chamber 241 (unloading 225 in FIG. 16).

[0139]

10 After the substrate 101 is carried out of the treatment chamber 241, for example, a NF<sub>3</sub> gas is introduced into the treatment chamber 241 and the inside of the treatment chamber 241 is cleaned (cleaning treatment 227 in FIG. 16). After that, treatment for forming a silicon nitride layer in the treatment chamber 241 is performed (precoating treatment 233 in FIG. 16). The silicon nitride layer is formed under the same 15 conditions as the silicon nitride layer formed as the gate insulating layer in Embodiment 4. By this treatment, the silicon nitride layer is formed on the inner wall of the treatment chamber 241. After that, the substrate 101 is carried into the treatment chamber 241 (loading 231 in FIG. 16).

[0140]

20 Next, source gases used for depositing the buffer layer 111 are introduced into the treatment chamber 241 (replacement of gases 215 in FIG. 16). Next, the buffer layer 111 is formed over an entire surface of the semiconductor layer 109. In a later step, the buffer layer 111 is patterned into the buffer layer 131. Here, as the buffer layer, in a manner similar to that of Embodiment 4, an amorphous silicon layer having

an NH group with a thickness of about 80 nm can be formed. After that, the plasma discharge is stopped (formation of a buffer layer 217 in FIG. 16). After that, these gases are exhausted and gases used for depositing the impurity semiconductor layer 113 are introduced (replacement of gases 219 in FIG. 16). In a manner similar to that of

5 Embodiment 4, the impurity semiconductor layer 113 is formed (formation of an impurity semiconductor layer 221 in FIG. 16).

[0141]

A silicon nitride layer is formed on the surface of the treatment chamber 241 in this embodiment. When a silicon nitride layer formed in the treatment chamber 241 is 10 exposed to plasma in a step of forming the buffer layer 111, nitrogen is preferably dissociated into an NH group or an NH<sub>2</sub> group, and thus at the early stage of depositing the buffer layer 111, nitrogen, preferably, an NH group or an NH<sub>2</sub> group can be mixed into the buffer layer 111. Further, when an amorphous semiconductor layer is deposited, different dangling bonds in the amorphous semiconductor layer can be 15 cross-linked. Further, when the amorphous semiconductor layer is deposited, dangling bonds in the amorphous semiconductor layer can be terminated.

[0142]

In the buffer layer 111 formed by such a method, the nitrogen concentration which is measured by secondary ion mass spectrometry has a peak at an interface 20 between the semiconductor layer 109 and the buffer layer 111 and is gradually reduced in a direction in which the semiconductor layer 109 is deposited.

[0143]

As described above, at least right before the semiconductor layer is formed, the inner wall of the treatment chamber is covered with a silicon nitride layer, whereby the

oxygen concentration can be suppressed low and the nitrogen concentration can be made higher than the oxygen concentration, and an amorphous semiconductor layer having an NH group can be formed.

[0144]

5       Further, covering the inner wall of the treatment chamber with the silicon nitride film can prevent elements that constitute the inner wall of the treatment chamber and the like from entering the semiconductor layer.

[0145]

10     Note that as indicated by a dashed line 237a in FIG. 16, in formation of a buffer layer 217, an ammonia gas may be made to flow in the reaction chamber. Instead of an ammonia gas, as indicated by a dashed line 237b, a nitrogen gas may be used. Further, an ammonia gas and a nitrogen gas may be used. As a result, the nitrogen concentration of the buffer layer 111 is increased, so that dangling bonds included in the buffer layer 111 are cross-linked, leading to reduction in the defect levels.

15     [0146]

      In the buffer layer 111 formed by such a method, the nitrogen concentration which is measured by secondary ion mass spectrometry has a peak at an interface between the semiconductor layer 109 and the buffer layer 111 and is constant in the direction in which the semiconductor layer 109 is deposited.

20     [0147]

      Note that in the description above, since the buffer layer 111 is formed in the same treatment chamber as that where the semiconductor layer 109 is formed, after the semiconductor layer 109 is formed, cleaning treatment and precoating treatment are performed; however, this embodiment may be carried out in combination with

Embodiment 4. That is, after the semiconductor layer 109 is deposited and a silicon nitride layer is formed in the treatment chamber 241, the flushing treatment 213 may be performed.

[0148]

5 Through the above steps, a thin film transistor with high on-current as compared to a thin film transistor in which an amorphous semiconductor is included in a channel formation region and with low off-current as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region can be manufactured.

10 [0149]

(Embodiment 6)

In this embodiment, a formation process of a buffer layer which can be applied to Embodiment 4 will be described.

[0150]

15 In this embodiment, by mixing nitrogen into a deposition gas for forming the buffer layer 111, the oxygen concentration is suppressed low and the nitrogen concentration is made higher than the nitrogen concentration. Since a series of steps from a step of forming the gate insulating layer 107 to a step of forming the semiconductor layer 109 can be performed in a manner similar to that of Embodiment 4, 20 here, a series of steps from a step of forming the semiconductor layer 109 to a step of forming the impurity semiconductor layer 113 will be described with reference to FIG. 17.

[0151]

The semiconductor layer 109 is formed over an entire surface of the gate

insulating layer 107. In a later step, the semiconductor layer 109 is patterned into the semiconductor layer 115. First, source gases used for depositing the semiconductor layer 109 are introduced into the treatment chamber. Here, as an example, in a manner similar to that of Embodiment 4, a microcrystalline silicon layer with a thickness of 5 about 50 nm is formed as the semiconductor layer 109. After that, the plasma discharge is stopped (formation of a semiconductor layer 211 in FIG. 17). After that, these gases are exhausted and gases used for depositing the buffer layer 111 are introduced (replacement of gases 215 in FIG. 17).

[0152]

10 Next, the buffer layer 111 is formed over the semiconductor layer 109. In a later step, the buffer layer 111 is patterned into the buffer layer 131. Here, as an example, an amorphous semiconductor layer with a thickness of about 50 nm, here, an amorphous silicon layer with a thickness of about 50 nm can be formed in such a manner that the source gases are introduced and stabilized, where the flow rate of SiH<sub>4</sub> 15 is 280 sccm, the flow rate of H<sub>2</sub> is 300 sccm, and the flow rate of NH<sub>3</sub> is 20 sccm; the pressure in the treatment chamber is 280 Pa; the temperature of the substrate is 280 °C; and plasma discharge is performed with the RF power source frequency of 13.56 MHz; and the power of the RF power source of 60W (formation of a buffer layer 217 in FIG. 17). After that, these gases are exhausted and gases used for depositing the impurity 20 semiconductor layer 113 are introduced (replacement of gases 219 in FIG. 17). In a manner similar to that of Embodiment 4, the impurity semiconductor layer 113 is formed (formation of an impurity semiconductor layer 221 in FIG. 17).

[0153]

Note that instead of an ammonia gas, as indicated by a dashed line 238, a

nitrogen gas may be used.

[0154]

The source gases for forming the buffer layer 111 in this embodiment include a gas containing nitrogen. The gas containing nitrogen is subjected to plasma discharge, 5 so that an NH group or an NH<sub>2</sub> group is generated. Further, as described above, dangling bonds included in the amorphous silicon layer are cross-linked with an NH group. Thus, an amorphous semiconductor layer having an NH group with which dangling bonds are cross-linked can be formed. Further, dangling bonds included in the amorphous silicon layer are terminated with an NH<sub>2</sub> group. Thus, an amorphous 10 semiconductor layer having an NH<sub>2</sub> group with which dangling bonds are terminated can be formed.

[0155]

In the buffer layer 111 formed by such a method, the nitrogen concentration which is measured by secondary ion mass spectrometry is constant.

15 [0156]

As described above, nitrogen is included in the gas used in depositing the buffer layer, whereby the oxygen concentration can be suppressed low and the nitrogen concentration can be made higher than the oxygen concentration, and thus the buffer layer which can be applied to Embodiment 4 can be formed.

20 [0157]

(Embodiment 7)

A method for manufacturing an amorphous semiconductor layer having an NH group in which the nitrogen concentration distribution is different in Embodiments 4 to 6 will be described with reference to FIG. 18 and FIG. 19.

[0158]

In this embodiment, nitrogen, and further an NH group are added into the buffer layer 111 in such a manner that in Embodiment 4, after formation of a semiconductor layer 211, a gas containing nitrogen is introduced into the reaction chamber by flushing treatment 213 and during formation of the buffer layer 111, a gas containing nitrogen is introduced again into the reaction chamber as indicated by a solid line 239c (see FIG. 18.). As a gas containing nitrogen, here, an ammonia gas is used. Note that instead of an ammonia gas, a nitrogen gas may be used as indicated by a dashed line 239d. Further, an ammonia gas and a nitrogen gas may be used. As a result, at the early stage of deposition of the buffer layer 111 and during deposition of the buffer layer 111, the nitrogen concentration is made high, so that the defect levels of the buffer layer 111 can be reduced.

[0159]

Alternatively, nitrogen, and further an NH group are added into the buffer layer 111 in such a manner that in Embodiment 5, after formation of a semiconductor layer, a silicon nitride layer is formed in the reaction chamber by precoating treatment 233 and during formation of the buffer layer 111, a gas containing nitrogen is introduced again into the reaction chamber as indicated by a solid line 239c (see FIG. 19.). As a gas containing nitrogen, here, an ammonia gas is used. Note that instead of an ammonia gas, a nitrogen gas may be used as indicated by a dashed line 239d. Further, an ammonia gas and a nitrogen gas may be used. As a result, at the early stage of deposition of the buffer layer 111 and during deposition of the buffer layer 111, the nitrogen concentration is made high, so that the defect level of the buffer layer 111 can be reduced.

[0160]

As described above, the nitrogen concentration on an upper side of the buffer layer, that is, a side of the source and drain regions is controlled, whereby the defect levels of the buffer layer can be reduced, so that off-current of a thin film transistor can  
5 be reduced.

[0161]

(Embodiment 8)

In this embodiment, a method for manufacturing a thin film transistor described in Embodiment 3 will be described. Also in this embodiment, a method for  
10 manufacturing an n-channel thin film transistor will be described.

[0162]

In a manner similar to that of Embodiment 4, the gate electrode layer 103 and the capacitor wiring 105 are formed over the substrate 101 through a first photolithography step.

15 [0163]

Next, the gate insulating layer 107, the semiconductor layer 109, the buffer layer 111, the impurity semiconductor layer 113, and the conductive layer 121 are formed so as to cover the gate electrode layer 103. After that, a resist mask 141 is formed over the conductive layer 121 through a second photolithography step (see FIG.  
20 20A).

[0164]

As a method for forming the gate insulating layer 107, the semiconductor layer 109, and the impurity semiconductor layer 113, any of the methods described in Embodiments 4 to 7 may be applied.

[0165]

The resist mask 141 has two regions with different thicknesses and can be formed using a multi-tone mask. The multi-tone mask is used, so that the number of photomasks to be used and the number of manufacturing steps are reduced, which is preferable. In this embodiment, the resist mask formed using a multi-tone mask can be used in a step of forming a pattern of the semiconductor layer and a step of separating the semiconductor layer into a source region and a drain region.

[0166]

A multi-tone mask is a mask capable of light exposure with multi-level light intensity, and typically, light exposure is performed with three levels of light intensity to provide an exposed region, a half-exposed region, and an unexposed region. When the multi-tone mask is used, one-time light exposure and development process allows a resist mask with plural thicknesses (typically, two levels of thicknesses) to be formed. Therefore, by using a multi-tone mask, the number of photomasks can be reduced.

15 [0167]

FIGS. 24A-1 and 24B-1 are cross-sectional views of typical multi-tone masks. FIG. 24A-1 illustrates a gray-tone mask 180 and FIG. 24B-1 illustrates a half-tone mask 185.

[0168]

20 The gray-tone mask 180 illustrated in FIG. 24A-1 includes a light-shielding portion 182 formed using a light-shielding layer on a substrate 181 having a light-transmitting property, and a diffraction grating portion 183 provided with a pattern of the light-shielding layer.

[0169]

The diffraction grating portion 183 has slits, dots, meshes, or the like that is provided at intervals which are less than or equal to the resolution limit of light used for the exposure, whereby the light transmittance can be controlled. Note that the slits, dots, or mesh provided at the diffraction grating portion 183 may be provided 5 periodically or non-periodically.

[0170]

As the substrate 181 having a light-transmitting property, a quartz substrate or the like can be used. The light-shielding layer for forming the light-shielding portion 182 and the diffraction grating portion 183 may be formed using a metal, and chromium, 10 chromium oxide, or the like is preferably used.

[0171]

In the case where the gray-tone mask 180 is irradiated with light for light exposure, as shown in FIG. 24A-2, the transmittance in the region overlapping with the light-shielding portion 182 is 0 %, and the transmittance in the region where both the 15 light-shielding portion 182 and the diffraction grating portion 183 are not provided is 100 %. Further, the transmittance at the diffraction grating portion 183 is basically in the range of 10 % to 70 %, which can be adjusted by the interval of slits, dots, or mesh of the diffraction grating, or the like.

[0172]

20 The half-tone mask 185 illustrated in FIG. 24B-1 includes a semi-light-transmitting portion 187 which is formed on a substrate 186 having a light-transmitting property, using a semi-light-transmitting layer, and a light-shielding portion 188 formed using a light-shielding layer.

[0173]

The semi-light-transmitting portion 187 can be formed using a layer of MoSiN, MoSi, MoSiO, MoSiON, CrSi, or the like. The light-shielding portion 188 may be formed using metal similar to that of the light-shielding layer of the gray-tone mask, and chromium, chromium oxide, or the like is preferably used.

5 [0174]

In the case where the half-tone mask 185 is irradiated with light for light exposure, as shown in FIG. 24B-2, the transmittance in the region overlapping with the light-shielding portion 188 is 0 %, and the transmittance in the region where both the light-shielding portion 188 and the semi-light-transmitting portion 187 are not provided 10 is 100 %. Further, the transmittance in the semi-light-transmitting portion 187 is approximately in the range of 10 % to 70 %, which can be adjusted by the kind, the thickness, or the like of the material to be formed.

[0175]

By light exposure using the multi-tone mask and development, a resist mask 15 which includes regions having different thicknesses can be formed.

[0176]

Next, with the use of the resist mask 141, the semiconductor layer 109, the buffer layer 111, the impurity semiconductor layer 113, and the conductive layer 121 are etched. Through this step, the semiconductor layer 109, the buffer layer 111, the 20 impurity semiconductor layer 113, and the conductive layer 121 are separated into each element to form a semiconductor layer 143, a buffer layer 145, an impurity semiconductor layer 147, and a conductive layer 149 (see FIG. 20B).

[0177]

Next, the resist mask 141 is made to recede to form a resist mask 151. Ashing

using oxygen plasma may be performed in order that the resist mask is made to recede. Here, ashing is performed on the resist mask 141 so that the resist mask 141 is separated over the gate electrode. As a result, the resist mask 151 is separated (see FIG. 21A).

[0178]

5 Next, the conductive layer 149 is etched using the resist mask 151 to form a wiring layer 153 and a wiring layer 155 (see FIG. 21B). The wiring layer 153 and the wiring layer 155 form a source electrode and a drain electrode. The conductive layer 149 is preferably etched in a manner similar to that of the conductive layer 121 described in Embodiment 4.

10 [0179]

Next, in a state where the resist mask 151 is formed, the impurity semiconductor layer 147 and part of the buffer layer 145 are etched to form the buffer layer 159 and the source and drain regions 157 (see FIG. 21C). After that, the resist mask 151 is removed. FIG. 23A is a top view of FIG. 21C.

15 [0180]

Next, dry etching may be performed in a manner similar to that of Embodiment 1. Further, a surface of the buffer layer 159 may be irradiated with water plasma, ammonia plasma, nitrogen plasma, or the like.

[0181]

20 Through the steps described above, a thin film transistor according to this embodiment can be manufactured. Like the thin film transistor described in Embodiment 4, the thin film transistor according to this embodiment can also be applied to a switching transistor in a pixel of a display device typified by a liquid crystal display device. Therefore, the insulating layer 133 is formed so as to cover this thin film

transistor (see FIG. 22A).

[0182]

Next, an opening 134 and an opening 160 are formed in the insulating layer 133 so as to reach the source electrode and the drain electrode formed using the wiring layers 153 and 155. The opening 134 and the opening 160 can be formed through a third photolithography step. After that, a pixel electrode layer 135 is provided over the insulating layer 133 through a fourth photolithography step so that connection through the openings 134 and 160 is obtained. In such a manner, a switching transistor in a pixel of a display device which is illustrated in FIG. 22B can be manufactured.

10 [0183]

Note that although not illustrated, an insulating layer formed using an organic resin by a spin coating method or the like may be formed between the insulating layer 133 and the pixel electrode layer 135.

[0184]

15 After that, as in Embodiment 4, in a vertical alignment (VA) liquid crystal display device, in the case of employing a multi-domain vertical alignment mode (so-called MVA mode) in which pixels are divided into a plurality of portions and the alignment of liquid crystal molecules in pixels in the divided portions is made different for viewing angle expansion, the protrusion 137 is preferably formed over the pixel 20 electrode layer 135 (see FIG. 22C). FIG. 23B is a top view of FIG. 22C.

[0185]

Through the steps described above, an element substrate which can be used for a liquid crystal display device and which has a thin film transistor with high on-current as compared to a thin film transistor in which an amorphous semiconductor is included

in a channel formation region and with low off-current as compared to a thin film transistor in which a microcrystalline semiconductor is included in a channel formation region can be manufactured with a small number of masks.

[0186]

5 (Embodiment 9)

In this embodiment, a structure of a thin film transistor which can reduce contact resistance will be described. Specifically, the source and drain regions described in Embodiments 1 to 8 are formed using a semiconductor layer having an impurity element imparting one conductivity type and an NH group or an NH<sub>2</sub> group 10 (hereinafter, referred to as an impurity semiconductor layer having an NH group).

[0187]

An impurity semiconductor layer having an NH group is formed by combining steps of forming the impurity semiconductor layer and the buffer layer in Embodiments 4 to 7. Specifically, in the case of combining a step of formation of a buffer layer 217 15 and a step of formation of an impurity semiconductor layer 221 described in Embodiment 4, in FIG. 15, flushing treatment 213 is performed between formation of a buffer layer 217 and replacement of gases 219, whereby the nitrogen concentration on the surface of the buffer layer may be made higher so that the nitrogen concentration in the impurity semiconductor layer may be made higher.

20 [0188]

Alternatively, in the case of combining a step of forming the amorphous semiconductor layer having an NH group and a step of forming the impurity semiconductor layer which are described in Embodiment 5, in FIG. 16, the steps from unloading 225 to loading 231 are performed between formation of a buffer layer 217

and replacement of gases 219 and a silicon nitride layer may be formed in the reaction chamber, whereby the nitrogen concentration in the reaction chamber may be made higher and the nitrogen concentration in the impurity semiconductor layer may be made higher.

5 [0189]

Further alternatively, in the case of combining a step of forming the amorphous semiconductor layer having an NH group and a step of forming the impurity semiconductor layer which are described in Embodiment 6, in a step of formation of an impurity semiconductor layer 221 in FIG. 17, an ammonia gas or a nitrogen gas may be 10 introduced, whereby the nitrogen concentration in the impurity semiconductor layer may be made higher.

[0190]

In addition to an impurity element imparting one conductivity type, an NH group or an NH<sub>2</sub> group is included in the source and drain regions, whereby the defect 15 levels of the source and drain regions can be reduced. Therefore, the mobility of the source and drain regions can be increased and contact resistance can be reduced.

[0191]

(Embodiment 10)

The thin film transistors described in Embodiments 1 to 3 can be used for 20 light-emitting display devices or light-emitting devices. As light-emitting elements used for light-emitting display devices or light-emitting devices, typically, light-emitting elements utilizing electroluminescence can be given. Light-emitting elements utilizing electroluminescence are roughly classified according to whether a light-emitting material is an organic compound or an inorganic compound. In general, the former is

referred to as organic EL elements and the latter as inorganic EL elements.

[0192]

Further, a light-emitting element is formed over the element substrate as described in Embodiments 4 and 8, whereby a light-emitting display device or a 5 light-emitting device can be manufactured.

[0193]

Since the thin film transistor having high on-current and low off-current is used as a pixel transistor in the light-emitting display device and the light-emitting device of this embodiment, a light-emitting display device and a light-emitting device having 10 preferable image quality (for example, high contrast) and low power consumption can be manufactured.

[0194]

(Embodiment 11)

Next, an example of a structure of a display panel included in a display device 15 to which the present invention can be applied will be described below.

[0195]

FIG. 25A illustrates a mode of a display panel in which only a signal line driver circuit 303 is formed separately and connected to a pixel portion 302 formed over a substrate 301. An element substrate provided with the pixel portion 302, a protective 20 circuit 306, and a scanning line driver circuit 304 is formed using the thin film transistor described in any of Embodiments 1 to 10. The signal line driver circuit 303 may be formed with a transistor using a single crystal semiconductor for a channel formation region, a thin film transistor using a polycrystalline semiconductor for a channel formation region, or a transistor using silicon on insulator (SOI) for a channel formation

region. The transistor using SOI for a channel formation region includes a transistor using a single crystal semiconductor layer provided over a glass substrate for a channel formation region. To each of the pixel portion 302, the signal line driver circuit 303, and the scanning line driver circuit 304, potential of power supply, various signals, and 5 the like are supplied through an FPC 305. The protective circuit 306 formed using the thin film transistor described in any of embodiments 1 to 10 may be provided between the signal line driver circuit 303 and the FPC 305 and/or between the signal line driver circuit 303 and the pixel portion 302. The protective circuit 306 may be provided with 10 one or more elements selected from a thin film transistor with another structure, a diode, a resistive element, a capacitor, or the like.

[0196]

Note that the signal line driver circuit and the scanning line driver circuit may both be formed over a substrate which is the same as the substrate over which a pixel transistor of the pixel portion is formed.

15 [0197]

Further, when the driver circuit is separately formed, a substrate provided with the driver circuit is not always necessary to be attached to a substrate provided with the pixel portion, and may be attached to, for example, the FPC. FIG. 25B illustrates a mode of a display panel in which an element substrate provided with a pixel portion 312, 20 a protective circuit 316, and a scanning line driver circuit 314 which are formed over a substrate 311 is connected to an FPC 315, with only a signal line driver circuit 313 formed separately. The pixel portion 312, the protective circuit 316, and the scanning line driver circuit 314 are formed using the thin film transistor described in the above Embodiment 1. The signal line driver circuit 313 is connected to the pixel portion 312

through the FPC 315 and the protection circuit 316. To each of the pixel portion 312, the signal line driver circuit 313, and the scanning line driver circuit 314, potential of power supply, various signals, and the like are supplied through the FPC 315. The protective circuit 316 may also be provided between the FPC 315 and the pixel portion 5 312.

[0198]

Furthermore, only part of the signal line driver circuit or part of the scanning line driver circuit may be formed over a substrate the same as the substrate over which the pixel portion is formed, using any of the thin film transistors described in the above 10 embodiments, and the rest may be formed separately and electrically connected to the pixel portion. FIG. 25C illustrates the mode of a display panel in which an analog switch 323a included in a signal line driver circuit is formed over a substrate the same as a substrate 321, over which a pixel portion 322 and a scanning line driver circuit 324 are formed, and a shift register 323b included in the signal line driver circuit is 15 separately formed over a different substrate and then attached to the substrate 321. The pixel portion 322, a protective circuit 326, and the scanning line driver circuit 324 are each formed using any of the thin film transistors described in the above embodiments. The shift register 323b included in the signal line driver circuit is connected to the pixel portion 322 through the analog switch 323a and the protective 20 circuit 326. To each of the pixel portion 322, the signal line driver circuit, and the scanning line driver circuit 324, potential of power supply, various signals, and the like are supplied through an FPC 325. The protective circuit 326 may also be provided between the FPC 325 and the analog switch 323a.

[0199]

As illustrated in each of FIGS. 25A to 25C, in the display device of this embodiment, the driver circuits can be entirely or partially formed using the thin film transistors described in the above embodiments over a substrate the same as the substrate over which the pixel portion is formed.

5 [0200]

Note that a connection method of a substrate which is separately formed is not particularly limited, and a known COG method, wire bonding method, TAB method, or the like can be used. In addition, a position for connection is not limited to the position illustrated in FIGS. 25A to 25C as long as electrical connection is possible. A 10 controller, a CPU, a memory, or the like may be formed separately and connected.

[0201]

Note that the signal line driver circuit used in this embodiment includes a shift register and an analog switch. In addition to the shift register and the analog switch, another circuit such as a buffer, a level shifter, or a source follower may be included. 15 The shift register and the analog switch are not necessarily provided, and for example, a different circuit such as a decoder circuit which can select signal lines may be used instead of the shift register, and a latch or the like may be used instead of the analog switch.

[0202]

20 (Embodiment 12)

An element substrate which is formed using the thin film transistor described in any of the above embodiments and a display device or the like with the use of this element substrate can be applied to an active-matrix display panel. That is, the present invention can be applied to all the electronic devices including the element substrate and

the display device in a display portion.

[0203]

Examples of such electronic devices include a camera such as a video camera or a digital camera, a head-mounted display (a goggle-type display), a car navigation system, a projector, a car stereo, a personal computer, and a portable information terminal (such as a mobile computer, a cellular phone, or an e-book reader). Examples of these devices are illustrated in FIGS. 26A to 26D.

[0204]

FIG. 26A illustrates a television device. The television device can be completed by incorporating the display panel to which the above embodiment is applied into a housing. A main screen 333 is formed with the display panel, and a speaker portion 339, operation switches, or the like are provided as other additional accessories.

[0205]

As illustrated in FIG. 26A, a display panel 332 utilizing a display element is incorporated into a housing 331. In addition to reception of general television broadcast by a receiver 335, communication of information in one direction (from a transmitter to a receiver) or in two directions (between a transmitter and a receiver or between receivers) can be performed by connection to a wired or wireless communication network through a modem 334. Operation of the television device can be performed by the switch incorporated into the housing or a remote control device 336 provided separately. This remote control device may also be provided with a display portion 337 for displaying output information. Further, the display portion 337 may also be provided with the thin film transistor described in any of Embodiments 1 to 10. Further, the television device may include a sub screen 338 formed with a second

display panel to display channels, volume, or the like, in addition to the main screen 333.

In this structure, the thin film transistor described in any of Embodiments 1 to 10 can be applied to either or both the main screen 333 and the sub screen 338.

[0206]

5 FIG. 27 is a block diagram illustrating a main structure of a television device. A display panel is provided with a pixel portion 371. A signal line driver circuit 372 and a scanning line driver circuit 373 may be mounted on the display panel by a COG method.

[0207]

10 As another external circuit, a video signal amplifier circuit 375 that amplifies a video signal among signals received by a tuner 374; a video signal processing circuit 376 that converts the signals outputted from the video signal amplifier circuit 375 into chrominance signals corresponding to respective colors of red, green, and blue; a control circuit 377 that converts the video signal into an input specification of the driver 15 IC; and the like are provided on an input side of the video signal. The control circuit 377 outputs a signal to both a scanning line side and a signal line side. In the case of digital driving, a structure may be employed in which a signal line dividing circuit 378 is provided on the signal line side and an input digital signal is divided into m pieces to be supplied.

20 [0208]

Among the signals received by the tuner 374, an audio signal is transmitted to an audio signal amplifier circuit 379, and an output thereof is supplied to a speaker 383 through an audio signal processing circuit 380. A control circuit 381 receives control information of a receiving station (received frequency) or a sound volume from an input

portion 382, and transmits signals to the tuner 374 and the audio signal processing circuit 380.

[0209]

Needless to say, the present invention is not limited to a television device, and 5 can be applied to monitors of personal computers, or display media having a large area, such as information display boards in railway stations, airports, and the like, and street-side advertisement display boards.

[0210]

As described above, a television device having high image quality and low 10 power consumption can be manufactured by applying the thin film transistor described in any of Embodiments 1 to 10 to either or both the main screen 333 and the sub screen 338.

[0211]

FIG. 26B illustrates one example of a cellular phone 341. The cellular phone 15 341 includes a display portion 342, an operation portion 343, and the like. The image quality thereof can be improved and the power consumption thereof can be reduced by applying, to the display portion 342, the thin film transistor described in any of Embodiments 1 to 10.

[0212]

20 A portable computer illustrated in FIG. 26C includes a main body 351, a display portion 352, and the like. The image quality thereof can be improved and the power consumption thereof can be reduced by applying, to the display portion 352, the thin film transistor described in Embodiment 1 or the like.

[0213]

FIG. 26D illustrates a desk lamp, which includes a lighting portion 361, a shade 362, an adjustable arm 363, a support 364, a base 365, a power source 366, and the like. The desk lamp is manufactured using, for the lighting portion 361, the light-emitting device which is described in the above embodiment. The image quality thereof can be improved and the power consumption thereof can be reduced by applying, to the lighting portion 361, the thin film transistor described in any of Embodiments 1 to 10.

[0214]

FIGS. 28A to 28C illustrate an example of a structure of a cellular phone, and the element substrate having the thin film transistor described in any of Embodiments 1 to 10 and the display device having the element substrate are applied to, for example, a display portion thereof. FIG. 28A is a front view, FIG. 28B is a rear view, and FIG. 28C is a development view. The cellular phone illustrated in FIG. 28A to 28C includes two housings, a housing 394 and a housing 385. The cellular phone illustrated in FIGS. 28A to 28C, which is also referred to as a smartphone, has both of functions of a cellular phone and a portable information terminal, incorporates a computer, and can perform a variety of data processing in addition to voice calls.

[0215]

The cellular phone includes two housings 394 and 385. The housing 394 includes a display portion 386, a speaker 387, a microphone 388, operation keys 389, a pointing device 390, a front camera lens 391, a jack 392 for an external connection terminal, an earphone terminal 393, and the like, while the housing 385 includes a keyboard 395, an external memory slot 396, a rear camera 397, a light 398, and the like. In addition, an antenna is incorporated in the housing 394.

[0216]

In addition to the structure described above, a non-contact IC chip, a small size memory device, or the like can be incorporated therein.

[0217]

The housings 394 and 385 are overlapped with each other in FIG. 28A and slid from a state illustrated in FIG. 28A, and the cellular phone is opened as illustrated in FIG. 28C. In the display portion 386, the display device described in any of Embodiments 1 to 10 can be incorporated, and display direction can be changed as appropriate depending on a use mode. Note that since the front camera lens 391 is provided in the same plane as the display portion 386, the cellular phone can be used as a videophone. A still image and a moving image can be taken by the rear camera 397 and the light 398 by using the display portion 386 as a viewfinder.

[0218]

The speaker 387 and the microphone 388 can be used for videophone, recording and playing sound, and the like without being limited to voice calls. With the use of the operation keys 389, operation of incoming and outgoing calls, simple information input such as electronic mail, scrolling of a screen, cursor motion, and the like are possible.

[0219]

If much information needs to be treated, such as documentation, use as a portable information terminal, and the like, it is convenient to use the keyboard 395. The housings 394 and 385 that are overlapped with each other (FIG. 28A) can be slid and the cellular phone is opened as illustrated in FIG. 28C, so that the cellular phone can be used as an information terminal. In addition, with the use of the keyboard 395 and the pointing device 390, smooth operation is possible. An AC adaptor and various

types of cables such as a USB cable can be connected to the jack 392 for an external connection terminal, through which charging and data communication with a personal computer or the like are possible. Moreover, by inserting a recording medium into the external memory slot 396, a large amount of data can be stored and transferred.

5 [0220]

In the rear surface of the housing 385 (FIG. 28B), the rear camera 397 and the light 398 are provided, and a still image and a moving image can be taken by using the display portion 386 as a viewfinder.

[0221]

10 Further, the cellular phone may have an infrared communication function, a USB port, a function of receiving one segment television broadcast, a non-contact IC chip, an earphone jack, or the like, in addition to the above structures.

[0222]

The image quality thereof can be improved and the power consumption thereof  
15 can be reduced by applying, to a pixel, the thin film transistor described in any of  
Embodiments 1 to 10.

[0223]

The present application is based on Japanese Patent Application serial No. 2008-169499 and Japanese Patent Application serial No. 2008-228242 which are filed  
20 with Japan Patent Office on June 27, 2008 and September 5, 2008, respectively, the entire contents of which are hereby incorporated by reference.

## CLAIMS

## 1. A thin film transistor comprising:

a gate insulating layer which covers a gate electrode over a substrate having an

5 insulating surface;

a first semiconductor layer which is in contact with the gate insulating layer;

a second semiconductor layer which is stacked over the first semiconductor  
layer; and

impurity semiconductor layers forming a source region and a drain region

10 which are in contact with part of the second semiconductor layer,

wherein the second semiconductor layer comprises an amorphous

semiconductor layer having an NH group or an NH<sub>2</sub> group.

2. The thin film transistor according to claim 1, wherein different

15 semiconductor atoms included in the second semiconductor layer are cross-linked with  
the NH group.

3. The thin film transistor according to claim 1, wherein different dangling

bonds in semiconductor atoms included in the second semiconductor layer are

20 terminated with the NH<sub>2</sub> group.

4. The thin film transistor according to claim 1, wherein the first semiconductor

layer is a microcrystalline semiconductor layer.

5. The thin film transistor according to claim 1, wherein the first semiconductor layer is a dispersed microcrystalline semiconductor layer or a net-like microcrystalline semiconductor layer.

5 6. The thin film transistor according to claim 1, wherein an oxygen concentration of the second semiconductor layer which is measured by secondary ion mass spectrometry is less than or equal to  $5 \times 10^{18} \text{ cm}^{-3}$ .

7. A thin film transistor comprising:

10 a gate insulating layer which is in contact with a gate electrode over a substrate having an insulating surface;

a semiconductor layer which is in contact with the gate insulating layer;

impurity semiconductor layers forming a source region and a drain region; and

15 a buffer layer which is formed between the semiconductor layer and the impurity semiconductor layers ,

wherein the buffer layer comprises an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group.

8. The thin film transistor according to claim 7, wherein different 20 semiconductor atoms included in the buffer layer are cross-linked with the NH group.

9. The thin film transistor according to claim 7, wherein different dangling bonds in semiconductor atoms included in the buffer layer are terminated with the NH<sub>2</sub> group.

10. The thin film transistor according to claim 7, wherein the semiconductor layer is a microcrystalline semiconductor layer.

5 11. The thin film transistor according to claim 7, wherein the semiconductor layer is a dispersed microcrystalline semiconductor layer or a net-like microcrystalline semiconductor layer.

10 12. The thin film transistor according to claim 7, wherein an oxygen concentration of the buffer layer which is measured by secondary ion mass spectrometry is less than or equal to  $5 \times 10^{18} \text{ cm}^{-3}$ .

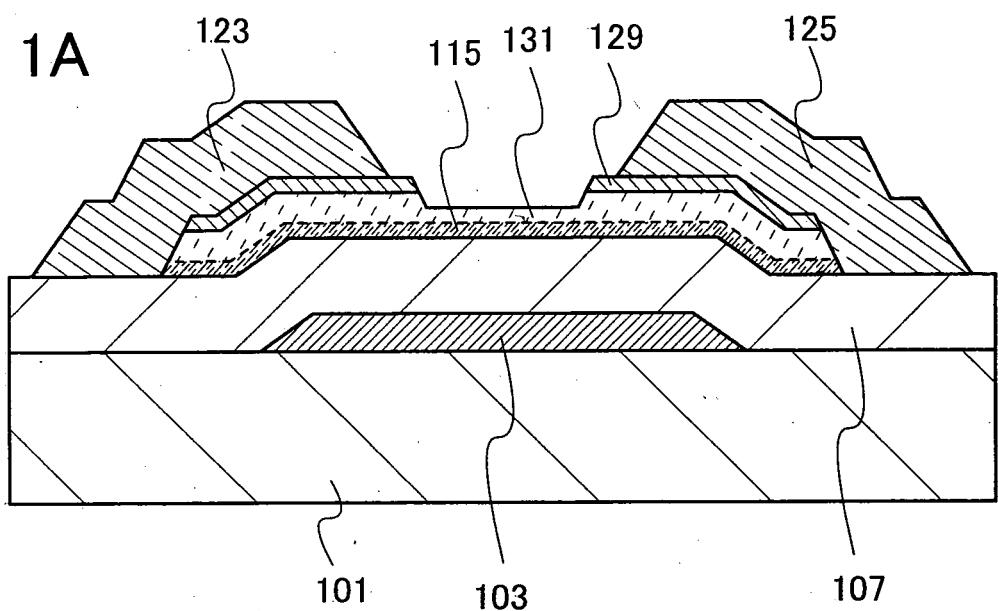
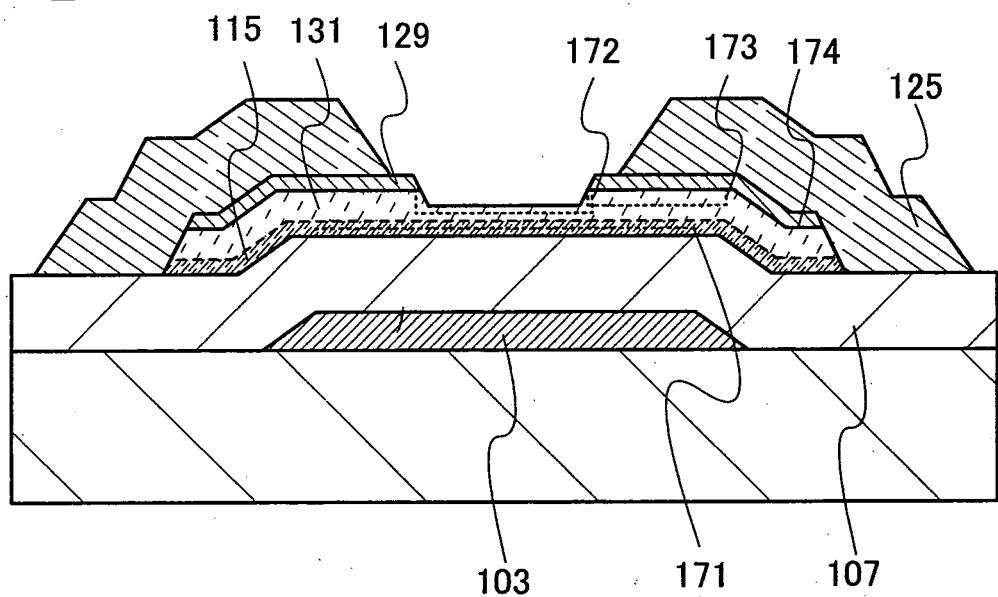
15 13. The thin film transistor according to claim 1 or claim 7, wherein an NH group is included in the impurity semiconductor layers forming the source region and the drain region.

14. A semiconductor device comprising:  
a thin film transistor comprising:  
a gate insulating layer which covers a gate electrode over a substrate  
20 having an insulating surface;  
a first semiconductor layer which is in contact with the gate insulating layer;  
a second semiconductor layer which is stacked over the first semiconductor layer; and

impurity semiconductor layers forming a source region and a drain region which are in contact with part of the second semiconductor layer, wherein the second semiconductor layer comprises an amorphous semiconductor layer having an NH group or an NH<sub>2</sub> group.

5

15. An electronic device having the semiconductor device according to claim 14, wherein the electronic device is selected from the group consisting of a television device, a cellular phone, a portable computer, and a desk lamp.

**FIG. 1A****FIG. 1B**

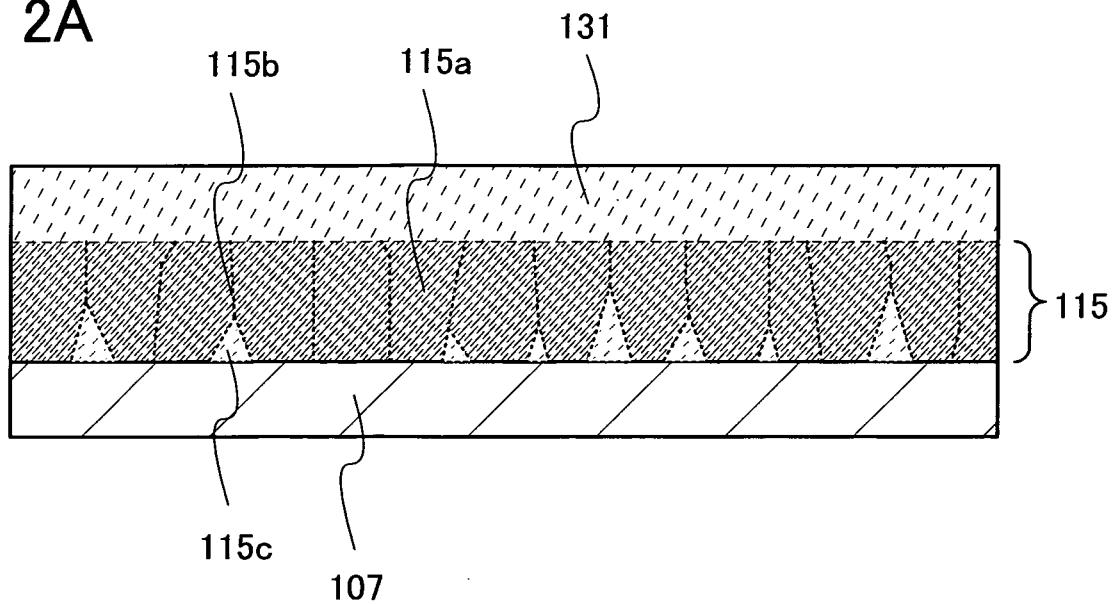
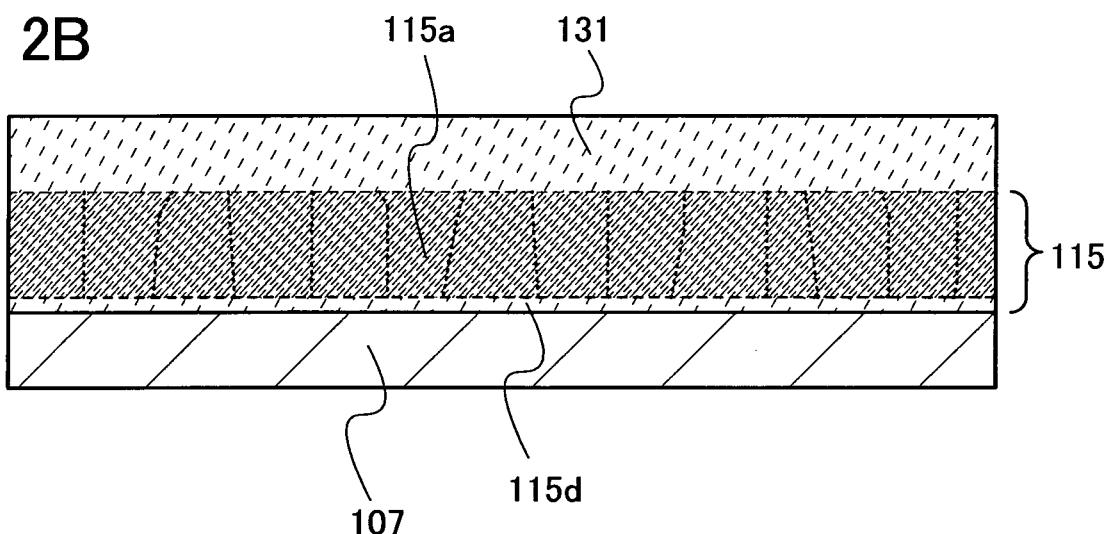
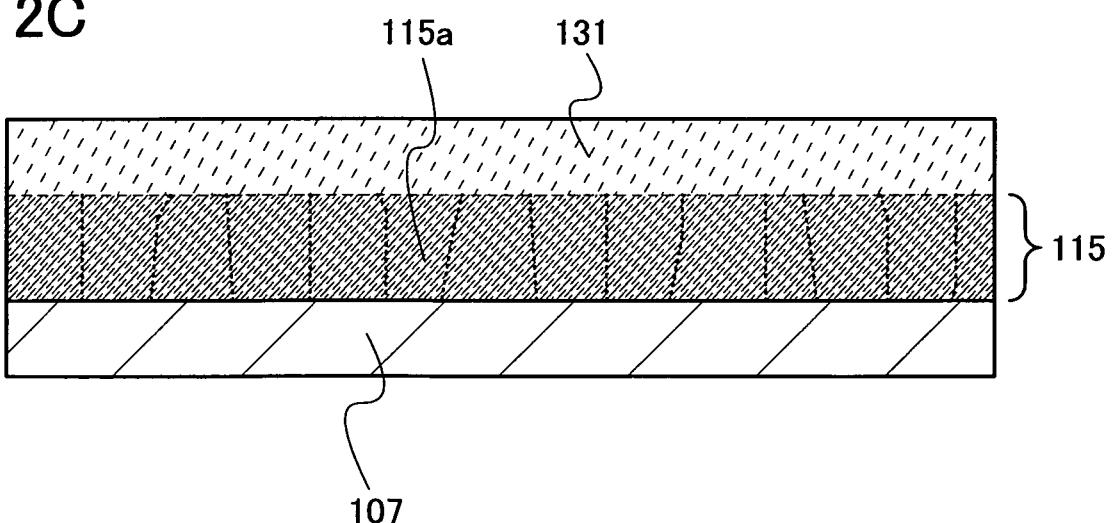
**FIG. 2A****FIG. 2B****FIG. 2C**

FIG. 3

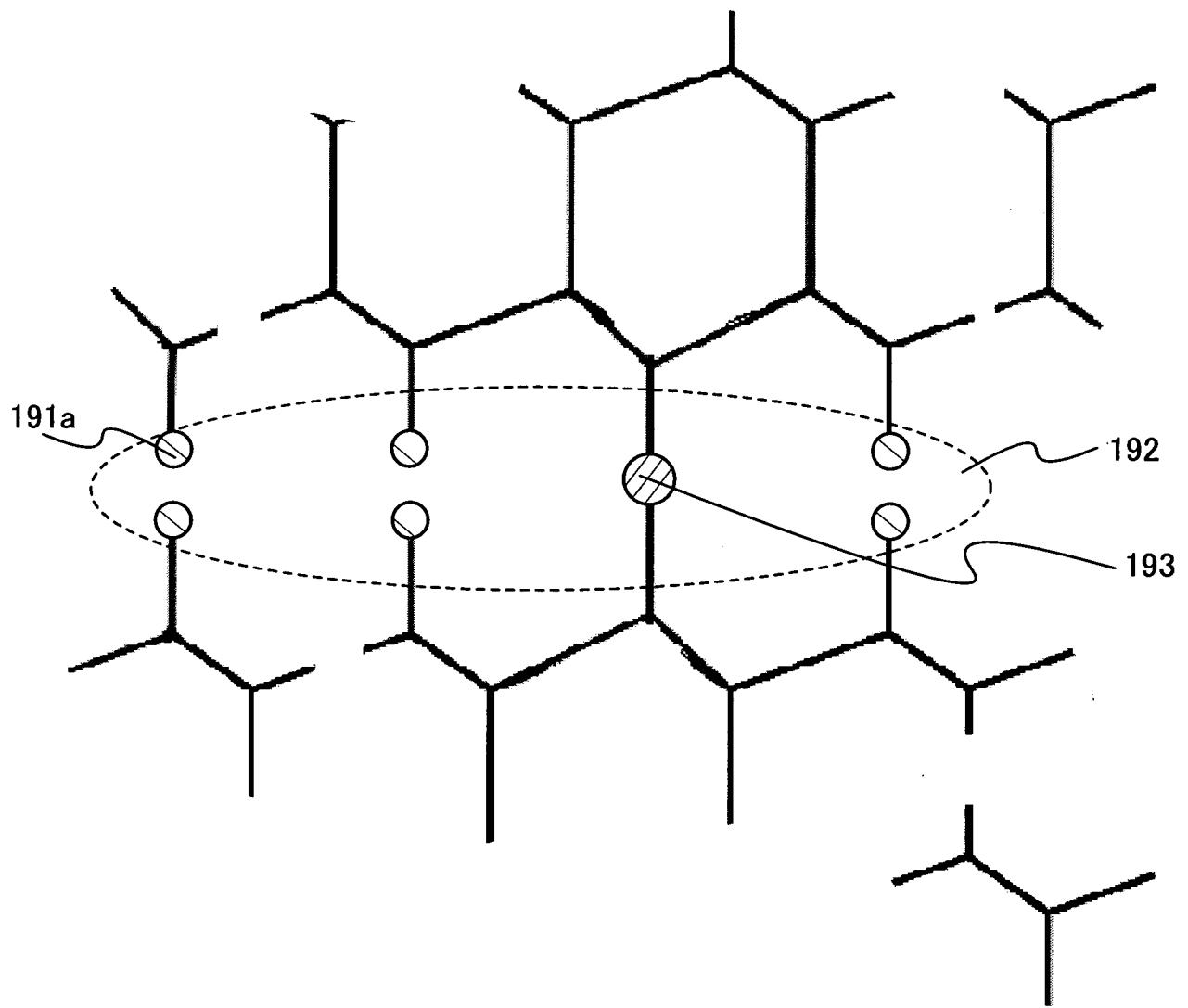


FIG. 4

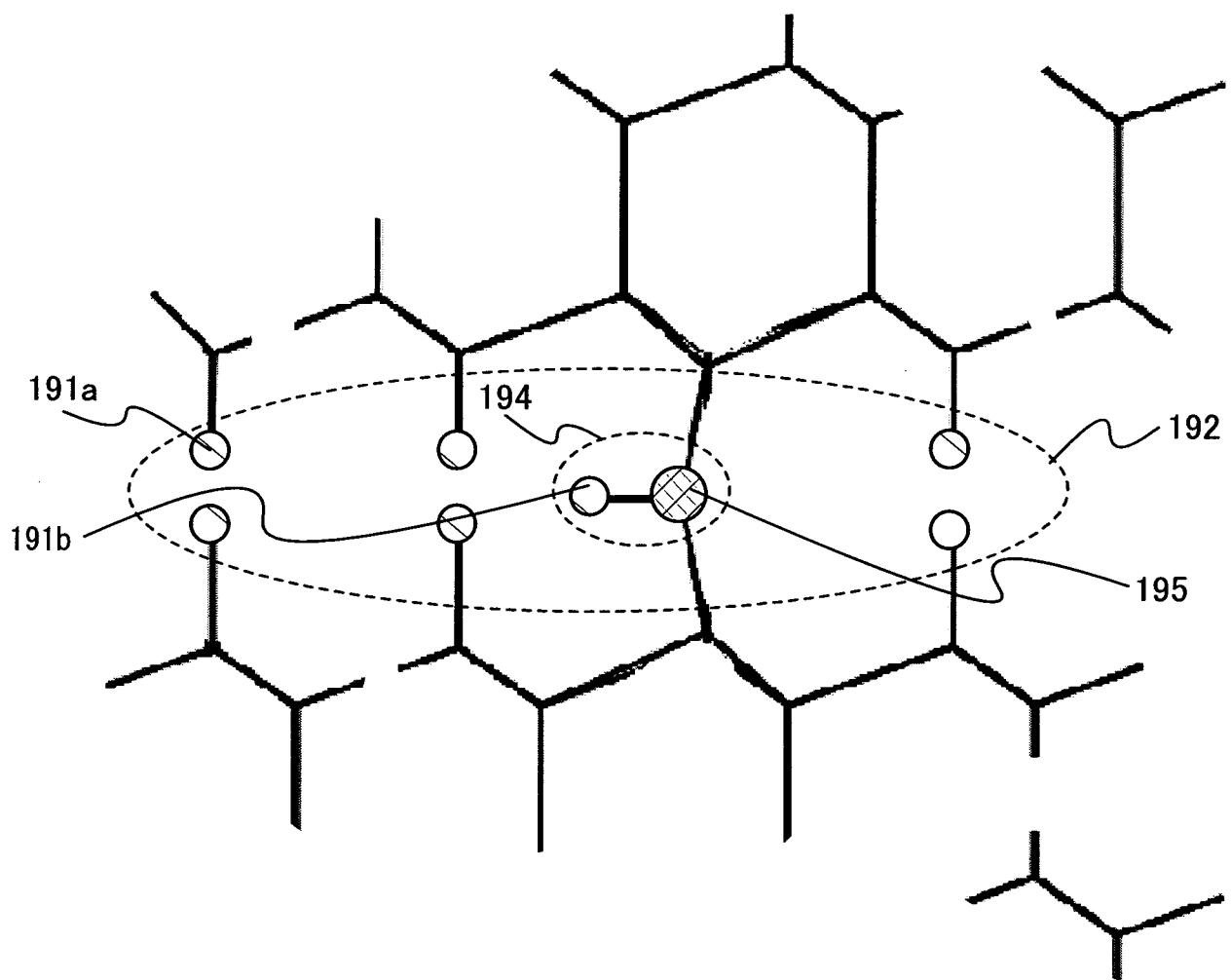


FIG. 5

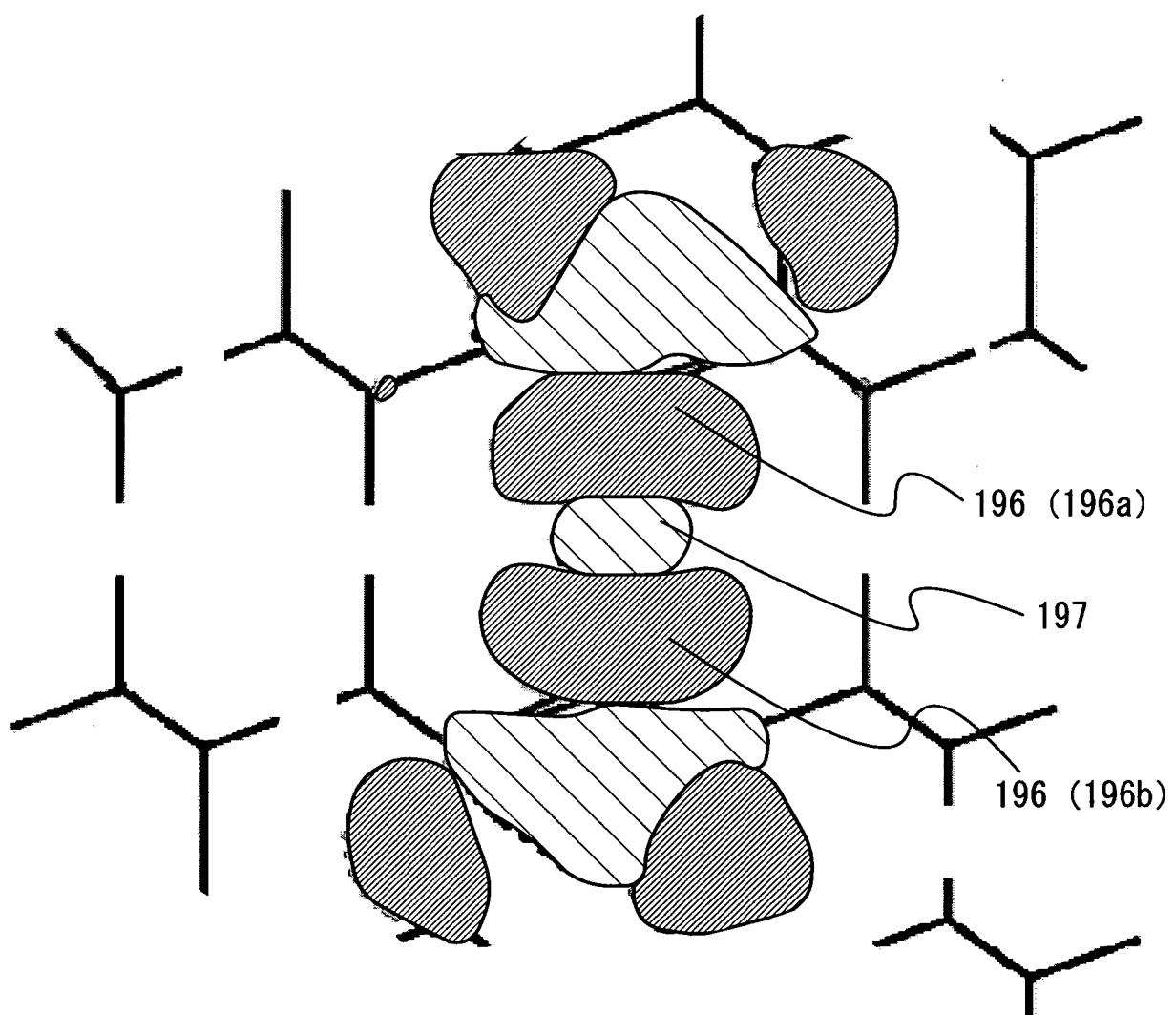
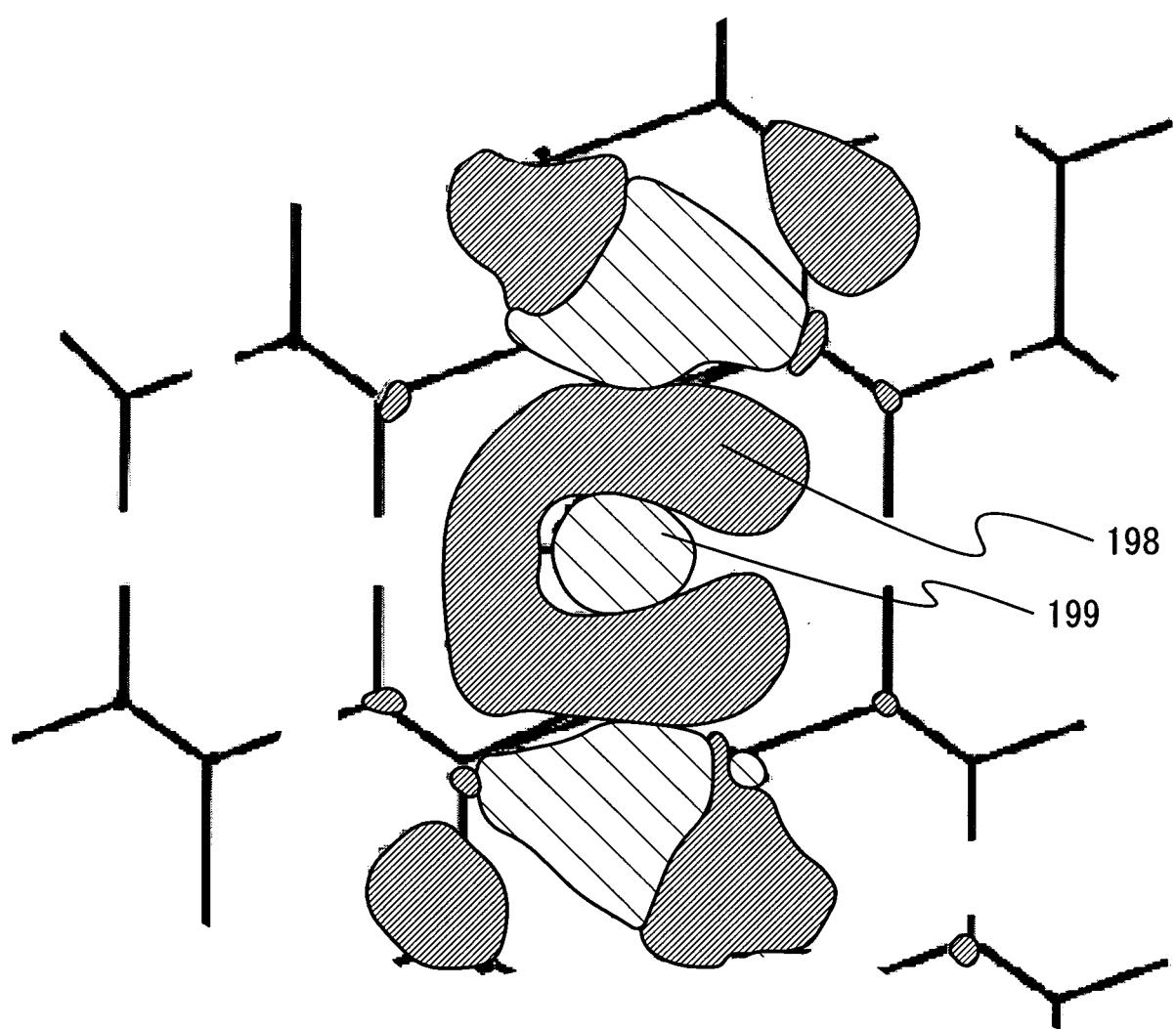
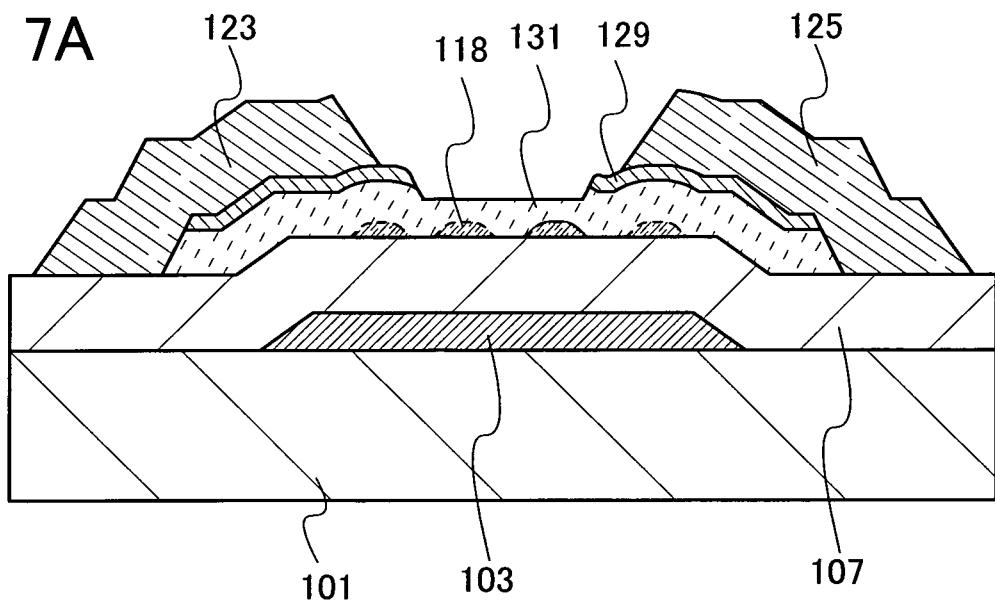
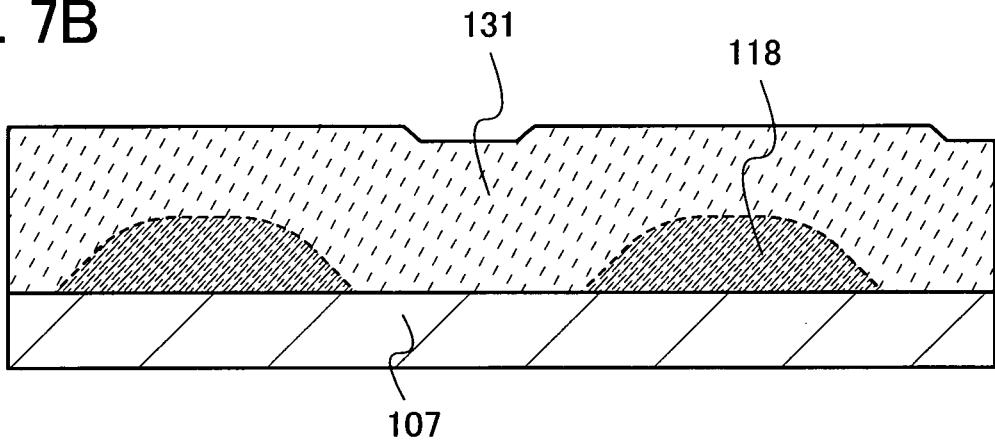
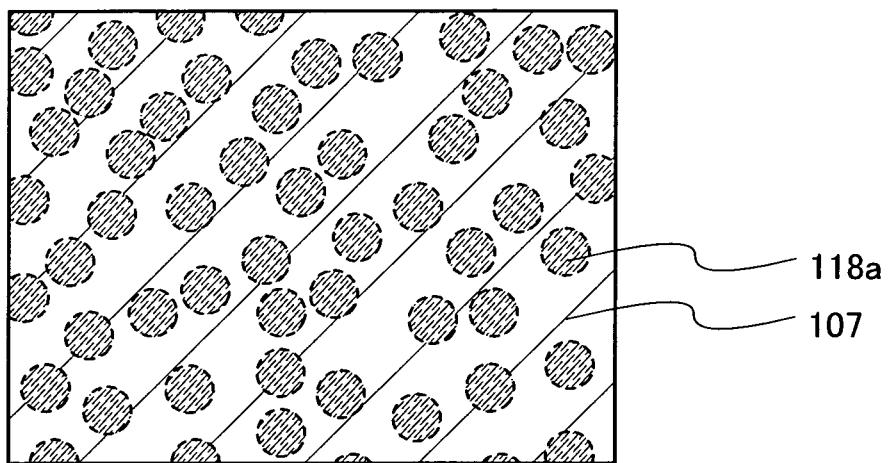
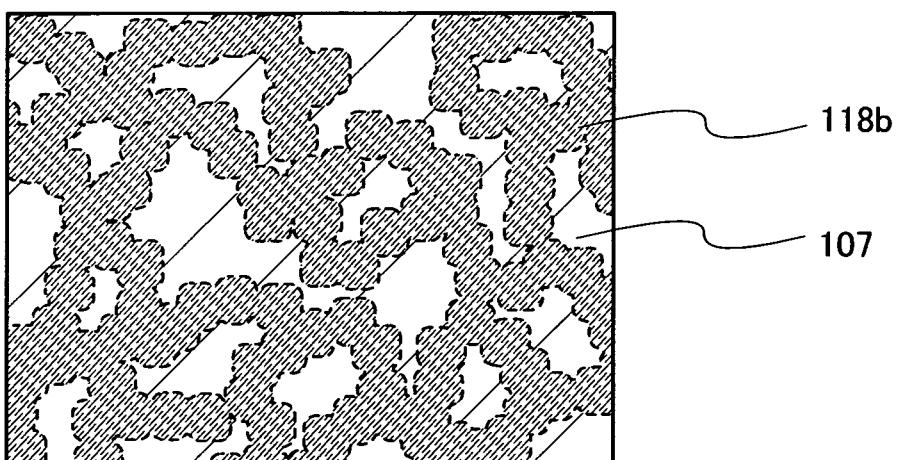
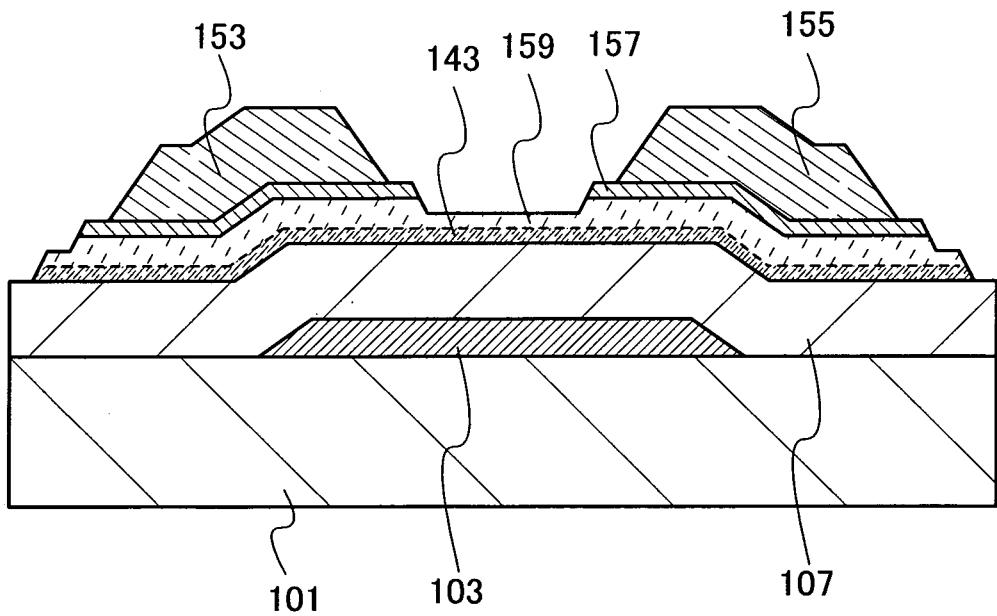
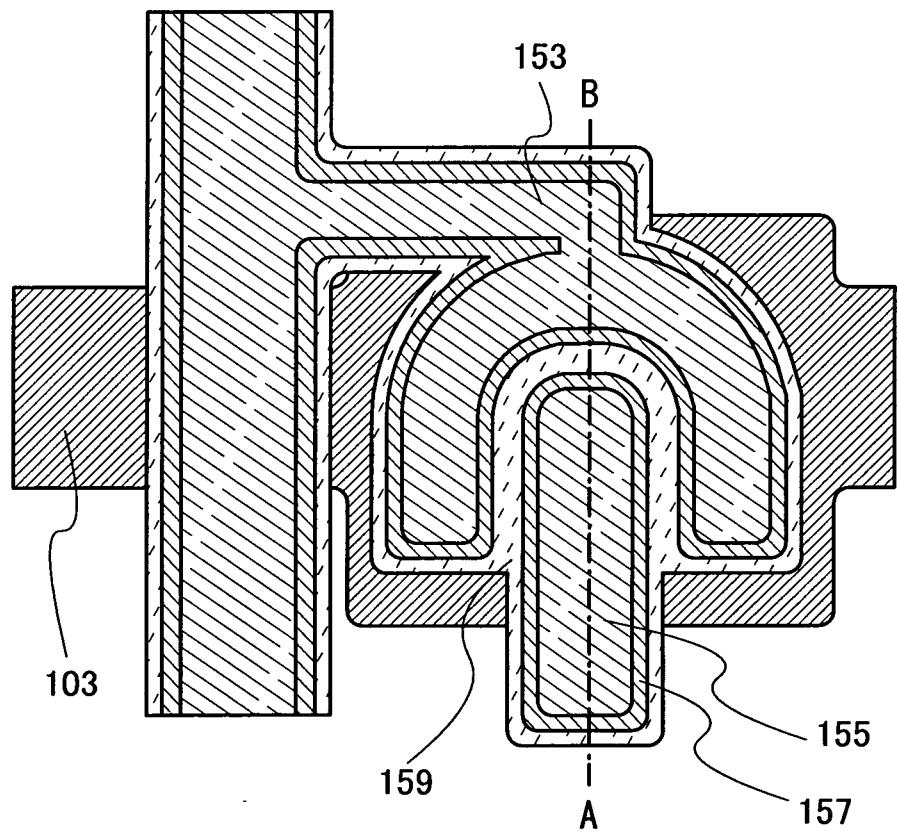


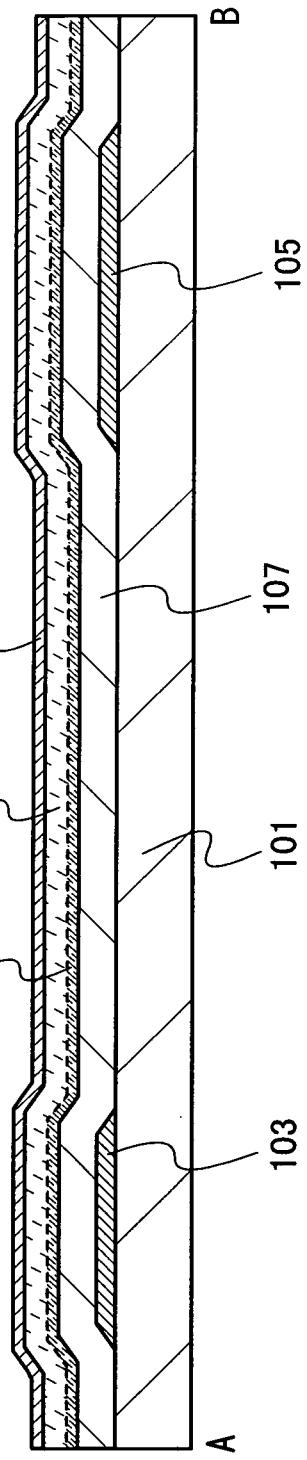
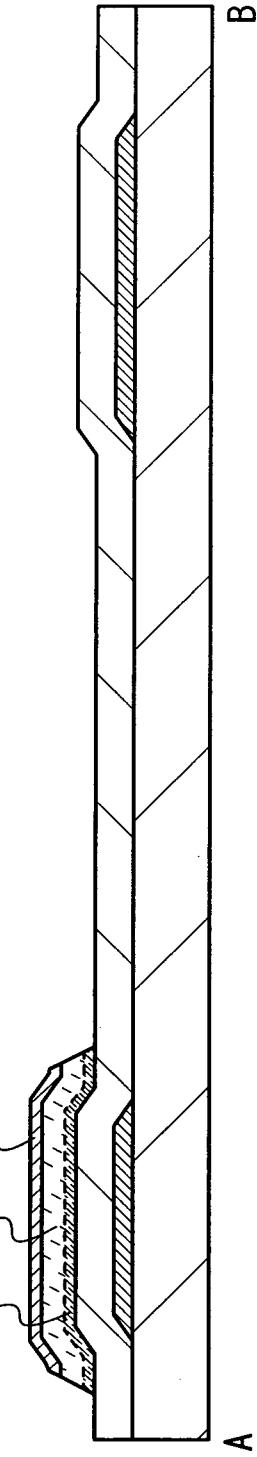
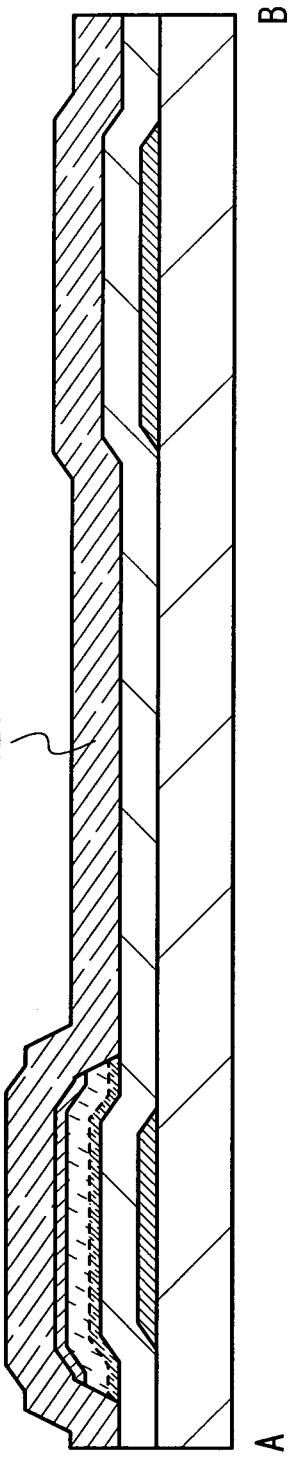
FIG. 6



**FIG. 7A****FIG. 7B**

**FIG. 8A****FIG. 8B**

**FIG. 9A****FIG. 9B**

**FIG. 10A****FIG. 10B****FIG. 10C**

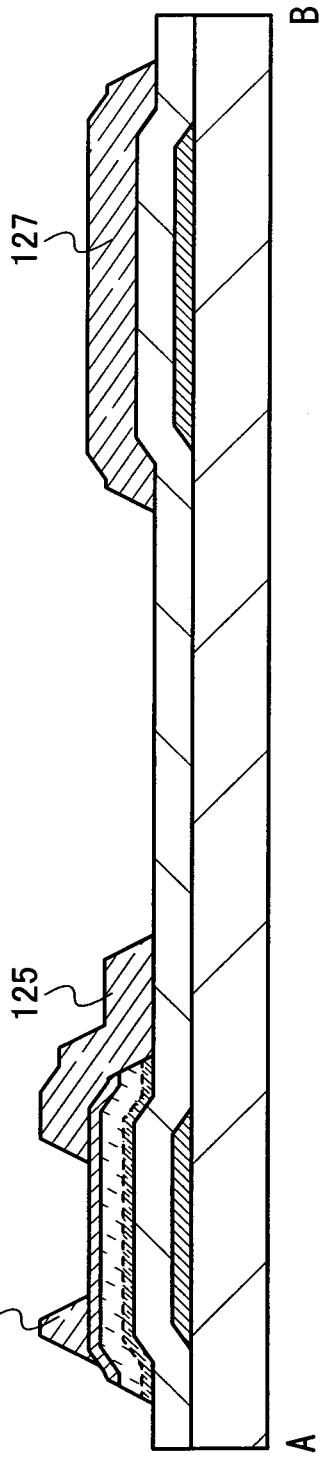
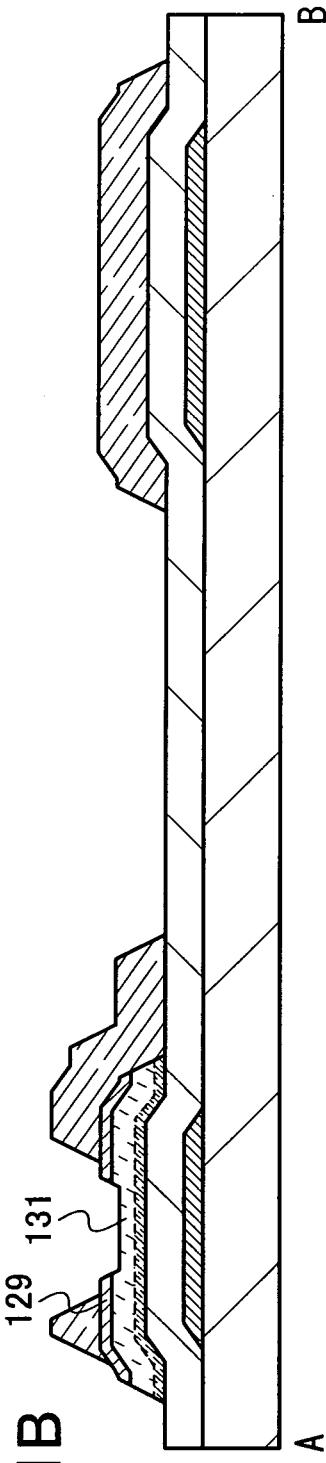
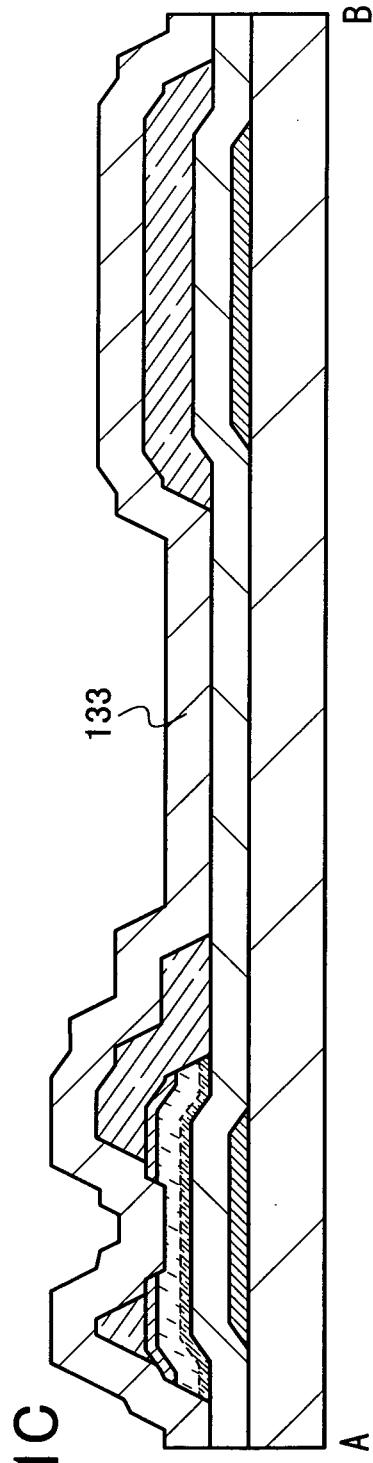
**FIG. 11A****FIG. 11B****FIG. 11C**

FIG. 12A

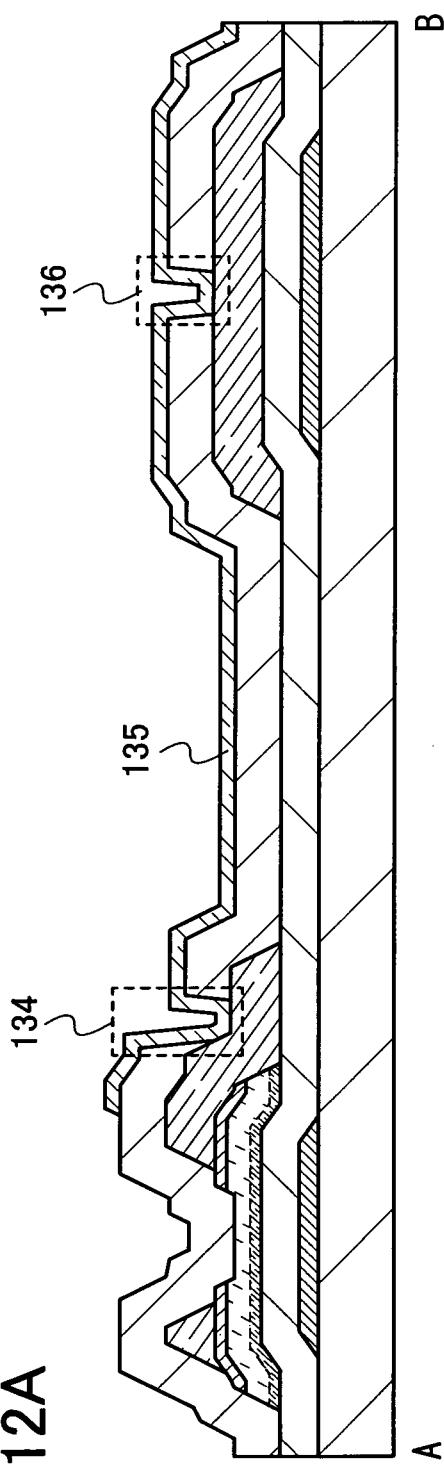


FIG. 12B

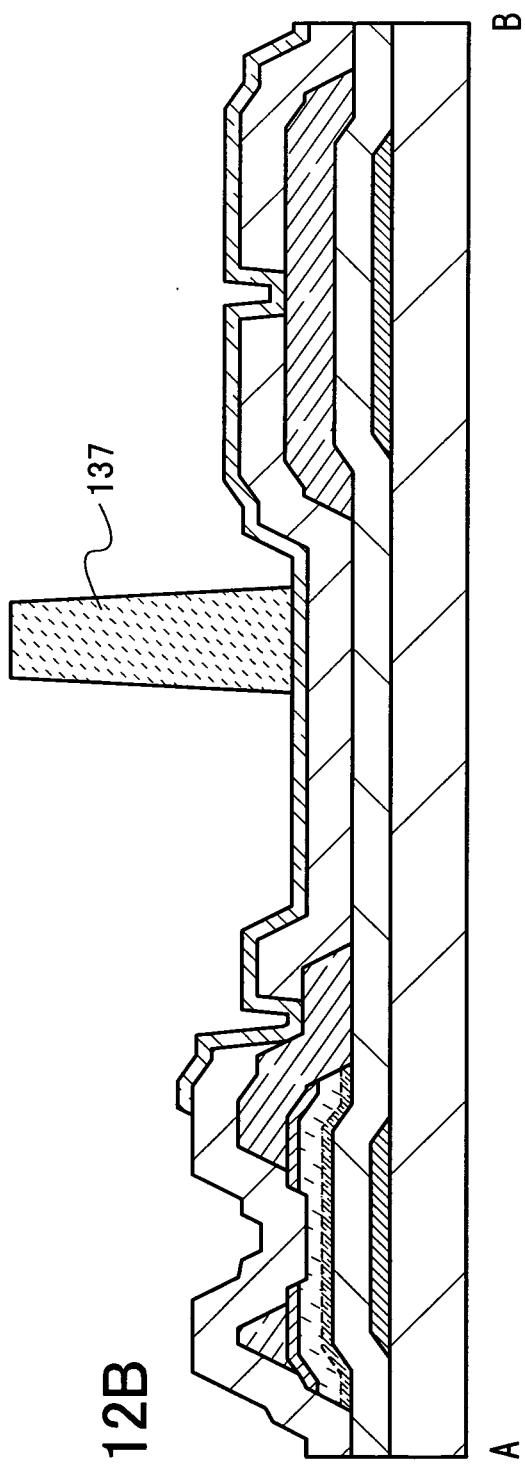


FIG. 13A

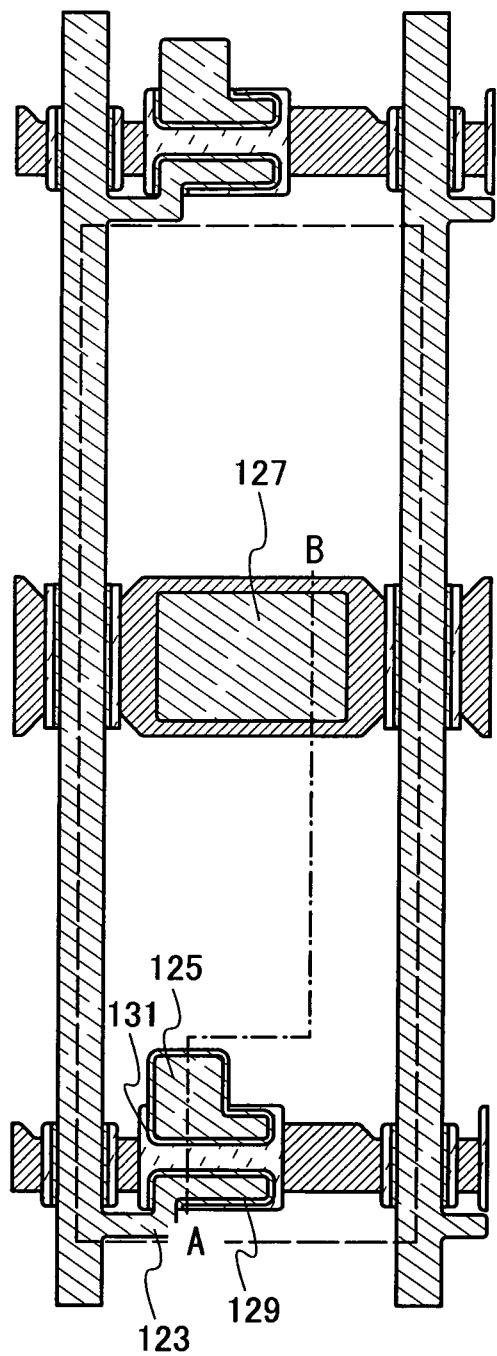


FIG. 13B

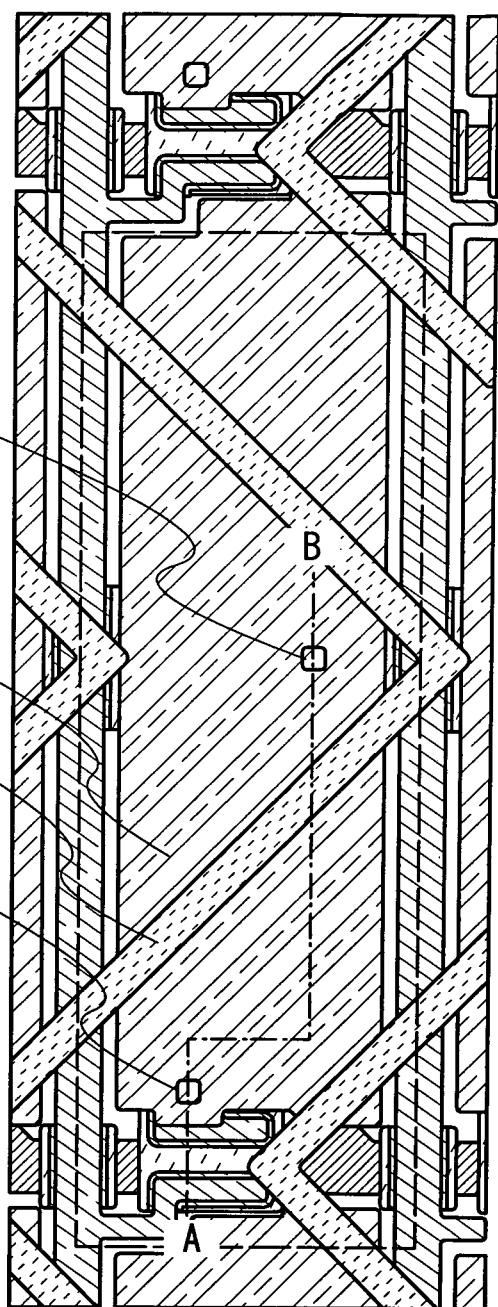


FIG. 14

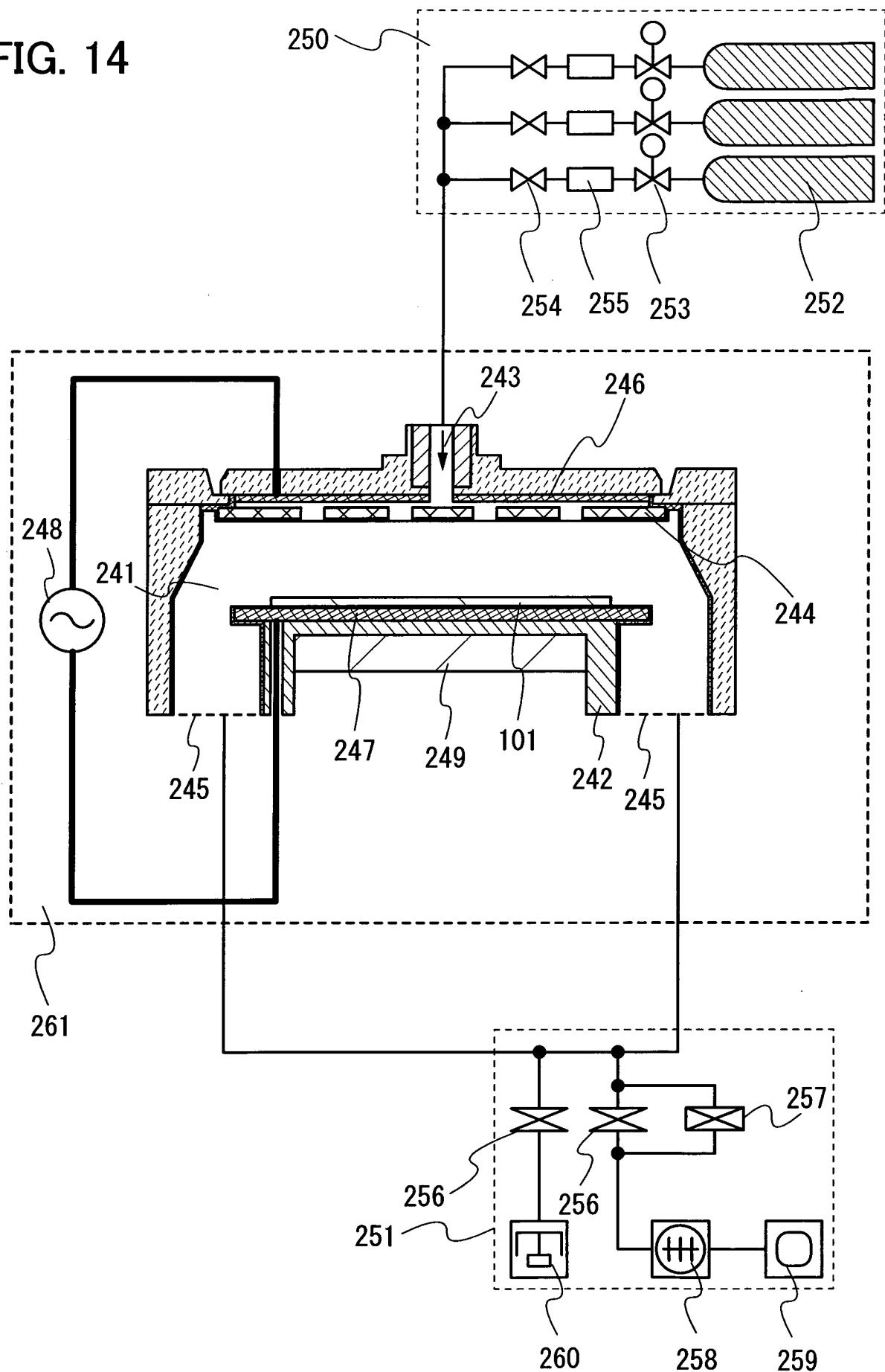


FIG. 15

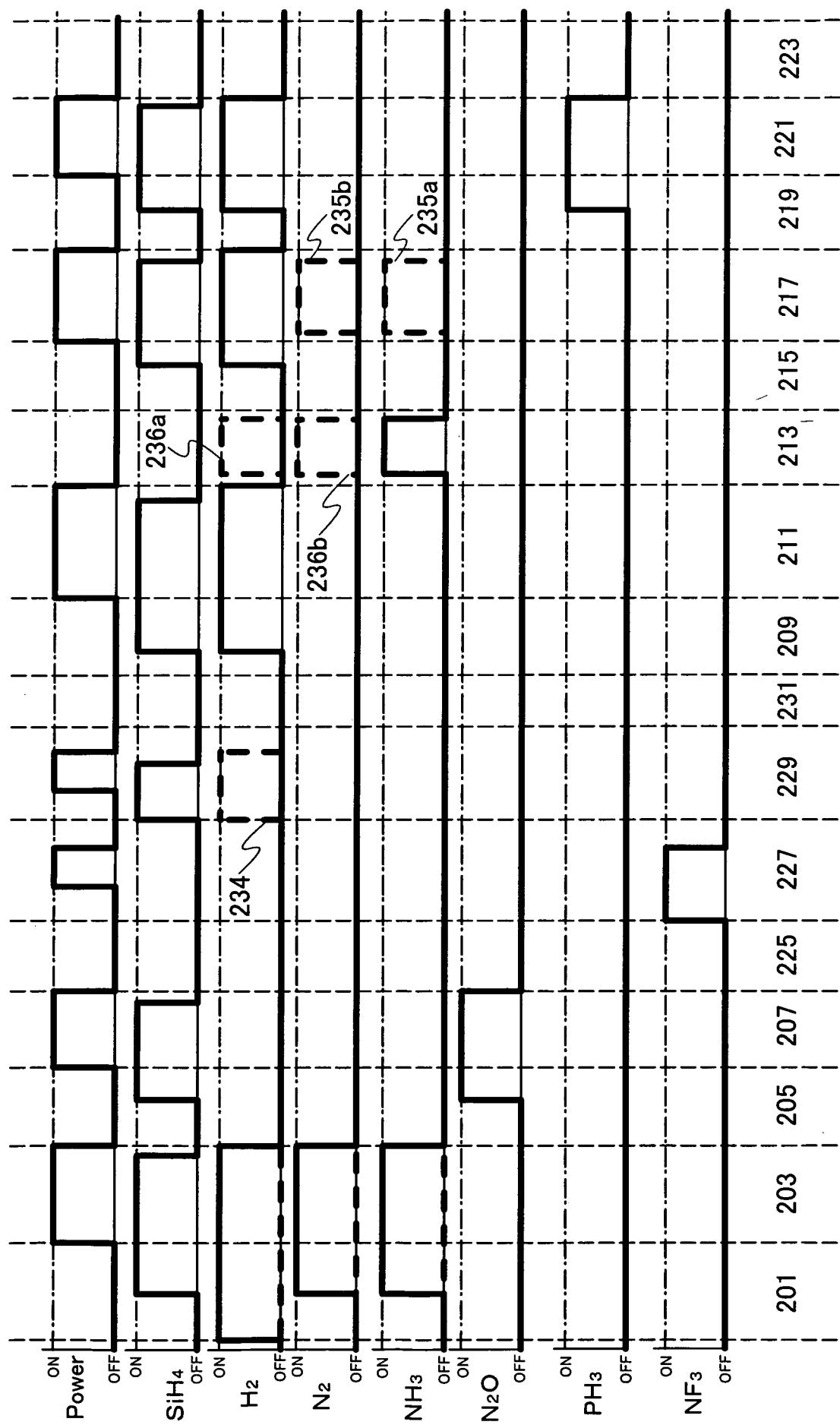
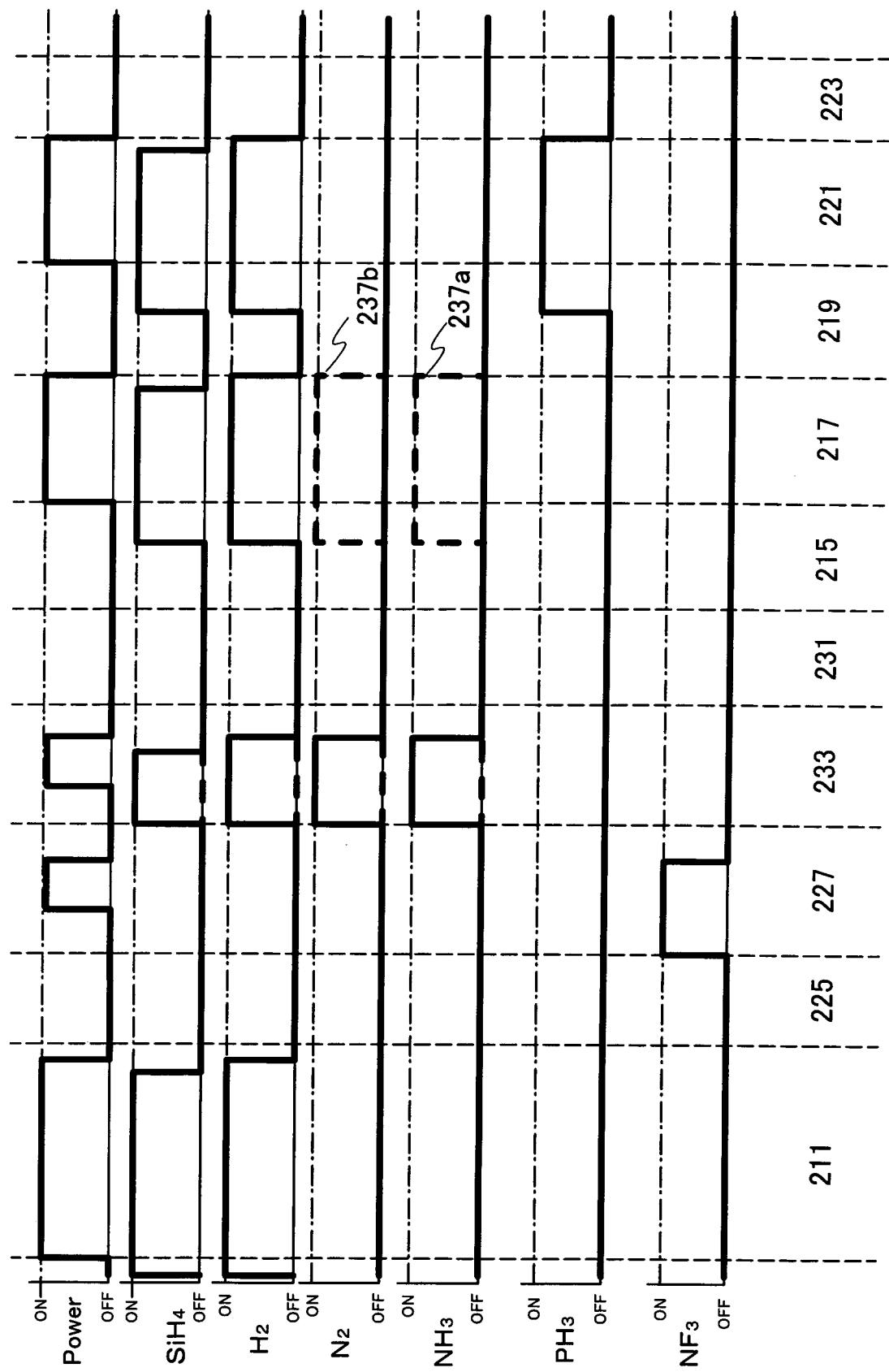


FIG. 16



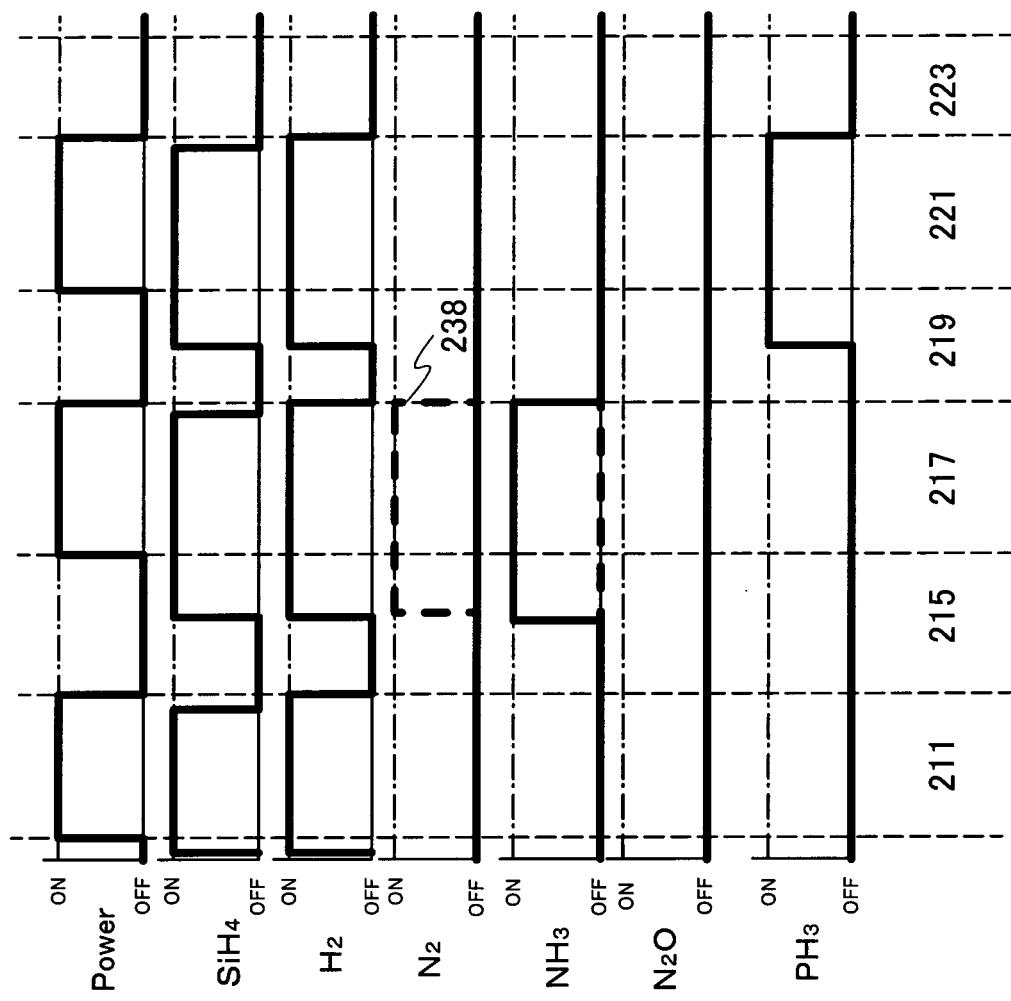


FIG. 17

FIG. 18

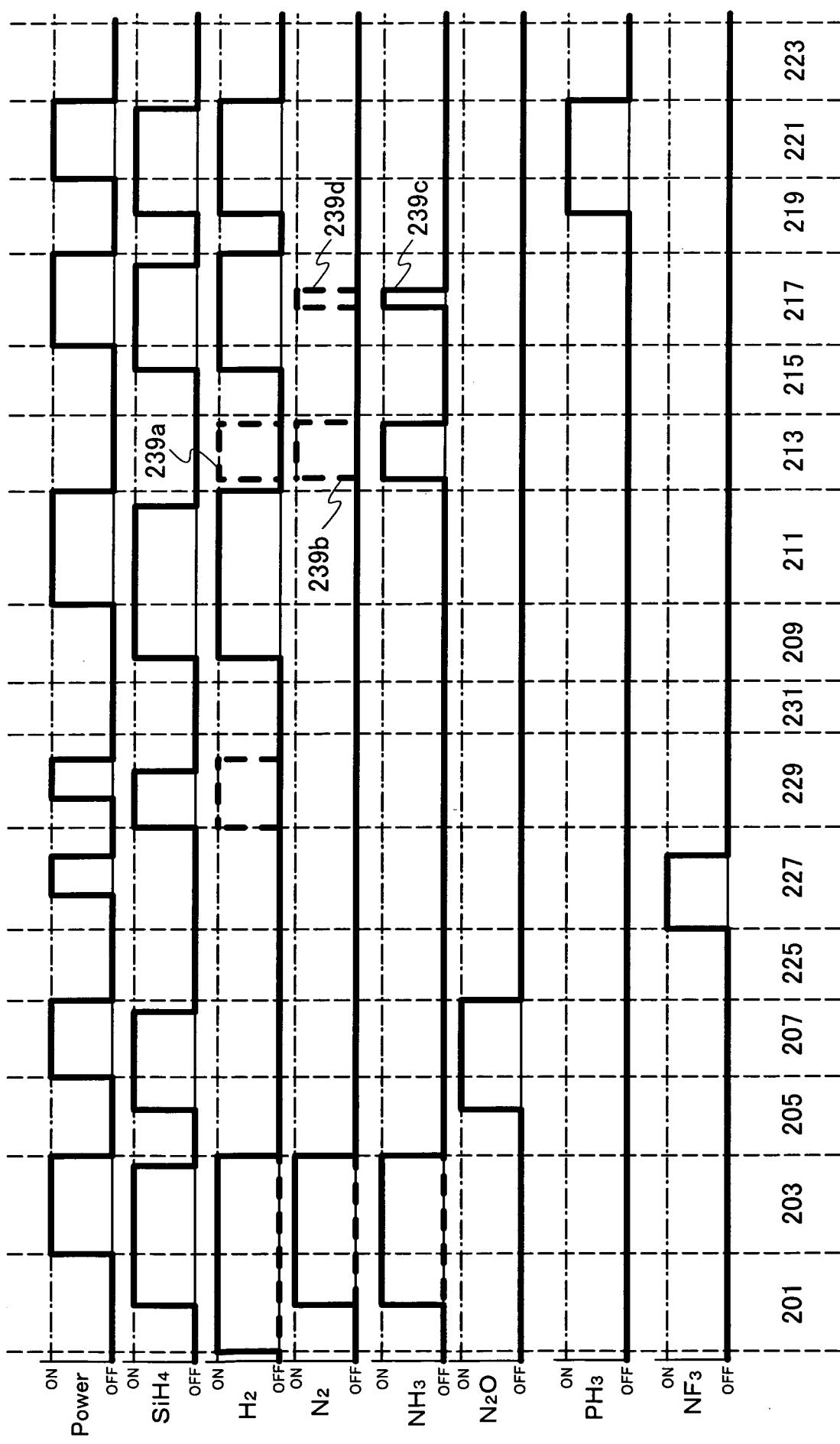


FIG. 19

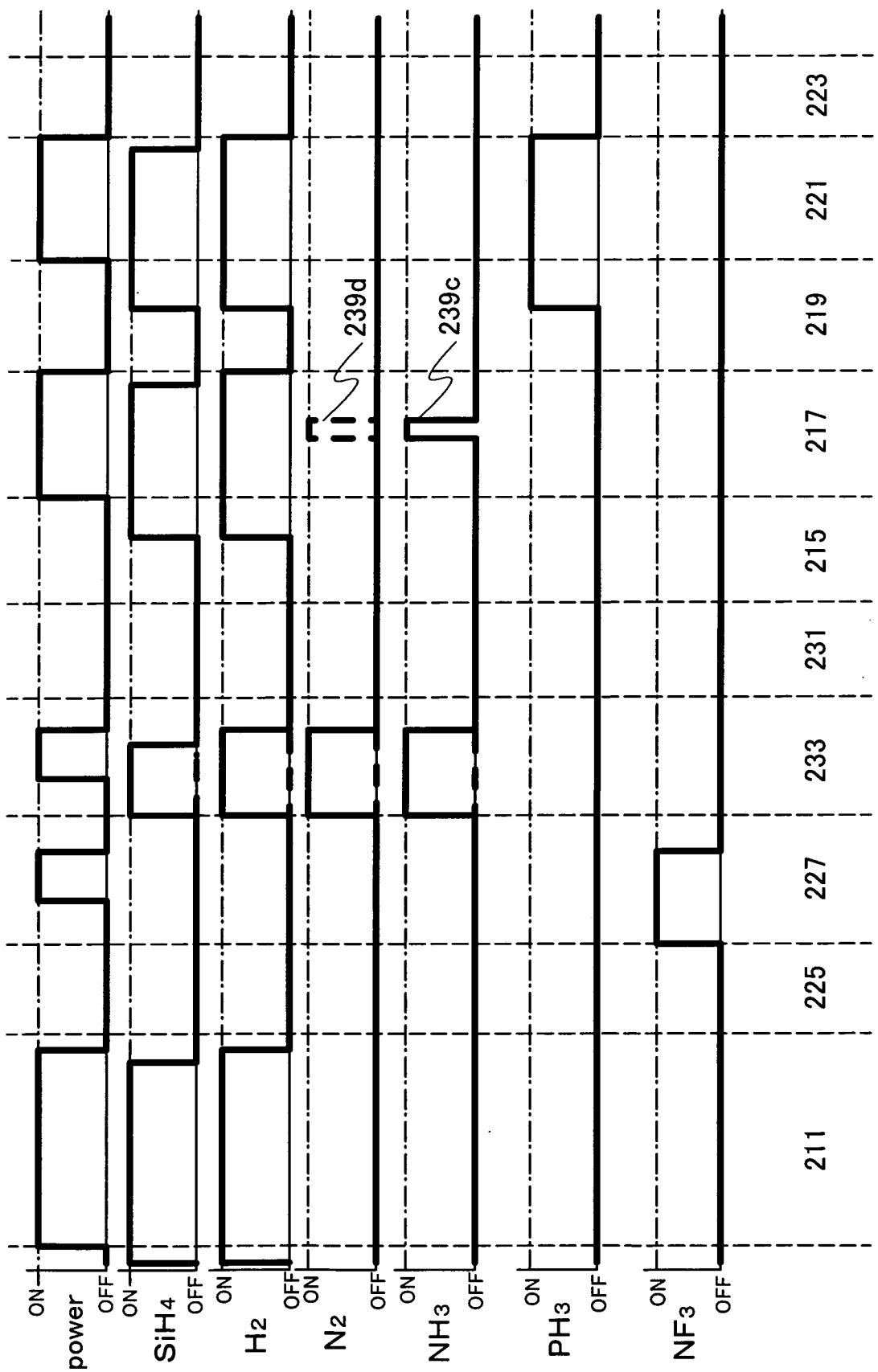


FIG. 20A

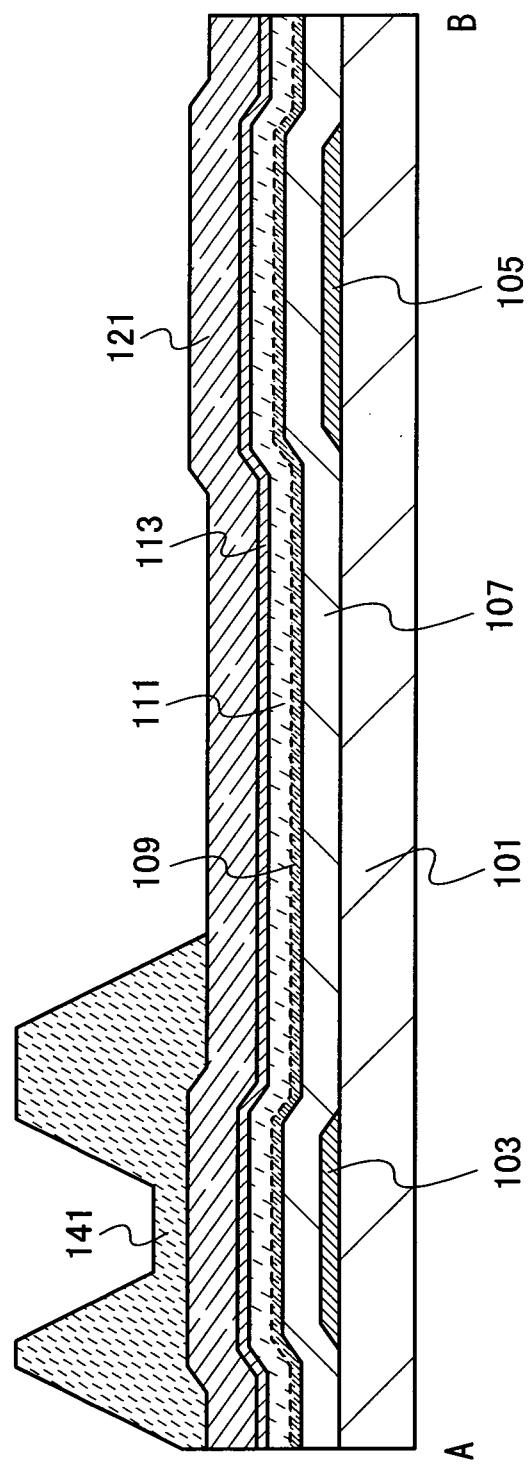
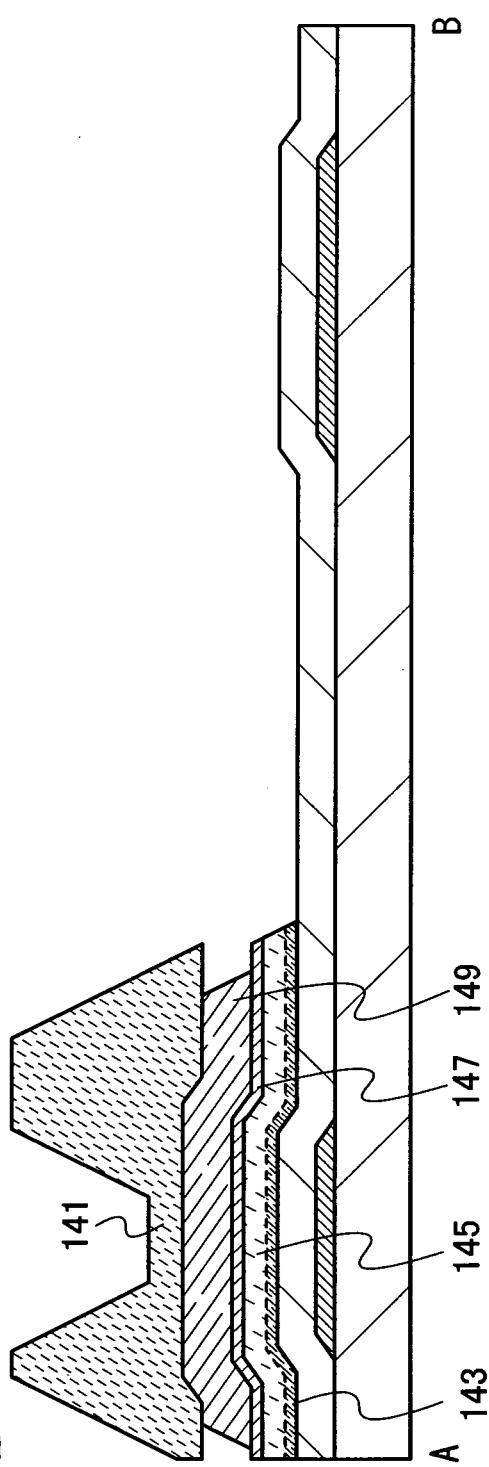


FIG. 20B



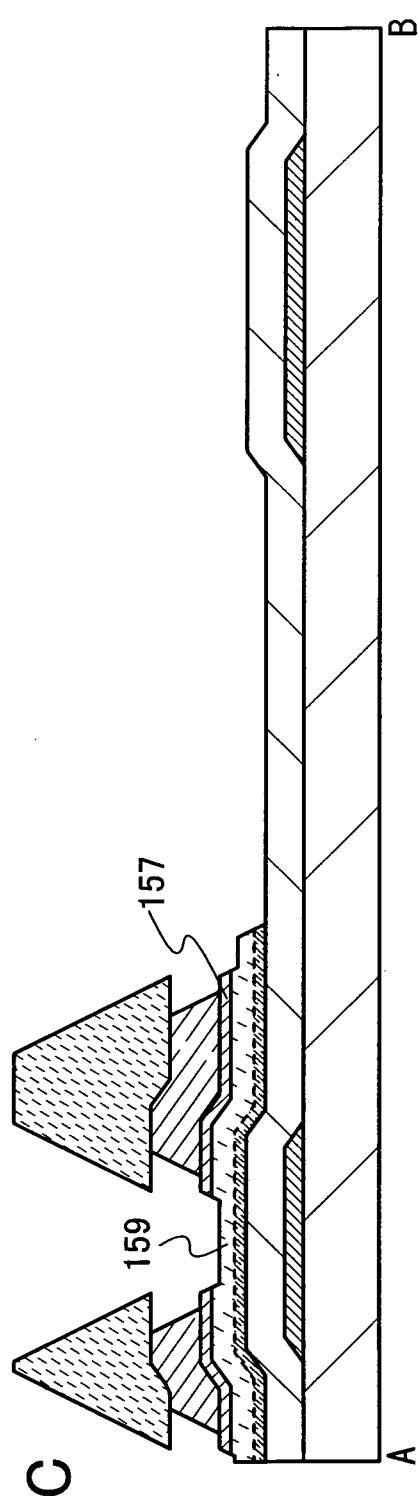
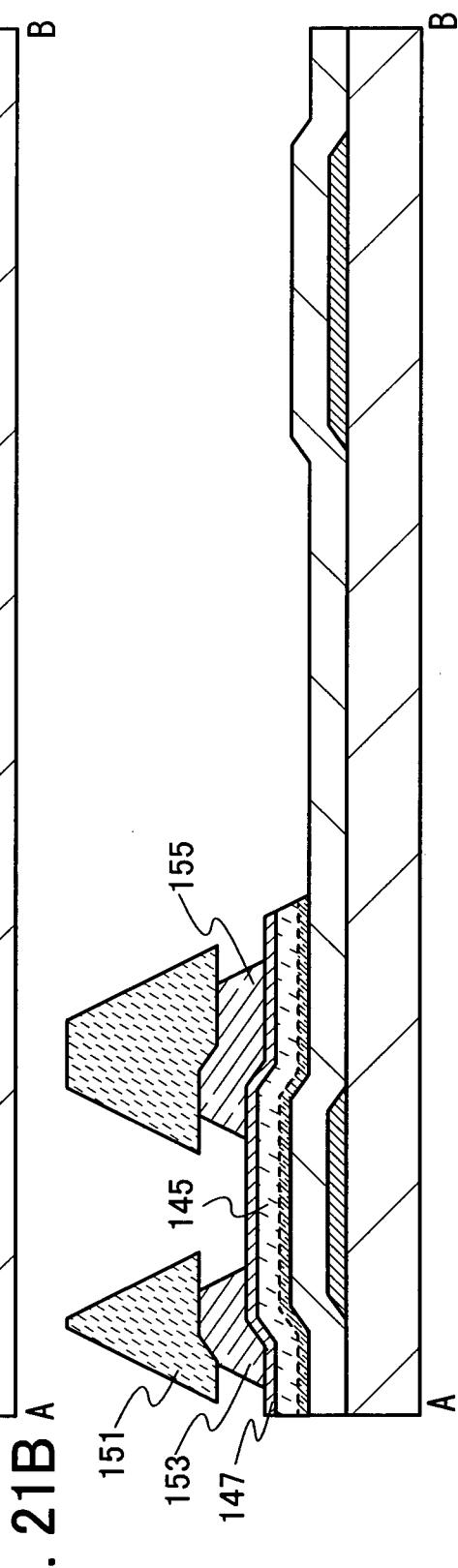
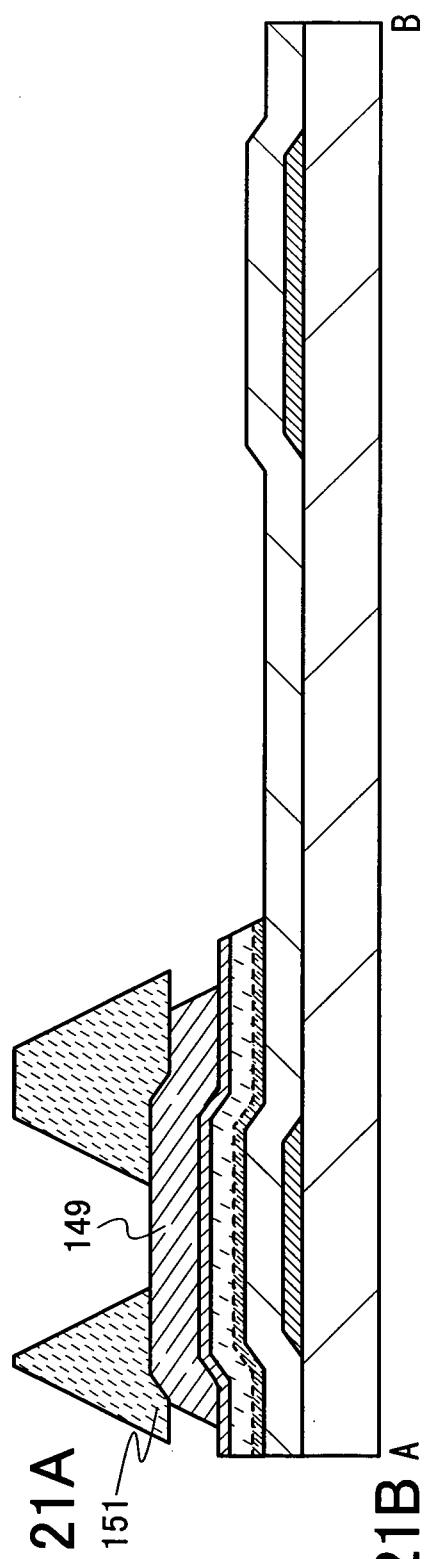


FIG. 22A

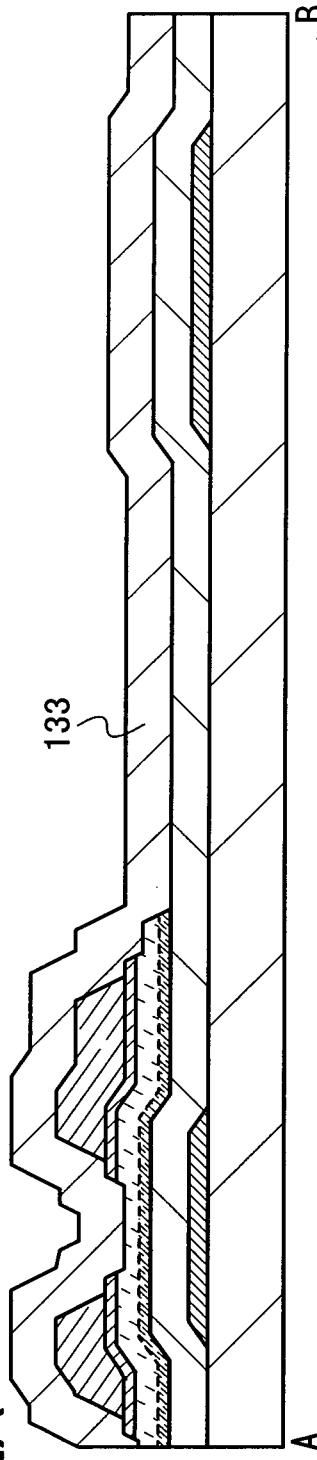


FIG. 22B

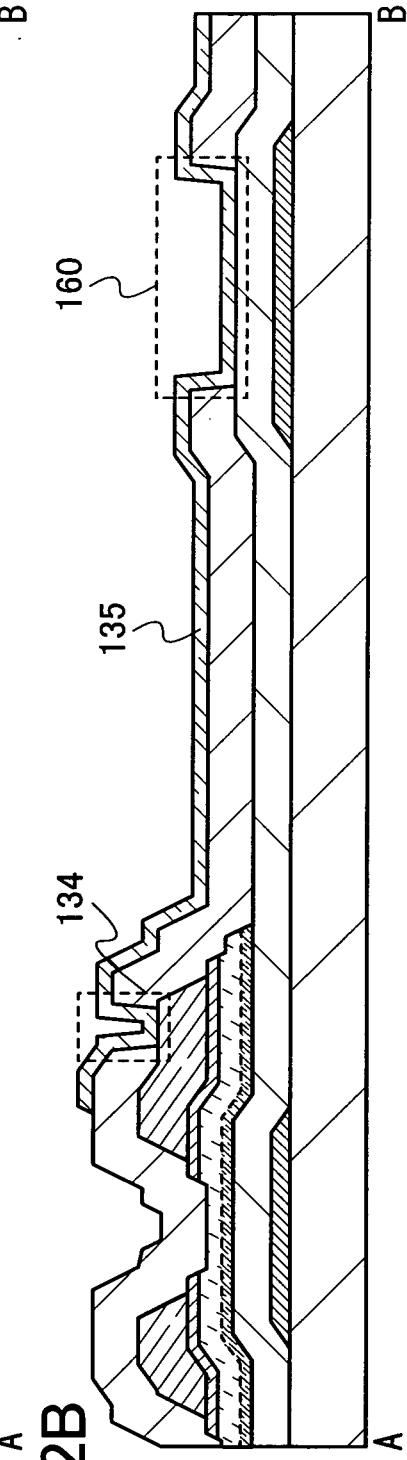


FIG. 22C

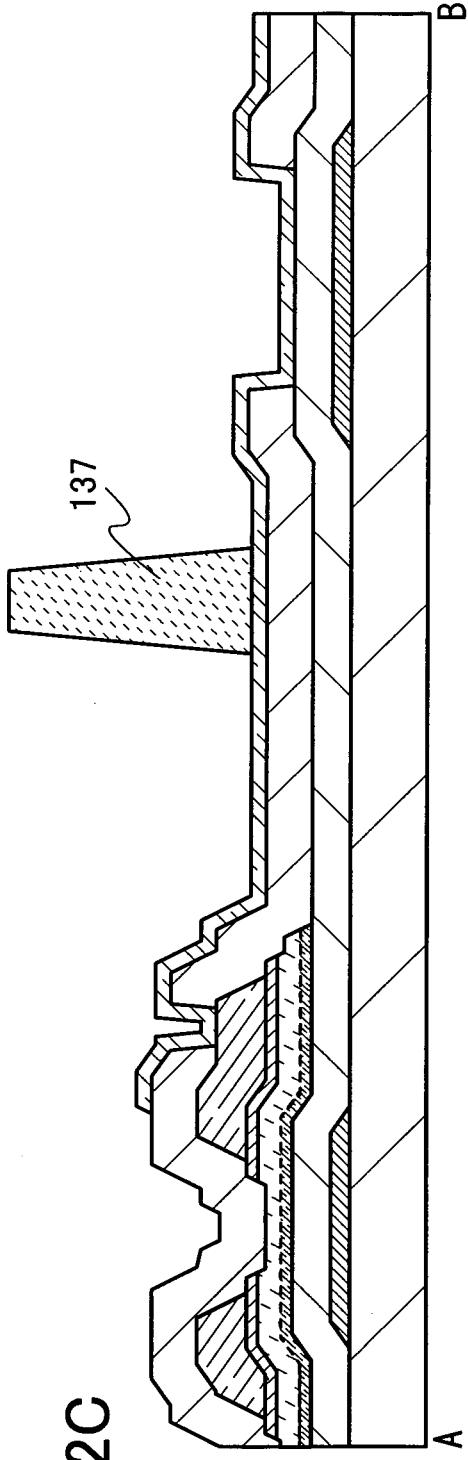


FIG. 23A

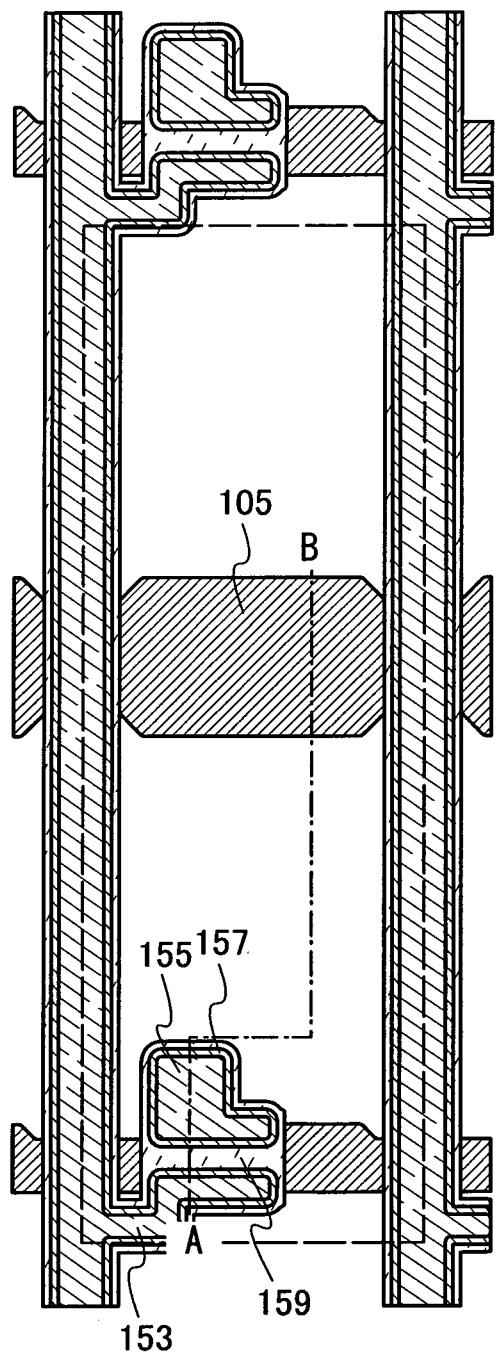
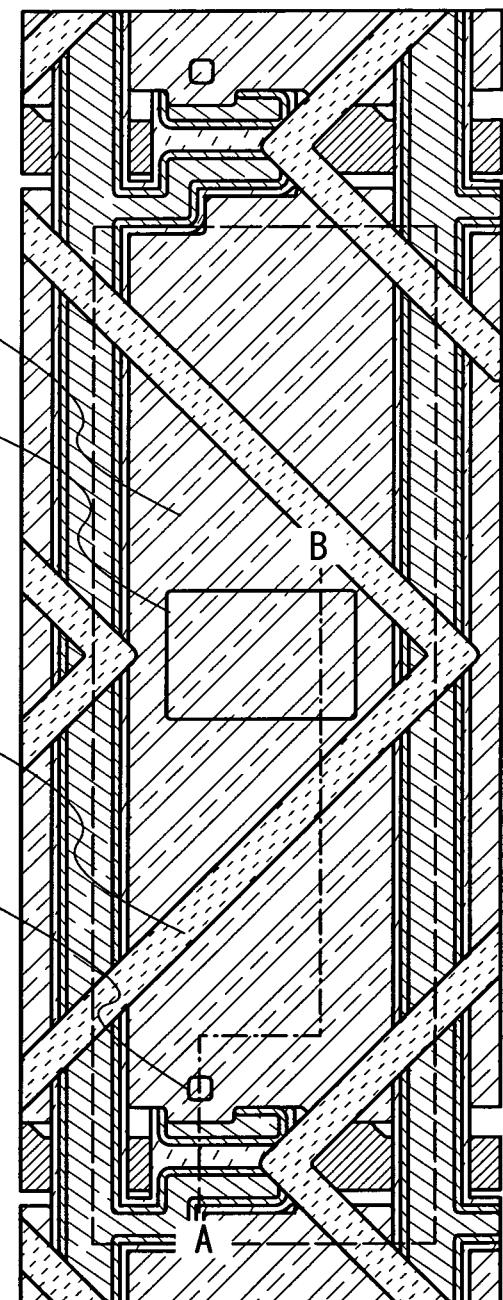
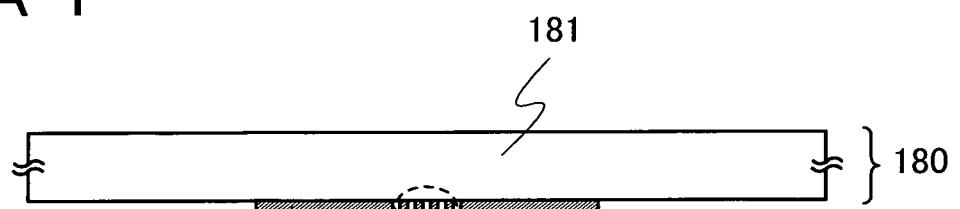
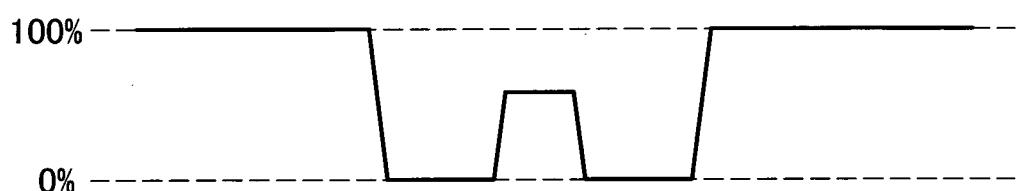
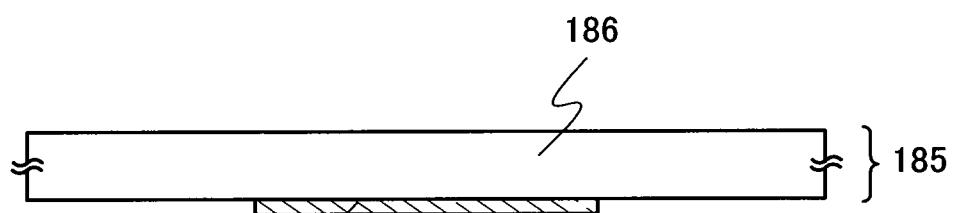


FIG. 23B

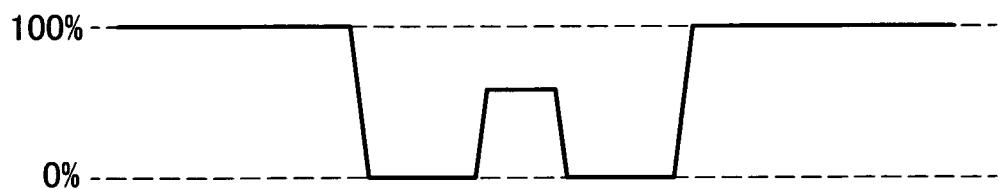


**FIG. 24A-1****FIG. 24A-2**

Transmittance

**FIG. 24B-1****FIG. 24B-2**

Transmittance



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FIG. 25A

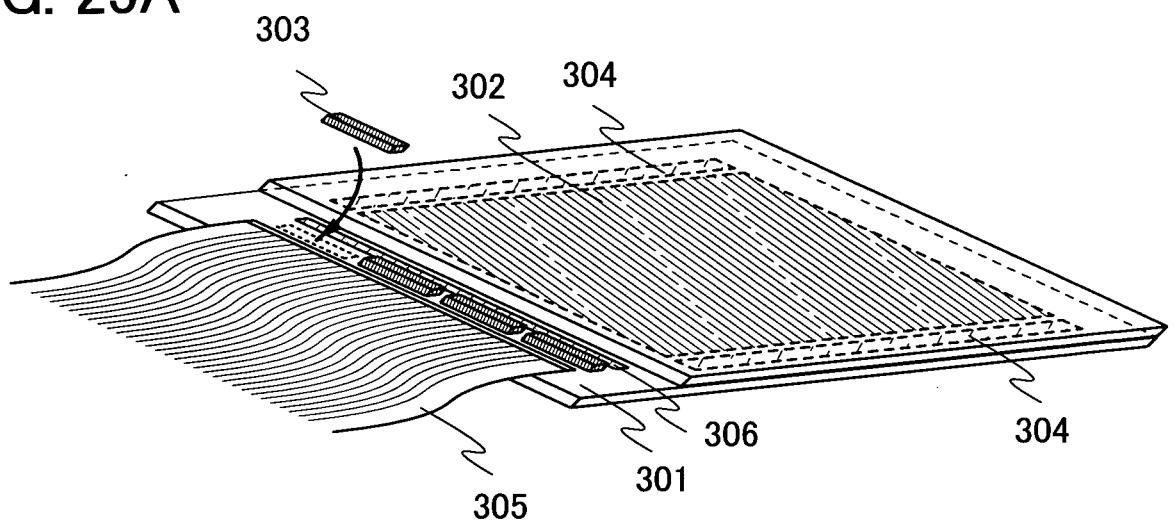


FIG. 25B

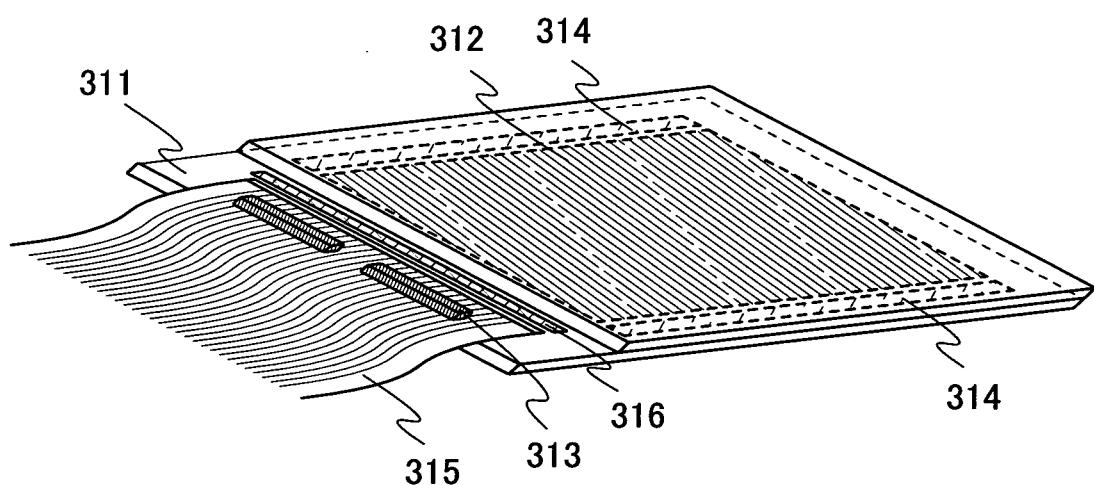
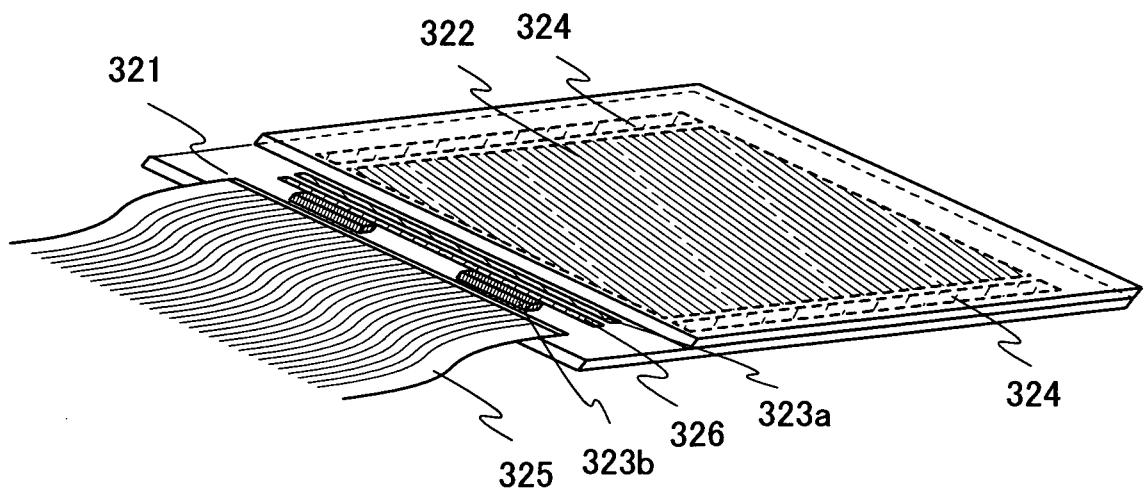


FIG. 25C



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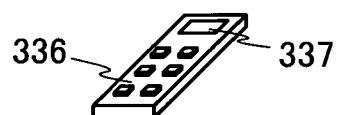
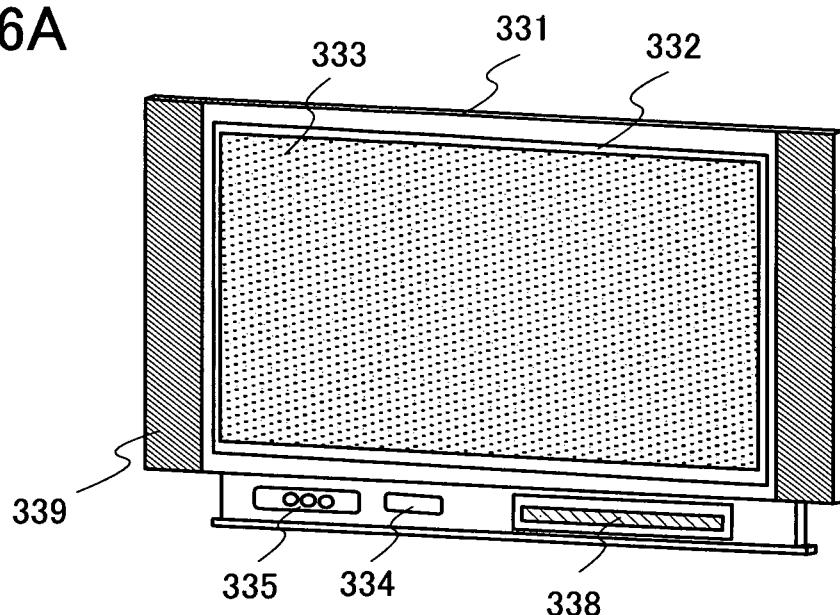
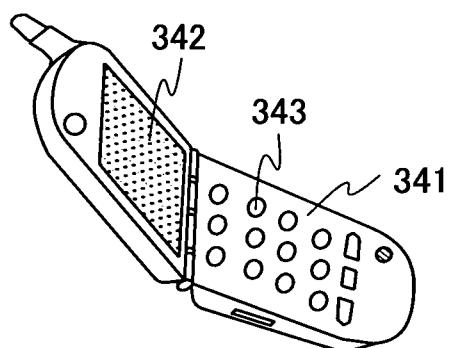
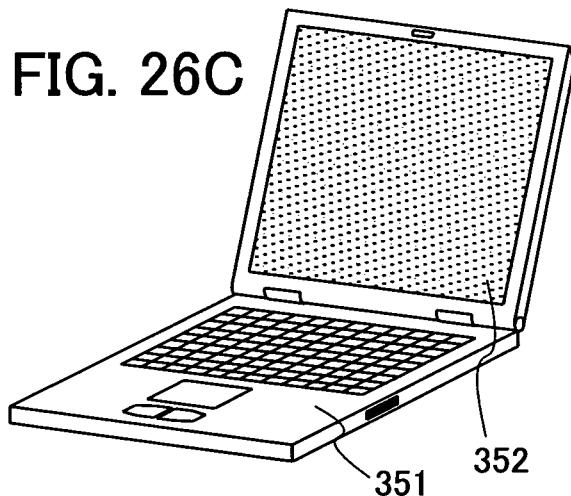
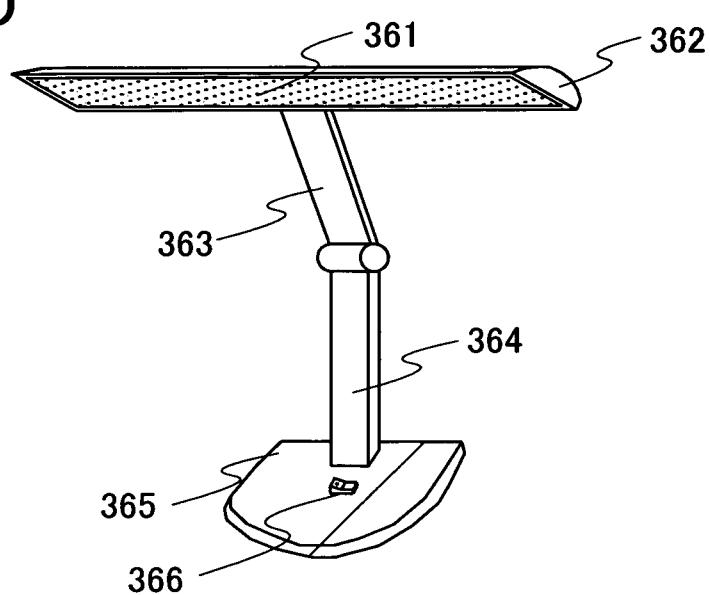
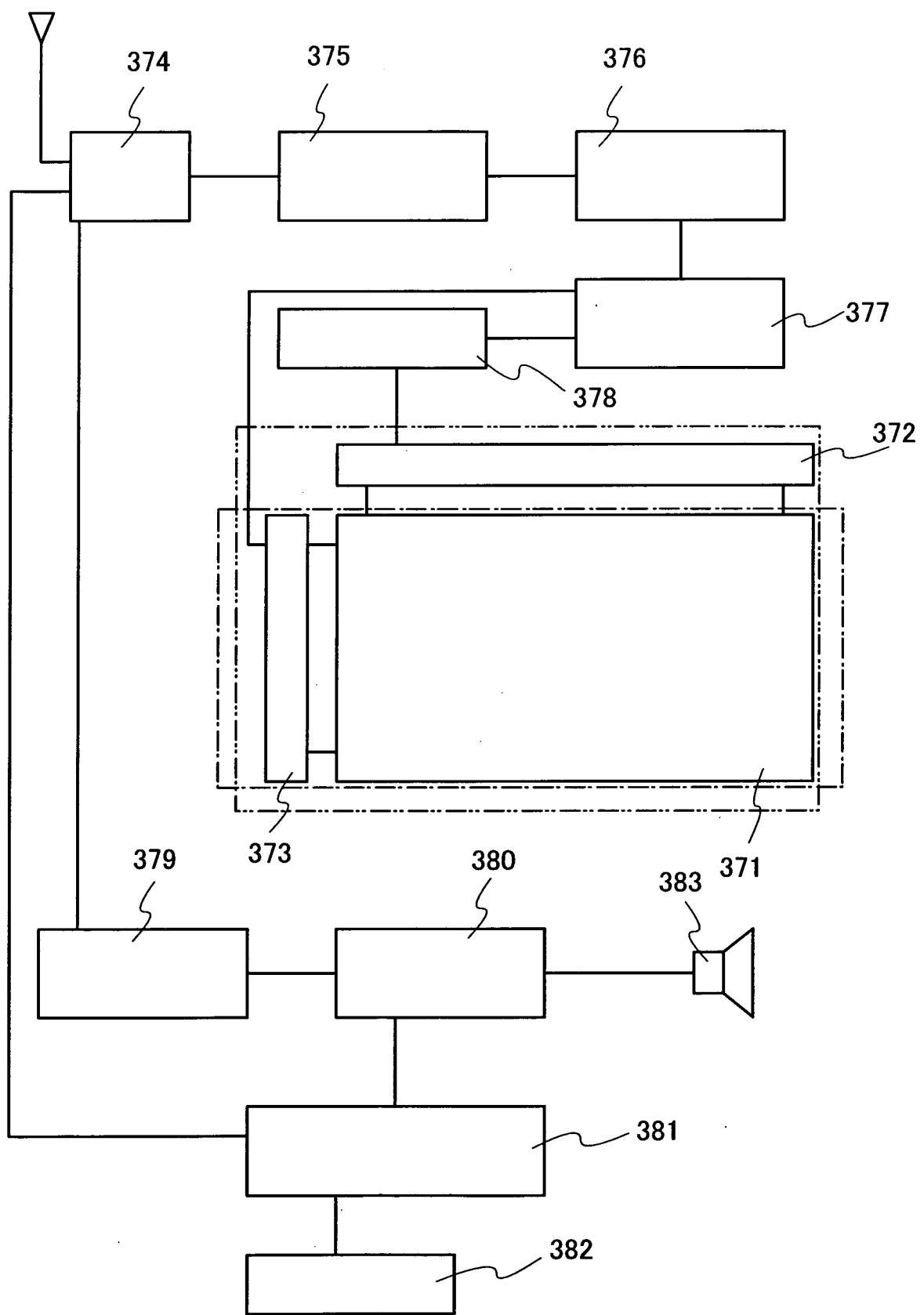
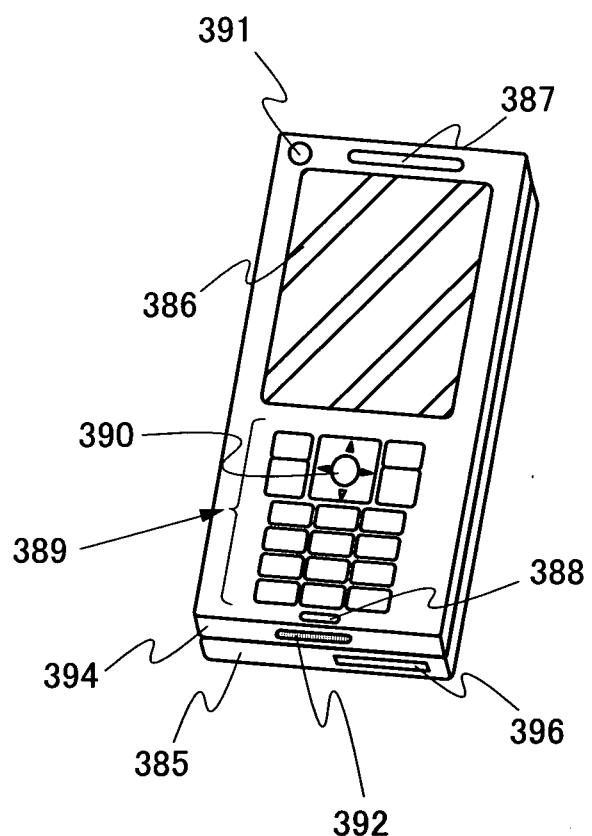
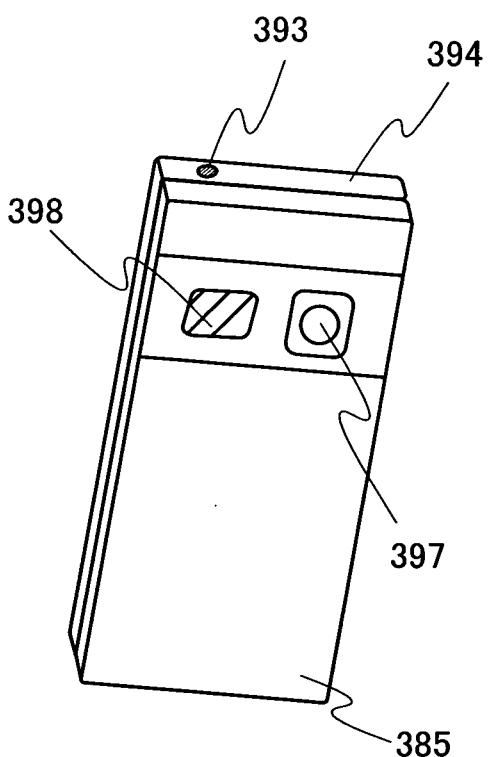
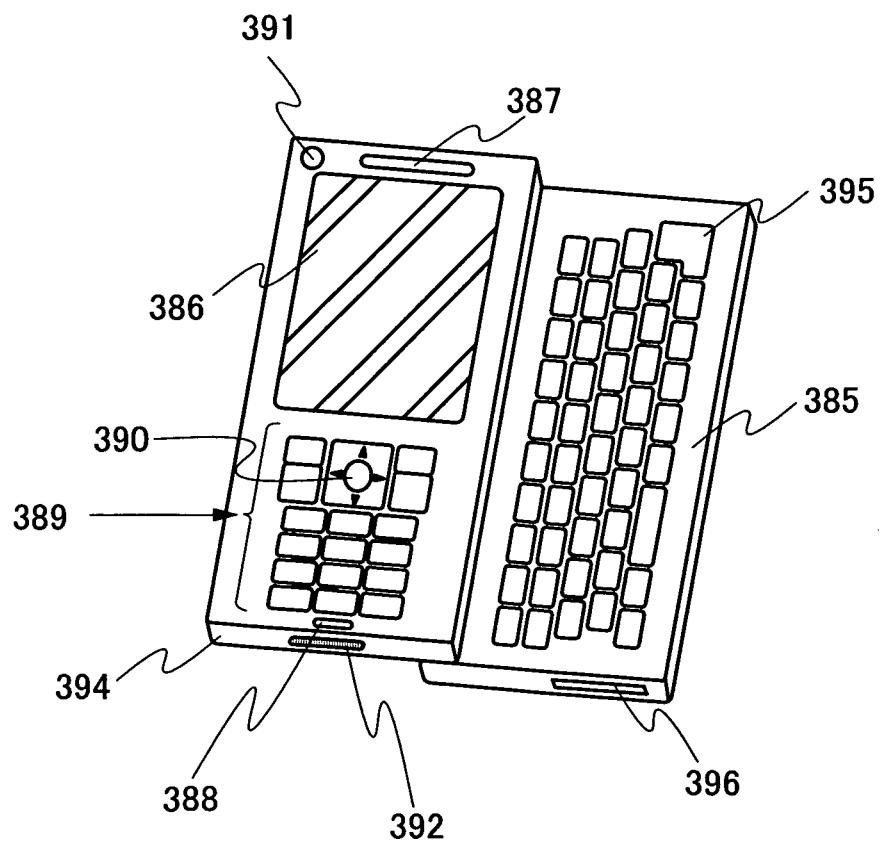
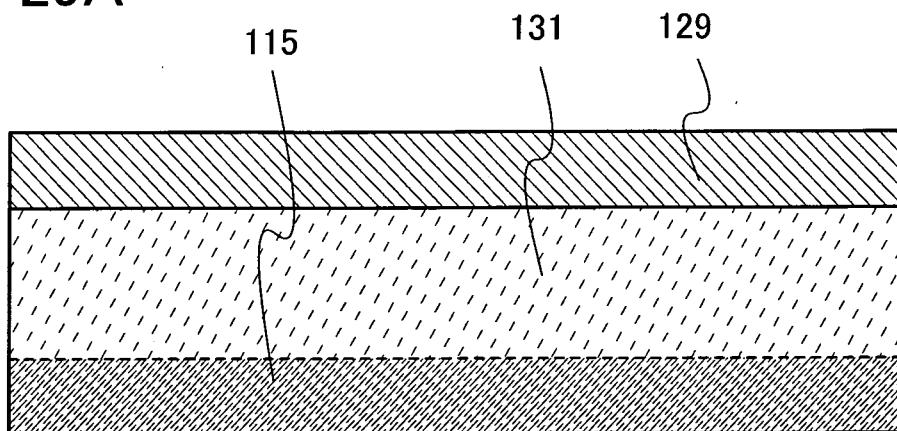
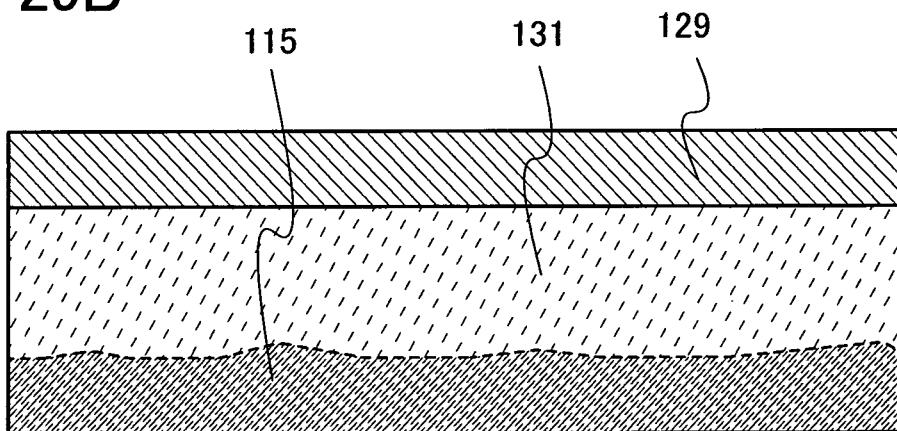
**FIG. 26A****FIG. 26B****FIG. 26C****FIG. 26D**

FIG. 27



**FIG. 28A****FIG. 28B****FIG. 28C**

**FIG. 29A****FIG. 29B**

## EXPLANATION OF REFERENCE

101: substrate, 103: gate electrode layer, 105: capacitor wiring, 107: gate insulating layer, 109: semiconductor layer, 111: buffer layer, 113: impurity semiconductor layer, 115: semiconductor layer, 117: buffer layer, 118: microcrystalline semiconductor, 119: impurity semiconductor layer, 121: conductive layer, 123: wiring layer, 125: wiring layer, 129: source region and drain region, 131: buffer layer, 132: resist mask, 133: insulating layer, 134: opening, 135: pixel electrode layer, 136: opening, 137: protrusion, 141: resist mask, 143: semiconductor layer, 145: buffer layer, 147: impurity semiconductor layer, 149: conductive layer, 151: resist mask, 153: wiring layer, 155: wiring layer, 157: source region and drain region, 159: buffer layer, 160: opening, 260: cryopump, 171: region, 172: region, 173: region, 174: region, 180: gray-tone mask, 181: substrate, 182: light-shielding portion, 183: diffraction grating portion, 185: half-tone mask, 186: substrate, 187: semi-light-transmitting portion, 188: light-shielding portion, 192: defect, 193: O atom, 194: NH group, 195: nitrogen atom, 196: region, 197: region, 198: region, 199: region, 201: pretreatment, 203: formation of SiN, 205: replacement of gases, 207: formation of SiON, 209: replacement of gases, 211: formation of a semiconductor layer, 212: wiring layer, 213: flushing treatment, 215: replacement of gases, 217: formation of a buffer layer, 219: replacement of gases, 221: formation of an impurity semiconductor layer, 223: exhaust, 225: unloading, 227: cleaning treatment, 229: precoating treatment, 231: loading, 233: precoating treatment, 234: dashed line, 241: treatment chamber, 242: stage, 243: gas supply portion, 244: shower plate, 245: exhaust port, 246: upper electrode, 247: lower electrode, 248: alternate-current power source, 249: temperature control portion, 250: gas supply means, 251: exhaust means, 252: cylinder, 253: pressure adjusting valve, 254: stop valve, 255: mass flow controller, 256: butterfly valve, 257: conductance valve, 258: turbo molecular pump, 259: dry pump, 261: plasma CVD apparatus, 301: substrate, 302: pixel portion, 303: signal line driver circuit, 304:

scanning line driver circuit, 305: FPC, 306: protective circuit, 311: substrate, 312: pixel portion, 313: signal line driver circuit, 314: scanning line driver circuit, 315: FPC, 316: protective circuit, 321: substrate, 322: pixel portion, 324: scanning line driver circuit, 325: FPC, 326: protective circuit, 331: housing, 332: display panel, 333: main screen, 334: modem, 335: receiver, 336: remote control device, 337: display portion, 338: sub screen, 339: speaker portion, 341: cellular phone, 342: display portion, 343: operation portion, 351: main body, 352: display portion, 361: lighting portion, 362: shade, 363: adjustable arm, 364: support, 365: base, 366: power source, 371: pixel portion, 372: signal line driver circuit, 373: scanning line driver circuit, 374: tuner, 375: video signal amplifier circuit, 376: video signal processing circuit, 377: control circuit, 378: signal line dividing circuit, 379: audio signal amplifier circuit, 380: audio signal processing circuit, 381: control circuit, 382: input portion, 383: speaker, 385: housing, 386: display portion, 387: speaker, 388: microphone, 389: operation keys, 390: pointing device, 391: front camera lens, 392: jack for an external connection terminal, 393: earphone terminal, 394: housing, 395: keyboard, 396: external memory slot, 397: rear camera, 398: light, 105a: amorphous semiconductor layer, 115a: needle-like crystal, 115b: crystal grain boundary, 115c: amorphous structure, 115d: amorphous layer, 118a: microcrystalline semiconductor, 118b: microcrystalline semiconductor, 191a: H atom, 191b: hydrogen atom, 196a: region, 196b: region, 235a: dashed line, 235b: dashed line, 236a: dashed line, 236b: dashed line, 237a: dashed line, 237b: dashed line, 239c: solid line, 239d: dashed line, 323a: analog switch, and 323b: shift register.

**INTERNATIONAL SEARCH REPORT**

International application No.  
PCT/JP2009/061794

**A. CLASSIFICATION OF SUBJECT MATTER**

Int.Cl. H01L29/786 (2006.01) i, H01L21/336 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996  
Published unexamined utility model applications of Japan 1971-2009  
Registered utility model specifications of Japan 1996-2009  
Published registered utility model applications of Japan 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 449539 A2 (KABUSHIKI KAISHA TOSHIBA) 1991.10.02,	<u>1-4, 7-10,</u> <u>14-15</u>
Y	column 3, line 17 to column 6, line 49,	<u>5, 11, 13</u>
A	Figs. 1 to 7 & JP 3-278466 A, page 3, right upper column, line 13 to page 5, left bottom column, line 11, Figs. 1 to 7 & US 5311040 A	<u>6, 12</u>
X	JP 5-175503 A (KYOCERA Corporation) 1993.07.13, [0015] to [0028], Figs. 1 to 3	<u>1-3, 7-9,</u> <u>14-15</u>
Y	(No Family)	<u>13</u>
Y	US 2007/0181945 A1 (Nakamura) 2007.08.09, [0032] & WO 2004/086487 A1, page 7, line 1 to 5	<u>5, 11</u>

Further documents are listed in the continuation of Box C.

See patent family annex.

\* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

03.09.2009

Date of mailing of the international search report

15.09.2009

Name and mailing address of the ISA/JP

**Japan Patent Office**

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

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**INTERNATIONAL SEARCH REPORT**

International application No.  
PCT/JP2009/061794

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
  
3.  Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

D1: EP 449539 A2  
D2: JP 5-175503 A

Claims 1 is disclosed by D1 and D2, and is not new. Therefore, there is no special technical feature common to Claim 1 to 15.

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2.  As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/JP2009/061794

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 4-266019 A (Canon Inc.) 1992.09.22, [0002] (No Family)	5,11
Y	JP 2-28624 A (Fujitsu Limited) 1990.01.30, page 3, left bottom column, line 20 to right bottom column, line 20, page 5, left upper column, line 2 to 5, Fig. 1 (No Family)	13
A	JP 60-27122 A (Semiconductor Energy Laboratory Co., Ltd.) 1985.02.12, page 4, right upper column, line 8 to left bottom column, line 2, page 5, right bottom column, line 17 to page 6, left upper column, line 4 (No Family)	6,12