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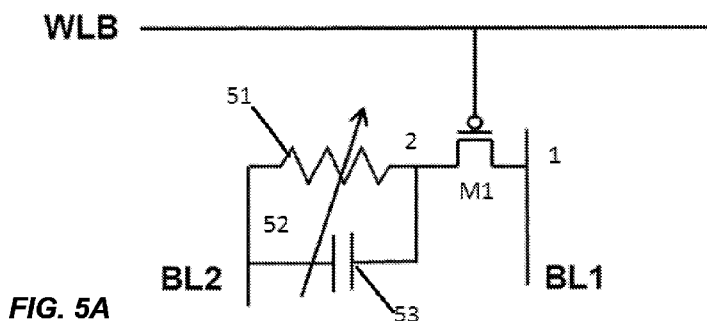
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(54) Title: METHOD, SYSTEM AND DEVICE FOR NON-VOLATILE MEMORY DEVICE OPERATION

(57) Abstract: Disclosed are methods, systems and devices for operation of non-volatile memory devices. In one embodiment, a non-volatile memory device may be placed in any one of multiple memory states in a write operation by controlling a current and a voltage applied to terminals of the non-volatile memory device. For example, a write operation may apply a programming signal across terminals of non-volatile memory device having a particular current and a particular voltage for placing the non-volatile memory device in a particular memory state.

METHOD, SYSTEM AND DEVICE FOR NON-VOLATILE MEMORY DEVICE OPERATION

Disclosed are techniques for utilizing memory devices.

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Non-volatile memories are a class of memory in which the memory cell or element does not lose its state after power supplied to the device is removed. The earliest computer memories, made with rings of ferrite that could be magnetized in two directions, were non-volatile, for example. As semiconductor technology evolved into higher levels of miniaturization, the ferrite devices were abandoned for the more commonly known volatile memories, such as DRAMs (Dynamic Random Access Memories) and SRAMs (Static-RAMs).

15 One type of non-volatile memory, electrically erasable programmable read-only memory (EEPROM) devices have large cell areas and may require a large voltage (e.g., from 12.0 to 21.0 volts) on a transistor gate to write or erase. Also, an erase or write time is typically of the order of tens of microseconds. One limiting factor with EEPROMs is the limited number of erase/write cycles to no more than slightly over 600,000--or of the order of 10^5 - 10^6 . The semiconductor industry has eliminated a need of a pass-gate switch transistor between EEPROMs and non-volatile transistors by sectorizing a memory array in such a way that "pages" (e.g., sub-arrays) may be erased at a time in EEPROMs called flash memory devices. In flash memory devices, an ability to keep random access (erase/write single bits) was sacrificed for speed and higher bit density.

More recently, FeRAMs (Ferroelectric RAMs) have provided low power, relatively high write/read speed, and endurance for read/write cycles exceeding 10 billion times. Similarly, magnetic memories (MRAMs) have provided high write/read speed and endurance, but with a high cost premium and higher power consumption. Neither of these technologies reaches the density of flash memory devices, for example. As such, flash remains a non-volatile memory of choice. Nevertheless, it is generally recognized that flash memory technology may not scale easily below 65 nanometers (nm); thus,

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new non-volatile memory devices capable of being scaled to smaller sizes are actively being sought.

5 Technologies considered for the replacement of flash memory devices have included memories based on certain materials that exhibit a resistance change associated with a change of phase of the material (determined, at least in part, by a long range ordering of atoms in the crystalline structure). In one type of variable resistance memory called a phase change memory (PCM/PCRAM) devices, a change in resistance occurs as the memory element
10 is melted briefly and then cooled to either a conductive crystalline state or a non-conductive amorphous state. Typical materials vary and may include GeSbTe, where Sb and Te can be exchanged with other elements of the same or similar properties on the Periodic Table. However, these resistance-based memories have not proved to be commercially useful because their transition
15 between the conductive and the insulating state depends on a physical structure phenomenon (e.g., melting at up to 600 degrees C) and returning to a solid state that cannot be sufficiently controlled for a useful memory in many applications.

20 Another variable resistance memory category includes materials that respond to an initial high "forming" voltage and current to activate a variable resistance function. These materials may include, for example, $\text{Pr}_x\text{Ca}_y\text{Mn}_z\text{O}_\epsilon$, with x, y, z and ϵ of varying stoichiometry; transition metal oxides (TMO), such as CuO, CoO, VO_x , NiO, TiO_2 , Ta_2O_5 ; and some perovskites, such as Cr;
25 SrTiO_3 . Several of these memory types exist and fall into the resistive RAMs (ReRAMs) or conductive bridge RAMS (CBRAM) classification, to distinguish them from the chalcogenide type memories. It is postulated that resistance switching in these RAMs is due, at least in part, to the formation of narrow conducting paths or filaments connecting the top and bottom conductive
30 terminals by the electroforming process, though the presence of such conducting filaments are still a matter of controversy. Since operation of a ReRAM/CBRAM may be strongly temperature dependent, a resistive switching mechanism in a ReRAM/CBRAM may also be highly temperature dependent. Additionally, these systems may operate stochastically as the formation and
35 movement of the filament is stochastic. Other types of ReRAM/CBRAM may

also exhibit unstable qualities. Further, resistance switching in ReRAM/CBRAMs tends to fatigue over many memory cycles. That is, after a memory state is changed many times, a difference in resistance between a conducting state and an insulative state may change significantly. In a commercial memory device, such a change may take the memory out of specification and make it unusable.

Given an inherent difficulty in forming a thin film resistance switching material that is stable over time and temperature, a workable resistance switching memory remains a challenge. Furthermore, all resistance switching mechanisms developed up to now have been inherently unsuitable for memories, due to high currents, electroforming, no measurable memory read or write windows over a reasonable range of temperatures and voltages, and many other problems such as stochastic behavior. Thus, there remains a need in the art for a non-volatile memory that is deterministic has low power, high speed, high density and stability, and in particular, such a memory that is scalable to feature sizes well below 65 nanometers (nm).

Figure 1A shows a plot of current density against voltage for a CES device;

Figure 1B is a schematic diagram of an equivalent circuit to a CES device;

Figure 2 is a schematic diagram of a memory circuit;

Figures 3A, 3B and 3C are schematic diagrams of alternative implementations of a sense circuit;

Figures 4A, 4B and 4C are schematic diagrams of alternative implementations of a write circuit; and

Figures 5A and 5B are schematic diagrams of alternative architectures for a bitcell.

Particular embodiments of the present disclosure incorporate a Correlated Electron Material (CEM) to form a correlated electron switch (CES). In this context, a CES may exhibit an abrupt conductor/insulator transition arising from electron correlations rather than solid state structural phase changes (e.g., crystalline/amorphous in phase change memory (PCM) devices or filamentary formation and conduction in resistive RAM devices as discussed above). An abrupt conductor/insulator transition in a CES may be responsive to a quantum mechanical phenomenon, in contrast to melting/solidification or filament formation. Such a quantum mechanical transition between conductive and insulative states in a CEM memory device may be understood in any one of several aspects.

A quantum mechanical transition of a CES between an insulative state and a conductive state may be understood in terms of a Mott transition. In a Mott transition, a material may switch from an insulative state to conductive state if a Mott transition condition occurs. The criteria may be defined by the condition $(n_c)^{1/3} a = 0.26$, where n_c is a concentration of electrons and "a" is a Bohr radius. If a critical carrier concentration is achieved such that the Mott criteria is met, a Mott transition may occur and state may change from a high resistance/capacitance to a low resistance/capacitance.

A Mott transition may be controlled by a localization of electrons. As carriers are localized, a strong coulomb interaction between electrons splits the bands of the material creating an insulator. If electrons are no longer localized, a weak coulomb interaction may dominate band splitting, leaving behind a metal (conductive) band. This is sometimes explained as a "crowded elevator" phenomenon. While an elevator has only a few people in it, the people can move around easily, which is analogous to a conducting state. While the elevator reaches a certain concentration of people, on the other hand, passengers can no longer move, which is analogous to the insulative state. However, it should be understood that this classical explanation provided for illustrative purposes, like all classical explanations of quantum phenomenon, is only an incomplete analogy, and that claimed subject matter is not limited in this respect.

In particular implementations, a resistive switching integrated circuit memory may comprise: a resistive switching memory cell including a CES device; a write circuit for placing the resistive switching memory cell in a first resistive state or a second resistive state depending on signals provided to the memory cell, wherein a resistance of the CES is higher in the second resistance state than in the first resistance state; and a read circuit for sensing the state of the memory cell and providing an electrical signal corresponding to the sensed state of the memory cell. A resistance of a CES in the second memory cell state may be more than 100 times the resistance in the second memory cell state. In a particular implementation, a CES device may switch resistive states responsive to a Mott-transition in the majority of the volume of the CES device. A CES device may comprise a material selected from a group comprising aluminum, cadmium, chromium, cobalt, copper, gold, iron, manganese, mercury, molybdenum, nickel, palladium, rhenium, ruthenium, silver, tin, titanium, vanadium, and zinc (which may be linked to a cation such as oxygen or other types of ligands), or combinations thereof.

In a particular embodiment, a CES device may be formed as a "CEM random access memory (CeRAM)" device. In this context, a CeRAM device comprises a material that may transition between or among a plurality of predetermined detectable memory states based, at least in part, on a transition of at least a portion of the material between a conductive state and an insulative state utilizing the quantum mechanical Mott transition. In this context, a "memory state" means a detectable state of a memory device that is indicative of a value, symbol, parameter or condition, just to provide a few examples. In one particular implementation, as described below, a memory state of a memory device may be detected based, at least in part, on a signal detected on terminals of the memory device in a read operation. In another particular implementation, as described below, a memory device may be placed in a particular memory state to represent or store a particular value, symbol or parameter by application of one or more signals across terminals of the memory device in a "write operation."

In a particular implementation, a CES element may comprise material sandwiched between conductive terminals. By applying a specific voltage and

current between the terminals, the material may transition between the
aforementioned conductive and insulative memory states. As discussed in
the particular example implementations below, material of a CES element
sandwiched between conductive terminals may be placed in an insulative or
5 high impedance memory state by application of a first programming signal
across the terminals having a voltage V_{reset} and current I_{reset} , or placed in a
conductive or low impedance memory state by application of a second
programming signal across the terminals having a voltage V_{set} and current
 I_{set} . In this context, it should be understood that terms such as "conductive
10 or low impedance" memory state and "insulative or high impedance" memory
state are relative terms and not specific to any particular quantity or value
for impedance or conductance. For example, while a memory device is in a
first memory state referred to as an insulative or high impedance memory
state the memory device is less conductive (or more insulative) than while
15 the memory device in a second memory state referred to as a conductive or
low impedance memory state.

In a particular implementation, CeRAM memory cells may comprise a
metal/CEM/metal (M/CEM/M) stack formed on a semiconductor. Such an
20 M/CEM/M stack may be formed on a diode, for example. In an example,
implementation, such a diode may be selected from the group consisting of a
junction diode and a Schottky diode. In this context, it should be understood
that "metal" means a conductor, that is, any material that acts like a metal,
including, for example, polysilicon or a doped semiconductor.

25 Figure 1A shows a plot of current density against voltage across
terminals (not shown) for a CES device according to an embodiment. Based,
at least in part, on a voltage applied to terminals of the CES device (e.g., in
a write operation), the CES device may be placed in a conductive state or an
insulative state. For example application of a voltage V_{set} and current density
30 J_{set} may place the CES device in a conductive memory state and application
of a voltage V_{reset} and a current density J_{reset} may place the CES device in an
insulative memory state. Following placement of the CES device in an
insulative state or conductive state, the particular state of the CES device

may be detected by application of a voltage V_{read} (e.g., in a read operation) and detection of a current or current density at terminals of the CES device.

According to an embodiment, the CES device of Figure 1A may include
5 any TMO, such as, for example, perovskites, Mott insulators, charge exchange insulators, and Anderson disorder insulators. In particular implementations, a CES device may be formed from switching materials such as nickel oxide, cobalt oxide, iron oxide, yttrium oxide, and perovskites such as Cr doped strontium titanate, lanthanum titanate, and the manganate family including
10 praeysdium calcium manganate, and praeysdium lanthanum manganite, just to provide a few examples. In particular, oxides incorporating elements with incomplete *d* and *f* orbital shells may exhibit sufficient resistive switching properties for use in a CES device. In an embodiment, a CES device may be prepared without electroforming. Other implementations may employ other
15 transition metal compounds without deviating from claimed subject matter. For example, $\{M(\text{chxn})_2\text{Br}\}\text{Br}_2$ where M may comprise Pt, Pd, or Ni, and chxn comprises 1R,2R-cyclohexanediamine, and other such metal complexes may be used without deviating from claimed subject matter.

20 The CES device of Figure 1A may comprise materials that are TMO metal oxide variable resistance materials, though it should be understood that these are exemplary only, and are not intended to limit claimed subject matter. Particular implementations may employ other variable resistance materials as well. Nickel oxide, NiO, is disclosed as one particular TMO. NiO materials
25 discussed herein may be doped with extrinsic ligands, which may stabilize variable resistance properties. In particular, NiO variable resistance materials disclosed herein may include a carbon containing ligand, which may be indicated by $\text{NiO}(\text{C}_x)$. Here, one skilled in the art may determine a value of *x* for any specific carbon containing ligand and any specific combination of
30 carbon containing ligand with NiO simply by balancing valences. In another particular example, NiO doped with extrinsic ligands may be expressed as $\text{NiO}(\text{L}_x)$, where L_x is a ligand element or compound and *x* indicates a number of units of the ligand for one unit of NiO. One skilled in the art may determine a value of *x* for any specific ligand and any specific combination of ligand with
35 NiO or any other transition metal simply by balancing valences.

If sufficient bias is applied (e.g., exceeding a band-splitting potential) and the aforementioned Mott condition is met (injected electron holes = the electrons in a switching region), the CES device may rapidly switch from a conductive state to an insulator state via the Mott transition. This may occur at point 108 of the plot in Figure 1A. At this point, electrons are no longer screened and become localized. This correlation may result in a strong electron-electron interaction potential which splits the bands to form an insulator. While the CES device is still in the insulative state, current may be generated by transportation of electron holes. If enough bias is applied across terminals of the CES, electrons may be injected into a metal-insulator-metal (MIM) diode over the potential barrier of the MIM device. If enough electrons have been injected and enough potential is applied across terminals to place the CES device in a set state, an increase in electrons may screen electrons and remove a localization of electrons, which may collapse the band-splitting potential forming a metal.

According to an embodiment, current in a CES device may be controlled by an externally applied "compliance" condition determined based, at least in part, on the external current limited during a write operation a write operation to place the CES device in an insulative state. This externally applied compliance current may also set a condition of a current density for a subsequent reset operation to place the CES in a conductive state. As shown in the particular implementation of Figure 1A, a current density J_{comp} applied during a write operation at point 116 to place the CES device in an insulative state may determine a compliance condition for placing the CES device in a conductive state in a subsequent write operation. As shown, the CES device may be subsequently placed in a conductive state by application of a current density $J_{reset} \geq J_{comp}$ at a voltage V_{reset} at point 108, where J_{comp} is externally applied.

The compliance therefore may set a number of electrons in a CES device which are to be "captured" by holes for the Mott transition. In other words, a current applied in a write operation to place a CES device in a conductive memory state may determine a number of holes to be injected to the CES

device for subsequently transitioning the CES device to an insulative memory state.

As pointed out above, a reset condition may occur in response to a Mott transition at point 108. As pointed out above, such a Mott transition may occur at condition in a CES device in which a concentration of electrons n equals a concentration of electron holes p . This condition may be modeled according to expression (1) as follows:

$$\lambda_{TF} n^{\frac{1}{3}} = C \sim 0.26 \quad (1)$$

$$n = \left(\frac{C}{\lambda_{TF}} \right)^3$$

where:

λ_{TF} is a Thomas Fermi screening length; and
 C is a constant.

According to an embodiment, a current or current density in a region 104 of the plot shown in Figure 1A may exist in response to injection of holes from a voltage signal applied across terminals of a CES device. Here, injection of holes may meet a Mott transition criterion for the conductive state to insulative state transition at current I_{MI} as a critical voltage V_{MI} is applied across terminals of CES device. This may be modeled according to expression (3) as follows:

$$I_{MI}(V_{MI}) = \frac{dQ(V_{MI})}{dt} \approx \frac{Q(V_{MI})}{t} \quad (3)$$

$$Q(V_{MI}) = qn(V_{MI})$$

Where $Q(V_{MI})$ is the charged injected (hole or electron) and is a function of an applied voltage.

Injection of electron holes to enable a Mott transition may occur between bands and in response to critical voltage V_{MI} . and critical current I_{MI} . By equating electron concentration n with a charge concentration to bring about a Mott transition by holes injected by I_{MI} in expression (3) according to

expression (1), a dependency of such a critical voltage V_{MI} on Thomas Fermi screening length λ_{TF} may be modeled according to expression (4) as follows:

$$\begin{aligned} I_{MI}(V_{MI}) &= \frac{Q(V_{MI})}{t} = \frac{qn(V_{MI})}{t} = \frac{q}{t} \left(\frac{C}{\lambda_{TF}} \right)^3 \\ J_{reset}(V_{MI}) &= J_{MI}(V_{MI}) = \frac{I_{MI}(V_{MI})}{A_{CeRam}} = \frac{q}{A_{CeRam}t} \left(\frac{C}{\lambda_{TF}} \right)^3 \end{aligned} \quad (4)$$

Where:

5 A_{CeRam} is a cross-sectional area of a CES element; and
 $J_{reset}(V_{MI})$ is a current density through the CES element to be applied to the CES element at a critical voltage V_{MI} to place the CES element in an insulative state.

10 According to an embodiment, a CES element may be placed in a conductive memory state (e.g., by transitioning from an insulative memory state) by injection of a sufficient number of electrons to satisfy a Mott transition criteria.

15 In transitioning a CES to a conductive memory state, as enough electrons have been injected and the potential across terminal of the CES device overcomes a critical switching potential (e.g., V_{set}), injected electrons begin to screen and unlocalize double-occupied electrons to reverse a disproportion reaction and closing the bandgap. A current density $J_{set}(V_{IM})$
 20 for transitioning the CES to the conductive memory state at a critical voltage V_{IM} enabling transition to the conductive memory state may be expressed according to expression (5) as follows:

$$\begin{aligned} I_{IM}(V_{IM}) &= \frac{dQ(V_{IM})}{dt} \approx \frac{Q(V_{IM})}{t} \\ 25 \quad Q(V_{IM}) &= qn(V_{IM}) \\ I_{IM}(V_{IM}) &= \frac{Q(V_{IM})}{t} = \frac{qn(V_{IM})}{t} = \frac{q}{t} \left(\frac{C}{a_B} \right)^3 \\ J_{set}(V_{IM}) &= J_{injection}(V_{IM}) = J_{IM}(V_{IM}) = \frac{I_{IM}(V_{IM})}{A_{CeRam}} = \frac{q}{A_{CeRam}t} \left(\frac{C}{a_B} \right)^3 \end{aligned} \quad (5)$$

30 where:

a_B is a Bohr radius.

According to an embodiment, a “read window” 102 for detecting a memory state of a CES device in a read operation may be set out as a difference between a portion 106 the plot of Figure 1A while the CES device is in an insulative state and a portion 104 of the plot Figure 1A while the CES device is in a conductive state at a read voltage V_{read} . In a particular implementation, read window 102 may be used to determine a Thomas Fermi screening length λ_{TF} of material making up the CES device. For example, at a voltage V_{reset} , current densities J_{reset} and J_{set} may be related to according to expression (6) as follows:

$$\lambda_{TF}(@V_{reset}) = a_B \left(\frac{J_{reset}}{J_{off}} \right)^{\frac{1}{3}} \quad (6)$$

In another embodiment, a “write window” 110 for placing a CES device in an insulative or conductive memory state in a write operation may be set out as a difference between V_{reset} (at J_{reset}) and V_{set} (at J_{set}). Establishing $|V_{set}| > |V_{reset}|$ enables a switch between conductive and insulative state. V_{reset} may be approximately at a band splitting potential arising from correlation and V_{set} may be approximately twice the band splitting potential. In particular implementations, a size of write window 110 may be determined, at least in part, by materials and doping of the CES device.

The transition from high resistance/capacitance to low resistance/capacitance in a CES device may be represented by a singular impedance of the CES device. Figure 1B depicts a schematic diagram of an equivalent circuit of an example variable impeder device (such as a CES device), such as variable impeder device 124. As mentioned, variable impeder device 124 may comprise characteristics of both variable resistance and variable capacitance. For example, an equivalent circuit for a variable impeder device may, in an embodiment, comprise a variable resistor, such as variable resistor 126 in parallel with a variable capacitor, such as variable capacitor 128. Of course, although a variable resistor 126 and variable capacitor 128 are depicted in Figure 1B as comprising discrete components,

a variable impeder device, such as variable impeder device 124, may comprise a substantially homogenous CEM, wherein the CEM comprises characteristics of variable capacitance and variable resistance. Table 1 below depicts an example truth table for an example variable impeder device, such as variable impeder device 100.

Resistance	Capacitance	Impedance
$R_{high}(V_{applied})$	$C_{high}(V_{applied})$	$Z_{high}(V_{applied})$
$R_{low}(V_{applied})$	$C_{low}(V_{applied}) \sim 0$	$Z_{low}(V_{applied})$

Table 1

Figure 2 is a schematic diagram of a memory circuit according to an embodiment. A bitcell circuit 200 may comprise one or more memory elements (e.g., non-volatile memory elements) comprising a CES device. In this context, a "bitcell" or "bitcell circuit" as referred to herein comprises a circuit or portion of a circuit capable of representing a value, symbol or parameter as a state. For example, a bitcell may comprise one or more memory devices that are capable of representing a value, symbol or parameter as a memory state of the memory device. In particular implementations, a bitcell may represent a value, symbol or parameter as a single bit or multiple bits.

According to an embodiment, bitcell circuit 200 may comprise memory elements having a behavior similar to that of the CES device discussed above in connection with Figure 1. For example, a memory element in bitcell 200 may be placed in a particular memory state (e.g., a conductive or low impedance memory state, or insulative or high impedance memory state) by independently controlling voltage and current applied across terminals of the memory element in a "write operation." As discussed below in particular implementations, such a write operation may be executed by application of a signal which is controlled to provide a critical current and voltage across terminals of the memory device to place the memory device in a particular

memory state. A memory state of a memory element in bitcell 200 may be detected or sensed in a "read operation" by precharging a bitline BL by closing transistor M0 in response to a drop in voltage of signal PRN to connect bitline BL with voltage $R_{VDD} = 0.4V$. Transistor M0 may subsequently open in response to an increase in voltage of signal PRN, followed by a closing of transistor M3 in response to an increase in voltage of signal RD_Col_Sel to connect bitline BL to sense circuit 203. In this context, a "bitline" comprises a conductor that is connectable to at least one terminal of a memory element during a write operation to transmit a signal altering a memory state of the memory element, or during a read operation to transmit a signal indicative of a current memory state of the memory element. Sense circuit 203 may detect a memory state of the memory element in bitcell 200 based on a magnitude of current or voltage from bitline BL through transistor M3 in a read operation. An output signal may have a voltage that is indicative of a current memory state of bitcell 200 (e.g., as a "1," "0" or other symbol). In one example of a read operation, to detect a current memory state of a memory element, a voltage of a signal applied across terminals of the memory element in bitcell 200 may be controlled so as to not detectably alter the current memory state of the memory element.

Figures 5A and 5B are directed to specific implementations of a bitcell circuit that include CES devices or elements to store a particular memory state. While the description below provides CeRAM devices or non-volatile memory elements as specific examples of devices in a bitcell capable of maintaining a memory state, it should be understood that these are merely example implementations. For example, it should be recognized a CES adapted for purposes other than a non-volatile memory device or CeRAM device may be used for storing a particular memory state (e.g., a conductive or low impedance memory state, or an insulative or high impedance memory state) in a write operation which is detectable in a subsequent read operation, and that claimed subject matter is not limited to either implementation of a CeRAM or non-volatile memory devices.

Particular example implementations of sense circuit 203 are shown in the schematic diagrams of Figures 3A through 3C. As shown in the particular

example implementations, a sense circuit may comprise a single-ended sense amplifier circuit including a voltage mode amplifier as shown in Figure 3A or a current mode amplifier as shown in Figure 3C. The particular implementation of Figure 3A comprises a differential voltage amplifier formed by field effect transistors (FETs) M7, M8, M9 and M10 to receive a signal from a bitline during a read operation and a reference voltage VREF. In a particular implementation, a signal maintained at a reference voltage VREF may be generated using a VREF circuit shown in the schematic diagram of Figure 3B according to an embodiment. Here, reference voltage VREF may be set to $V_{IN}/2$, where V_{IN} is a voltage level on a bitline during a read operation. The VREF circuit of Figure 3B may be activated during a read operation and generate a signal maintained at reference voltage VREF voltage using a resistor divider of two equal value hi-res Poly or Nwell resistors, R1 and R2, for example. It should be understood that this is merely an example of a circuit to generate a signal maintained at a reference voltage, and that claimed subject matter is not limited in this respect. For example, a differential voltage mode sense amplifier is for illustrative purposes only. A differential latch based voltage mode sense amplifier may also be used without deviating from claimed subject matter.

As pointed out above, another particular example implementation of a sense circuit is shown in the particular example implementation of a current mode sense amplifier shown in Figure 3C. Here, a first stage comprises a current mirror which senses the voltage on the bitline, V_{IN} at a gate terminal of transistor M12. A default state of the current sense mode amplifier of Figure 3C is reading a value of "1" since the bitline is precharged to a particular voltage (e.g., 0.4V) while the sense circuit of Figure 3C is in a standby state with a voltage at SAE=0.0 V at a beginning of a read cycle. If a bitcell is written to a "0" level, the bitline may be pulled from 0.4V to 0.0V which appears as V_{IN} while at the same signal SAE may be pulled to voltage VDD. This may turn on transistor M12 to mirror a current into a second stage forcing node 7 to be pulled to 0.0 V while pulling the sense circuit output SAOUT is to voltage VDD. At the end of a read cycle, signal SAE may return to 0.0V and the sense circuit of Figure 3C may return to a standby state. It should be understood that the above described implementations of a sense

circuit as illustrated in Figures 3A through 3C are merely example implementations, and that claimed subject matter is not limited by these particular example implementations.

5 In another example, bitcell 200 may be changed to or placed in a particular memory state (e.g., set or reset) in a write operation by applying a voltage signal Wrt_Col_SelN to close transistor M4, connecting an adjustable driver circuit of write circuit 202 to bitline BL. In a particular implementation, write circuit 202 may drive a write supply voltage, WVDD, 10 to a bitcell while a signal Wrt_Col_SelN is maintained at 0.0 V. As pointed out above, a memory state of a CES device may be placed in a set or reset memory by controlling a voltage and a current applied to terminals of the CES device. In a particular non-limiting example implementation, a signal generated by a write supply voltage WVDD may be driven to particular 15 voltage levels to match the reset and set voltages V_{reset} and V_{set} for a CES device (e.g., 0.6V or 1.2V). In addition, write circuit 202 may comprise an adjustable strength driver to control a current density supplied to the CES device.

20 As pointed out above in Figure 1, a memory state of a CES device in bitcell 200 may be changed or determined based on a particular voltage and current applied to bitline BL. For example, providing a signal to bitline BL having a voltage V_{reset} and a sufficient current I_{reset} may place a CES device of bitcell 200 in an insulative or high impedance memory state. Likewise, 25 providing a signal to bitline BL having a voltage V_{set} and a sufficient current I_{set} may place a CES device of bitcell 200 in a conductive or low impedance memory state. As may be observed from Figure 1, that while a magnitude of voltage V_{set} is greater than a magnitude of voltage V_{reset} , a magnitude of current I_{set} is lower than a magnitude of current I_{reset} .

30 Figures 4A and 4B are schematic diagrams of alternative implementations for write circuit 202 according to alternative implementations. In particular, a write operation is described as a particular process of placing a memory device such as a CES element in a particular 35 memory state of a plurality of predetermined memory states by applying a

“programming signal” to terminals of the memory device. Particular ones of the predetermined memory states may correspond to particular voltage levels to be applied to the memory device (e.g., V_{set} and V_{reset}). Similarly, particular ones of the predetermined memory states may correspond to particular current levels to be applied to the memory device (e.g., I_{set} and I_{reset}). Accordingly, in a particular embodiment, a programming signal to place a CES device in a particular memory state in a write operation may be controlled to have a particular voltage level and current level corresponding to the particular memory state. The specific example embodiments of Figures 4A and 4B are directed to providing a programming signal to a “single-ended” bitcell to place the particular bitcell in a particular memory state. It should be understood, however, that the specific example embodiments of FIGs, 4A and 4B may be applicable to generating one or more programming signals to place multiple CES elements in a bitcell to memory states based on a data signal, and that claimed subject matter is not limited to the specific example embodiments of Figures 4A and 4B. For example, a first write circuit according to Figure 4A or 4B may be configured to apply a first programming signal placing a first CES element of a bitcell in a particular memory state and a second, replicated write circuit may be configured to apply a second programming signal placing a second CES element of the bitcell in a complementary memory state.

As described in a particular implementation below, a voltage signal having a voltage level for a programming signal to place a memory device in a predetermined memory state may be selected at a signal selection circuit based, at least in part, on a data signal. Conducting elements connected to the signal selection circuit may selectively connect the voltage signal to or disconnect the voltage signal from the memory device at a current level corresponding to the predetermined memory state based, at least in part, on the data signal. In this context, a “conducting element” comprises a circuit element capable of permitting current to pass between two nodes. In a particular implementation, a conducting element may vary a current permitted to pass between nodes based, at least in part, on a particular condition. The particular implementations described below employ FETs as conducting elements to permit current to pass between source and drain

terminals based, at least in part, on a voltage applied to a gate terminal. It should be understood, however, that other types of devices such as, a bipolar transistor, diode, variable resistor, etc. may be used as a conducting element, and that claimed subject matter is not limited in this respect. In this context, a conducting element having first and second terminals may "connect" the first and second terminals by providing a conductive path between the first and second terminals having a very small or negligible impedance for a particular signal. In one particular example implementation, a conductive element may vary an impedance between the first and second terminals based, at least in part, on a signal provided to a third terminal of the conductive element (e.g., based on a voltage or current applied to the third terminal). In one example, a conductive element may "close" to thereby connect first and second terminals in response to a signal provided on the third terminal. Likewise, a conductive element may "open" to thereby disconnect first and second terminals in response to a different signal provided on the third terminal. In an example, a conductive element in an open state may isolate a first portion of a circuit from a second portion of the circuit by removing or disrupting a conductive path between the first and second portions of the circuit. In another example, a conducting element may vary an impedance between first and second terminals between an opened and closed state based on a signal provided to a third terminal.

According to an embodiment, a signal may be provided to a bitline in an operation based, at least in part, on whether the operation is a read operation or a write operation. A signal WE may be received at an inverter 304 to provide a signal WEN to gates of FETs M34 and M30. If the particular operation is a read operation, transistor M34 may be closed in response to signal WE while FETs M30 and M32 may be opened in response to a voltage of signal WE to provide a voltage V_{read} to the bitline. Furthermore, connecting voltage V_{read} to FET M4 allows for less precise timing of closing M4 at the commencement of a write operation to apply a programming signal to a memory element. While Figures 4A, 4B and 4C show that FET M4 connects a single bitline BL to a write circuit, in particular implementations FET M4 may be among multiple conducting elements in a multiplexer to selectively connect an output signal of a write circuit to a bitline selected among multiple bitlines

(e.g., where the write circuit is configured to provide a programming signal to any one of multiple bitlines leading to bitcells). In other embodiments in which one write circuit is provided per bitline, an output signal of a write circuit may be connected directly to a bitline without a connection from a conducting element responsive to a column select signal (e.g., without FET M4).

If the particular operation is a write operation, signal WEN may be at 0.0 V and FET M34 may be opened in response to a drop of a voltage on signal WEN to disconnect bitline BL from voltage V_{read} . In response to a lowered voltage on signal WEN, bitline BL will connect to a programming signal maintained at a particular voltage and current to place a bitcell in either a conductive or low impedance memory state, or an insulative or high impedance memory state. FET M32 may be closed in a write operation to place the memory element in an insulative or high impedance memory state (e.g., for writing a "0") in a reset operation. For example, as shown in Figure 4A, this may occur as signal WEN is low while Data = "0" to close FET M32 as a voltage expressed by the condition "WEN or Data" is applied to a gate terminal of FET M32.

According to an embodiment, a multiplexer 302 may receive a voltage signal having a voltage V_{set} and a voltage signal having a voltage V_{reset} (e.g., critical voltages for placing a CES device in a conductive or low impedance memory state, or an insulative or high impedance memory state). According to an embodiment, voltage signals having voltages V_{set} and V_{reset} may be generated using any one of several circuits (not shown) including amplifiers and the like for generating a signal having a controlled voltage and/or current. Multiplexer 302 may select between providing a signal at voltage V_{set} or voltage V_{reset} to FETs M30 and M32 based, at least in part, on a data signal having a value of "1" or "0." In an embodiment, FET M30 may close in response to a lowered voltage on signal WEN to connect a selected voltage signal to bitline BL. Depending on whether the data signal has a value of "1" or "0," a magnitude of current provided to bitline BL may be affected. As illustrated above with reference to Figure 1, a write operation to modify a memory state of a CES device to an insulative or high impedance memory

state may be accomplished with a higher current density J_{reset} than a current density J_{set} to modify the memory state to a conductive or low impedance memory state. In a particular implementation, FET M32 and FET M30 may connect V_{reset} to the bitline based on the value of the data signal received at multiplexer 302. As such, if a data signal received at multiplexer 302 in a write operation is a "0" for placing a CeRAM device in an insulative or high impedance memory state, both FETs M30 and M32 may be closed to permit sufficient current to flow to bitline BL at voltage V_{reset} for placing the CeRAM device in an insulative or high impedance memory state. On the other hand, if a data signal received at multiplexer 302 in a write operation is a "1" for placing a CeRAM device in a conductive or low impedance memory state, FET M30 may be closed in response to a raised voltage of signal WE while FET M32 remains open to limit current flowing to bitline BL at voltage V_{set} for placing the CeRAM device in a conductive or low impedance memory state.

In the alternative implementation of Figure 4B, multiplexer 352 may select between providing V_{set_ref} or V_{reset_ref} to FETs M38 and M40 in a write operation based, at least in part, on a data signal having a value of "1" or "0." In a read operation, a voltage of signal WE may be lowered such that transistor M36 is closed to connect a voltage V_{read_ref} to bitline BL, and such that FETs M38 and M40 are opened to disconnect multiplexer 352 from bitline BL. In a write operation, a voltage of signal WE may be raised such that FET M36 is opened to disconnect voltage V_{read_ref} from bitline BL, and such that FET M38 is closed to connect a signal selected at multiplexer 352 to bitline BL through at least FET M38. If a data signal received at multiplexer 352 in a write operation is a "0" for placing a CeRAM element in an insulative or high impedance memory state, both FETs M38 and M40 may be closed to permit sufficient current to flow to bitline BL at voltage V_{reset_ref} to place the CeRAM element in an insulative or high impedance memory state. On the other hand, if a data signal received at multiplexer 352 in a write operation is a "1" for placing a CeRAM element in a conductive or low impedance memory state, transistor M38 may be closed while transistor M40 remains open to limit current flowing to bitline BL at voltage V_{set_ref} to place the CeRAM element in a conductive or low impedance memory state.

The particular example implementations of Figures 4A and 4B are capable of providing a read voltage signal to bitline BL during read operations. Here, signal Wrt_Col_SeIN may be lowered during read operations to close FET M4 and connect the read voltage signal to bitline BL (in addition to being
5 lowered during write operations to connect a programming signal to bitline BL). In alternative implementations (as described below), a read voltage may be generated locally at bitcell 200 to be provided to terminals of a memory element during read operations. In which case, signal Wrt_Col_SeIN may be raised during read operations to open FET M4 signal and disconnect write
10 circuit from bitline BL.

In the particular example embodiments of Figures 4A and 4B above, multiplexers 302 and 352 provide examples of a "signal selection circuit." In this context, a signal selection circuit provides circuit for selection of a signal
15 having a particular voltage and current to be applied to a device. It should be understood, that multiplexers 302 and 352 are merely examples of a signal selection circuit, and that claimed subject matter is not limited in this respect. For example, a signal selection circuit may select a signal generated from a source external to the signal selection circuit or generate a selected signal
20 internally. In the particular write circuit of Figure 4C, for example, a value of Data as "0" may close FET M44 and open FET M46 to provide a signal having a current I_{reset} . FETs M48, M52 and M54 may also close to provide a lower voltage. A value of Data as "1," on the other hand, may open FET M44 and close FET M46 to provide a signal having a current I_{set} . FETs M48, M52 and
25 M54 may also open to provide a higher voltage.

Figures 5A and 5B are schematic diagrams of alternative architectures for a bitcell according to particular embodiments. In a particular implementation of a read operation, a bitline may be connected to a terminal
30 of a non-volatile memory (NVM) element through a first conducting element in response to a voltage signal on a wordline. As pointed out above, a "non-volatile memory" comprises an integrated circuit device in which a memory cell or element maintains its memory state (e.g., a conductive or low impedance memory state, or an insulative or high impedance memory state)
35 after power supplied to the device is removed. In this context, a "wordline"

comprises a conductor for transmitting a signal to select a particular bitcell or group of bitcells to be accessed in a read operation or a write operation. In a particular example implementation, a voltage of a signal on a wordline may be raised or lowered to select or deselect a particular bitcell or group of bitcells to be connected to a corresponding bitline or group of bitlines during a read or write operation. It should be understood, however, that this is merely an example of a wordline and that claimed subject matter is not limited in this respect. Also, in this context, a "reference node" comprises a node in a circuit that is maintained at a particular voltage level or at a particular voltage difference from another node in the circuit. In one example, a reference node may comprise or be connected to a ground node. In other particular implementations, a reference node may be maintained at a particular voltage relative to that of a ground node.

According to an embodiment, in a first write operation to place an NVM element in a first memory state, a bitline may be connected to a first terminal of the NVM element through a conducting element in response to a voltage signal on a wordline. In the first write operation, a programming signal having a first write voltage and a first write current may be applied across terminals of the NVM element to place the NVM element in a first memory state. In a second write operation to place the NVM element in a second memory state, the bitline may be connected again to the first terminal of the NVM element through the first conducting element in response to the voltage signal on the wordline. The second write operation may apply a programming signal having a second write voltage and a second write current between terminals of the NVM element to place the NVM element in a second memory state. In a particular implementation, the NVM element may comprise a CES element or CeRAM element having one or more properties discussed above with reference to Figure 1 in that $|V_{\text{reset}}| < |V_{\text{set}}|$ while $|I_{\text{reset}}| > |I_{\text{set}}|$. Accordingly, in the particular examples illustrated in Figures 5A and 5B, a magnitude of the first write voltage (e.g. $|V_{\text{set}}|$) may be greater than a magnitude of the second write voltage (e.g. $|V_{\text{reset}}|$), and a magnitude of the first write current (e.g. $|I_{\text{set}}|$) may be less than a magnitude of the second write current (e.g. $|I_{\text{reset}}|$). Following placement of the NVM element in the second memory state, a third voltage (e.g., V_{read}) may be applied across the terminals of the

NVM element in a read operation to detect a current memory state of the NVM element. While the third voltage is being applied during the read operation, a current between the first and second terminals may be limited to less than a magnitude of the first current to maintain the second memory state of the NVM element.

In one embodiment, NVM element 52 comprises a CES element connected to a FET M1 at a first terminal and a bitline BL2 at a second terminal. In response to a wordline voltage WLB applied to a gate terminal of FET M1, M1 may connect the first terminal of NVM element 52 to bitline BL1 during read or write operations. In one particular implementation, bitline BL2 may be connected to a reference node such as a ground node (not shown). In other implementations, bitlines BL1 and BL2 may comprise complementary bitlines to apply an appropriate voltage (e.g., V_{set} or V_{reset}) and current (e.g., I_{set} or I_{reset}) across first and second terminals of NVM 52 in a write operation to place NVM 52 in a desired memory state, or to apply an appropriate voltage (e.g., V_{read}) in a read operation. In this particular example implementation, BL2 may be connected to a write circuit through an additional conducting element (not shown) in response to a wordline signal voltage.

As pointed out above, a write circuit may independently control a voltage and a current of a signal applied to NVM element 52 in a write operation based, at least in part, on whether the write operation is to place NVM element 52 in a conductive or low impedance memory state, or an insulative or high impedance memory state. For example, for a write operation to place NVM element 52 in a conductive or low impedance memory state, a signal having a voltage V_{set} and a current I_{set} may be applied. Likewise, for a write operation to place NVM element 52 in an insulative or high impedance memory state, a signal having a voltage V_{reset} and a current I_{reset} may be applied. As illustrated in Figure 1, voltage V_{set} may have a greater magnitude than voltage V_{reset} while current I_{set} may have a smaller magnitude than current I_{reset} . As discussed above in a particular implementation, write circuit 202 may independently control voltage and current to provide a signal to a bitline to place a non-volatile memory device

in a conductive or low impedance memory state, or an insulative or high impedance state.

To detect a current memory state of NVM element 52, M1 may connect
5 bitline BL1 to node 2 to apply a read voltage V_{read} across first and second
terminals of NVM 52 in a read operation. While read voltage V_{read} is applied,
a current flowing through bitline BL1 may then be sensed (e.g., at sense
circuit 203) to detect a current state of NVM element 52. According to an
embodiment, a magnitude of a current flowing through terminals of NVM
10 element 52 during a read operation may be limited to less than the magnitude
of I_{reset} . This may prevent an unintended transition of a current state of NVM
element 52 in a conductive or low impedance memory state to an insulative
or high impedance memory state during a read operation. Current flowing
through terminals of NVM element 52 during a read operation may be
15 controlled, for example, by controlling a voltage applied to a gate of FET M1
during read operations. In the particular implementation of Figure 5B, FET
M1 is configured as an NFET. Here, a boosted wordline voltage signal WL
may be applied during a write operation to permit sufficient current flowing
through NVM element 52 to place NVM element 52 in a particular memory
20 state. A voltage of wordline voltage signal WL may then be lowered during
read operations to limit current flowing through NVM element 52.
Alternatively, a voltage source applying a read voltage to bitline BL1 and/or
BL2 (e.g., write circuit 202) may limit a current flowing to bitline BL1 and/or
BL2 during a read operation.

25

In Figures 5A and 5B, in a particular implementation where NVM
element 52 comprises a CES element, NVM element 52 may have properties
of a resistor 51 and a capacitor 53. In a particular implementation where
NVM element 52 comprises a CES element, it should be understood that NVM
30 element 52 comprises a single monolithic material between terminals having
a variable resistance and variable capacitance determined based, at least in
part, on a particular memory state of NVM element 52. As such, it should be
understood that resistor 51 and capacitor 53 (shown as parallel devices in
Figures 5A and 5B) are not formed as separate or discrete elements, but that
35 resistor 51 and capacitor 53 as depicted in Figures 5A and 5B are intended to

represent resistive and capacitive properties of the monolithic material forming a CES element.

5 According to an embodiment, a capacitance of capacitor 53 and a resistance of resistor 51 may vary depending on a particular memory state of NVM element 52. For example, the capacitance of capacitor 53 and the resistance of resistor 51 may be high as NVM element 52 is in an insulative or high impedance memory state. Likewise, the capacitance of capacitor 53 and the resistance of resistor 51 may be low as NVM element 52 is in a
10 conductive or low impedance memory state. Here, if NVM element 52 comprises a CES element, a capacitance of capacitor 53 may increase or decrease in response to a quantum mechanical physical transformation to place NVM element 52 in different memory states as discussed above.

15 As NVM element 52 is placed in an insulative or high impedance state (e.g., in a write operation with application of V_{reset} and I_{reset}), current may continue to flow from bitline BL1 to NVM element 52 even following a transition to the insulative or high impedance memory state. While resistor 51 may not permit additional current to flow between first and second
20 terminals of NVM element 52, charge from current flowing through FET M1 to NVM element 52 may be stored in capacitor 53. As FET M1 opens to disconnect BL1 from NVM element 52, charge stored in capacitor 53 may dissipate through resistor 51.

25 Figures 5A and 5B employ different implementations of FET M1 as a conducting element to connect BL1 to node 2 during write or read operations. Table 2 below summarizes aspects of operation of the circuit of Figure 5A in different states/modes. During a set operation to place NVM element 52 in a conductive or low impedance memory state, current I_{set} may determine a
30 compliance current I_{comp} to affect a current to be applied in a subsequent reset operation I_{reset} as discussed above in connection with Figure 1. Also, voltages applied between bitlines BL1 and BL2 during write or read operations consider a voltage drop V_{ds} across FET M1.

State	R,C	WLB	$V_{BL1} - V_{BL2}$	$V_2 - V_{BL2}$	I_{BL1}
Powerup	L	-	0	0	-
W0 set	L	0	$V_{set} + V_{ds}$	V_{set}	I_{comp}
W1 reset	H	0	$V_{reset} + V_{ds}$	V_{reset}	I_{NFET}
Half select	-	0	$< V_t$	0	-
Unselect W0	H	1	V_{op}	0^*	Leak, capacitor discharge
Unselect W1	L	1	V_{op}	0	leak
Read	L,H	1	$V_t < V < V_{reset}$	$V_{read} < V_{reset}$	H/L
Hold	-	1	$V_t + V_{reset}$	0^*	-

Table 2

Table 3 below summarizes aspects of operation of the particular implementation of Figure 5B in which transistor M1 is configured as an NFET. Here, Table 3 differs from Table 2 to reflect that different wordline voltages are applied to a gate of transistor M1 during read and write operations.

State	R,C	WL	$V_{BL1} - V_{BL2}$	$V_2 - V_{BL2}$	I_{BL1}
Powerup	L	-	0	0	-
W0 set	L	1	$V_{set} + V_{ds}$	V_{set}	I_{comp}
W1 reset	H	1	$V_{reset} + V_{ds}$	V_{reset}	I_{NFET}
Half select	-	1	$< V_t$	0	-
Unselect W0	H	0	V_{op}	0^*	Leak, capacitor discharge
Unselect W1	L	0	V_{op}	0	leak
Read	L,H	0	$V_t < V < V_{reset}$	$V_{read} < V_{reset}$	H/L
Hold	-	0	$V_t + V_{reset}$	0^*	-

10 Table 3

It should be understood that the particular implementations discussed above with reference to Figures 5A and 5B are merely non-limiting examples,

and that other particular implementations may be used without deviating from claimed subject matter.

References throughout this specification to one implementation, an
5 implementation, one embodiment, an embodiment and/or the like means that
a particular feature, structure, and/or characteristic described in connection
with a particular implementation and/or embodiment is included in at least
one implementation and/or embodiment of claimed subject matter. Thus,
appearances of such phrases, for example, in various places throughout this
10 specification are not necessarily intended to refer to the same implementation
or to any one particular implementation described. Furthermore, it is to be
understood that particular features, structures, and/or characteristics
described are capable of being combined in various ways in one or more
implementations and, therefore, are within intended claim scope, for
15 example. In general, of course, these and other issues vary with context.
Therefore, particular context of description and/or usage provides helpful
guidance regarding inferences to be drawn.

While there has been illustrated and described what are presently
20 considered to be example features, it will be understood by those skilled in
the art that various other modifications may be made, and equivalents may
be substituted, without departing from claimed subject matter. Additionally,
many modifications may be made to adapt a particular situation to the
teachings of claimed subject matter without departing from the central
25 concept described herein. Therefore, it is intended that claimed subject
matter not be limited to the particular examples disclosed, but that such
claimed subject matter may also include all aspects falling within the scope
of the appended claims, and equivalents thereof.

30

CLAIMS

1. A non-volatile memory cell comprising:
a CES element; and
5 a conducting element to connect a first terminal of the CES element to a bitline responsive to a voltage signal on a wordline,
wherein the CES element is responsive to application of a first voltage across the first terminal and a second terminal of the CES element while maintaining a first current through the CES element to place a memory state
10 of the CES element in a first memory state;
wherein the CES element is responsive to application of a second voltage between the first terminal and the second terminal while maintaining a second current through the CES element to place the memory state of the CES element in a second memory state; and
15 wherein the memory state of the CES element is detectable based, at least in part, on a measured current through the CES element in response to application of a third voltage between the first and second terminals in a read operation.
- 20 2. The memory cell of claim 1, wherein the CES element comprises a resistance and a capacitance, and wherein the capacitance is increased in response to transition of the CES element from the first memory state to the second memory state, the increased capacitance to absorb excess charge on the first terminal and substantially dissipate the excess charge through the
25 resistance if the first terminal is subsequently disconnected from the bitline.
3. The memory cell of claim 2, wherein the capacitance is increased in response to a physical transformation of the CES element.
- 30 4. The memory cell of any preceding claim, wherein a magnitude of the third voltage is limited to being less than or equal to a magnitude of the second voltage.

5. The memory cell of any preceding claim, wherein the memory cell is placed in the second memory state in response to application of the second voltage between the first and second terminals for a dwell time.
- 5 6. The memory cell of any preceding claim, wherein a magnitude of the first voltage is greater than a magnitude of the second voltage, and wherein the magnitude of the second current is greater than a magnitude of the first current.
- 10 7. The memory cell of any preceding claim, wherein the first memory state comprises a conductive or low impedance memory state, and wherein the second memory state comprises an insulative or high impedance memory state.
- 15 8. The memory cell of any preceding claim, wherein the CES element comprises a CeRAM element.
9. The memory cell of any preceding claim, wherein a magnitude of the measured current is limited to less than a magnitude of the first and second current during the read operation to preserve the memory state of the CES element.
- 20 10. A method comprising:
applying a first voltage between a first terminal of a non-volatile memory element and a second terminal of the non-volatile memory element while maintaining a first current between the first and second terminals to place the non-volatile memory element in a first memory state in a first write operation;
applying a second voltage between the first and second terminals of the non-volatile memory element while maintaining a second current between the first and second terminals to place the non-volatile memory element in a second memory state in a second write operation; and
applying a third voltage between the first terminal and the second terminal in a read operation.
- 35

11. The method of claim 10, wherein a capacitance between the first and second terminals increases in response to the memory cell being placed in the second memory state, and wherein the capacitance decreases in response to the non-volatile memory element being placed in the first memory state.
- 5 12. The method of claim 10 or claim 11, wherein the non-volatile memory element comprises a CES element.
- 10 13. The method of any of claims 10 to 12, wherein the non-volatile memory element comprises a resistance and a capacitance, and further comprising:
increasing the capacitance in response to placing the non-volatile memory element in the second memory state, the increased capacitance to absorb charge on the first terminal; and
dissipating the absorbed charge through the resistance in response to
15 disconnecting the first terminal from a bitline.
- 14 The method of any of claims 10 to 12, wherein the non-volatile memory element comprises a resistance and a capacitance, and further comprising:
increasing the capacitance in response to placing the non-volatile memory
20 element in the first memory state, the increased capacitance to absorb charge on the first terminal; and
dissipating the absorbed charge through the resistance in response to disconnecting the first terminal from a bitline.
- 25 15. The method of claim 13 or claim 14, wherein the capacitance is increased in response to a physical transformation of the non-volatile memory element.
- 30 16. The method of any of claims 10 to 15, wherein the memory cell is placed in the second memory state in response to application of the second voltage between the first and second terminals for a dwell time.
17. The method of any of claims 10 to 16, wherein the first memory state comprises a conductive or low impedance memory state, and wherein the

second memory state comprises an insulative or high impedance memory state.

18. The method of any of claims 10 to 17, and further comprising detecting
5 the memory state of the non-volatile memory element based, at least in part,
on the third current through the non-volatile memory element measured
during application of the third voltage during the read operation, wherein a
magnitude of the third current is limited to less than the magnitude of the
first current to maintain the memory state of the non-volatile memory
10 element during the read operation.

19 The method according to any of claims 10 to 18, wherein a magnitude
of the first voltage is greater than a magnitude of the second voltage, and
wherein a magnitude of the second current is greater than a magnitude of
15 the first current.

20 The method according to any of claims 10 to 19, wherein a magnitude
of the second voltage is greater than a magnitude of the first voltage, and
wherein a magnitude of the first current is greater than a magnitude of the
second current.
20

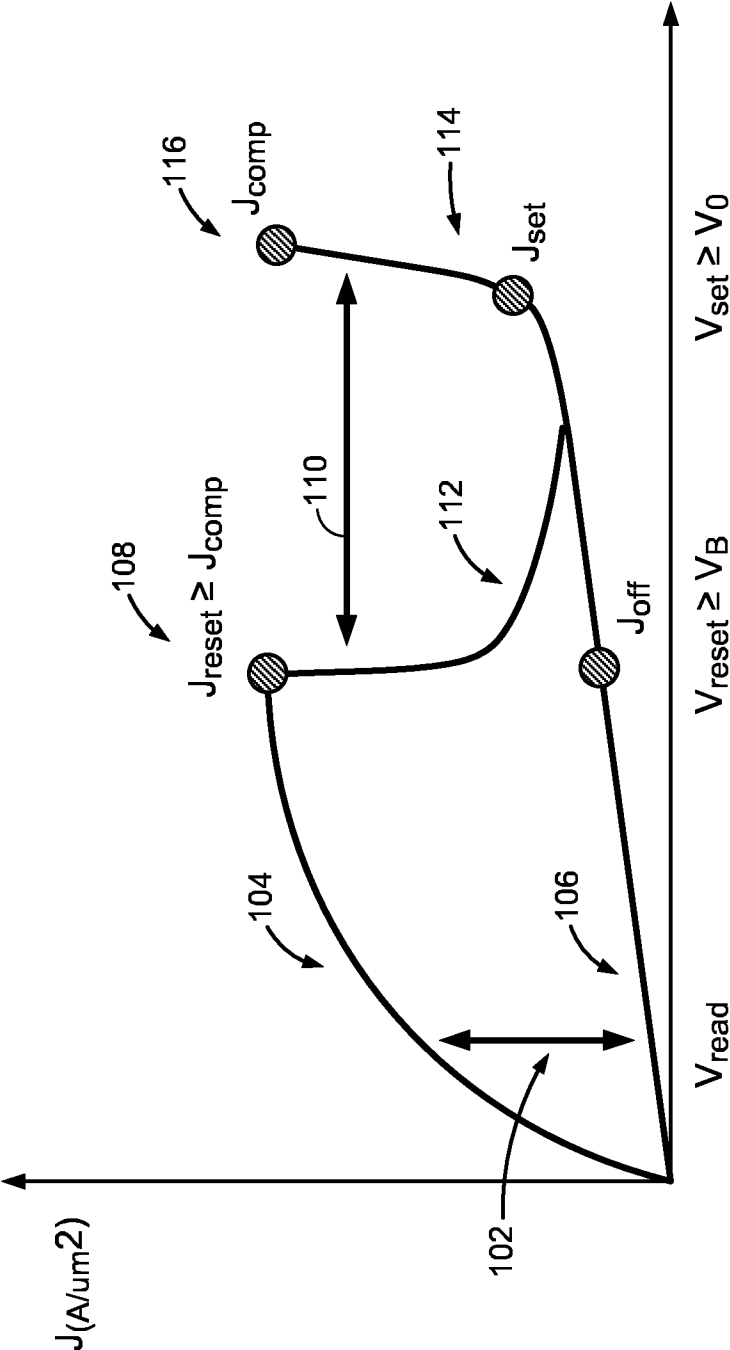


FIG. 1A

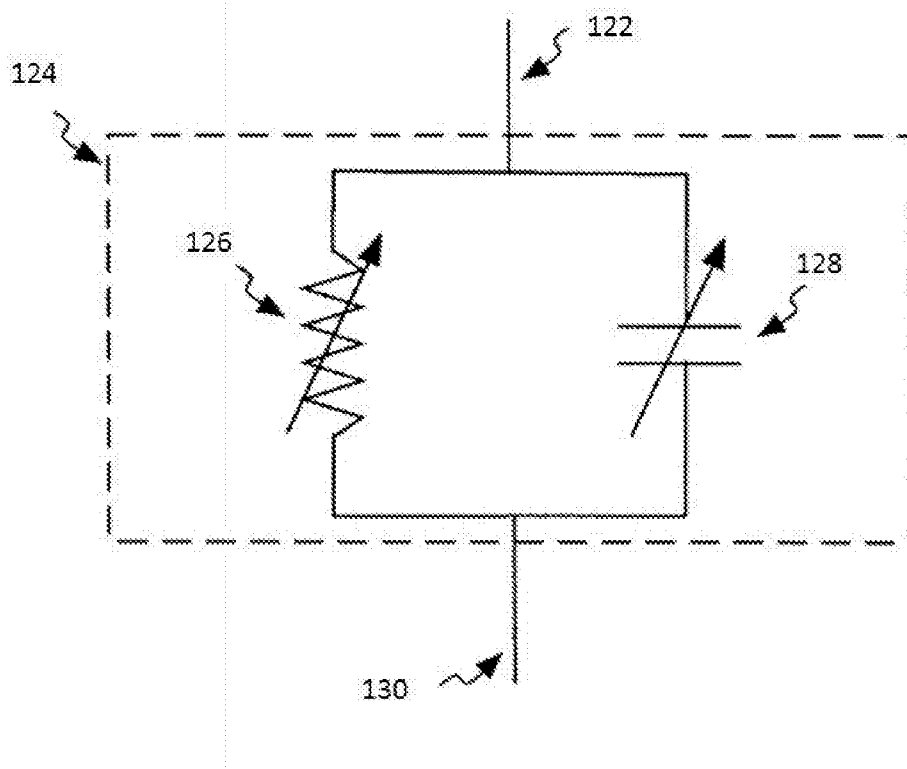
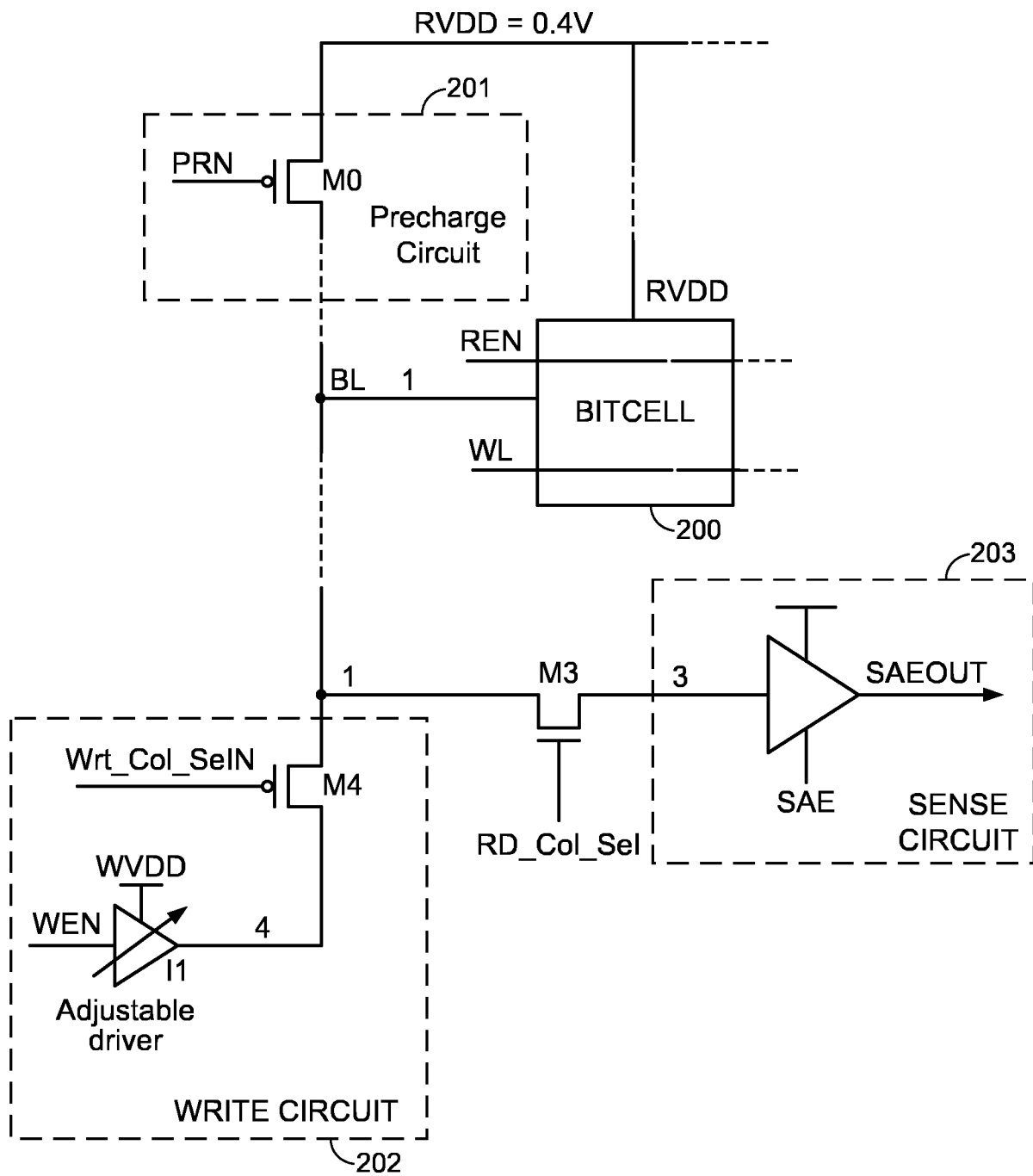
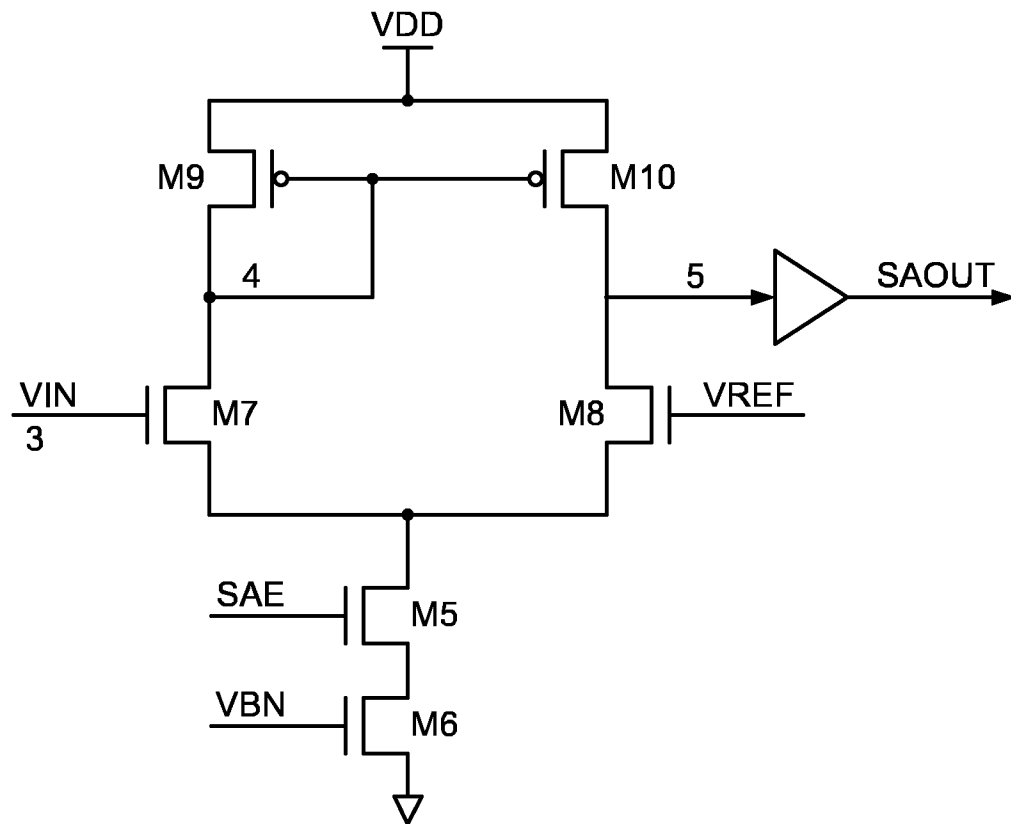
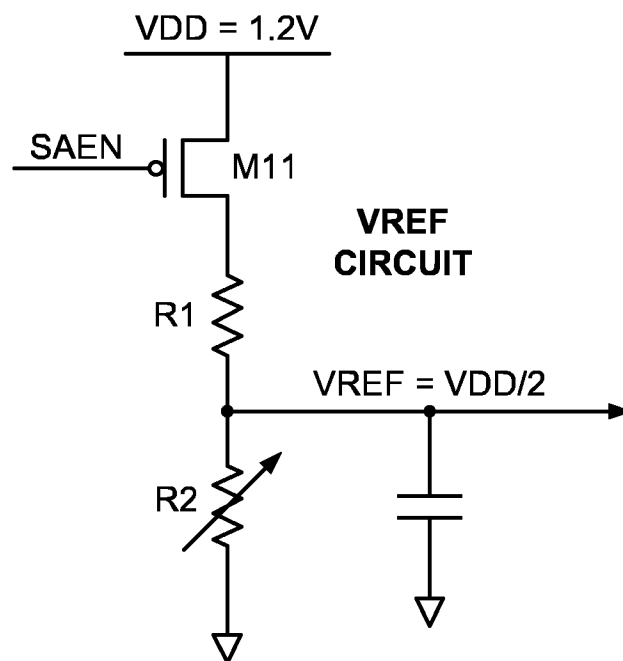


FIG. 1B

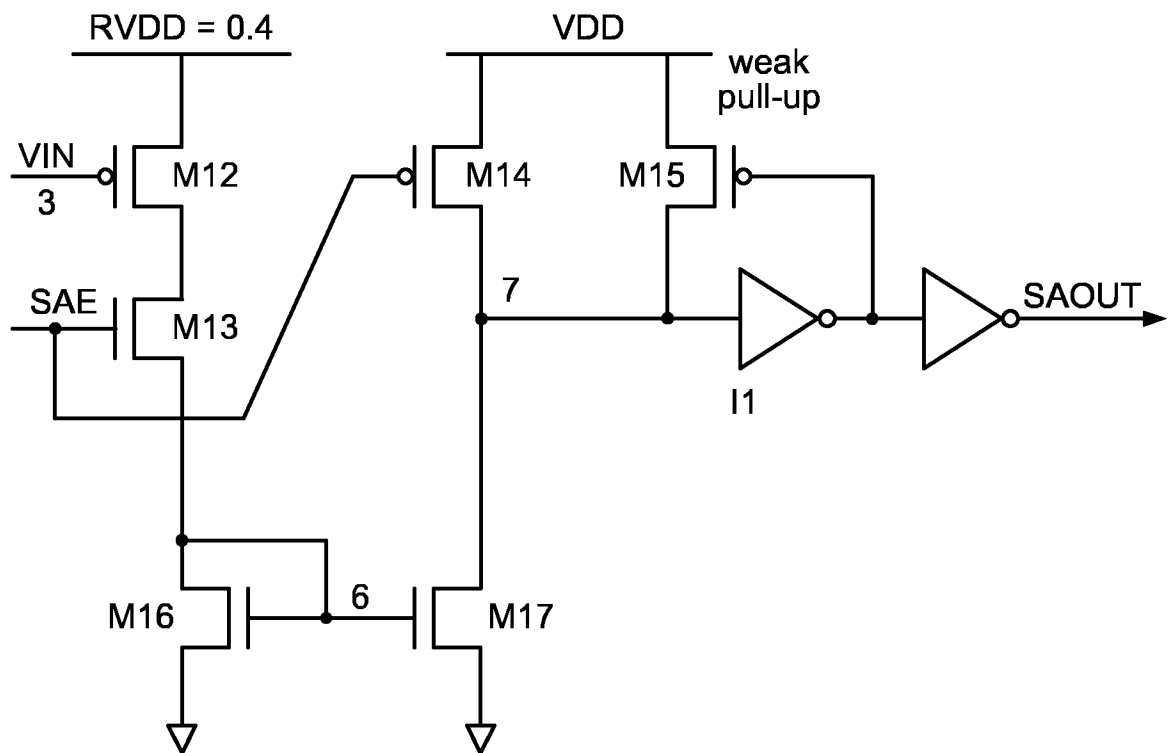
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**FIG. 2**

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**FIG. 3A****FIG. 3B**

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**FIG. 3C**

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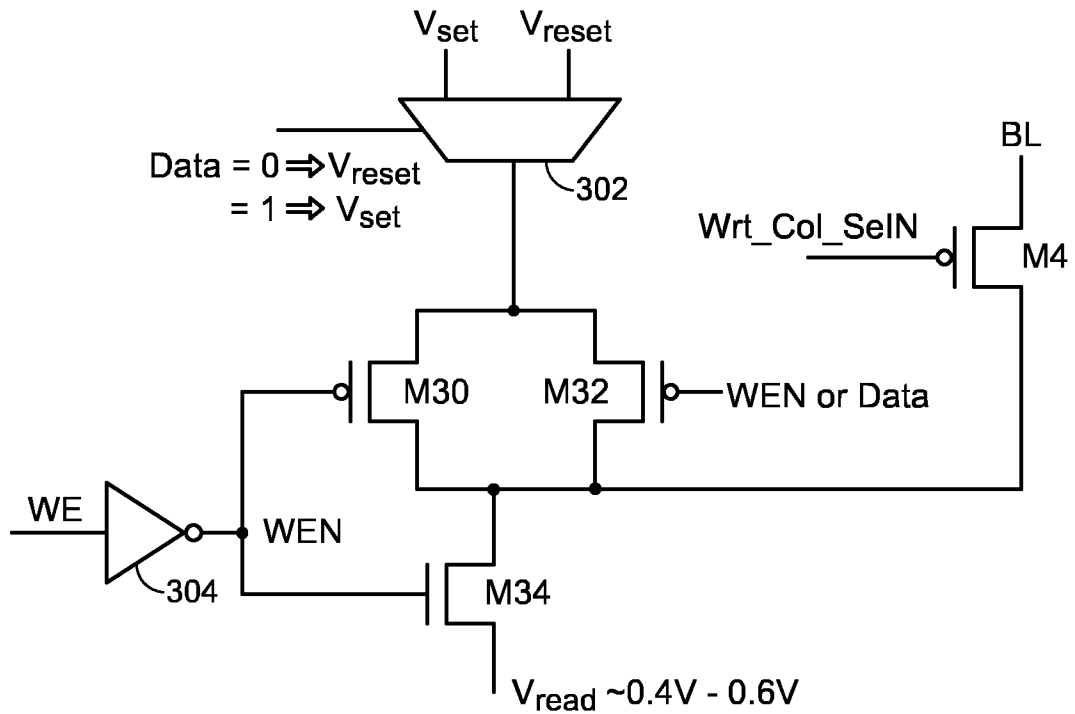


FIG. 4A

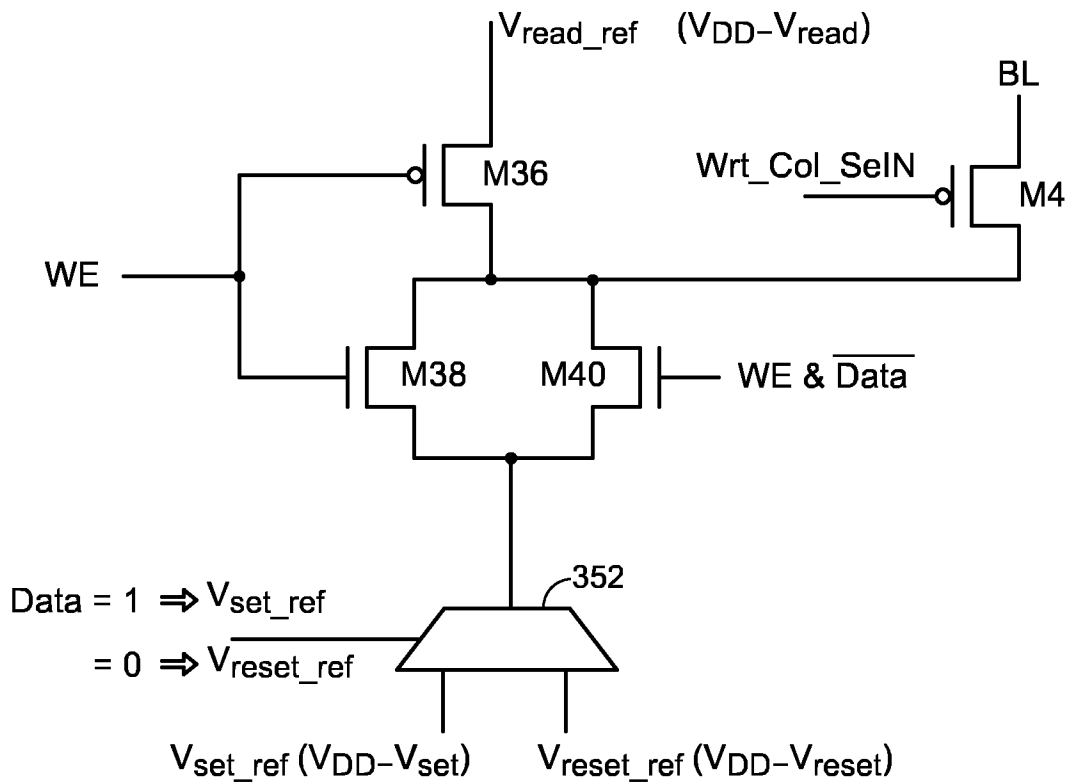


FIG. 4B

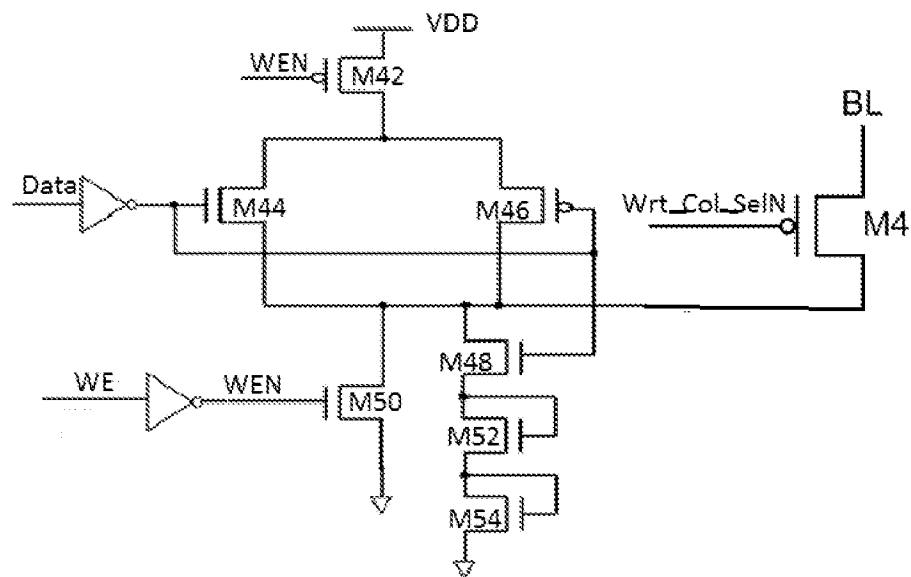


FIG. 4C

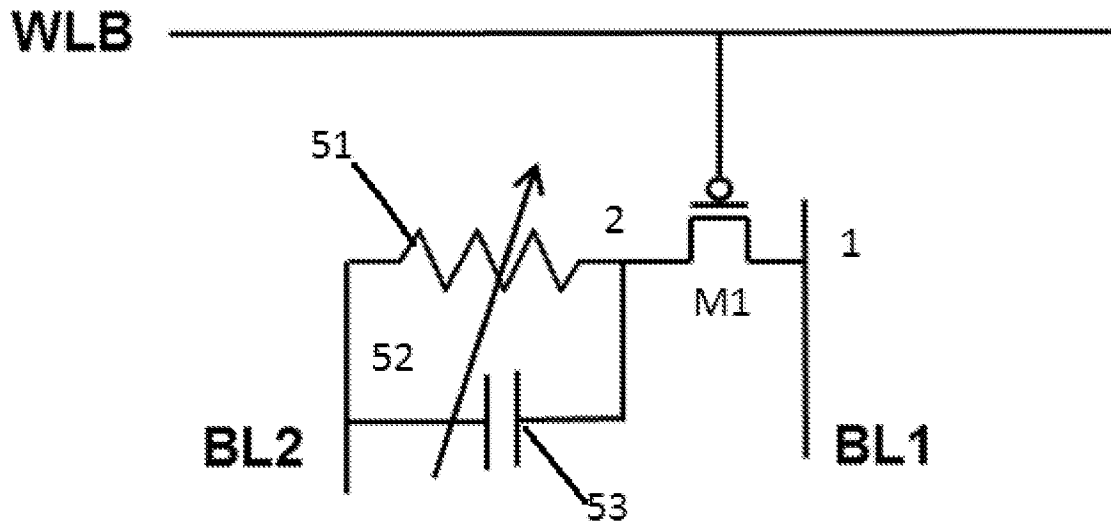


FIG. 5A

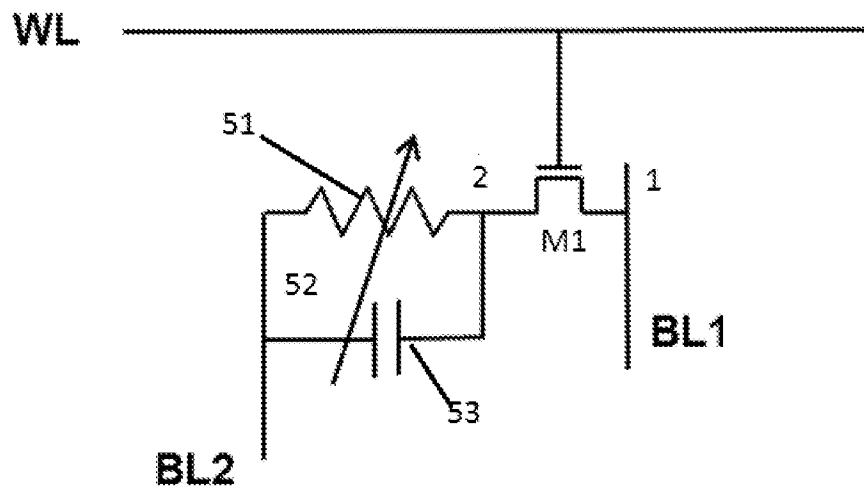


FIG. 5B

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2016/052519

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C13/00

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/127779 A1 (SCHEUERLEIN ROY E [US] ET AL) 24 May 2012 (2012-05-24)	10,11
Y	paragraphs [0003] - [0006], [0087] - [0092], [0113] - [0117], [0128] - [0133], [0261] - [0265]; figures 1A, 3, 4A, 5, 17A, 19A, 19B	1-9, 12-20
X	US 2010/118591 A1 (SUGIBAYASHI TADAHIKO [JP]) 13 May 2010 (2010-05-13)	10,11
Y	paragraphs [0004] - [0011], [0032] - [0041]; figures 1-5	1-9, 12-20
	----- -/--	



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

14 October 2016

Date of mailing of the international search report

21/10/2016

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INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2009/140299 A2 (SYMETRIX CORP [US]; CELINSKA JOLANTA [US]; PAZ DE ARAUJO CARLOS A [US]) 19 November 2009 (2009-11-19) page 2, lines 13-31; figures 1, 3, 4, 6a, 6b, 8 page 7, line 23 - page 8, line 24 page 9, lines 4-24 page 11, lines 7-28 page 12, line 9 - page 13, line 4 page 15, lines 3-11 -----	1-9, 12-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2016/052519

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012127779	A1	24-05-2012	NONE

US 2010118591	A1	13-05-2010	JP 5146847 B2 20-02-2013
		US 2010118591 A1	13-05-2010
		WO 2008120480 A1	09-10-2008

WO 2009140299	A2	19-11-2009	NONE
