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(54) Title: SYSTEM AND METHOD FOR CONTROLLING MODULATION

(57) Abstract: A system and method for controlling modulation. The system includes a plurality of modulators and a transmitting unit. The plurality of modulators decodes data from a data signal and also encodes the data into a clock signal. The transmitting unit transmits the encoded clock signal. According to the system and method disclosed herein, the present invention provides optimized coding efficiency while minimizing overall power consumption.



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SYSTEM AND METHOD FOR CONTROLLING MODULATION

FIELD OF THE INVENTION

The present invention relates to data transmission, and more particularly to a system and method for controlling modulation.

BACKGROUND OF THE INVENTION

High-speed serial data transmission between integrated circuits is a major source of power consumption due to high switching rates and driving currents associated with signal and clock transmission. One conventional solution is to use single-channel serial transmission (SCST), which causes a dynamic power draw. However, SCST suffers from board noise sensitivity. Another conventional solution is to use differential transmission, which is more immune to board noise. However, differential transmission requires twice as many board traces, making it expensive to manufacture. Also, differential transmission draws a significant amount of static current during operation.

Another conventional solution is to use frequency modulation techniques, which are effective at compressing data and providing noise immunity. However, these techniques require additional circuitry and do not address the high-power consumption issues. In fact, frequency modulation techniques consume too much power for most applications.

Accordingly, what is needed is an improved system and method for transmitting data. The system and method should be efficient, simple, cost effective and capable of being easily adapted to existing technology. The present invention addresses such a need.

SUMMARY OF THE INVENTION

A system and method for controlling modulation is disclosed. The system includes a plurality of modulators and a transmitting unit. The plurality of modulators decodes data from a data signal and also encodes the data into a clock signal. The transmitting unit transmits the encoded clock signal. According to the system and method disclosed herein, the present invention provides optimized coding efficiency while minimizing overall power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a modulator in accordance with the present invention.

Figure 2 is a flow chart showing a method for controlling phase modulation in accordance with the present invention.

Figure 3 is a block diagram showing phase modulators, which can be used to implement the phase modulators of Figure 1, in accordance with the present invention.

Figure 4 is a block diagram of a decoder, which can be used to implement one of the phase modulators of Figure 3, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to data transmission, and more particularly to a system and method for controlling phase modulation. The following description is presented to enable one of ordinary skill in the art to make and use the invention, and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features described herein.

A system and method in accordance with the present invention for controlling modulation are disclosed. The system includes a modulator that encodes data into a clock signal, where the encoding is based on relative phase positions. This optimizes coding efficiency and minimizes switching, which minimizes power consumption. To more particularly describe the features of the present invention, refer now to the following description in conjunction with the accompanying figures.

Although the present invention disclosed herein is described in the context of phase modulation and chip/board level signal transmission, the present invention may apply to other types of modulation and other levels of signal transmission and still remain within the spirit and scope of the present invention.

Figure 1 is a block diagram of a modulator 100 in accordance with the present invention. In a specific embodiment, the modulator 100 is a 21-bit modulator, which includes phase modulators 102, 104, 106, 108, 110, 112, and 114. The phase modulators 102-114 are 3-bit phase modulators. The modulator 100 also includes 8-bit units 120,

122, 124, 126, 128, 130, 132, and 136, and feedback glitch filters 140 and 142.

Figure 2 is a flow chart showing a method for controlling phase modulation in accordance with the present invention. Referring to both Figures 1 and 2 together, the modulator 100 decodes data from a data signal, in a step 202. Next, each of the phase modulators 102-114 encodes the data into an edge of a reference clock signal, in a step 204. Since the phase modulators 102-114 are 3-bit phase modulators, 3-bit words are encoded. Encoding 3 bits into each edge of the reference clock signal maximizes the amount of data in each transmission signal. While the phase modulators 102-114 are 3-bit phase modulators, the exact number of bits per modulator will depend on the specific application. Modulators of greater than 3-bits can be used and still remain within the spirit and scope of the present invention.

In this specific embodiment, there are seven 3-bit phase modulators 102-114. As a result, a total 21 bits of data are transmitted during each reference clock cycle. The exact number of 3-bit phase modulators will depend on the specific application. Next, the 8-bit units 120-136 transmit the data encoded reference clock signal, in a step 206.

Because data and clock information is combined into one transmission signal, the transmission signal can be transmitted at lower frequency without compromising performance. Operating at lower frequencies contributes to lower overall power consumption. For example, by using a 3-bit encoding scheme in specific embodiments of the present invention, the signal switching rate can be reduced by 20% with respect to conventional serial transmission schemes. Furthermore, the phase modulators of the present invention consume little power by themselves and can be completely powered down while retaining settings in digital registers.

Furthermore, by minimizing the number of transmitting channels, the number of board traces is lowered. This makes the modulator 100 less susceptible to board noise. In addition, modulator 100 maintains a fixed switching rate, which makes it easier to transmit and recover data.

Next, the feedback filters 140 and 142 calibrate a reference clock signal, in a step 208. This prevents glitches along the transmission line. The calibrating is accomplished by resetting the reference clock after the data has been transmitted through the modulator 100. This self-reset feature is done automatically and provides calibration with respect to the specific data set that is transmitted in a particular edge. Automatically resetting the reference clock eliminates phase error accumulation and compensates for process

variation. This also ensures that each edge is later decoded correctly.

Figure 3 is a block diagram showing phase modulators 302, 304, 306, 308, 310, 312, and 314, which can be used to implement the phase modulators 102-114 of Figure 1, respectively, in accordance with the present invention. Storage registers 320, 322, 324, 326, and 328 store data provided by the phase modulators 302-314. The storage registers 320-328 together store 21 bits of data, which are subsequently transmitted in the reference clock signal.

In operation, generally, the phase modulators 302-314 decode data from a data signal, which is received via an input unit 330. The input unit 330 reads in the first edge of a data signal and then feeds the first edge into each of the phase modulators 302-314. In a specific embodiment, the first edge is a rising edge. Each of the phase modulators 302-314 enables an edge of the transmission signal to carry a 3-bit digital value. The seven 3-bit modulators output a total of 21 bits of data. The storage registers 230-238 store the 21 bits.

Figure 4 is a block diagram of a decoder 400, which can be used to implement one of the phase modulators 302-314 of Figure 3, in accordance with the present invention. The decoder 400 is a 3-bit decoder and includes filters 402, 404, 406, 408, 410, 412, and 414. In a specific embodiment, the filters 402-414 are 8-bit finite impulse response (FIR) counter filters. Each of the filters 402-414 stores an 8-bit value, providing high performance on a granular scale.

In operation, the decoder 400 decodes data from a data signal. Each filter 402-414 then reads a phase position from a delay chain. Based on the decoded data and the phase readings, the decoder 400 outputs a 3-bit digital value that indicates one of eight possible phase positions. The 3-bit digital value represents a 3-bit word, which is subsequently combined with other 3-bit words from other decoders to provide a 21-bit word.

The phase positions are relative to a reference phase provided by the reference clock. The decoder 400 is asynchronous in that the reference clock is separate and independent from the system clock. Accordingly, the decoder 400 does not rely on the system clock to decode or to generate the phase reference. This is possible because the modulator 100 is data-locked to a reference clock signal.

According to the system and method disclosed herein, the present invention provides numerous benefits. For example, data-locked dual-edge phase modulation

(DEPM) is provided with optimized coding efficiency and minimized power consumption. Embodiments of the present invention also provide a fixed switching rate and high noise rejection, eliminate phase error accumulation, and compensate for process variation.

A system and method for controlling modulation has been disclosed. The system includes a modulator that encodes data into a clock signal. This optimizes coding efficiency and minimizes switching, which minimizes power consumption.

The present invention has been described in accordance with the embodiments shown. One of ordinary skill in the art will readily recognize that there could be variations to the embodiments, and that any variations would be within the spirit and scope of the present invention. For example, the present invention can be implemented using hardware, software, a computer readable medium containing program instructions, or a combination thereof. Software written according to the present invention is to be either stored in some form of computer-readable medium such as memory or CD-ROM, or is to be transmitted over a network, and is to be executed by a processor. Consequently, a computer-readable medium is intended to include a computer readable signal, which may be, for example, transmitted over a network. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A modulator circuit comprising:
a plurality of modulators, wherein the plurality of modulators decodes data from a data signal and also encodes the data into a clock signal; and
a transmitting unit coupled to the plurality of modulators, wherein the transmitting unit transmits the encoded clock signal.
2. The circuit of claim 1 wherein the plurality of modulators encode the data, based on relative phase positions, into the clock signal.
3. The circuit of claim 1 further comprising a feedback filter coupled to the plurality of modulators, wherein the feedback filter calibrates a clock signal.
4. The circuit of claim 3 wherein the clock is reset after the data has been transmitted.
5. The circuit of claim 3 wherein the clock is reset automatically.
6. The circuit of claim 1 wherein each of the plurality of modulators is at least a 3-bit modulator.
7. The circuit of claim 1 wherein each of the plurality of modulators comprises a plurality of decoders, wherein each decoder of the plurality of decoders decodes data from the data signal, reads a phase position from a delay chain, and outputs a value, wherein the value indicates a phase position.
8. The circuit of claim 7 wherein the value represents a word.
9. The circuit of claim 8 wherein the word is combined with other words from other decoders of the plurality of decoders to provide at least a 21-bit word.

10. The circuit of claim 1 wherein the plurality of modulators encodes the data into an edge of the clock signal.
11. A modulator circuit comprising:
 - a plurality of modulators, wherein the plurality of modulators decodes data from a data signal and also encodes the data, based on relative phase positions, into a clock signal;
 - a transmitting unit coupled to the plurality of modulators, wherein the transmitting unit transmits the encoded clock signal; and
 - a feedback filter coupled to the plurality of modulators, wherein the feedback filter automatically calibrates a clock signal, wherein the calibrating occurs after the data has been transmitted.
12. The circuit of claim 11 wherein each of the plurality of modulators comprises a plurality of decoders, wherein each decoder of the plurality of decoders decodes data from the data signal, reads a phase position from a delay chain, and outputs a value, wherein the value indicates a phase position.
13. The circuit of claim 12 wherein the value represents a word.
14. The circuit of claim 13 wherein the word is combined with other words from other decoders of the plurality of decoders to provide at least a 21-bit word.
15. The circuit of claim 11 wherein the plurality of modulators encodes the data into an edge of the clock signal.
16. A method for controlling modulation, the method comprising:
 - decoding data from a data signal;
 - encoding the data into a clock signal; and
 - transmitting the encoded clock signal.
17. The method of claim 16 further comprising calibrating the clock signal.

18. The method of claim 17 wherein the calibrating step comprises resetting the clock signal, wherein the resetting occurs after the data has been transmitted.
19. The method of claim 18 wherein the clock is reset automatically.
20. The method of claim 16 wherein the encoding step comprises:
reading a phase position from a delay chain; and
outputting a value, wherein the value indicates a phase position.
21. The method of claim 20 wherein the value represents a word.
22. The method of claim 21 further comprising combining the word with other words to provide at least a 21-bit word.
23. The method of claim 16 wherein the encoding step comprises encoding the data into an edge of the clock signal.
24. A method for controlling modulation, the method comprising:
decoding data from a data signal;
encoding the data into a clock signal, wherein the encoding step is based on relative phase positions; and
transmitting the encoded clock signal.
25. A computer readable medium containing program instructions for controlling modulation, the program instructions which when executed by a computer system cause the computer system to execute a method comprising:
decoding data from a data signal;
encoding the data into a clock signal; and
transmitting the encoded clock signal.
26. The computer readable medium of claim 25 wherein the encoding step is based on relative phase positions.

27. The computer readable medium of claim 25 further comprising program instructions for calibrating the clock signal.
28. The computer readable medium of claim 27 wherein the calibrating step comprises program instructions for resetting the clock signal, wherein the resetting occurs after the data has been transmitted.
29. The computer readable medium of claim 28 wherein the clock is reset automatically.
30. The computer readable medium of claim 25 wherein the calibrating step comprises program instructions for resetting the clock signal, wherein the resetting occurs after the data has been transmitted.
31. The computer readable medium of claim 30 wherein the clock is reset automatically.
32. The computer readable medium of claim 25 wherein the encoding step comprises program instructions for:
reading a phase position from a delay chain; and
outputting a value, wherein the value indicates a phase position.
33. The computer readable medium of claim 32 wherein the value represents a word.
34. The computer readable medium of claim 33 further comprising program instructions for combining the word with other words to provide at least a 21-bit word.
35. The computer readable medium of claim 25 wherein the encoding step comprises program instructions for encoding the data into an edge of the clock signal.

FIG.1/1	FIG.1/2	FIG.1/3	FIG.1/4
FIG.1/5	FIG.1/6	FIG.1/7	FIG.1/8
FIG.1/9	FIG.1/10	FIG.1/11	FIG.1/12
FIG.1/13	FIG.1/14	FIG.1/15	FIG.1/16

FIG.1 100

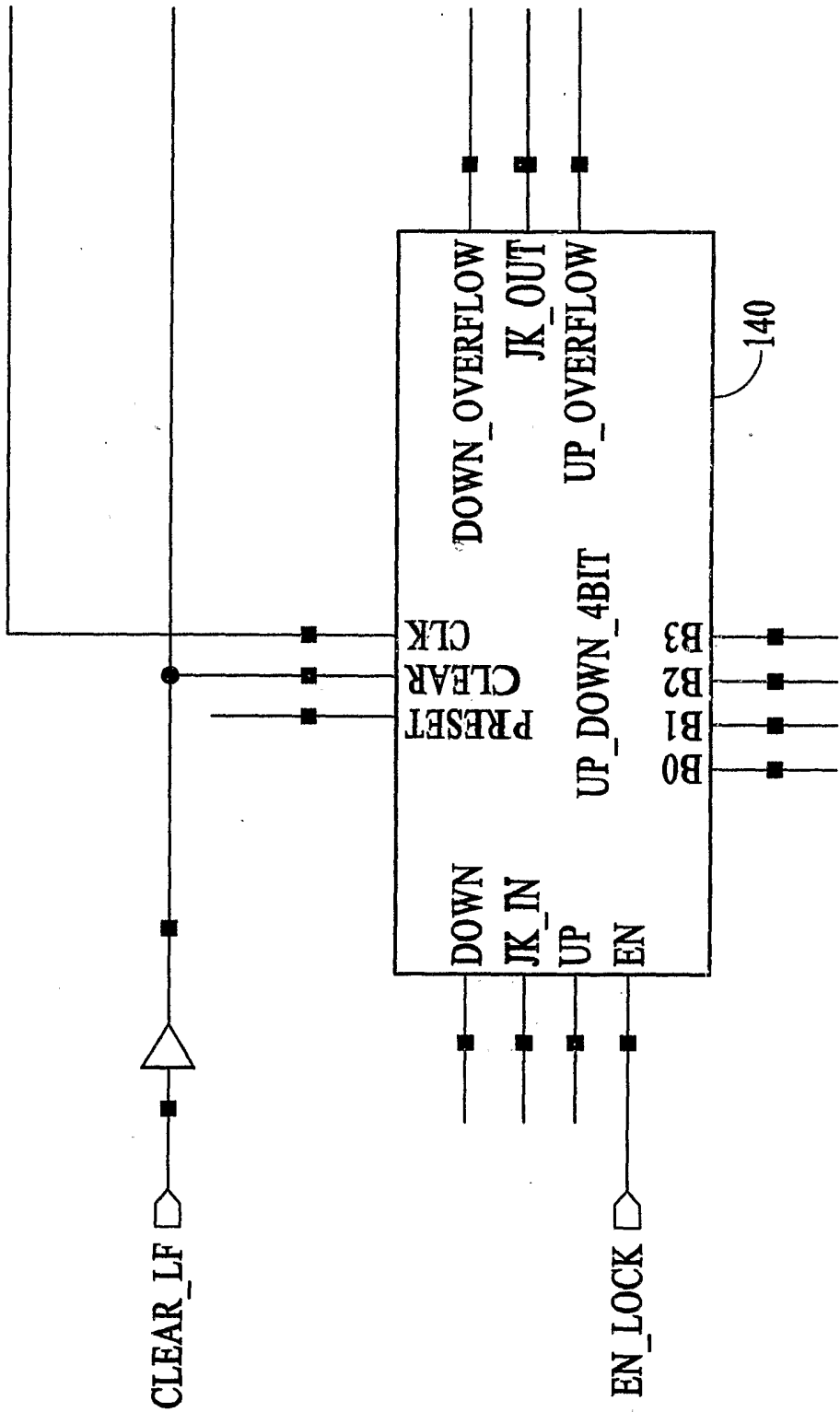


FIG.1/1

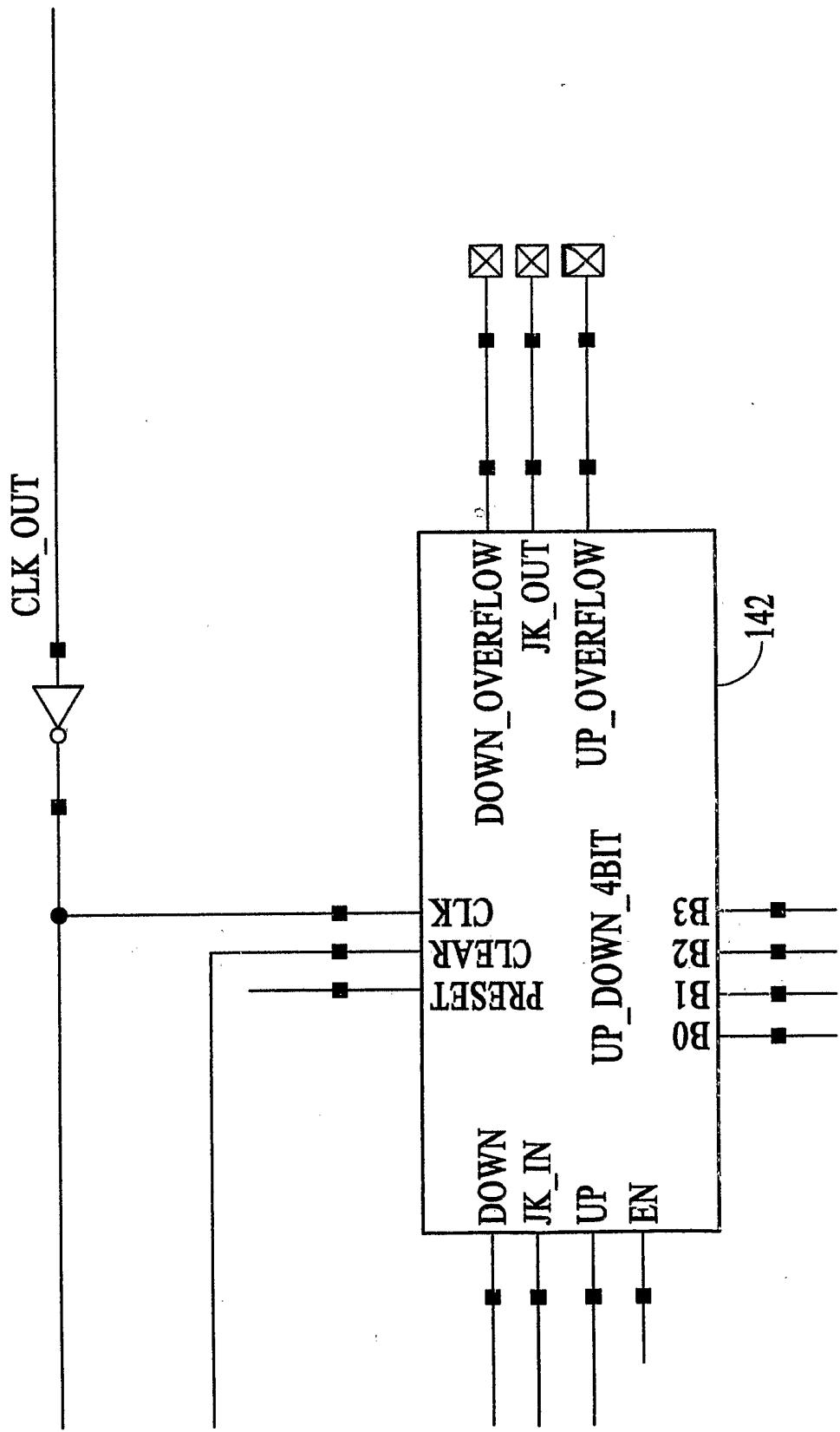
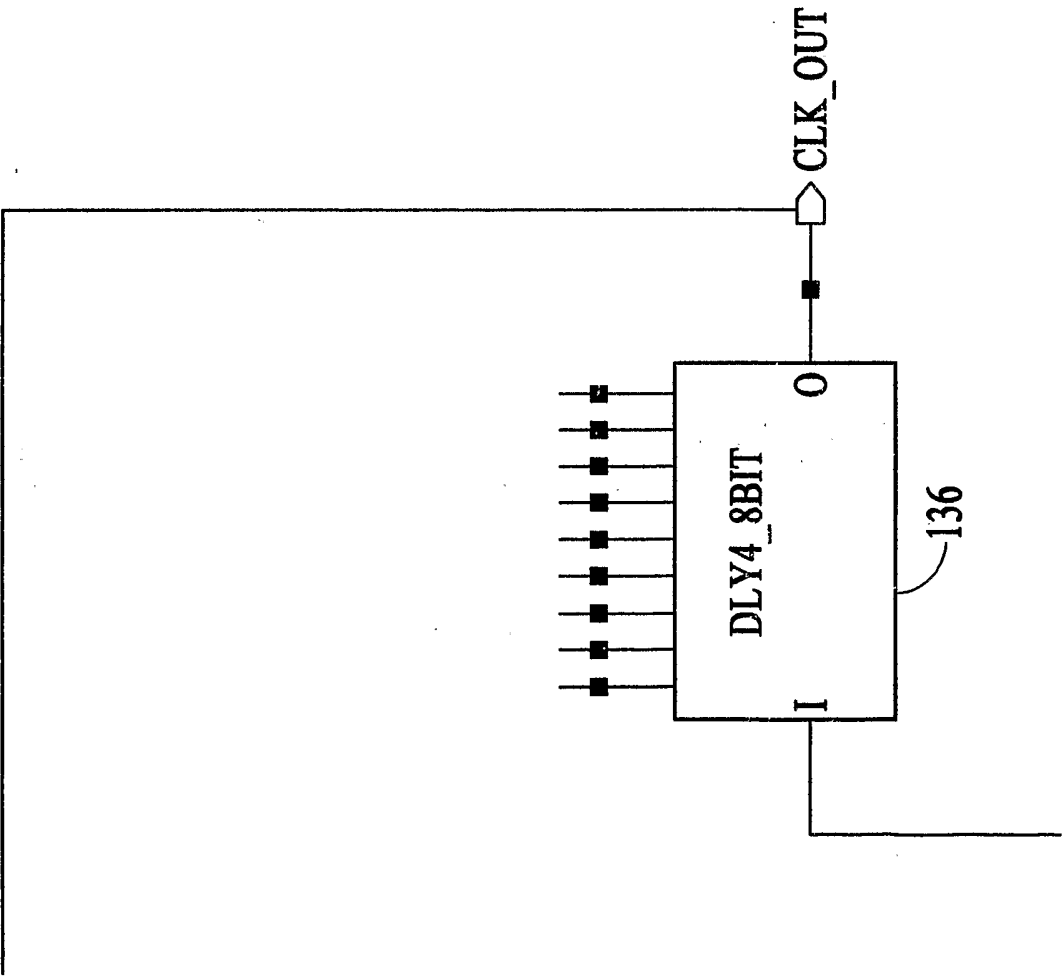


FIG.1/2

FIG. 1/3

FIG.1/4



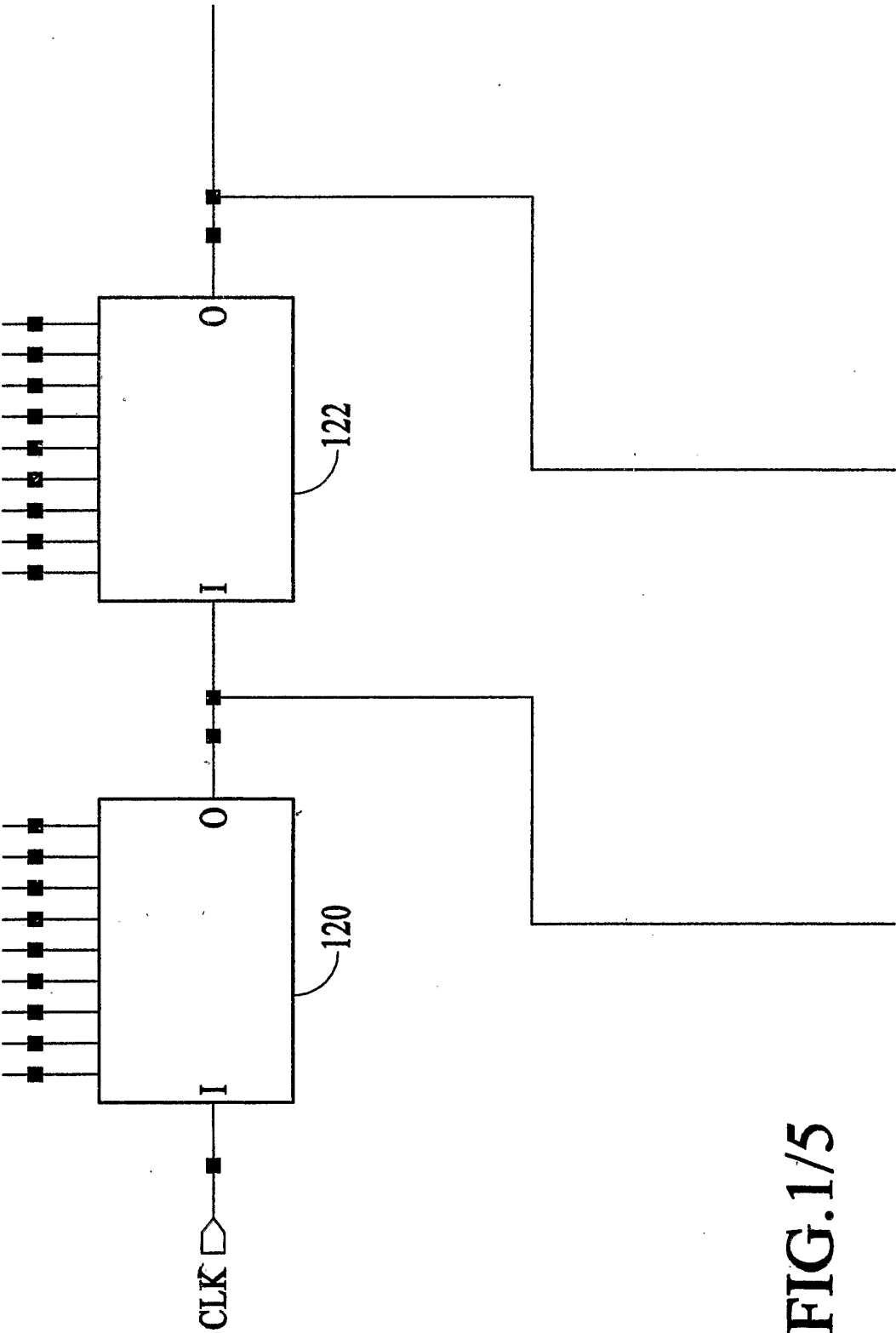
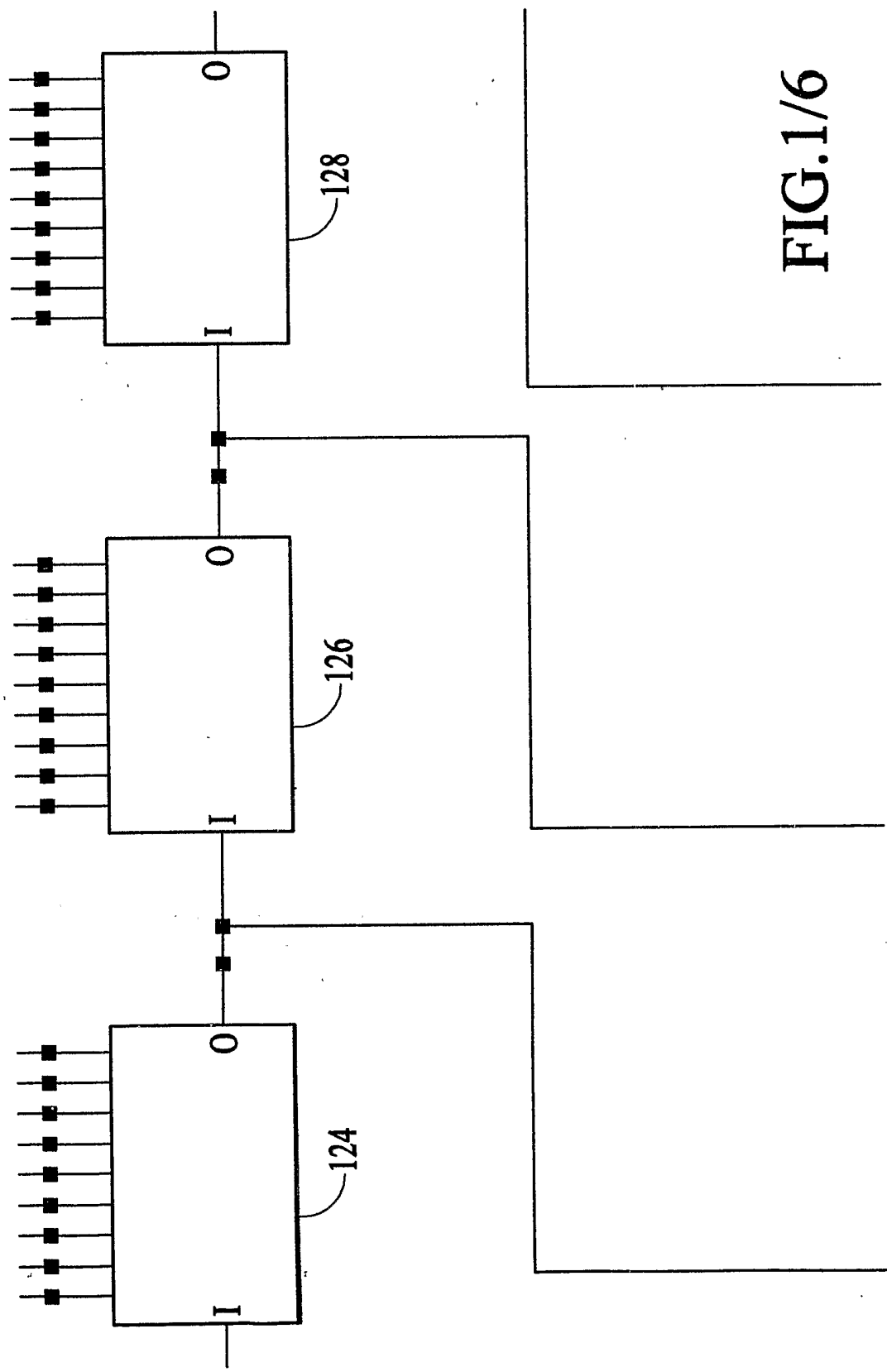


FIG.1/5



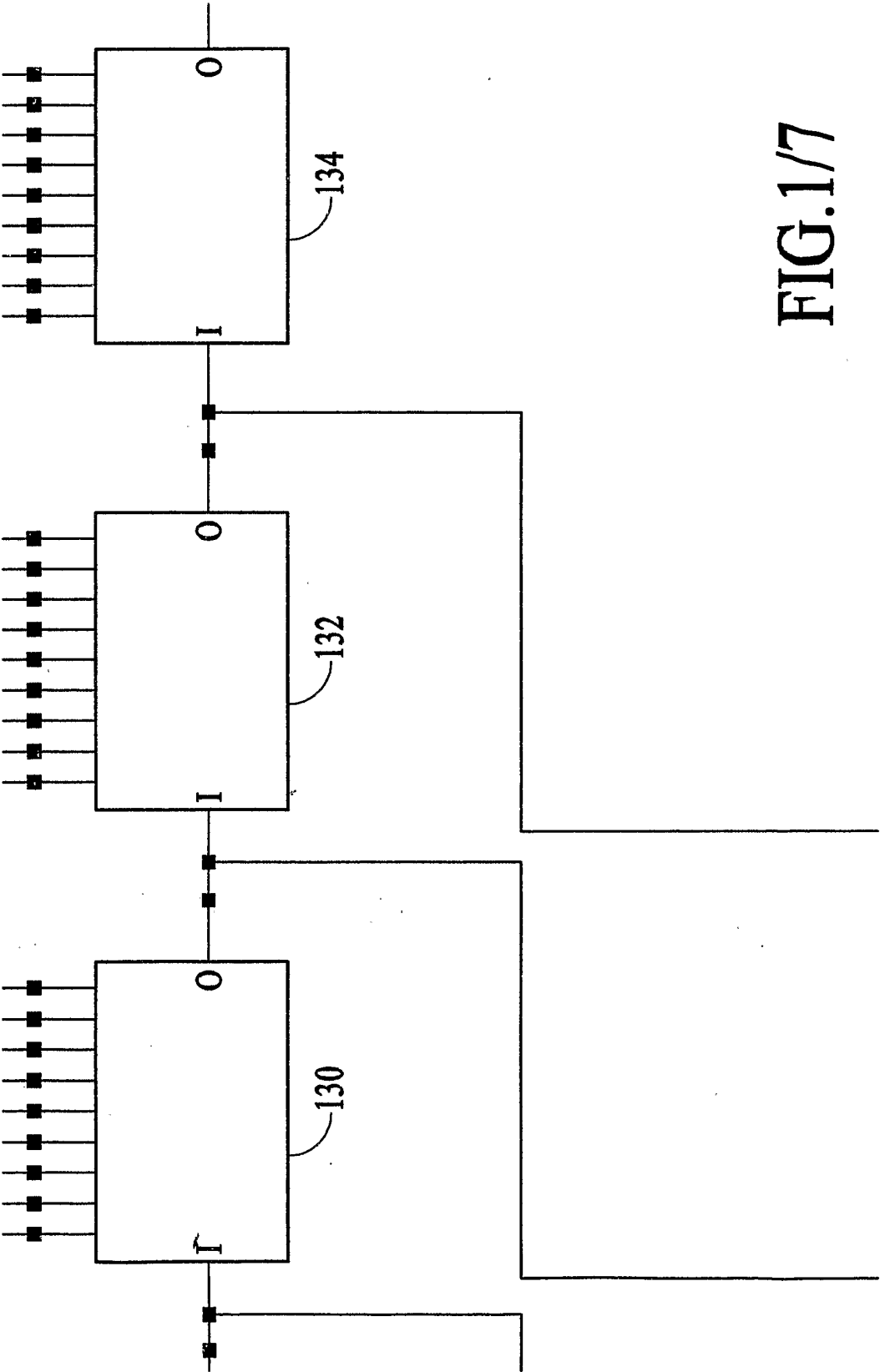


FIG.1/7

FIG. 1/8



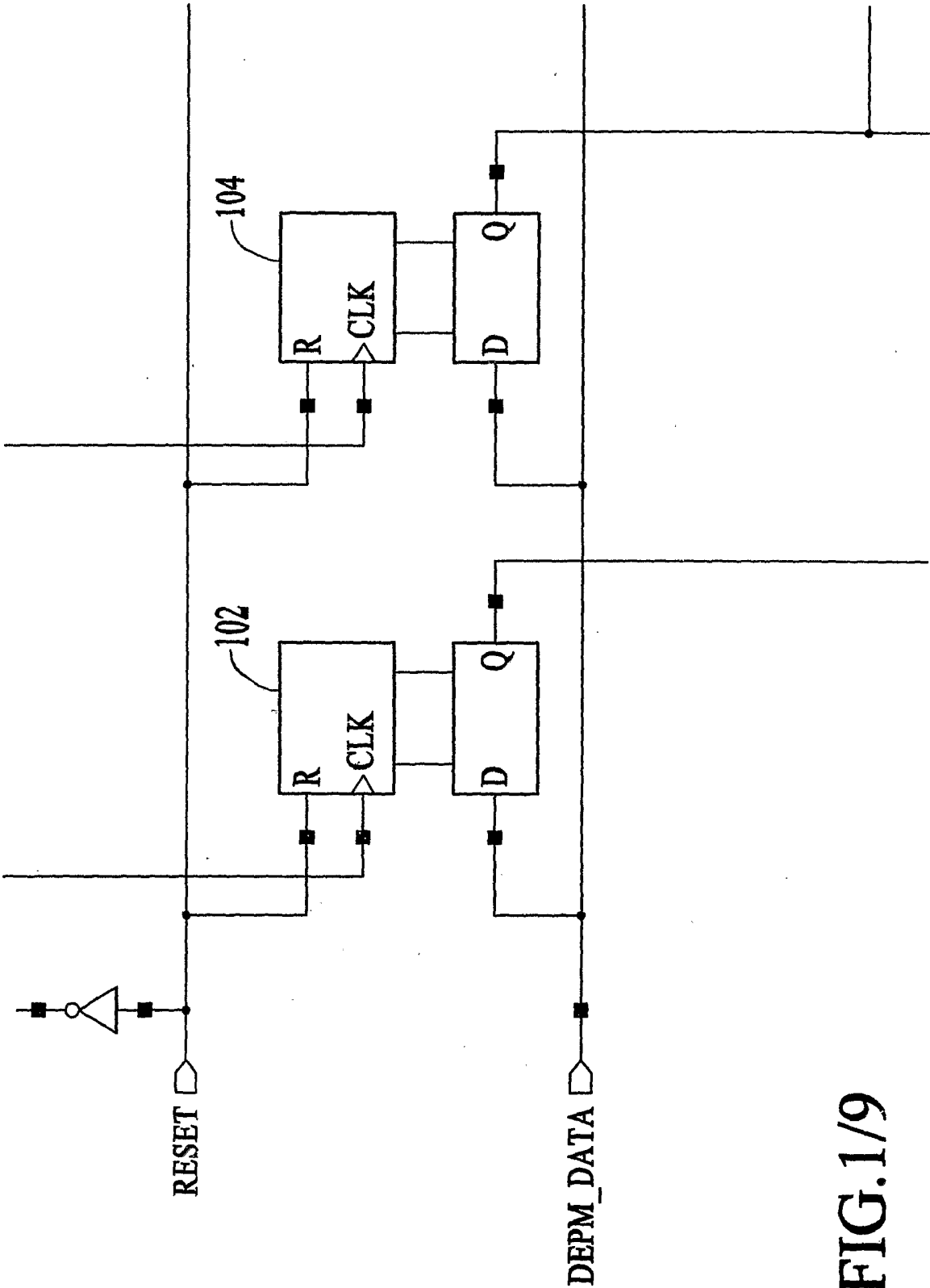


FIG.1/9

FIG. 1/10

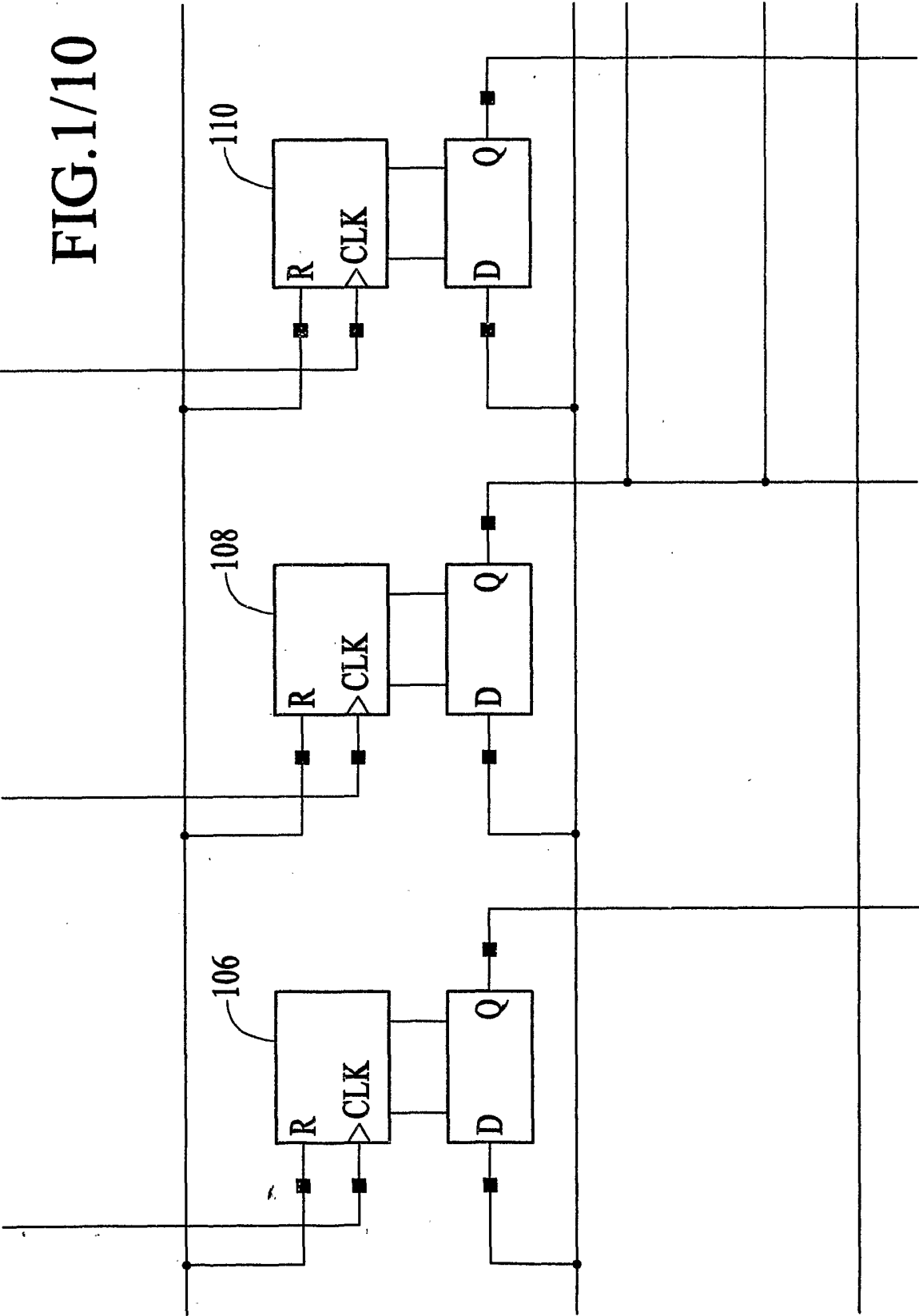


FIG.1/11

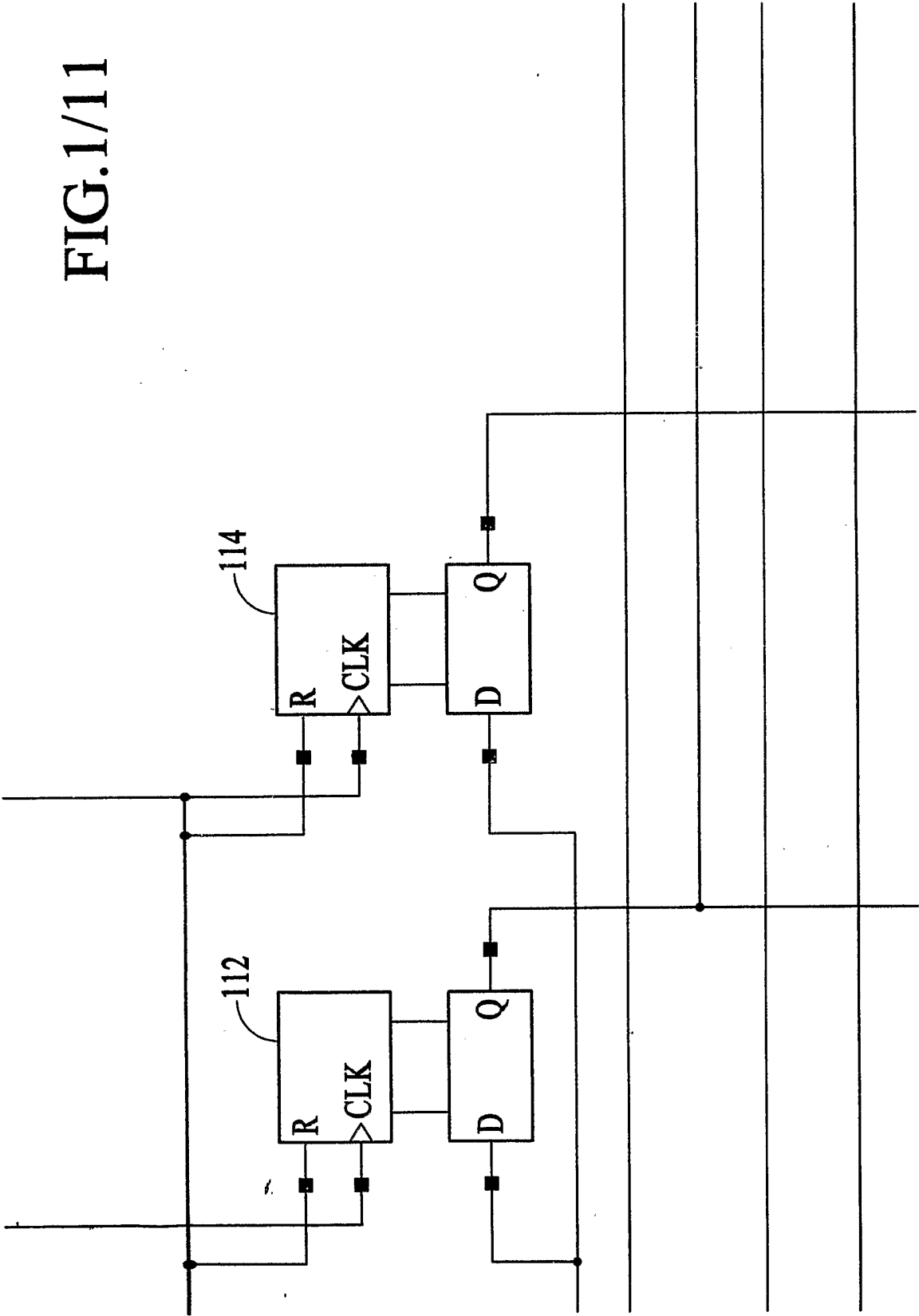
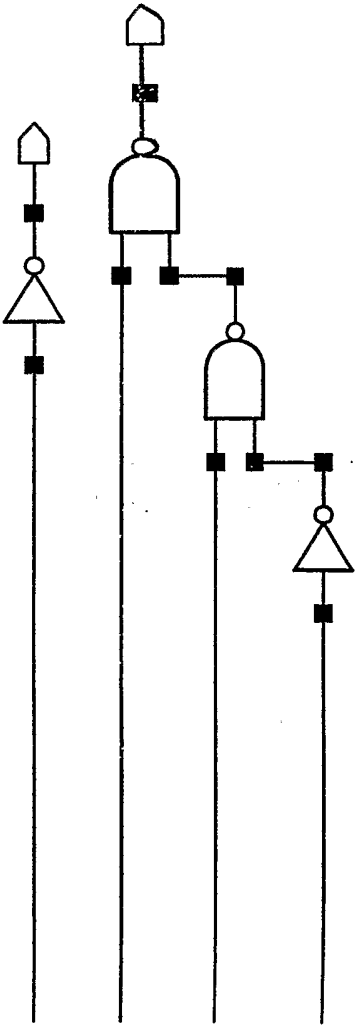


FIG. 1/12



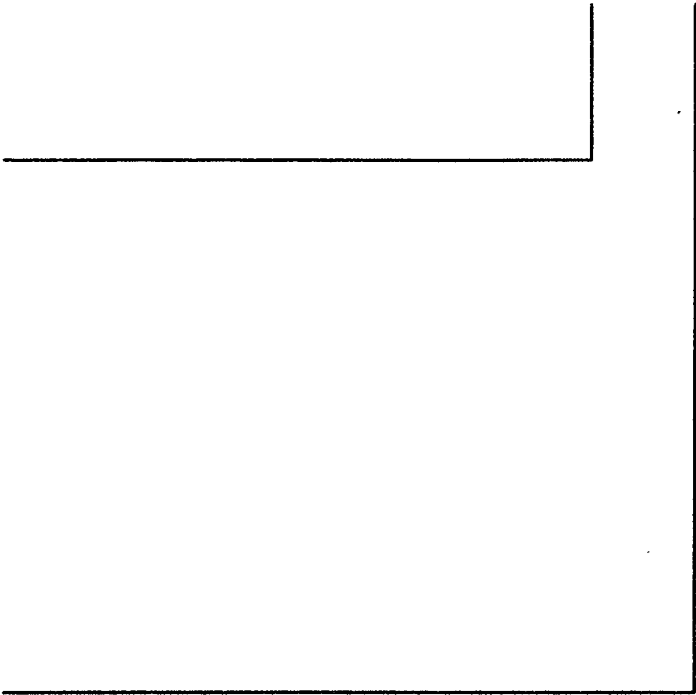


FIG.1/13

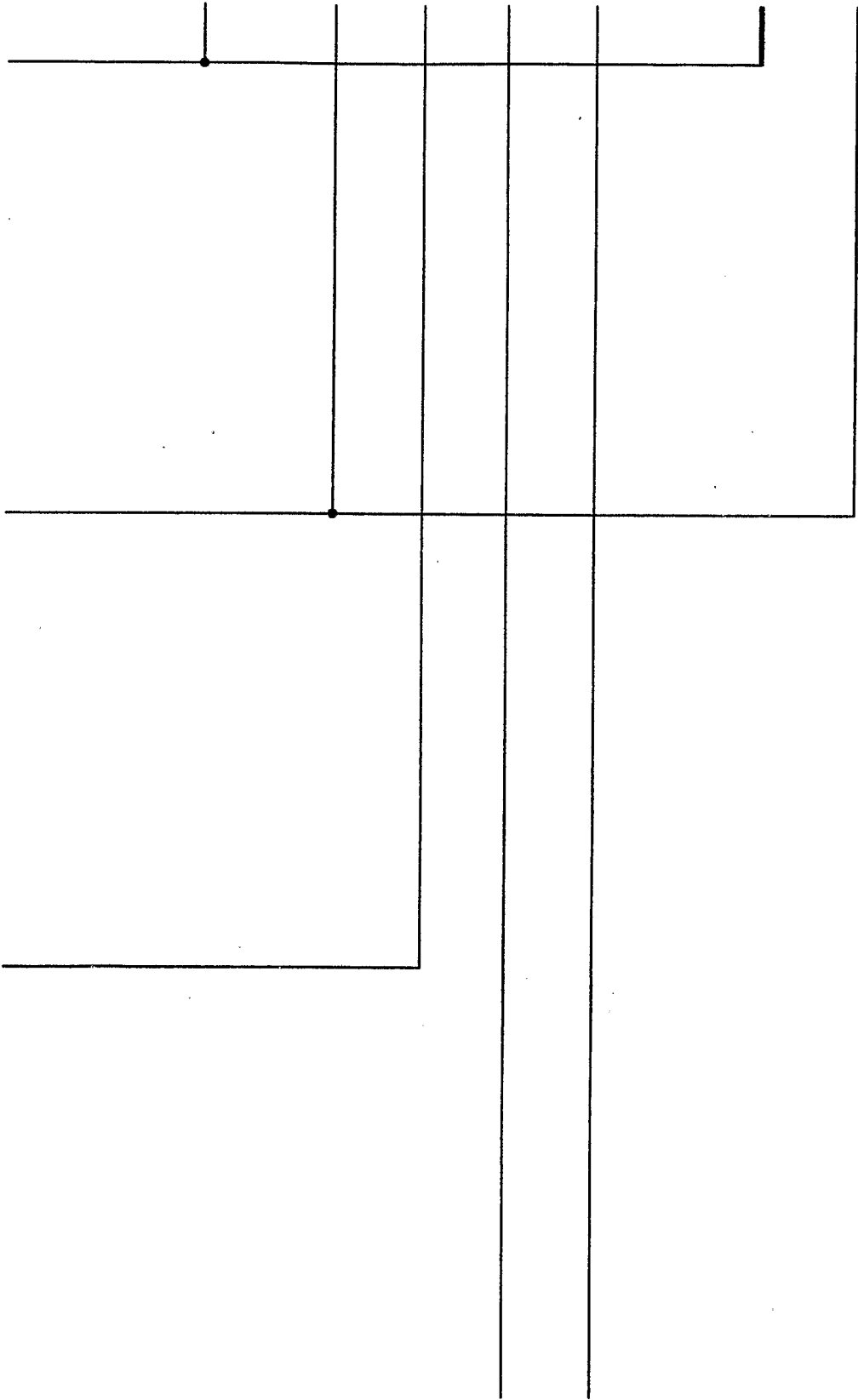


FIG.1/14

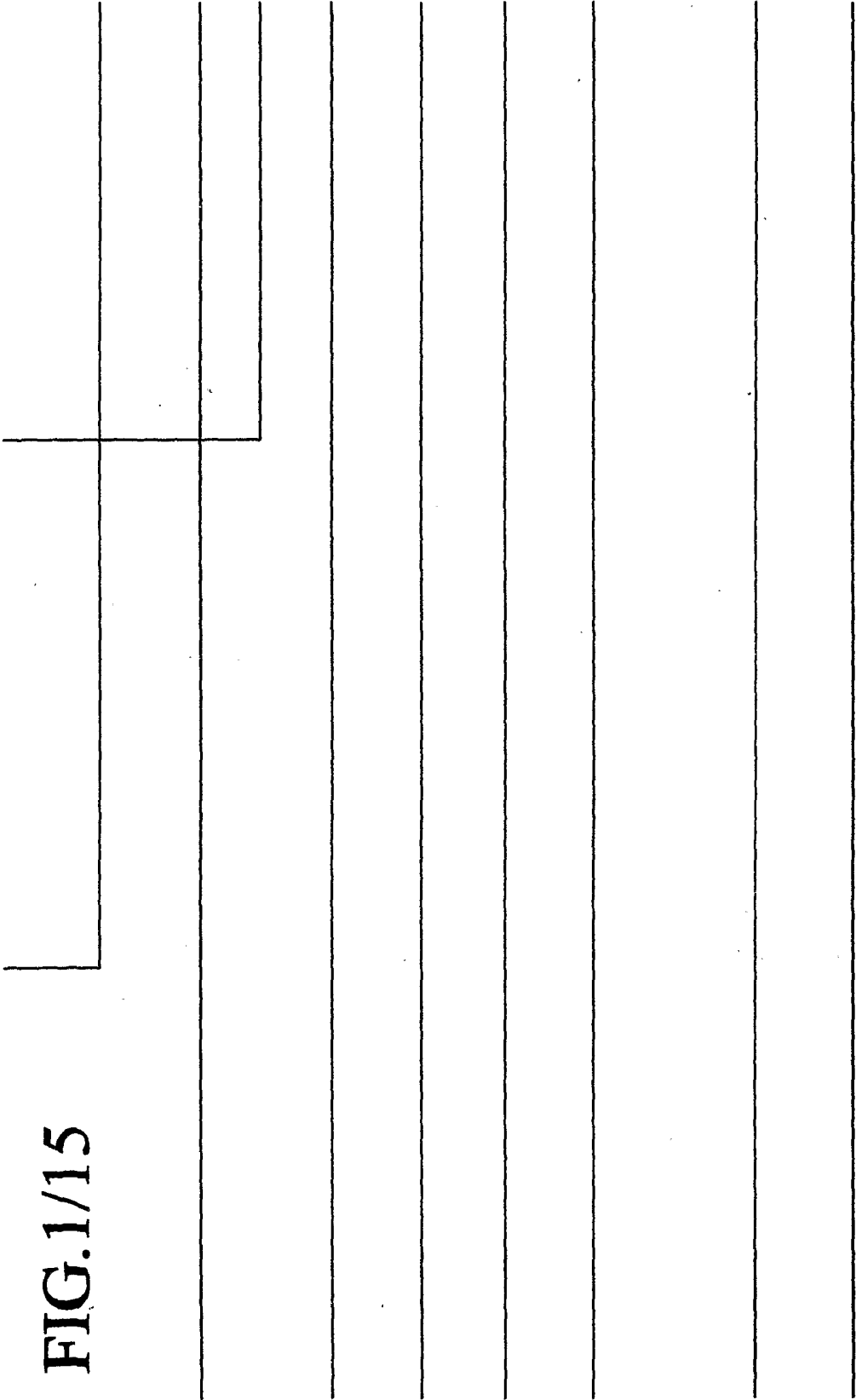
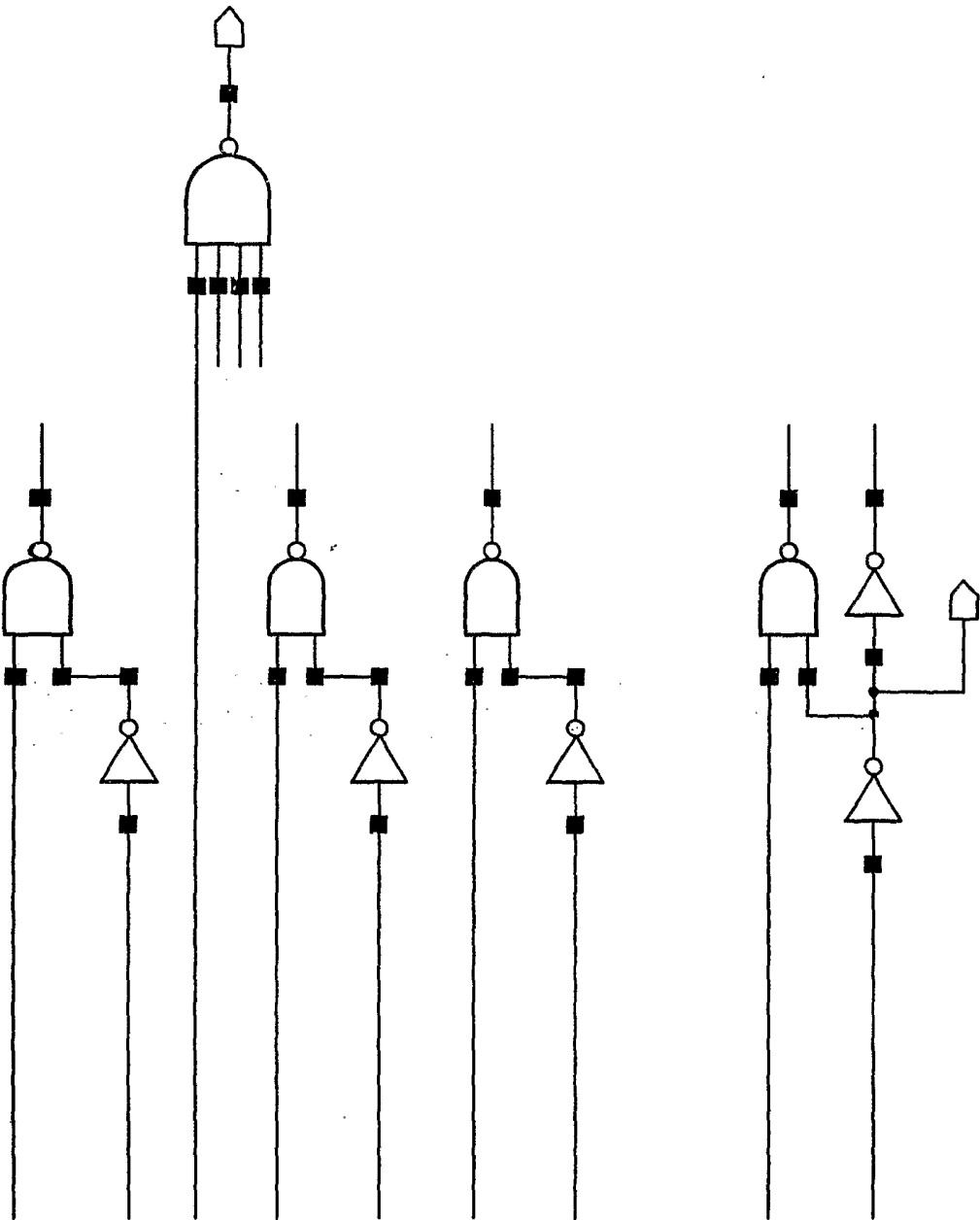


FIG.1/16



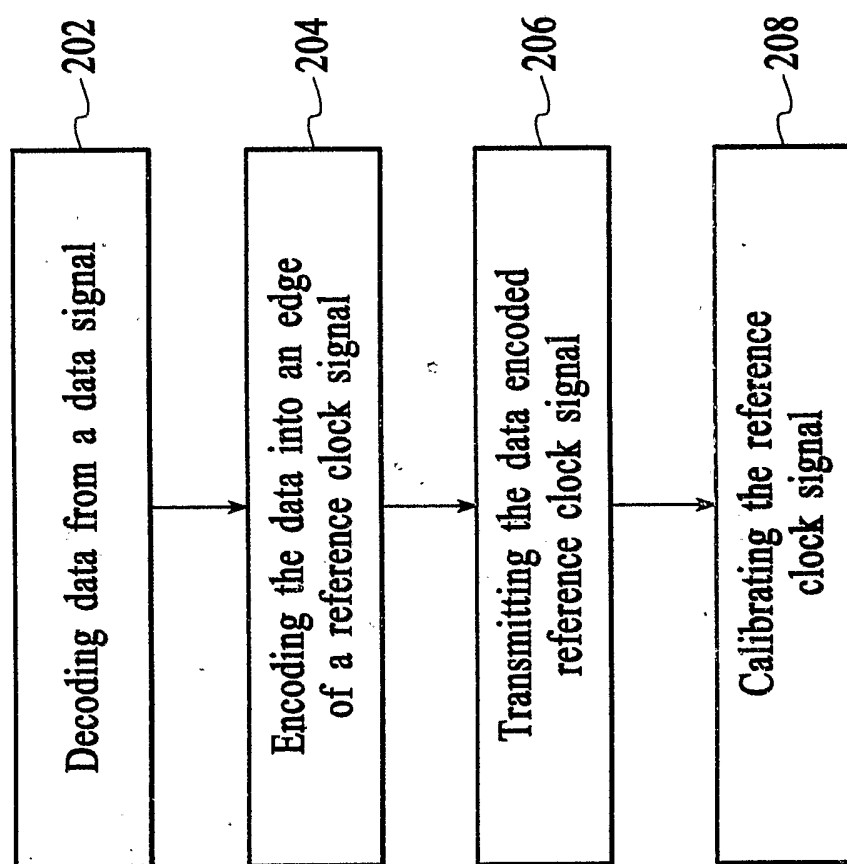


FIG. 2

FIG.3/1	FIG.3/2	FIG.3/3	FIG.3/4	FIG.3/5	FIG.3/6	FIG.3/7
FIG.3/8	FIG.3/9	FIG.3/10	FIG.3/11	FIG.3/12	FIG.3/13	FIG.3/14
FIG.3/15					FIG.3/16	FIG.3/17

FIG.3

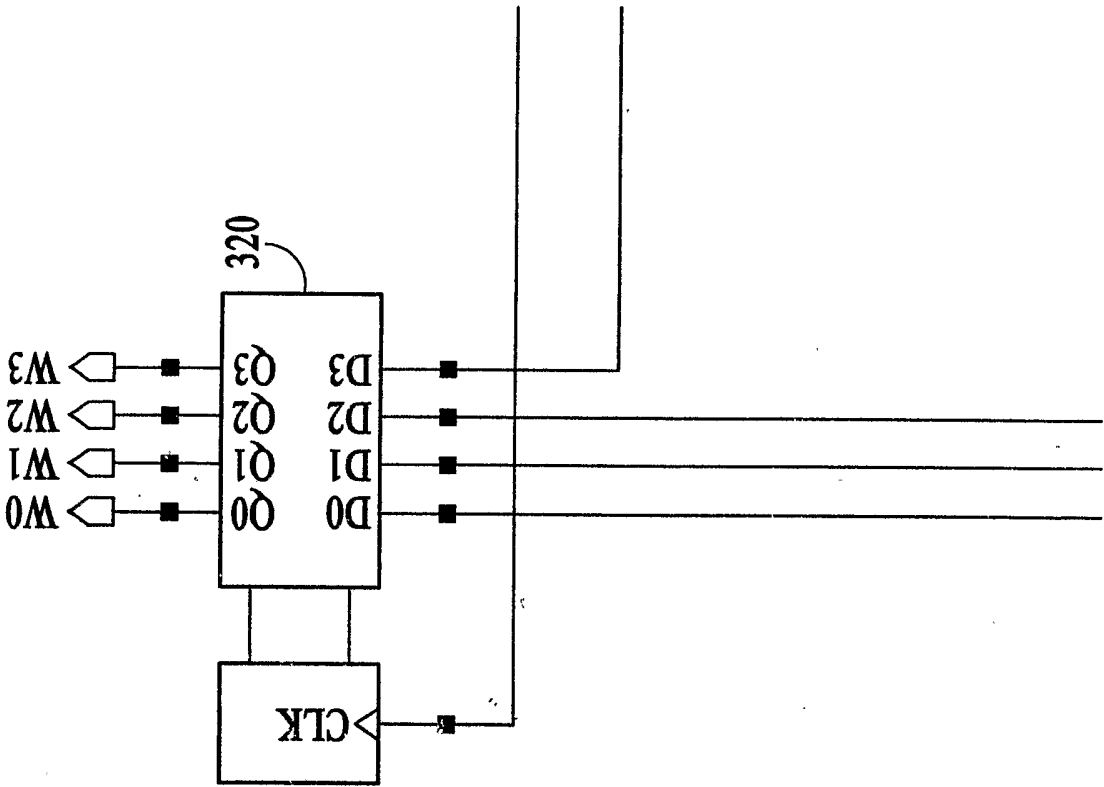


FIG.3/1

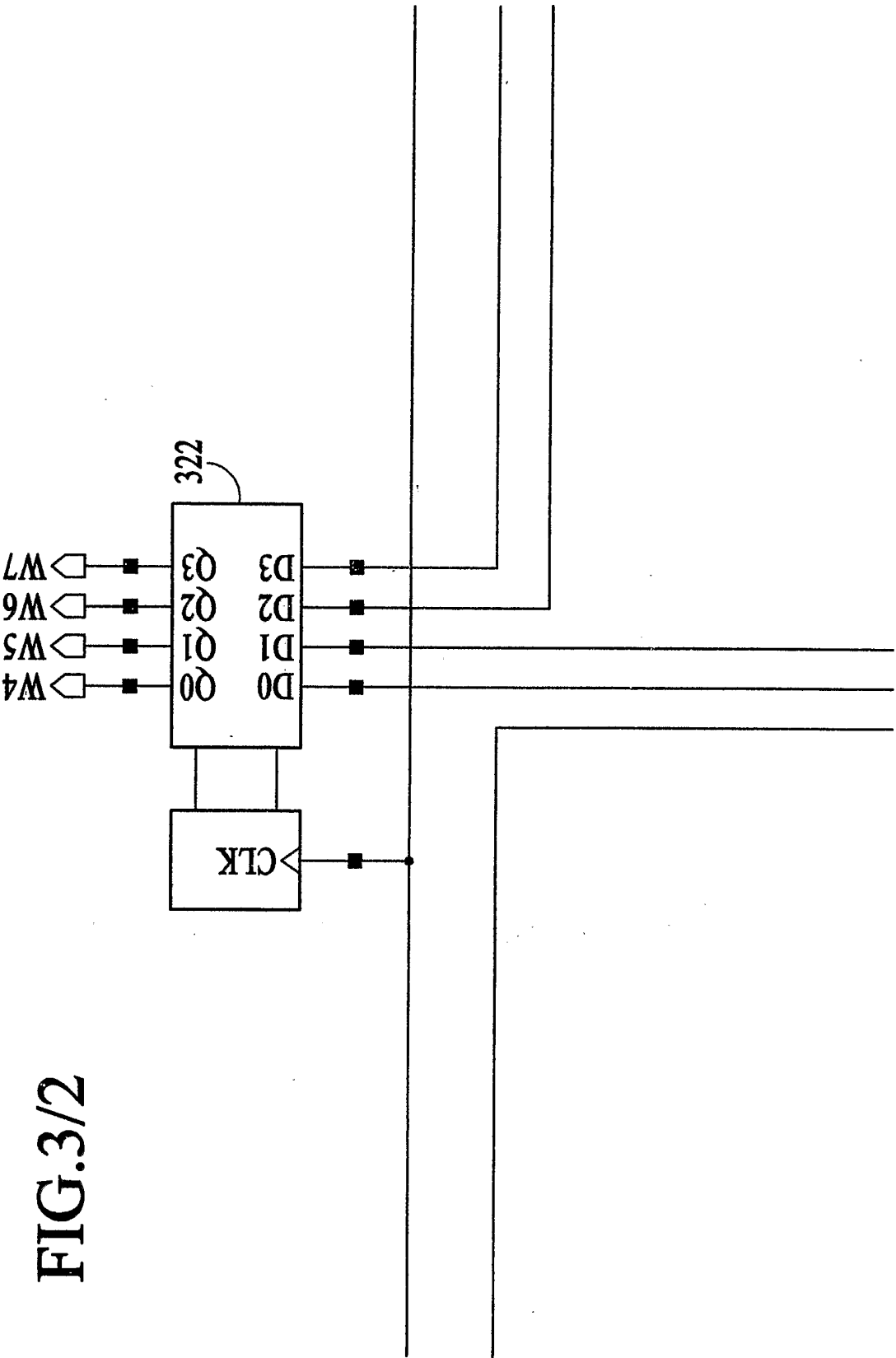


FIG. 3/2

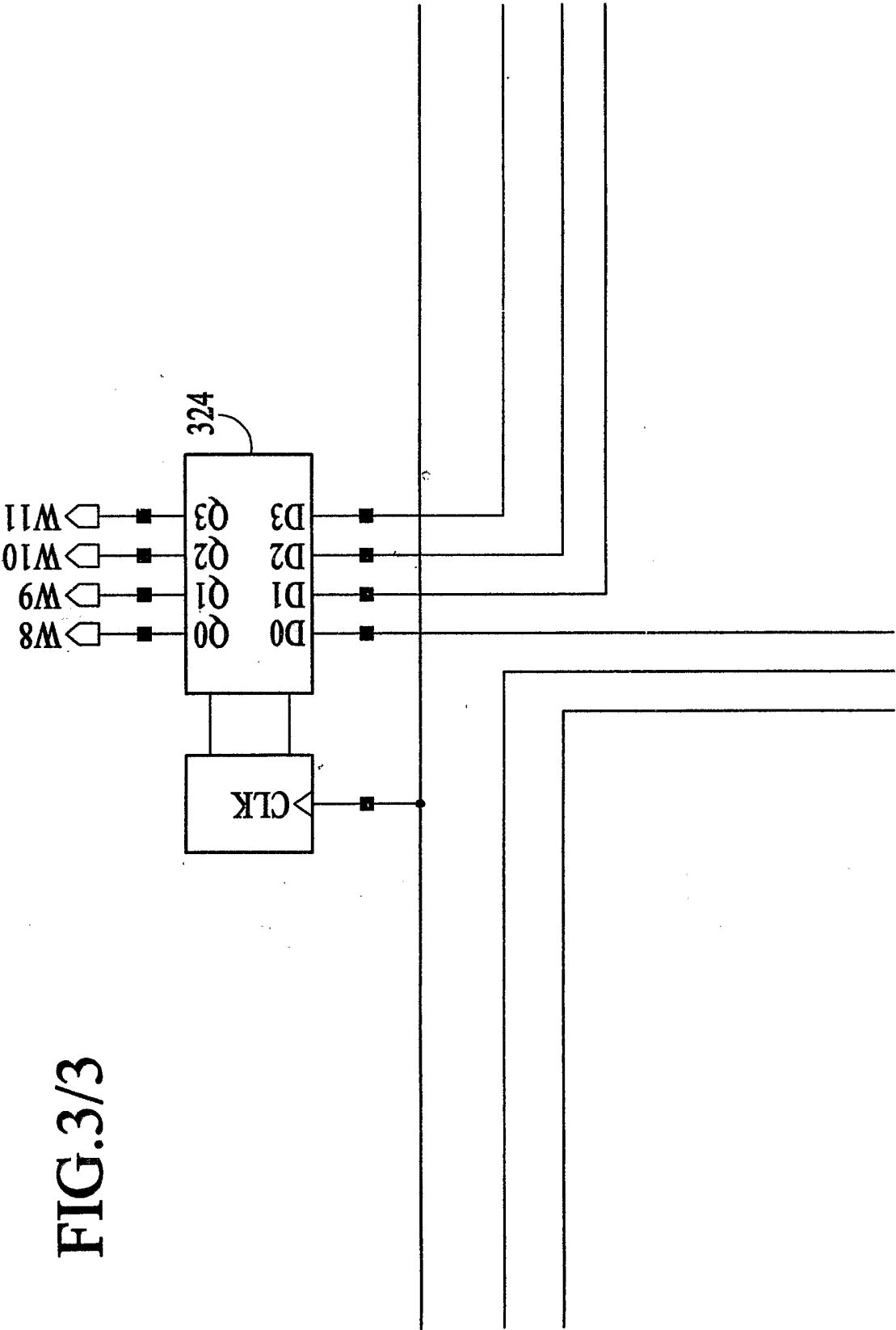


FIG. 3/3

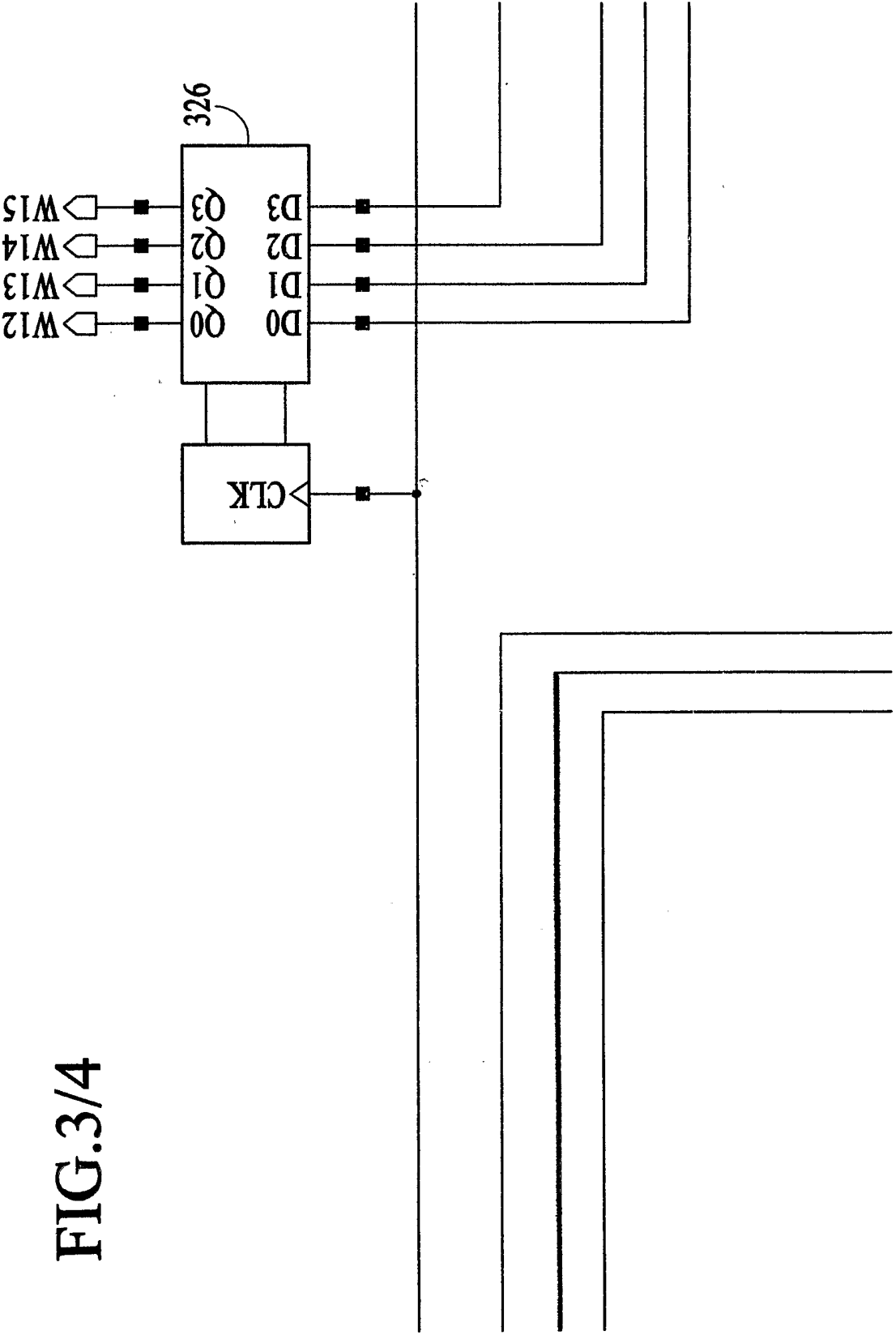


FIG. 3/4

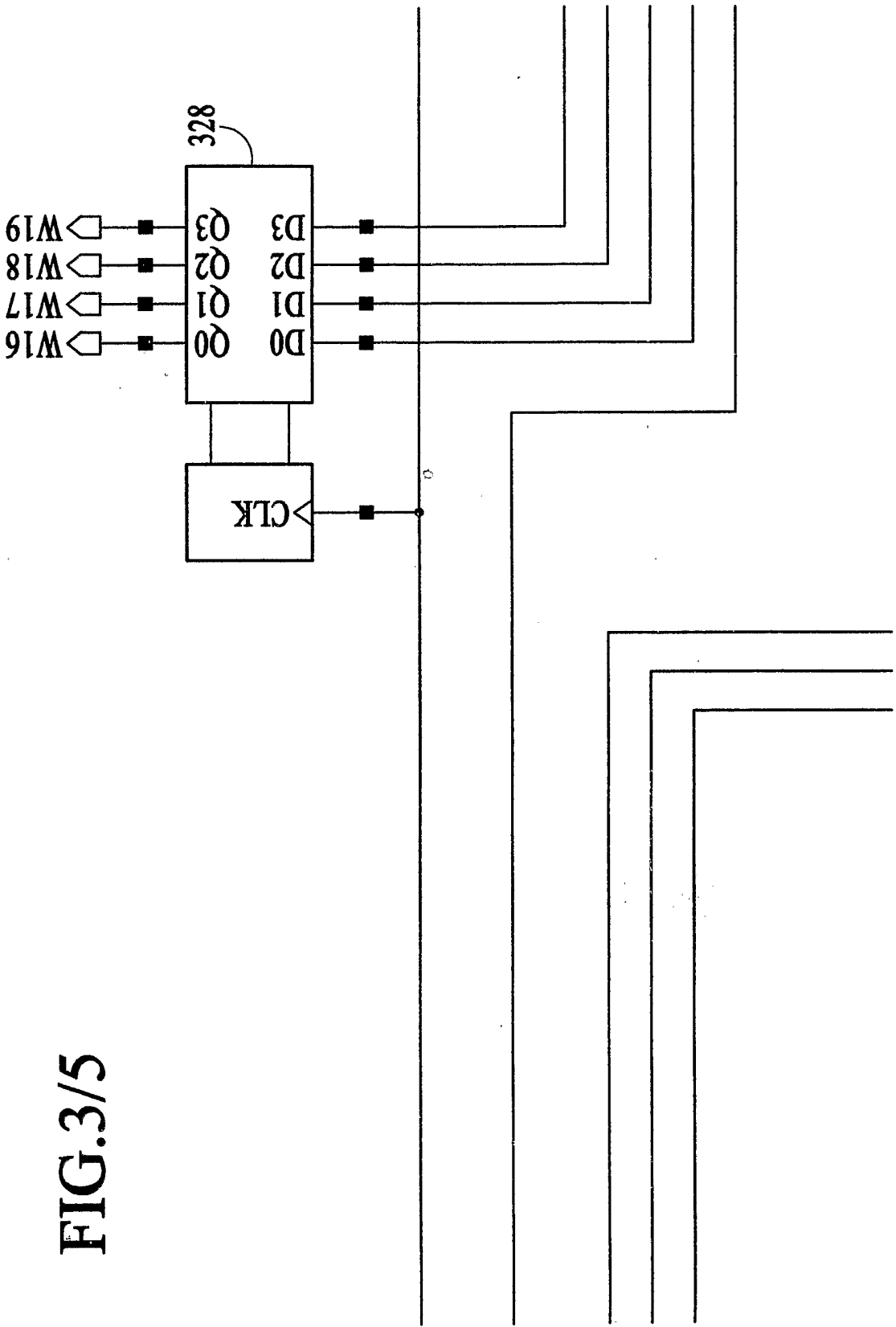


FIG.3/5

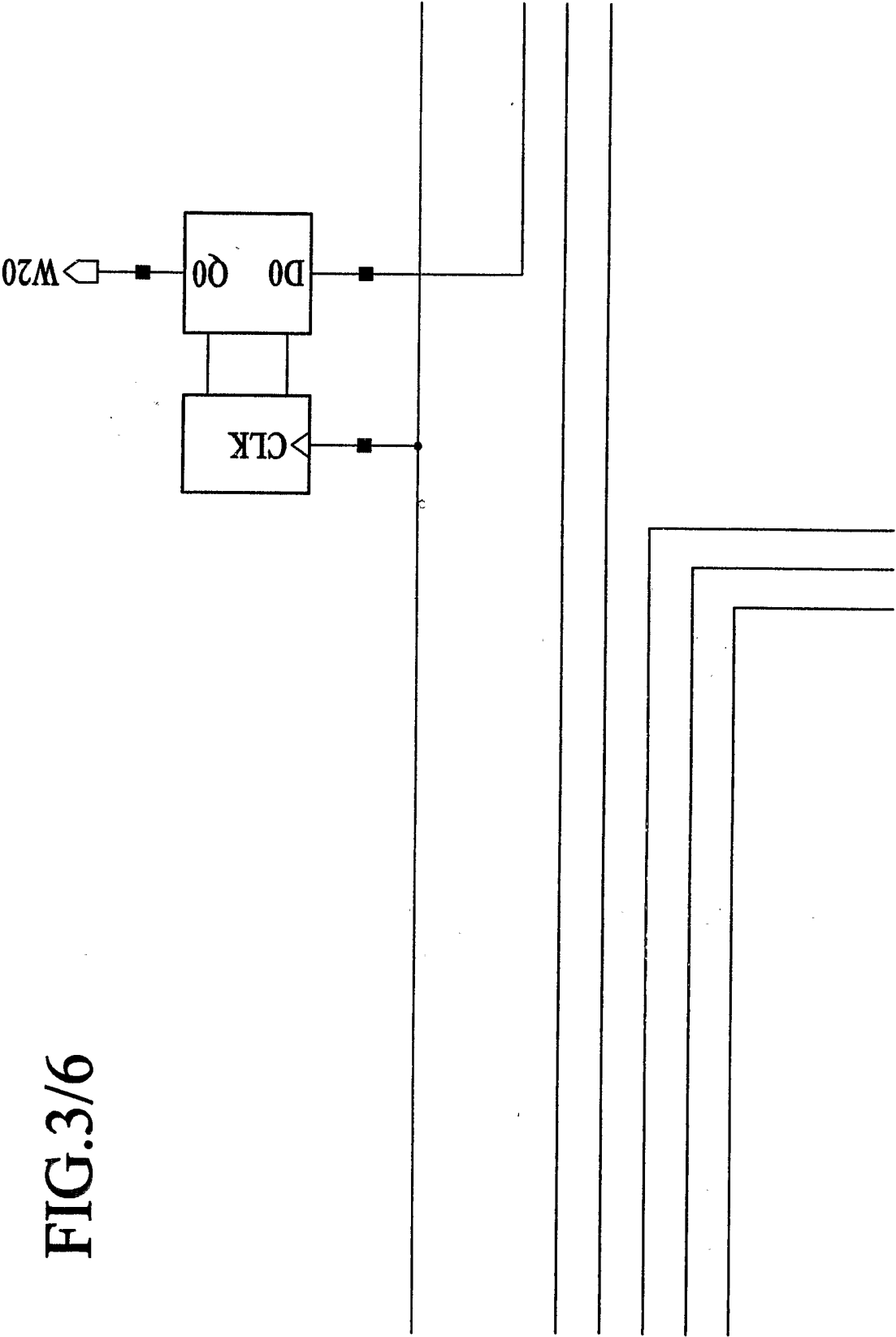
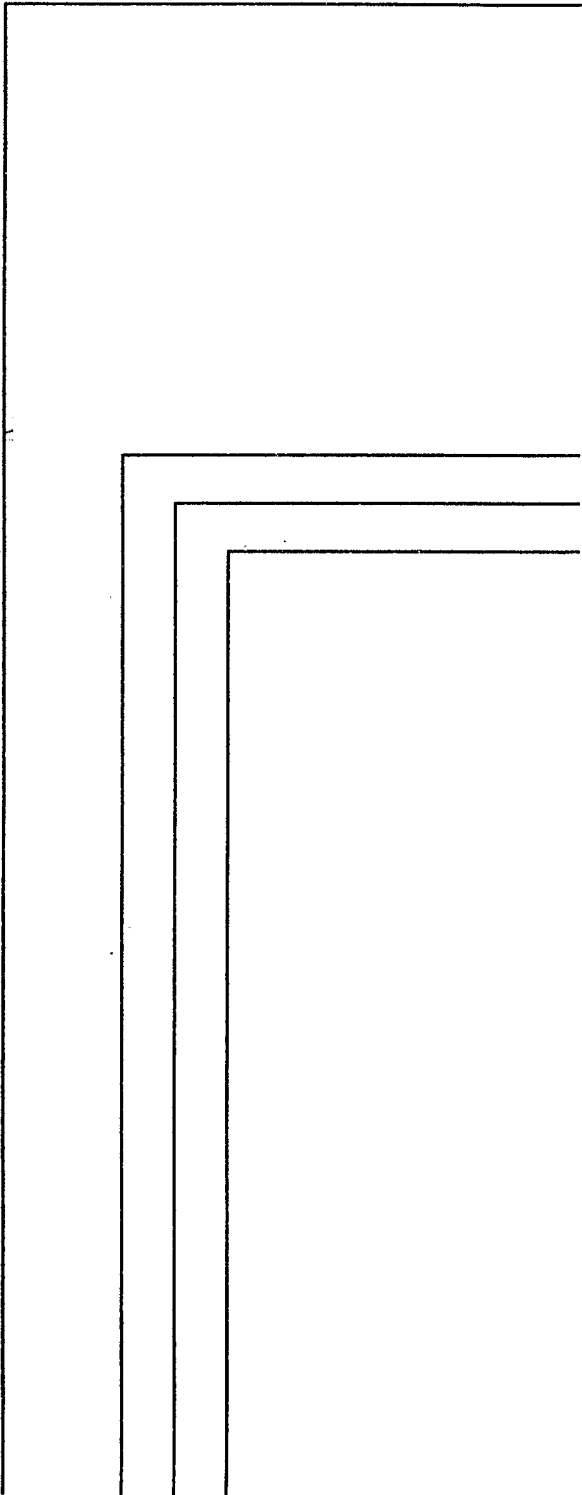
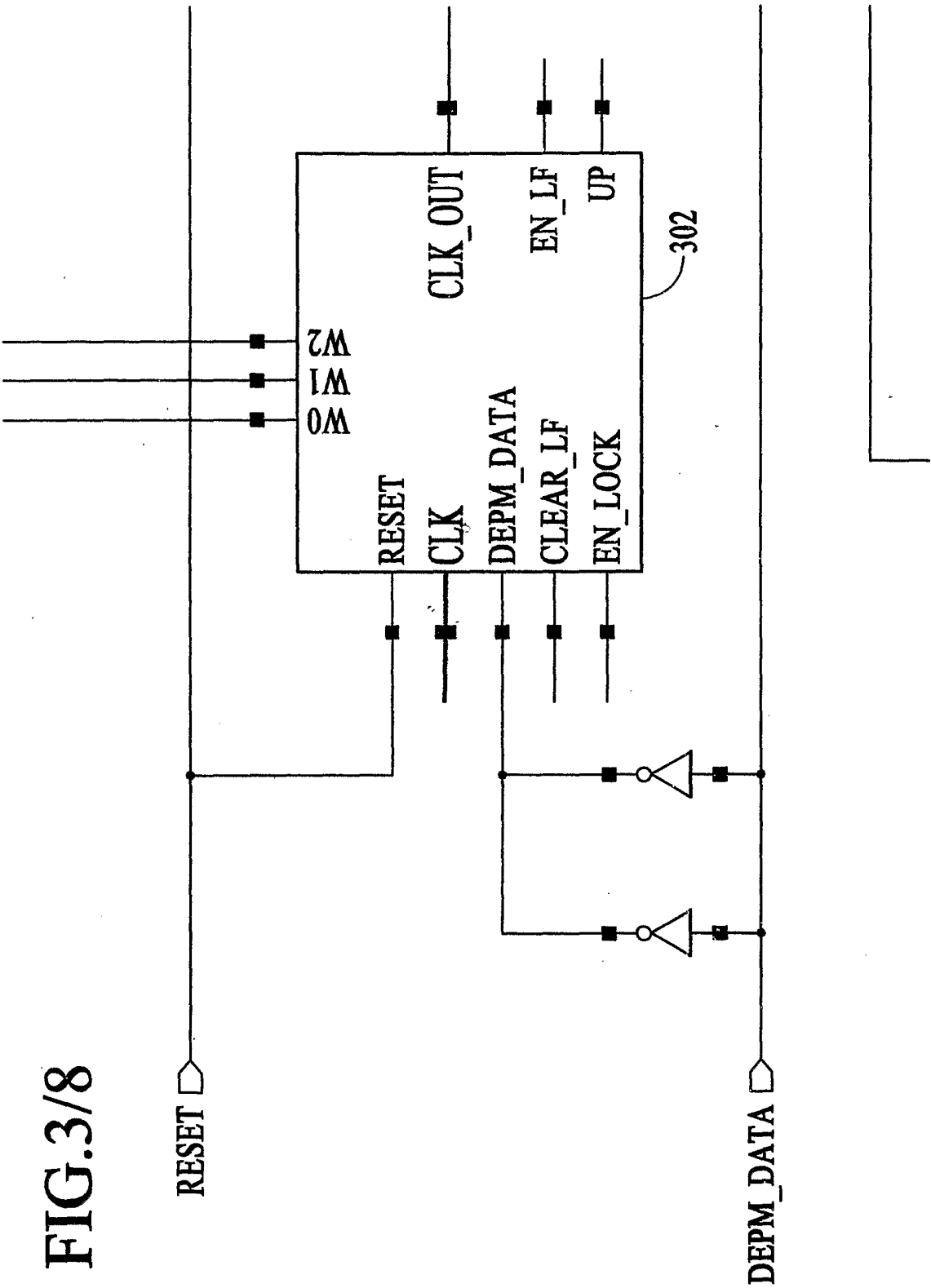


FIG. 3/6

FIG.3/7





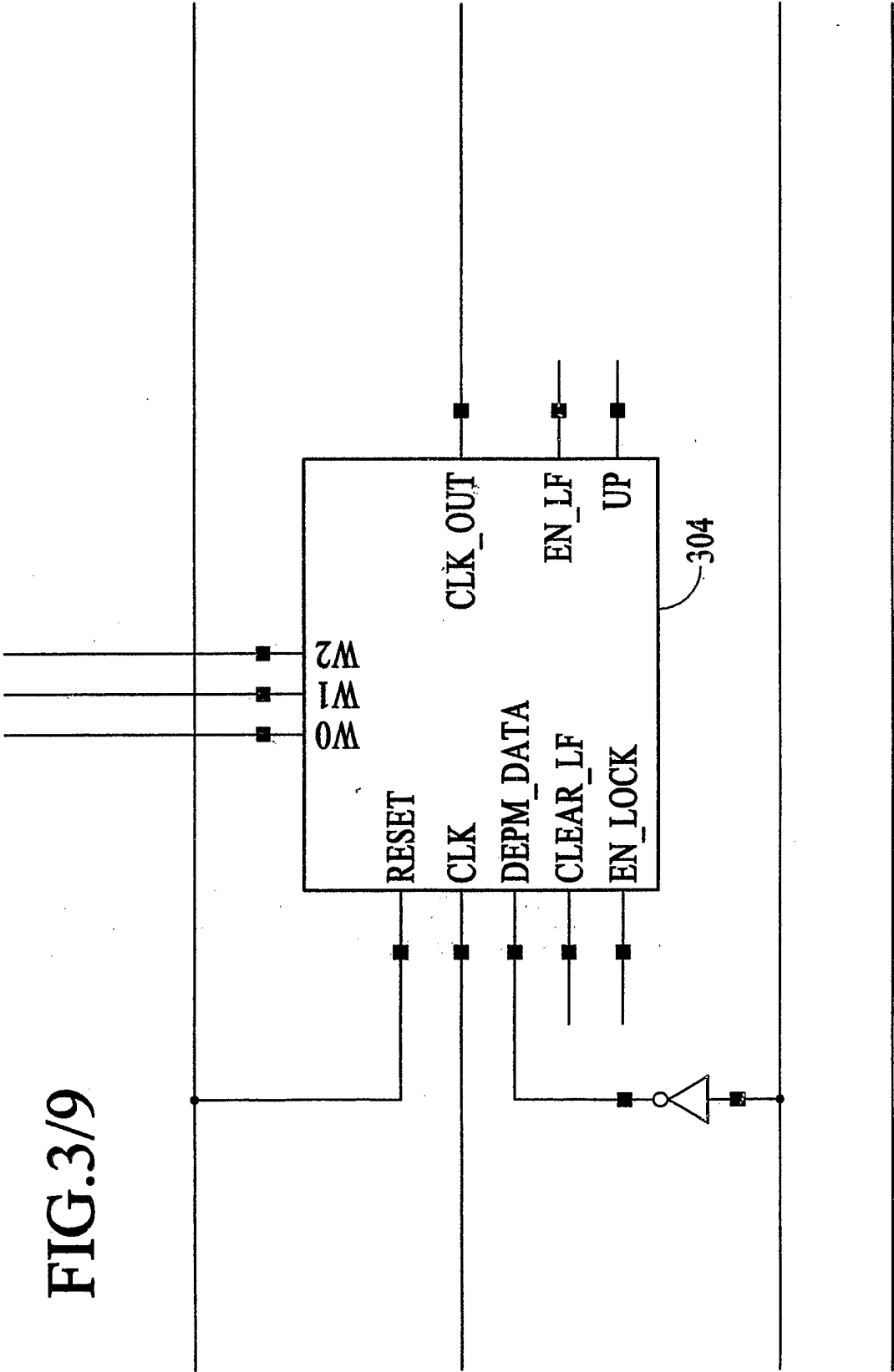


FIG.3/10

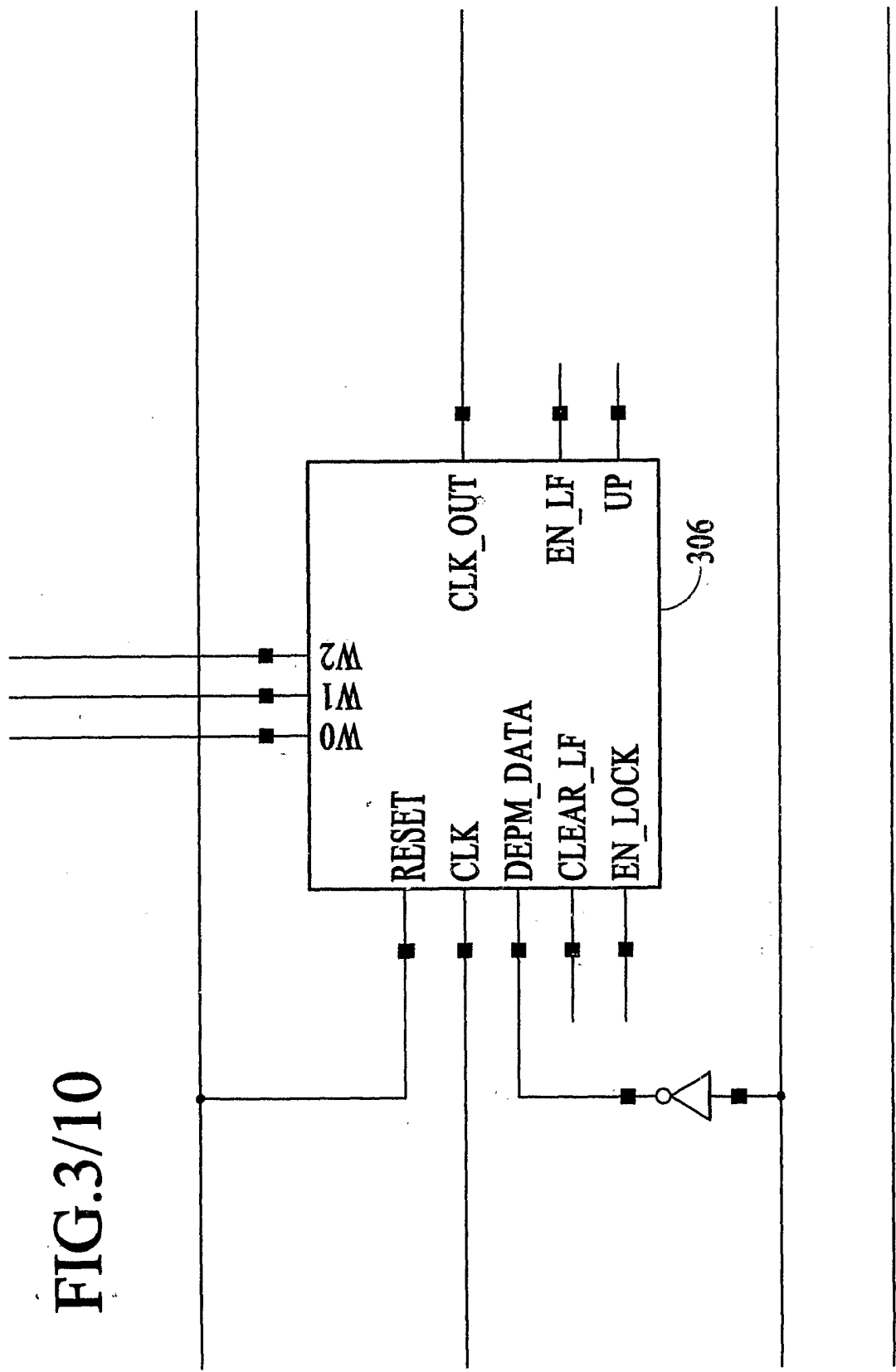


FIG.3/11

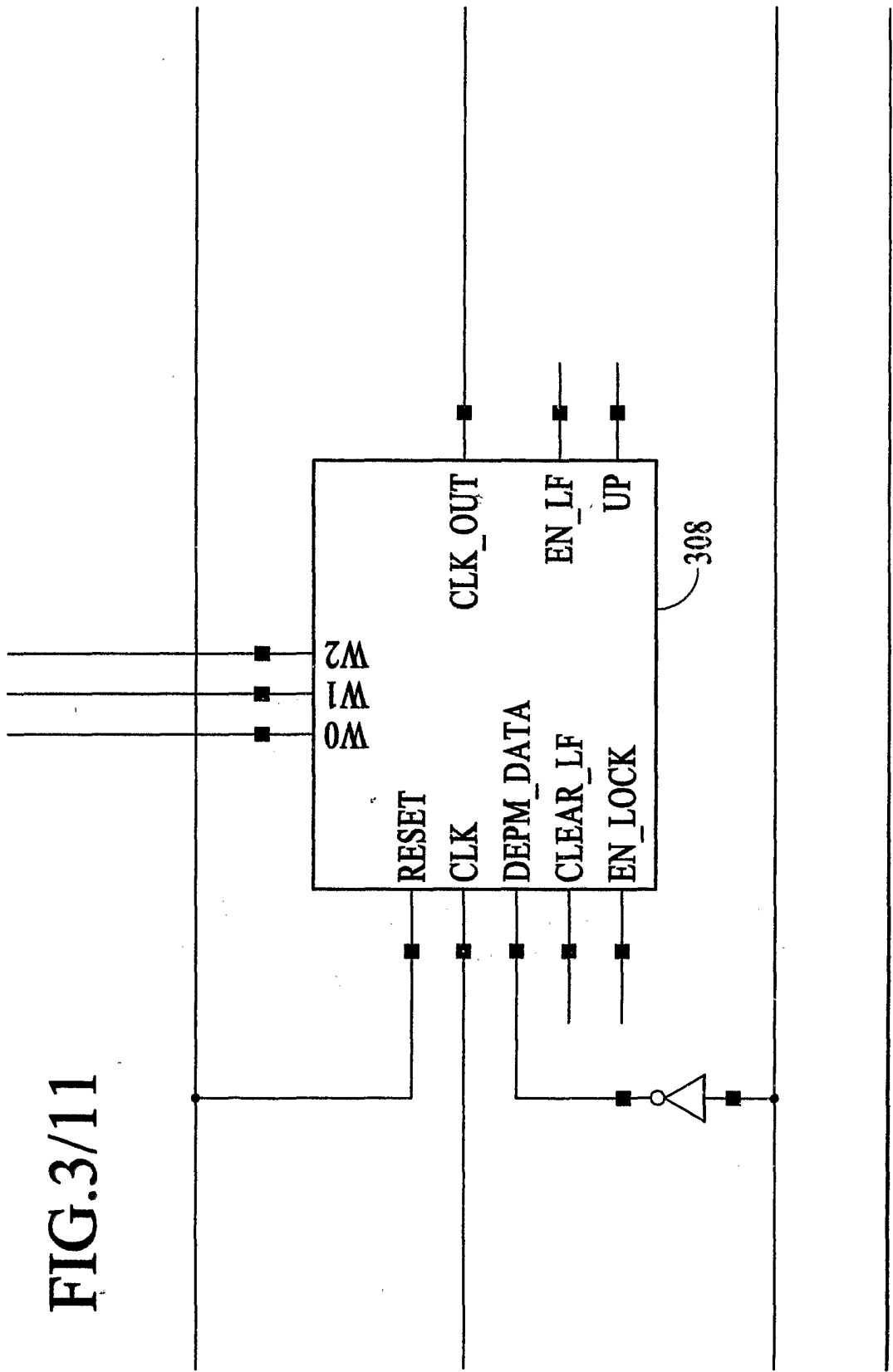
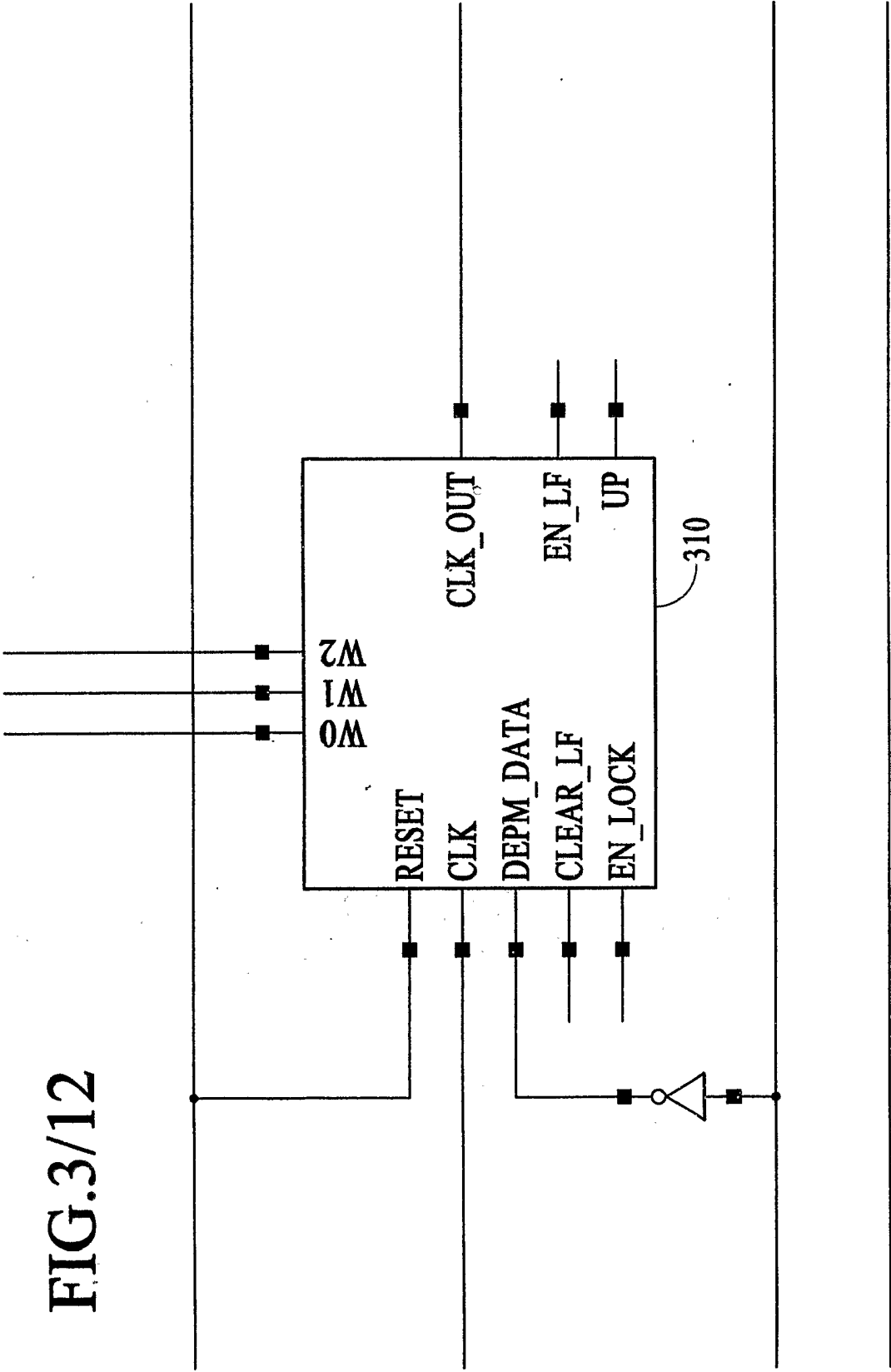
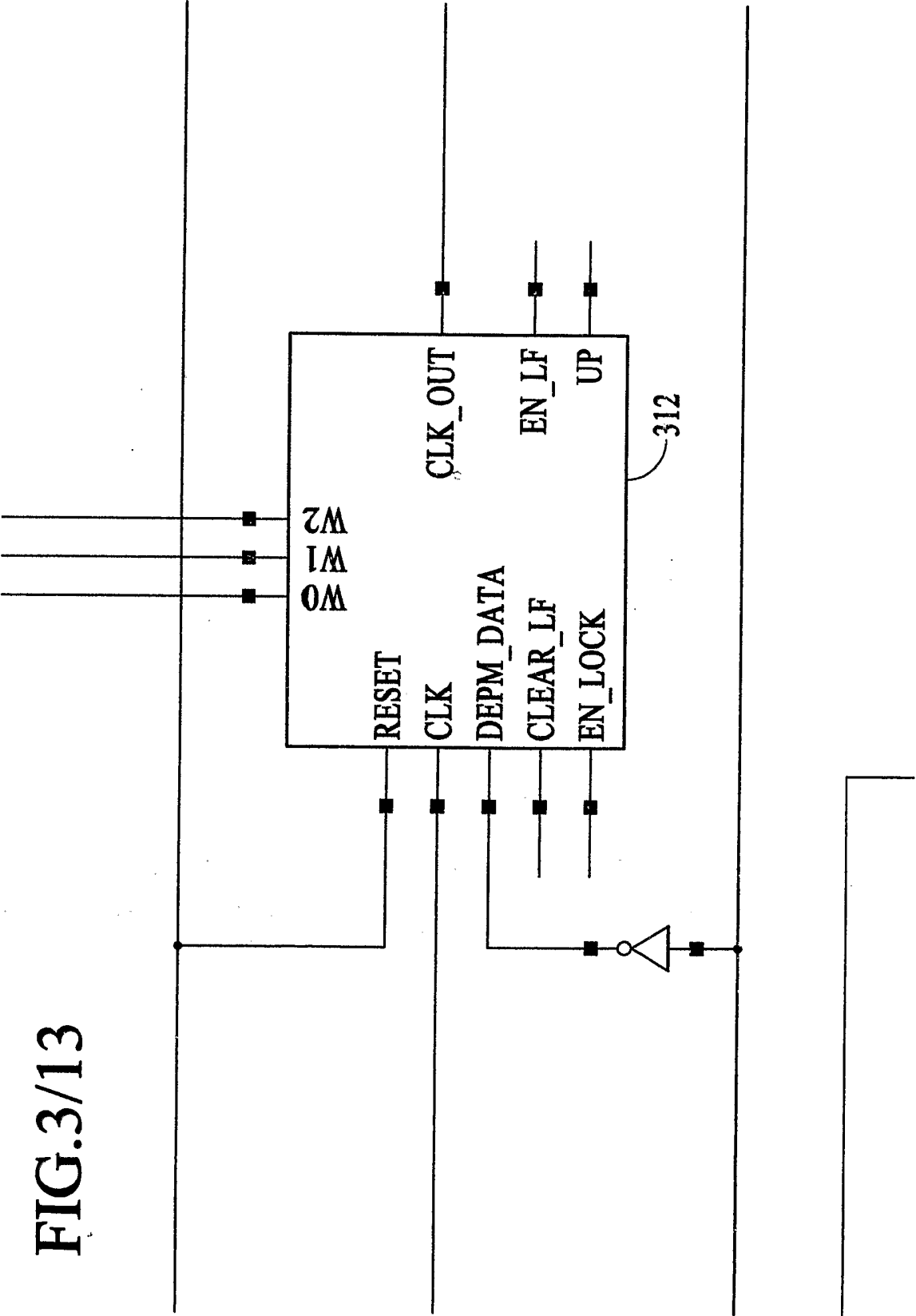


FIG.3/12





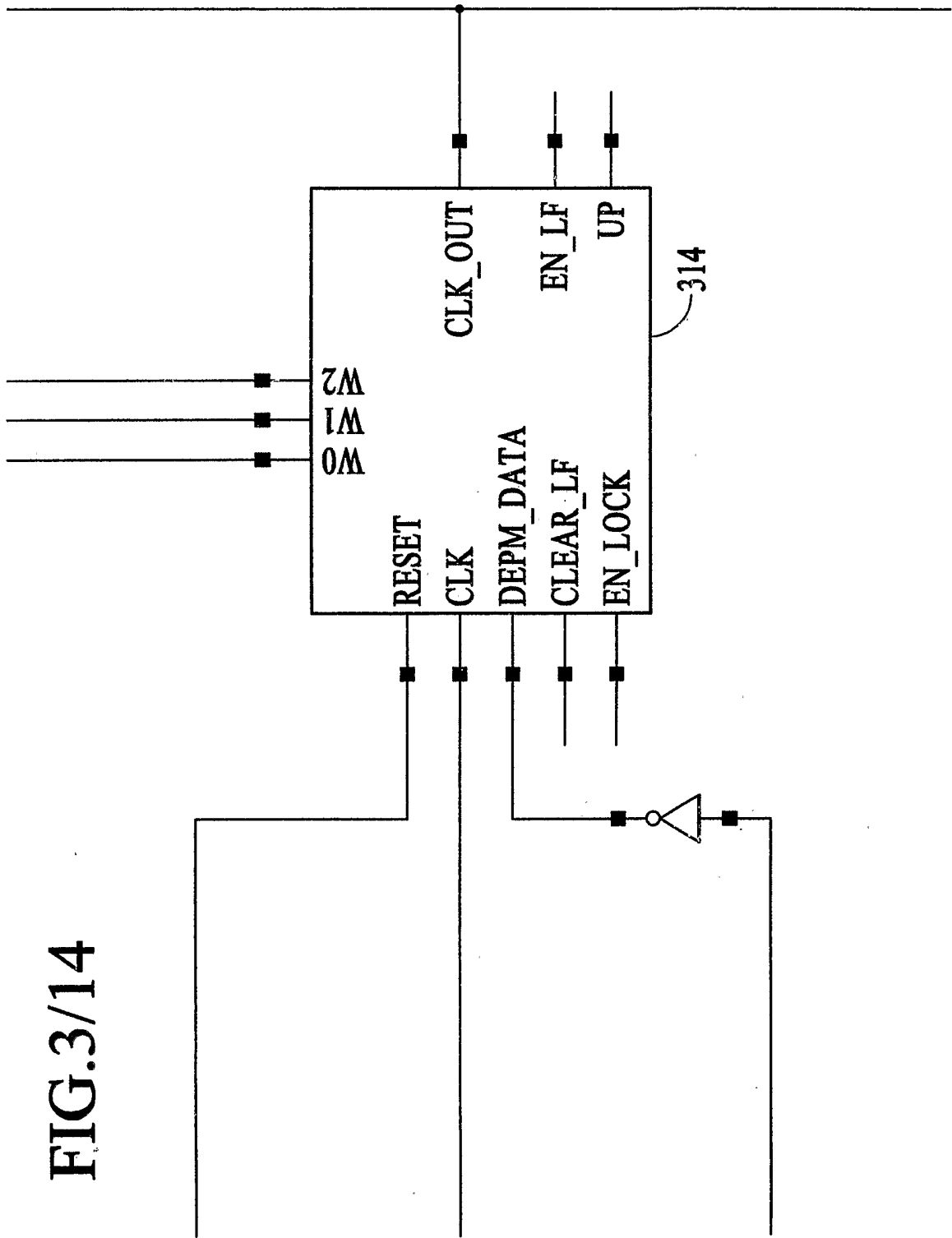


FIG.3/14

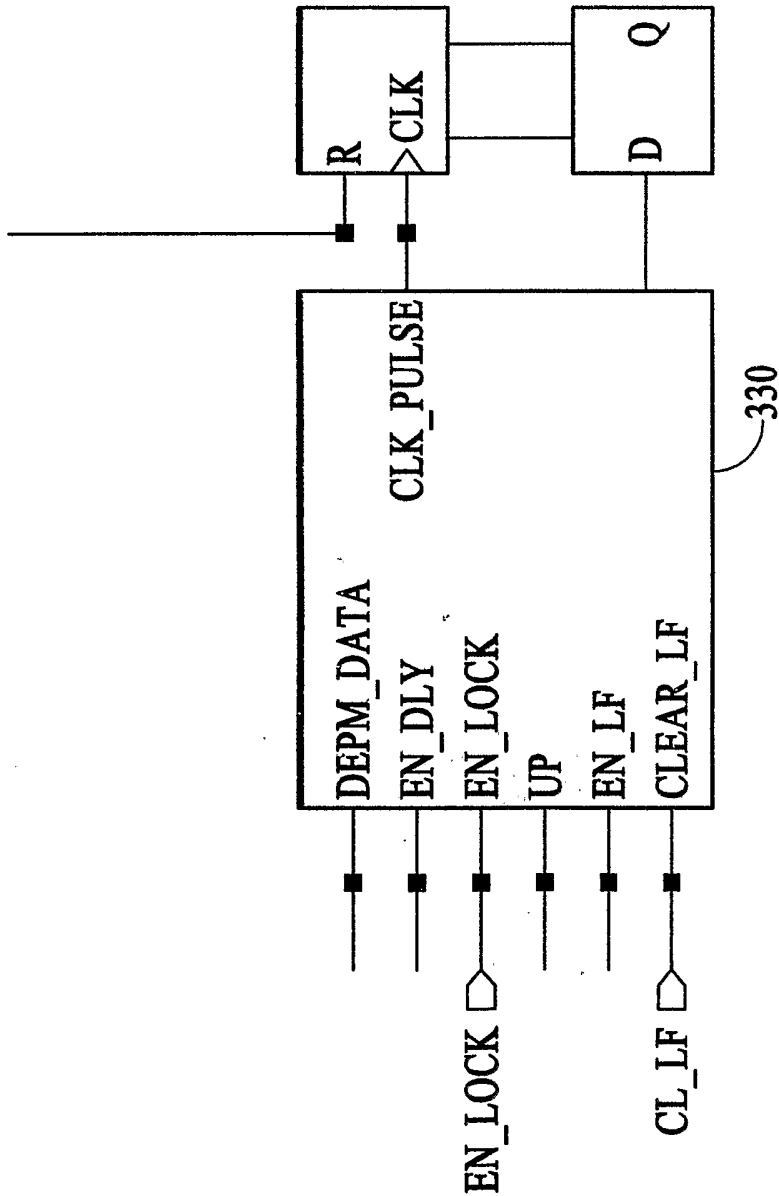


FIG.3/15

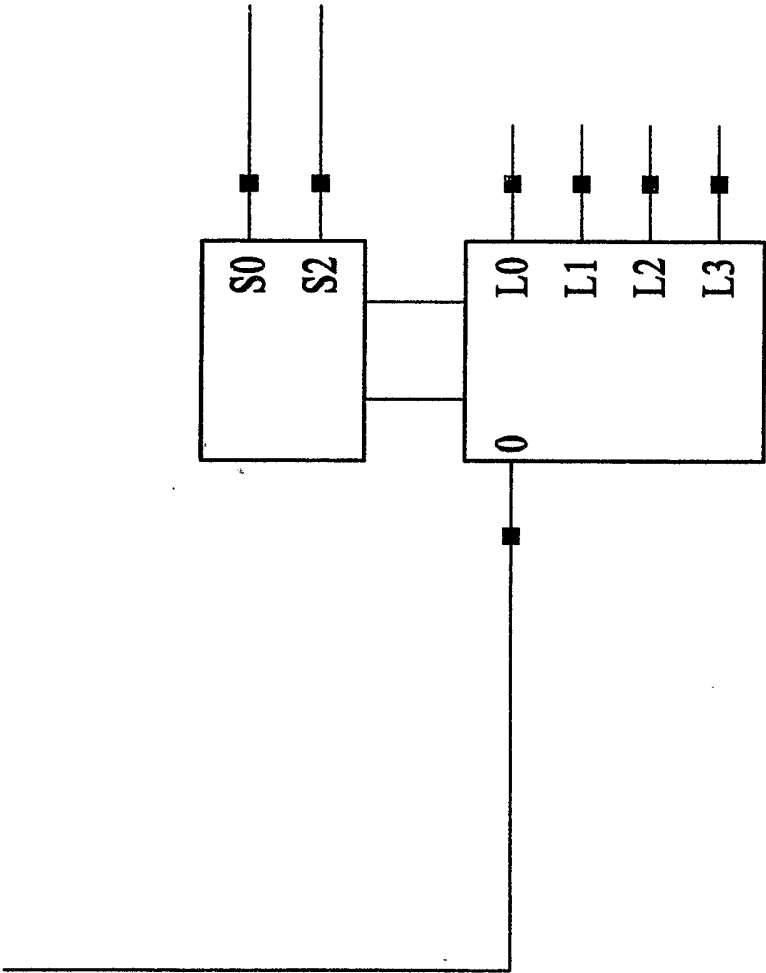


FIG.3/16

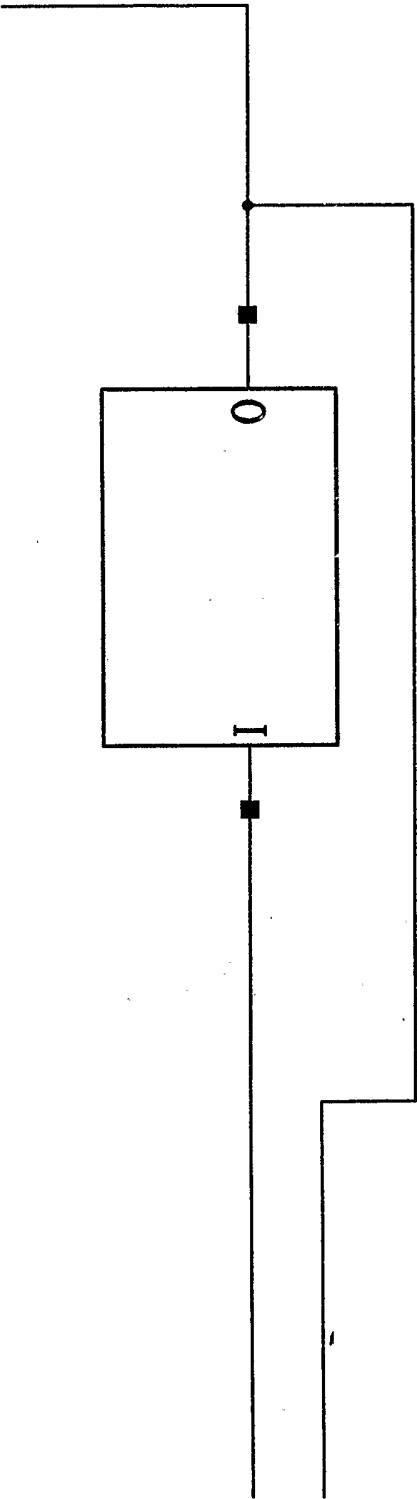


FIG.3/17

FIG.4/1	FIG.4/2	FIG.4/3	FIG.4/4	FIG.4/5		
	FIG.4/6	FIG.4/7	FIG.4/8	FIG.4/9	FIG.4/10	
	FIG.4/11	FIG.4/12	FIG.4/13	FIG.4/14	FIG.4/15	FIG.4/16

400

FIG.4

FIG.4/1

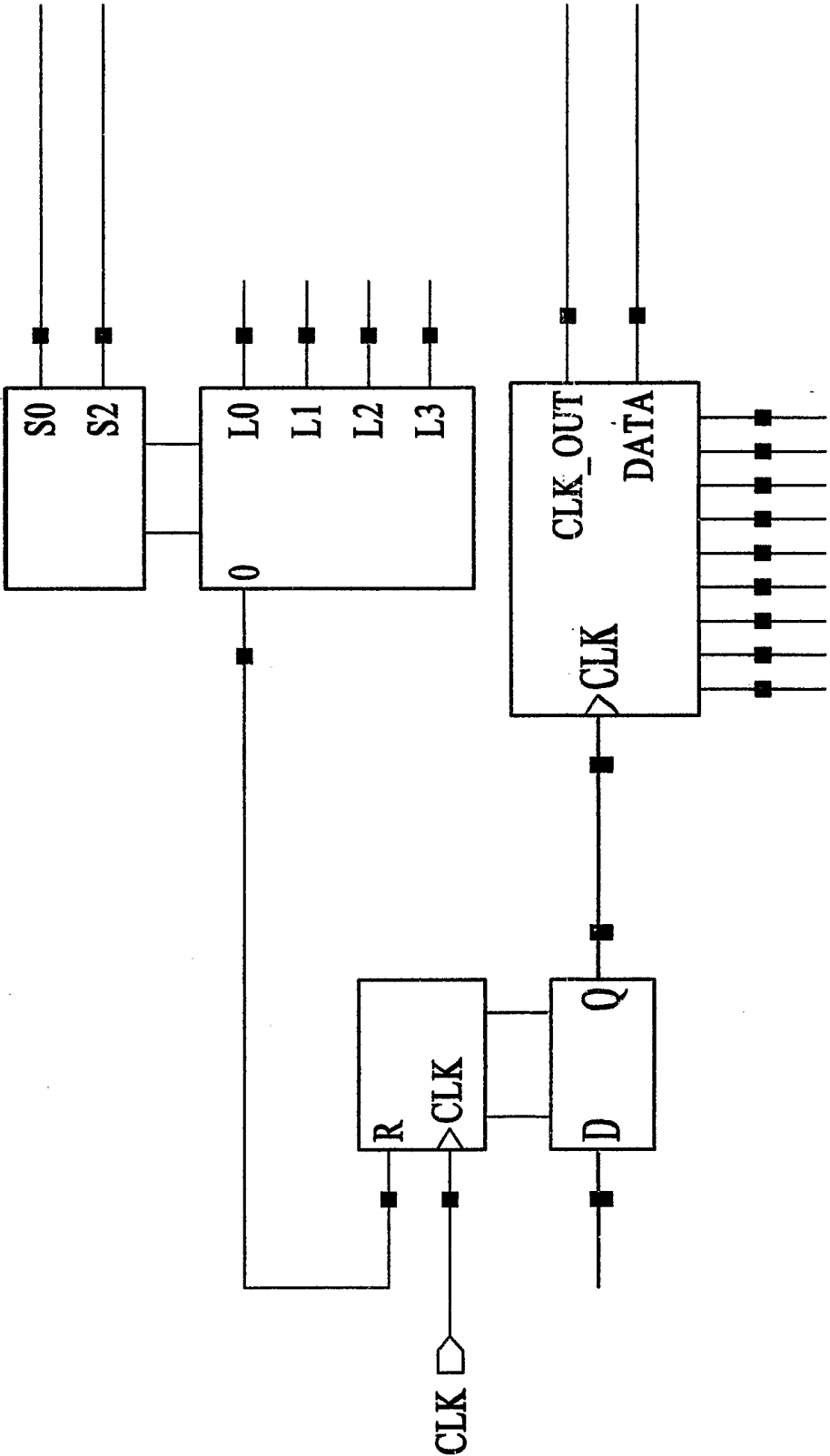


FIG. 4/2

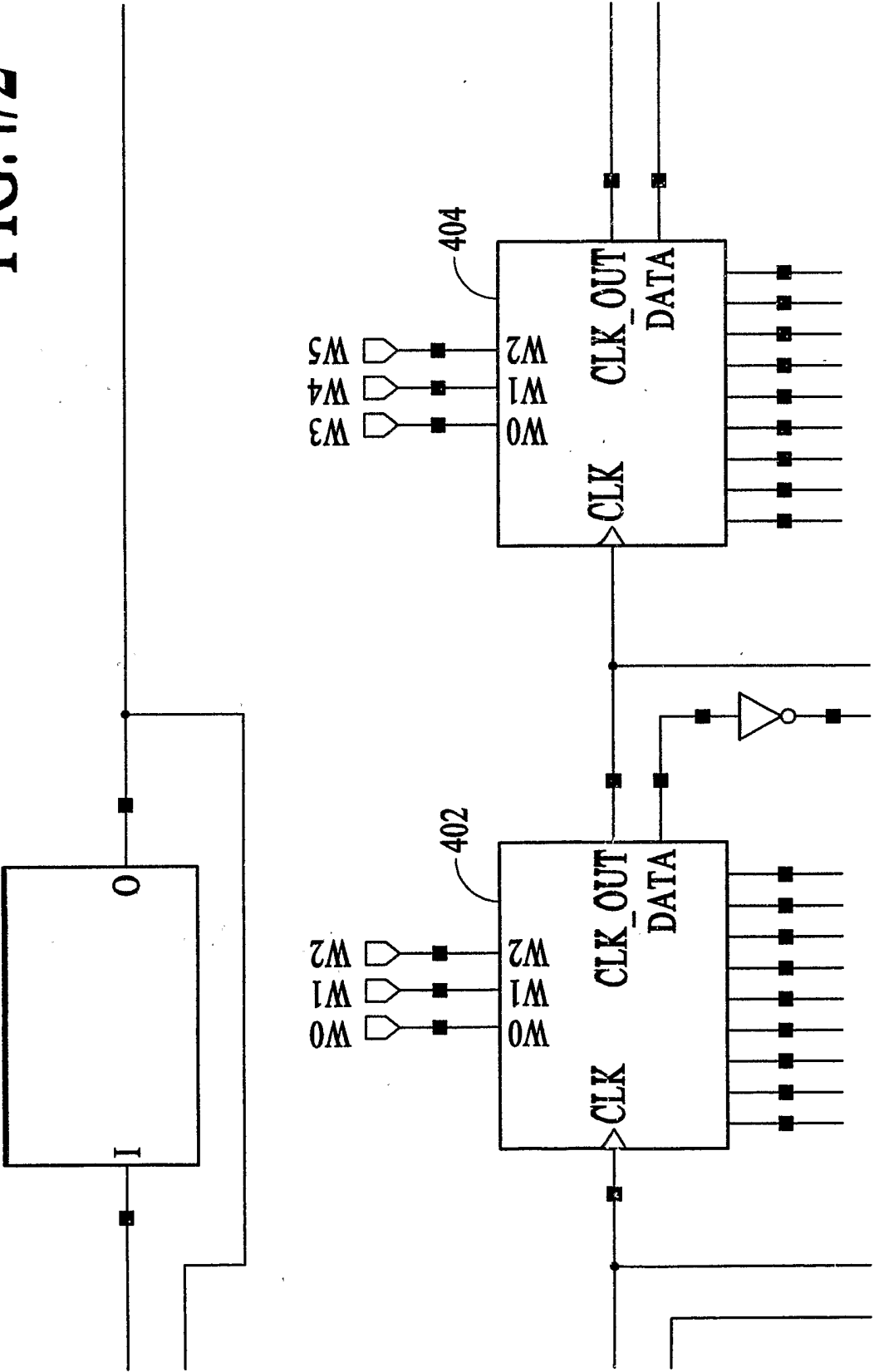


FIG.4/3

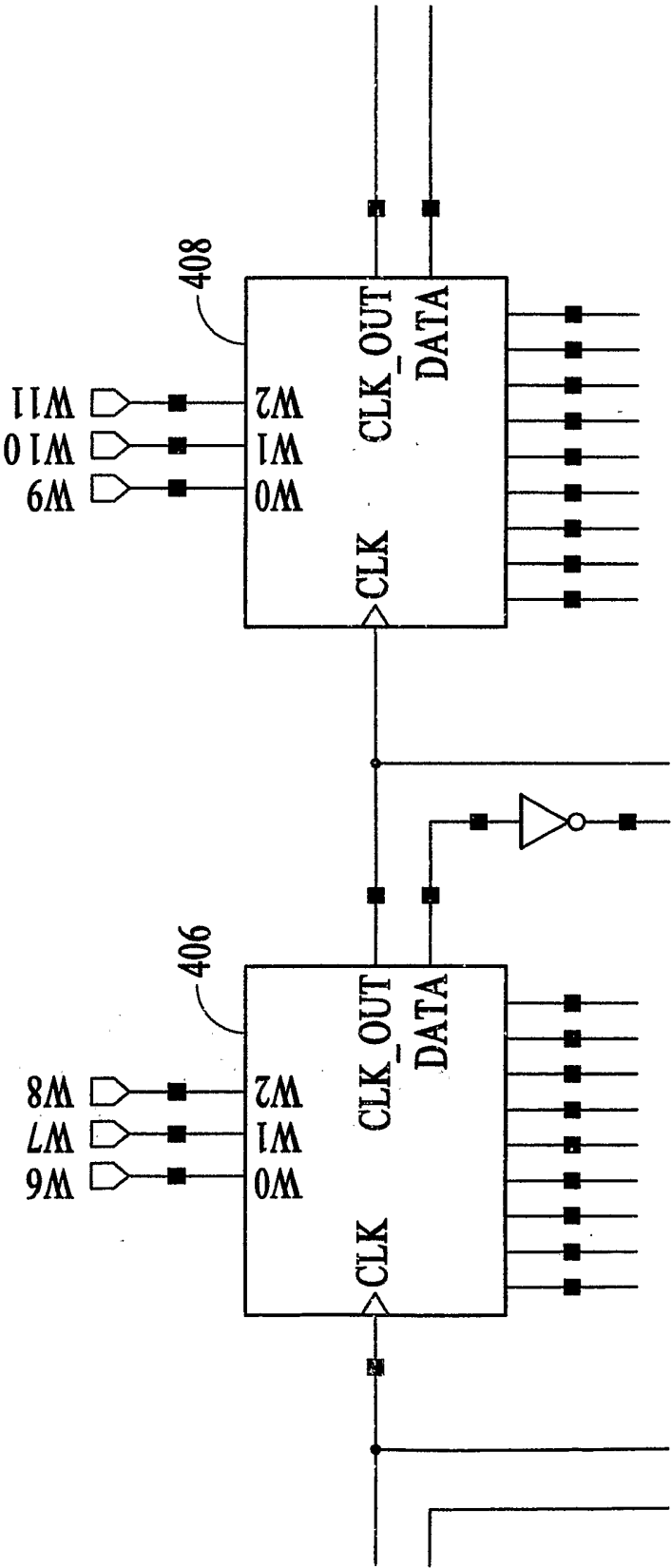


FIG. 4/4

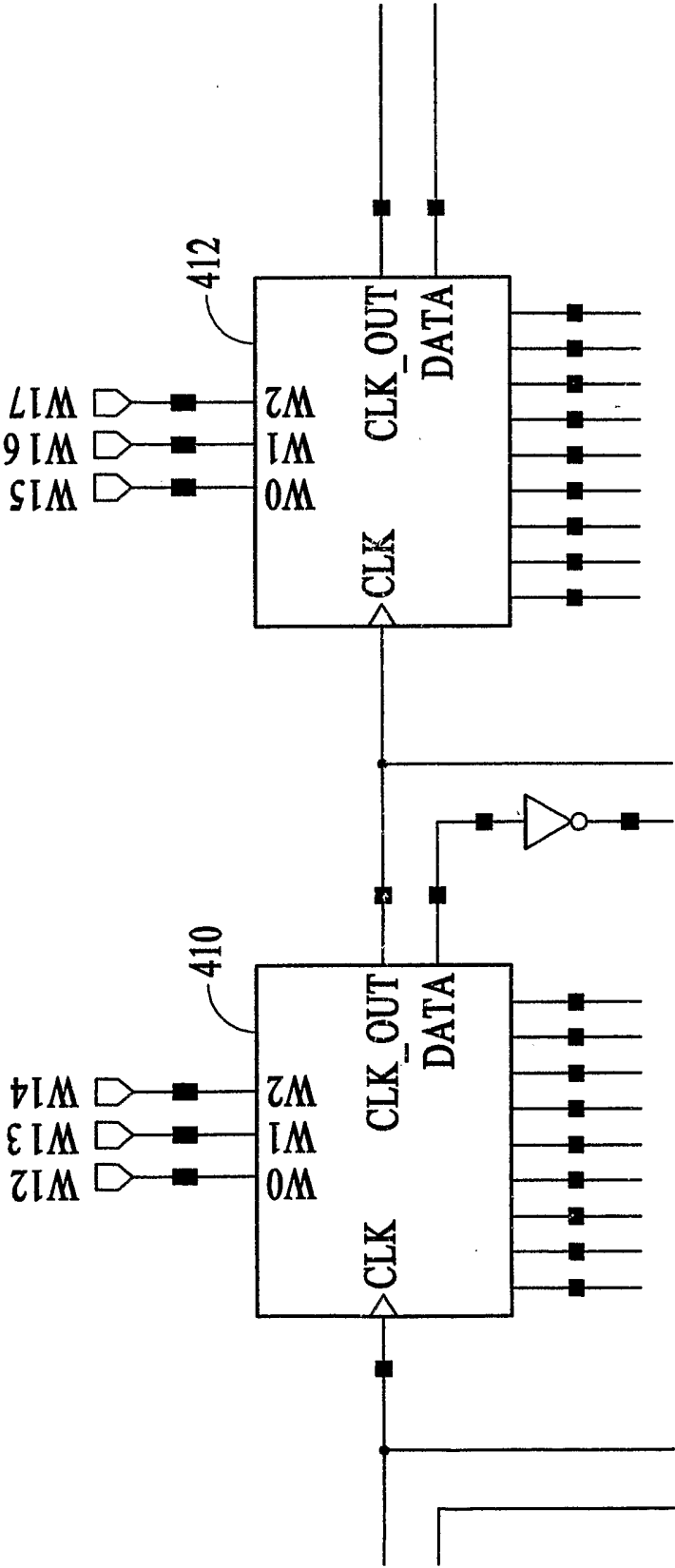
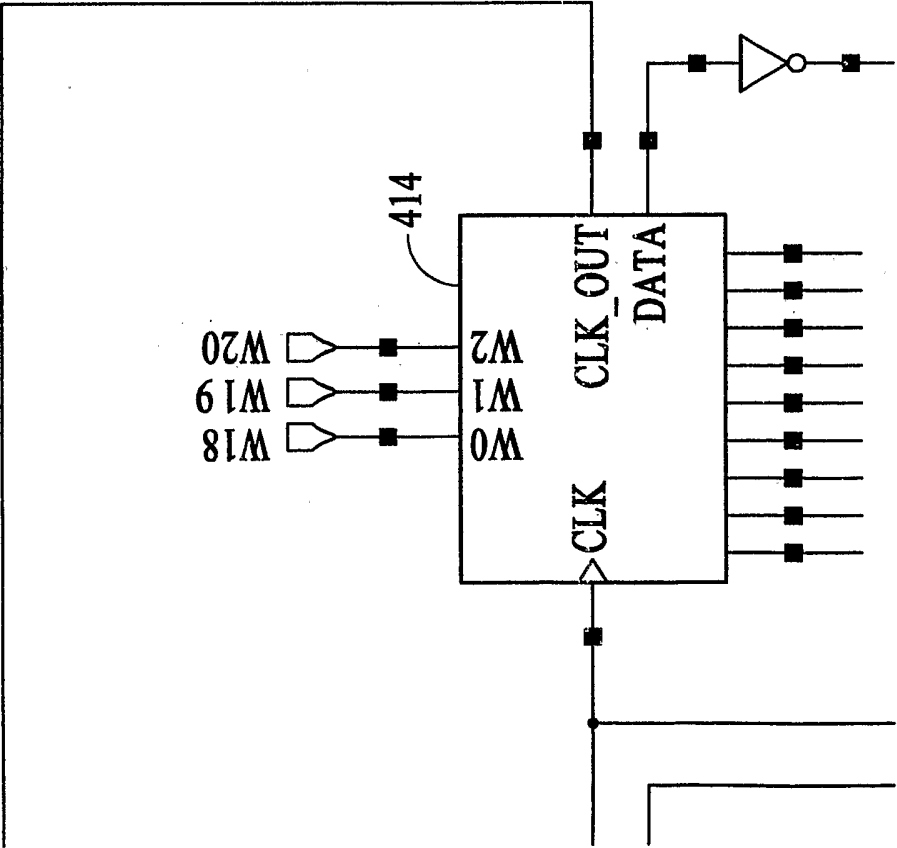


FIG.4/5



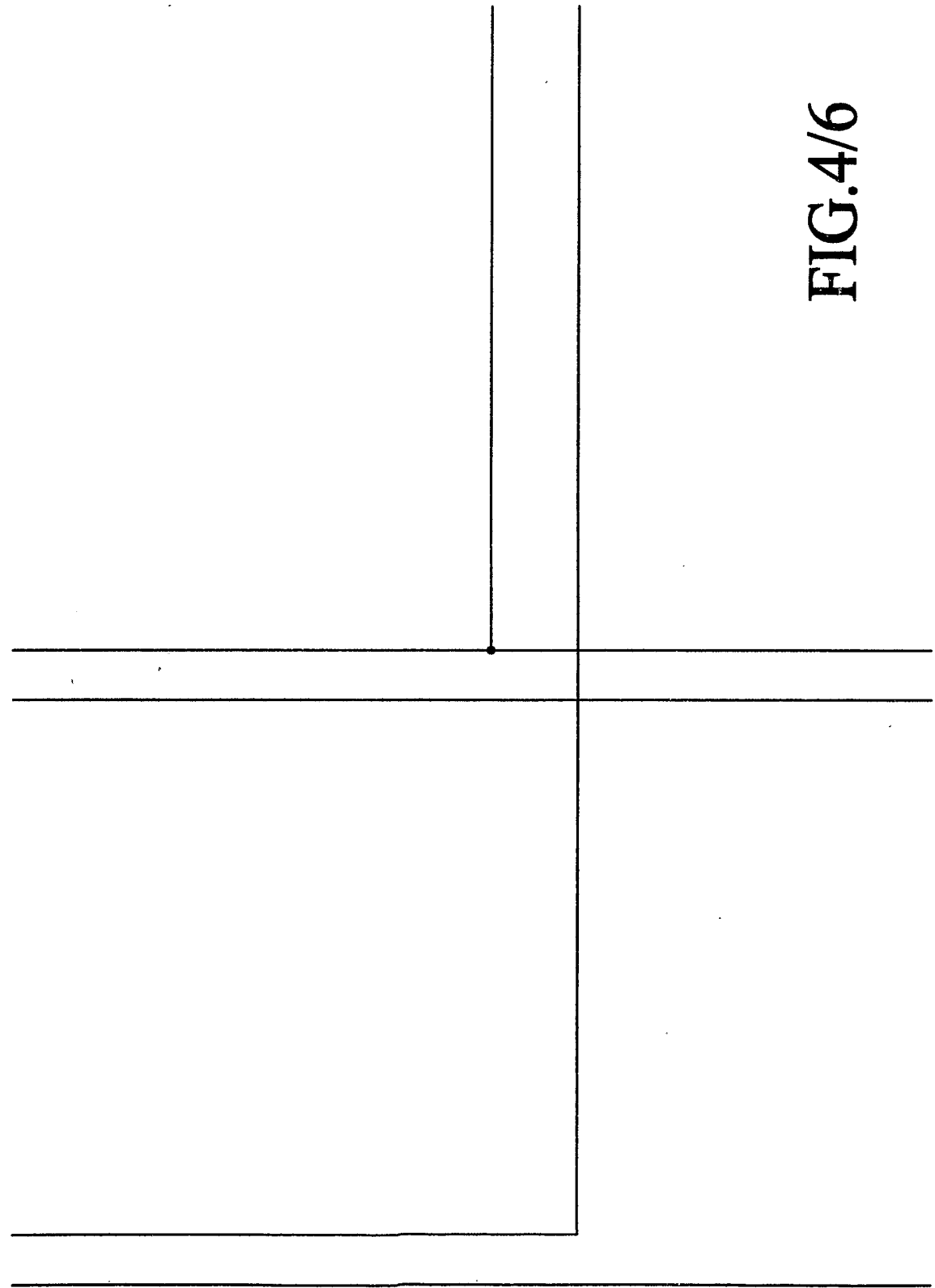


FIG. 4/6

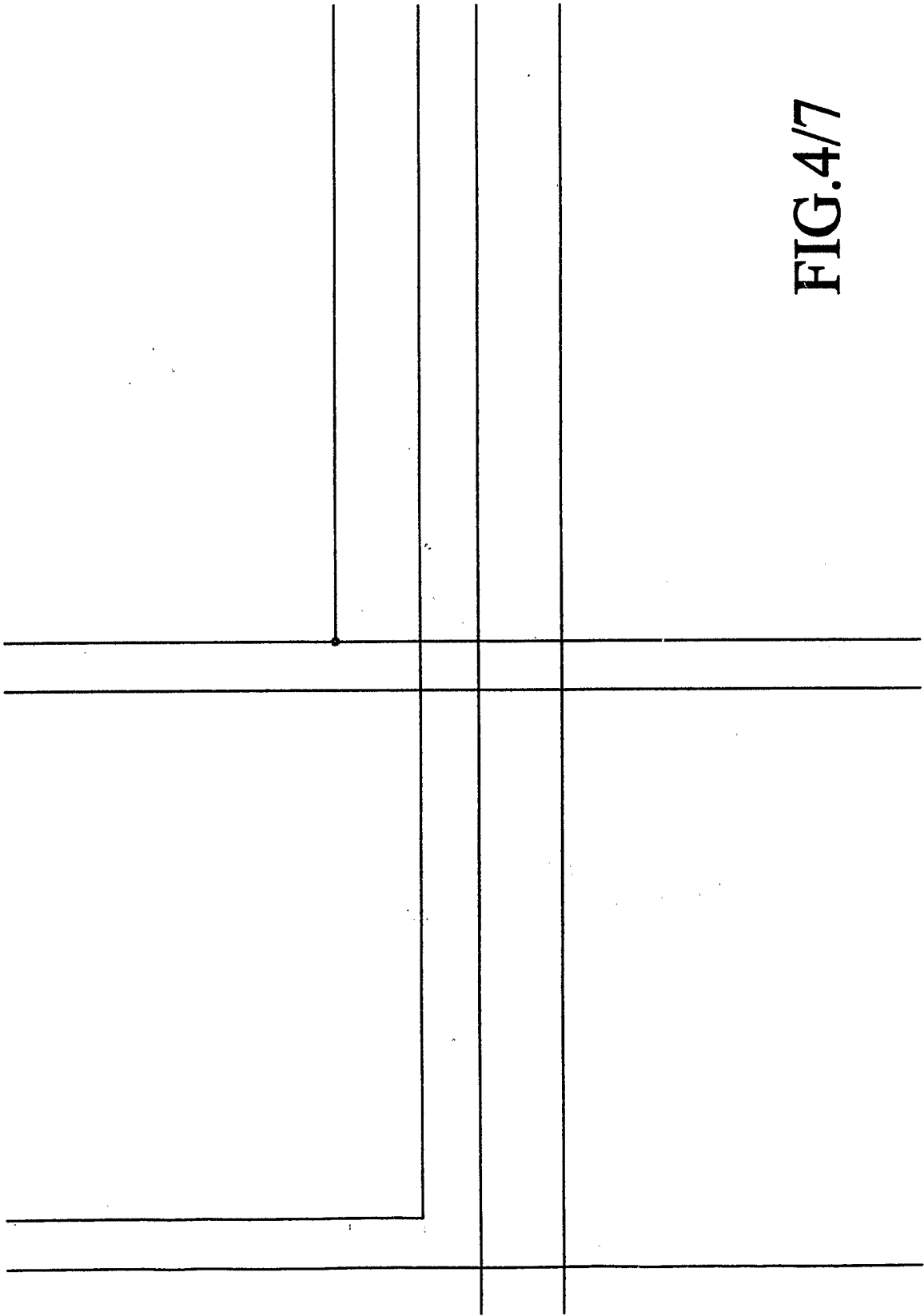


FIG.4/7

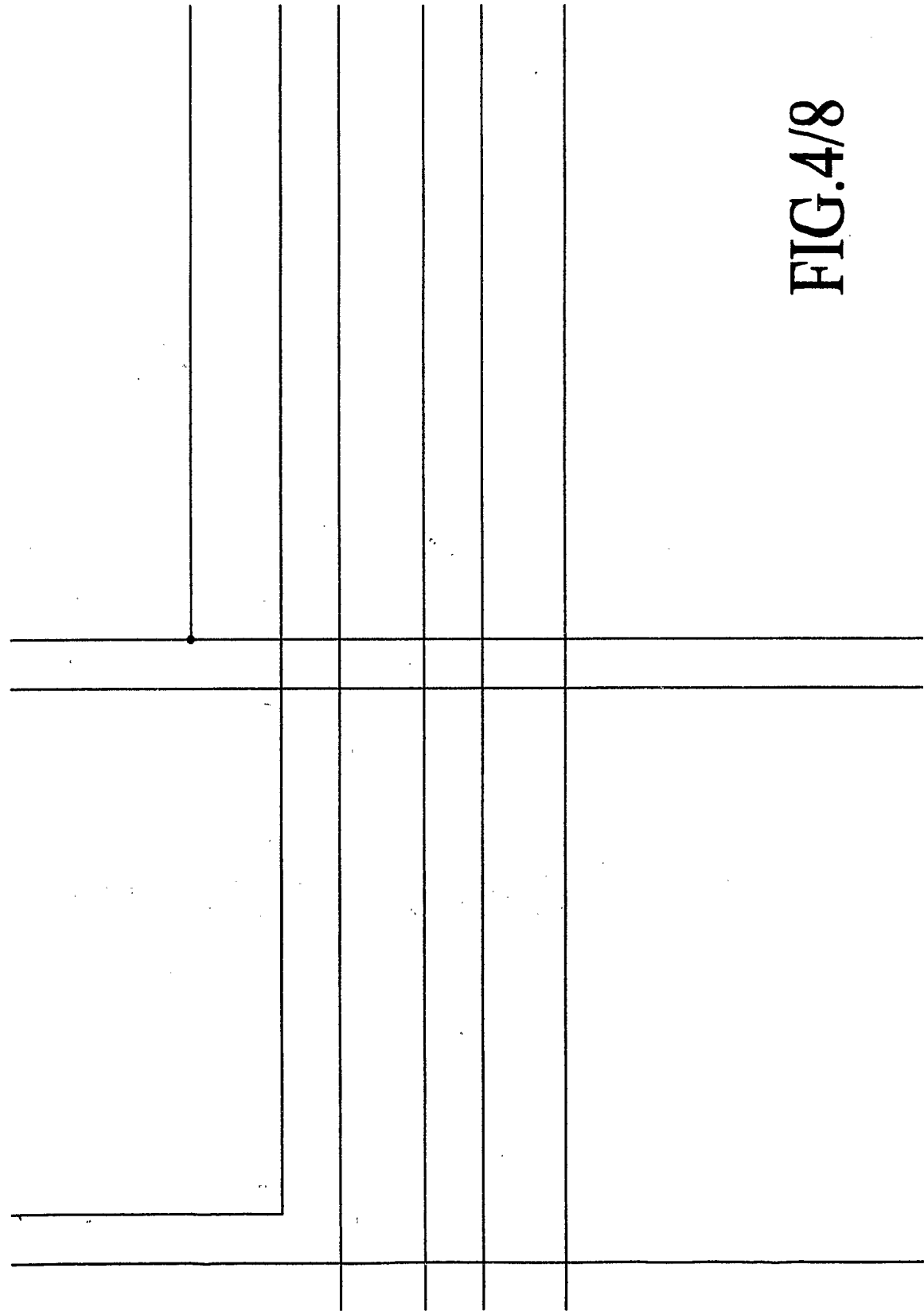


FIG. 4/8

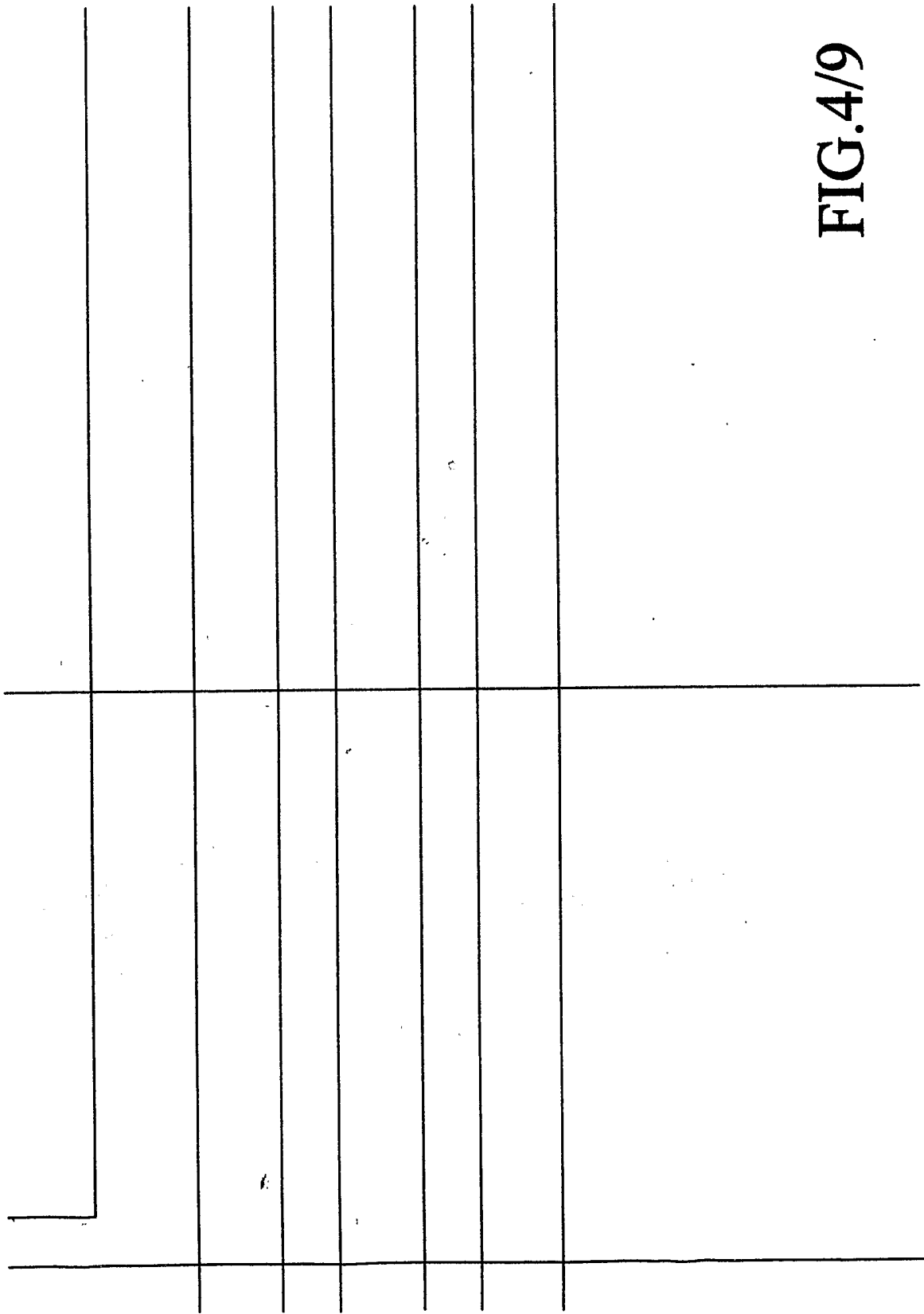


FIG.4/9

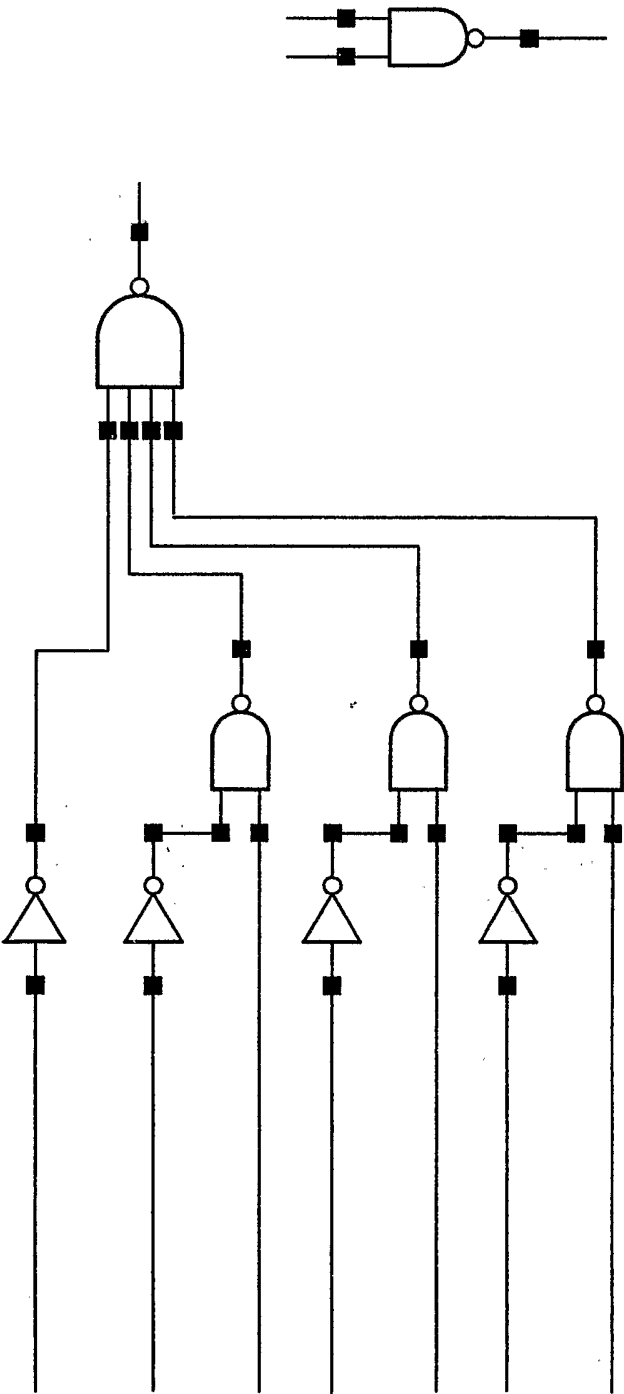


FIG.4/10

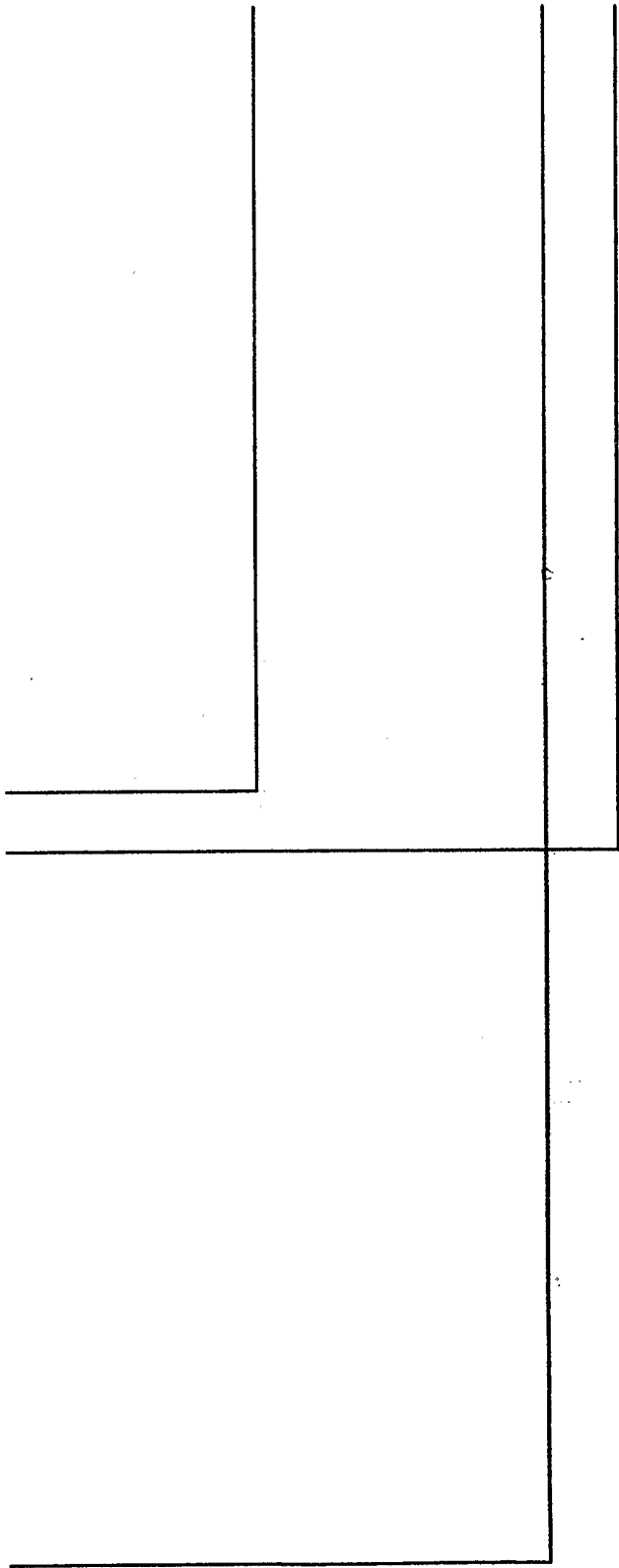


FIG.4/11

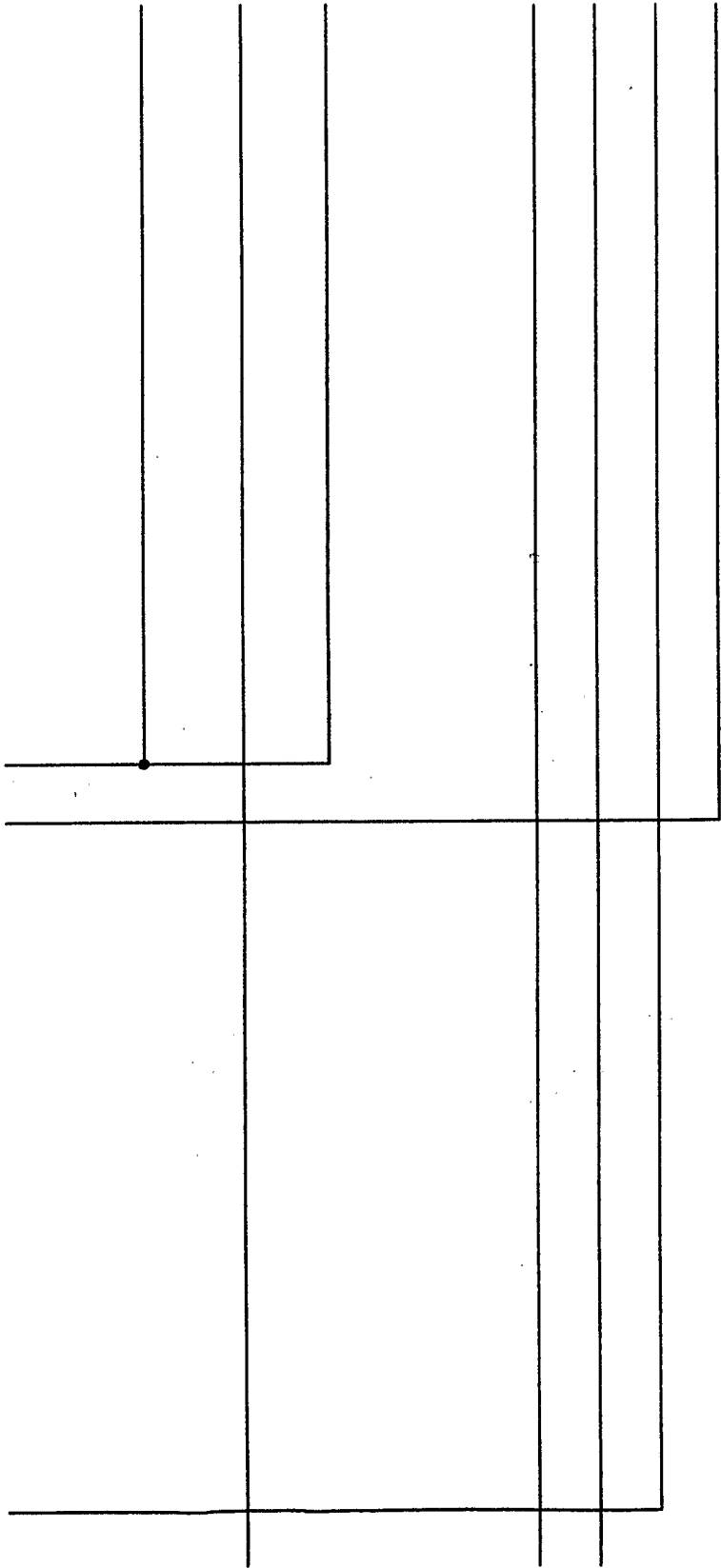


FIG. 4/12

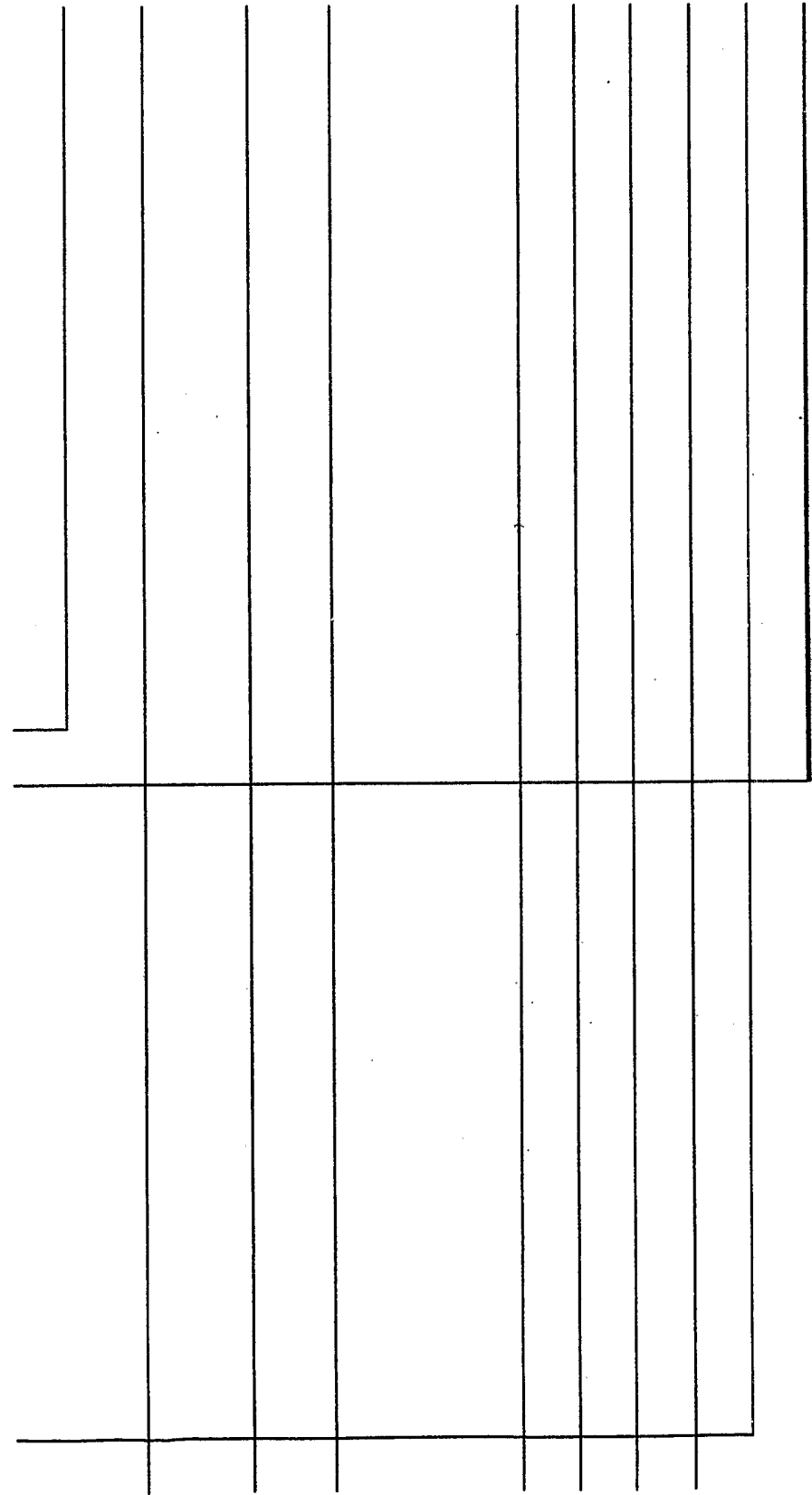


FIG. 4/13

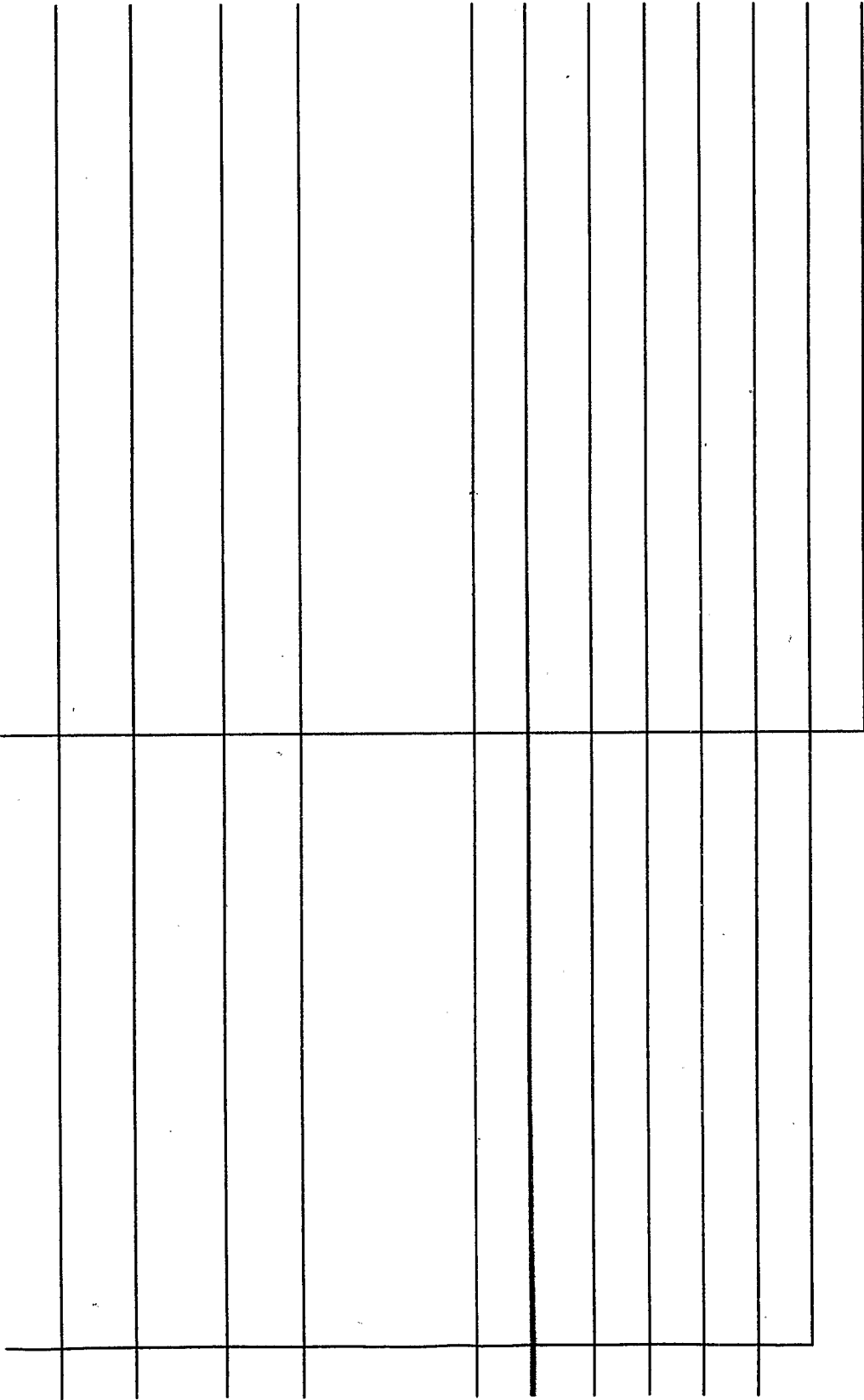


FIG.4/14

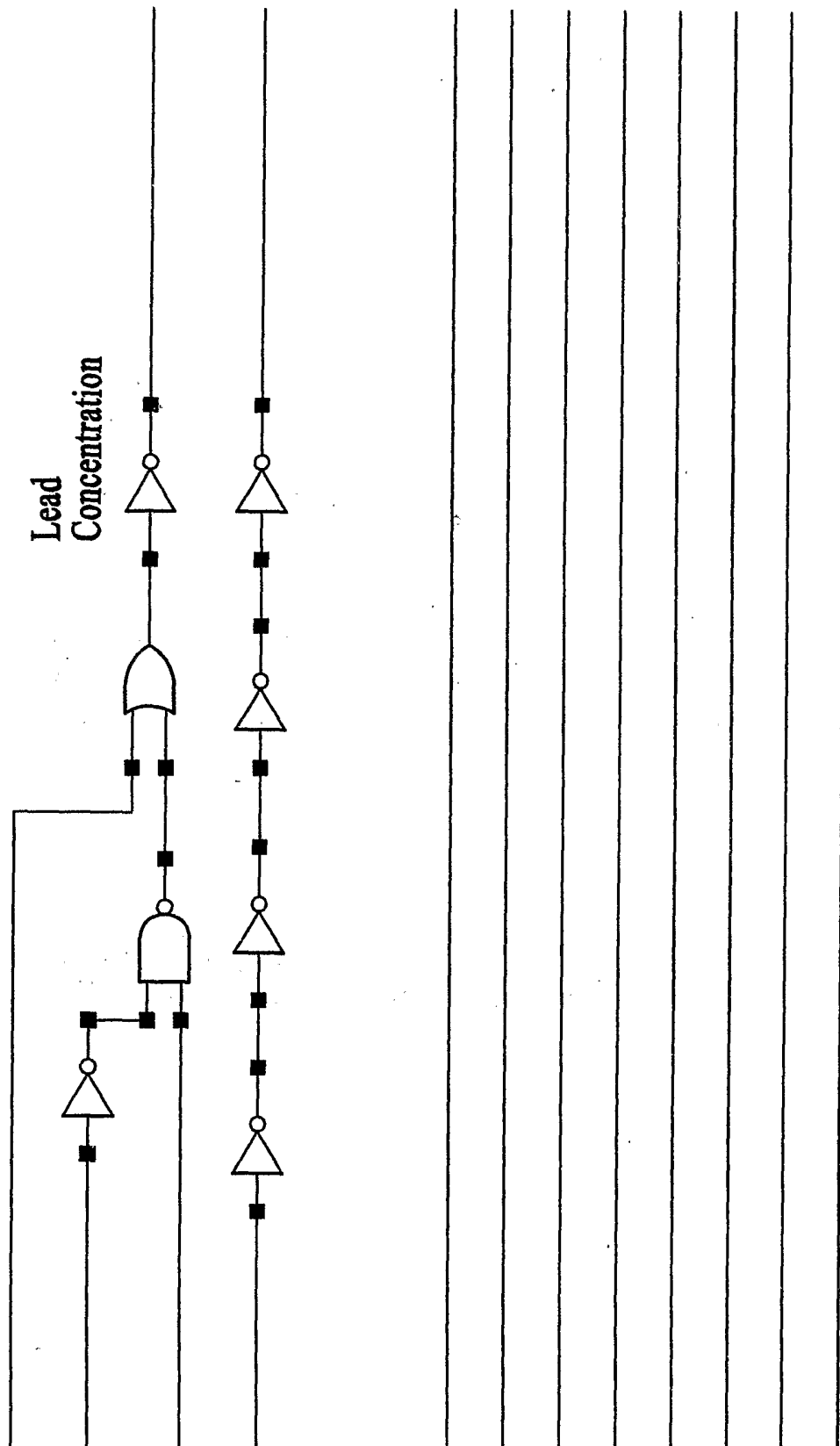


FIG. 4/15

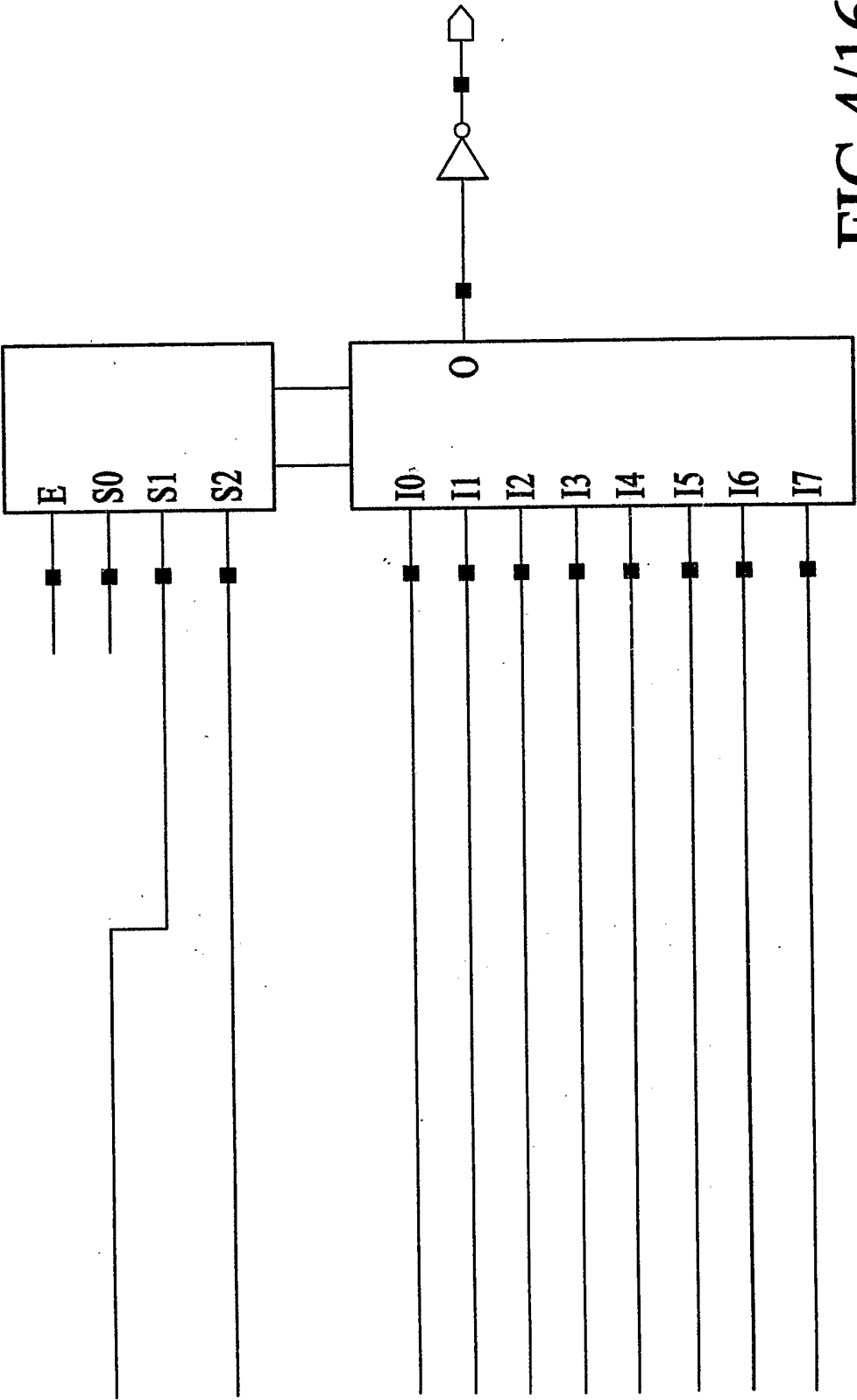


FIG.4/16