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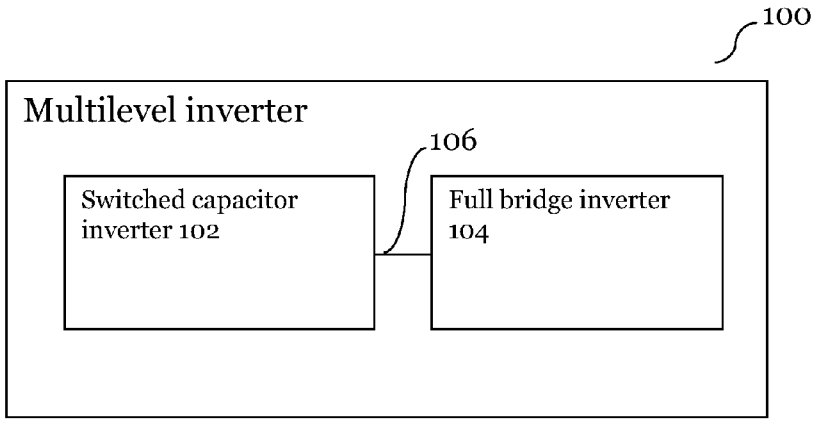

Figure 1

(57) Abstract: A multilevel inverter is disclosed. The multilevel inverter may include: a switched capacitor inverter configured to output a unipolar sequence of DC voltages; and a full bridge inverter configured to receive the unipolar sequence of DC voltages and to output a bipolar sequence of DC voltages.

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MULTILEVEL INVERTERS

PRIORITY CLAIMS

[0001] The present application claims priority to United States of America provisional patent application number 62,307,590. The present application furthermore claims priority to United States of America provisional patent application number 62,307,591.

TECHNICAL FIELD

[0002] The following discloses a multilevel inverter. In particular, a multilevel inverter with a switched-capacitor inverter and a full bridge inverter may be provided.

BACKGROUND ART

[0003] Power distribution systems with frequencies above utility frequency (50 Hz or 60 Hz) are traditionally referred to as high frequency AC (alternating current) power distribution systems. High frequency AC power distribution systems find application for example in aerospace, telecommunication, lighting, computer power supply, micro-grids and auxiliary power supply units for automotive. High frequency AC power distribution systems offer significant advantages over conventional direct current (DC) power distribution systems and low frequency alternating current power distribution systems.

[0004] However, presently used systems suffer for example from the requirement of a high number of components. Thus, there is a want for improved systems.

[0005] Furthermore, other desirable features and characteristics will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and this background of the disclosure.

SUMMARY OF INVENTION

[0006] According to an aspect of the invention, multilevel inverter is disclosed. The multilevel inverter may include: a switched capacitor inverter configured to output a unipolar

sequence of DC voltages; and a full bridge inverter configured to receive the unipolar sequence of DC voltages and to output a bipolar sequence of DC voltages.

[0007] According to various embodiments, the unipolar sequence may include or may be a periodic sequence. According to various embodiments, the unipolar sequence may include or may be a rising sub-sequence and a falling sub-sequence. According to various embodiments, the bipolar sequence may include or may be a periodic sequence. According to various embodiments, the bipolar sequence may include or may be a rising sub-sequence and a falling sub-sequence.

[0008] According to various embodiments, the switched capacitor inverter may include or may be a charge pump. According to various embodiments, the switched capacitor inverter may be configured to be connected to a single voltage source. According to various embodiments, the switched capacitor inverter may be configured to be connected to a plurality of voltage sources.

[0009] According to various embodiments, the full bridge inverter may be configured to selectively pass through the DC voltages of the unipolar sequence or to negate the DC voltages of the unipolar sequence.

[0010] According to various embodiments, the switched capacitor inverter may be configured to be connected to a first voltage source and to a second voltage source. According to various embodiments, the switched capacitor inverter may include a first switched capacitor inverter switch, a second switched capacitor inverter switch, a third switched capacitor inverter switch, a first diode, a second diode and a capacitor.

[0011] According to various embodiments, the first switched capacitor inverter switch may be connected to the second voltage source, the second diode, and the second switched capacitor inverter switch; the second switched capacitor inverter switch may be connected to the first switched capacitor inverter switch, the second diode, the capacitor, and the third switched capacitor inverter switch; the third switched capacitor inverter switch may be connected to the first voltage source, the second voltage source, the second switched capacitor inverter switch, the capacitor, and the full bridge inverter; the first diode may be connected to the first voltage source and the second diode; the second diode may be connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the first

diode, and the capacitor; and the capacitor may be connected to the second switched capacitor inverter switch, the third switched capacitor inverter switch, the first diode, the second diode, and the full bridge inverter.

[0012] According to various embodiments, the unipolar sequence may include or may be DC voltages of four different levels corresponding to a zero voltage, a voltage of the first voltage source, a voltage of the second voltage source, and a sum of the voltage of the first voltage source and the voltage of the second voltage source. According to various embodiments, the bipolar sequence may include or may be DC voltages of seven different levels corresponding to a zero voltage, the voltage of the first voltage source, the voltage of the second voltage source, the sum of the voltage of the first voltage source and the voltage of the second voltage source, an inverted voltage of the first voltage source, an inverted voltage of the second voltage source, and an inverted sum of the voltage of the first voltage source and the voltage of the second voltage source.

[0013] According to various embodiments, the switched capacitor inverter may be configured to output a voltage of the first voltage source to the full bridge inverter if the third switched capacitor inverter switch is in an on state and the first switched capacitor inverter switch and the second switched capacitor inverter switch are in an off state. According to various embodiments, the switched capacitor inverter may be configured to output a voltage of the second voltage source to the full bridge inverter if the first switched capacitor inverter switch is in an on state and the second switched capacitor inverter switch and the third switched capacitor inverter switch are in an off state. According to various embodiments, the switched capacitor inverter may be configured to output a voltage corresponding to a sum of the voltage of the first voltage source and the voltage of the second voltage source to the full bridge inverter if the first switched capacitor inverter switch and the second switched capacitor inverter switch are in an on state and the third switched capacitor inverter switch is in an off state.

[0014] According to various embodiments, the switched capacitor inverter may include or may be a voltage increaser configured to selectively increase a voltage of at least one of the first voltage source or the second voltage source. According to various embodiments, the switched capacitor inverter may include or may be a voltage doubler configured to selectively double a voltage of at least one of the first voltage source or the second voltage source.

According to various embodiments, the switched capacitor inverter may include or may be a voltage reducer configured to selectively reduce a voltage of at least one of the first voltage source or the second voltage source. According to various embodiments, the switched capacitor inverter may include or may be a voltage reducer configured to selectively half a voltage of at least one of the first voltage source or the second voltage source.

[0015] According to various embodiments, the unipolar sequence may include or may be DC voltages of five different levels; and the bipolar sequence may include or may be DC voltages of nine different levels.

[0016] According to various embodiments, the switched capacitor inverter may be configured to be connected to at least three voltage sources; and the switched capacitor inverter may be configured to selectively output voltages corresponding to combinations of voltages of the three voltage sources to the full bridge inverter.

[0017] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a relay. According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a transistor. According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a bipolar junction transistor. According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be an insulated-gate bipolar transistor. According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a metal–oxide–semiconductor field-effect transistor.

[0018] According to various embodiments, the switched capacitor inverter may be configured to be connected to a single voltage source; and the switched capacitor inverter may include or may be a first switched capacitor inverter switch, a second switched capacitor

inverter switch, a third switched capacitor inverter switch, a fourth switched capacitor inverter switch, a first diode, a second diode, a first capacitor, and a second capacitor.

[0019] According to various embodiments, the first switched capacitor inverter switch may be connected to the voltage source, the first diode, the first capacitor, the second switched capacitor inverter switch, and the fourth switched capacitor inverter switch; the second switched capacitor inverter switch may be connected to the voltage source, to the first switched capacitor inverter switch, to the first capacitor, to the fourth switched capacitor inverter switch, and to the full bridge inverter; the third switched capacitor inverter switch may be connected to the fourth switched capacitor inverter switch, the first diode, the second diode, the first capacitor, and the second capacitor; the fourth switched capacitor inverter switch may be connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, the first capacitor, and the second capacitor; the first diode may be connected to the voltage source, the first switched capacitor inverter switch, the third switched capacitor inverter switch, and the second diode; the second diode may be connected to the third switched capacitor inverter switch, the first diode, the first capacitor, the second capacitor, and the full bridge inverter; the first capacitor may be connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, the fourth switched capacitor inverter switch, the first diode, and the second diode; and the second capacitor may be connected to the third switched capacitor inverter switch, the fourth switched capacitor inverter switch, the second diode, and the full bridge inverter.

[0020] According to various embodiments, the unipolar sequence may include or may be DC voltages of four different levels corresponding to a zero voltage, a voltage of the voltage source, a doubled voltage of the voltage source, and a tripled voltage of the voltage source; and the bipolar sequence may include or may be DC voltages of seven different levels corresponding to a zero voltage, a voltage of the voltage source, a doubled voltage of the voltage source, and a tripled voltage of the voltage source, an inverted voltage of the voltage source, an inverted doubled voltage of the voltage source, and an inverted tripled voltage of the voltage source.

[0021] According to various embodiments, the switched capacitor inverter may be configured to output a voltage of the voltage source to the full bridge inverter if the second

switched capacitor inverter switch and the fourth switched capacitor inverter switch are in an on state and the first switched capacitor inverter switch and the third switched capacitor inverter switch are in an off state. According to various embodiments, the switched capacitor inverter may be configured to output a doubled voltage of the voltage source to the full bridge inverter if the first switched capacitor inverter switch is in an on state and the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch are in an off state. According to various embodiments, the switched capacitor inverter may be configured to output a tripled voltage of the voltage source to the full bridge inverter if the first switched capacitor inverter switch and the third switched capacitor inverter switch are in an on state and the second switched capacitor inverter switch and the fourth switched capacitor inverter switch are in an off state.

[0022] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a relay.

[0023] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a transistor. According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a bipolar junction transistor. According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be an insulated-gate bipolar transistor. According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a metal–oxide–semiconductor field-effect transistor.

[0024] According to various embodiments, the switched capacitor inverter may be configured to be connected to a single voltage source; and the switched capacitor inverter may

include or may be a plurality of voltage increasers configured to selectively increase a voltage of the voltage source.

[0025] According to various embodiments, the switched capacitor inverter may be configured to be connected to a single voltage source; and the switched capacitor inverter may include or may be a plurality of voltage doublers configured to selectively double a voltage of the voltage source.

[0026] According to various embodiments, the switched capacitor inverter may be configured to be connected to a single voltage source; and the switched capacitor inverter may include or may be a plurality of voltage reducers configured to selectively reduce a voltage of the voltage source.

[0027] According to various embodiments, the switched capacitor inverter may be configured to be connected to a single voltage source; and the switched capacitor inverter may include or may be a plurality of voltage reducers configured to selectively half a voltage of the voltage source.

[0028] According to various embodiments, the full bridge inverter may include a first full bridge inverter switch, a second full bridge inverter switch, a third full bridge inverter switch, and a fourth full bridge inverter switch.

[0029] According to various embodiments, the first full bridge inverter switch may be connected to the switched capacitor inverter the second full bridge inverter switch, the fourth full bridge inverter switch, and an output of the full bridge inverter; the second full bridge inverter switch may be connected to the switched capacitor inverter, the first full bridge inverter switch, the third full bridge inverter switch, and the output; the third full bridge inverter switch may be connected to the switched capacitor inverter, the second full bridge inverter switch, the fourth full bridge inverter switch, and the output; and the fourth full bridge inverter switch may be connected to the switched capacitor inverter, the first full bridge inverter switch, the third full bridge inverter switch, and the output.

[0030] According to various embodiments, the full bridge inverter may be configured to output a voltage received from the switched capacitor inverter if the first full bridge inverter

switch and the third full bridge inverter switch are in an on state and the second full bridge inverter switch and the fourth full bridge inverter switch are in an off state.

[0031] According to various embodiments, the full bridge inverter may be configured to invert a voltage received from the switched capacitor inverter and output the inverted voltage if the second full bridge inverter switch and the fourth full bridge inverter switch are in an on state and the first full bridge inverter switch and the third full bridge inverter switch are in an off state.

[0032] According to various embodiments, the full bridge inverter may be configured to output a zero voltage after having output a positive voltage with the first full bridge inverter switch in an on state and the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch in an off state.

[0033] According to various embodiments, a body diode associated with the second full bridge inverter switch may be configured to provide freewheeling.

[0034] According to various embodiments, the full bridge inverter may be configured to output a zero voltage after having output a negative voltage with the fourth full bridge inverter switch in an on state and the first full bridge inverter switch, the second full bridge inverter switch, and the third full bridge inverter switch in an off state.

[0035] According to various embodiments, a body diode associated with the fourth full bridge inverter switch may be configured to provide freewheeling.

[0036] According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be a relay.

[0037] According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be a transistor. According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and

the fourth full bridge inverter switch may include or may be a bipolar junction transistor. According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be an insulated-gate bipolar transistor. According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be a metal–oxide–semiconductor field-effect transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to illustrate various embodiments, by way of example only, and to explain various principles and advantages in accordance with a present embodiment.

[0039] Figure 1 shows a multilevel inverter in accordance with an embodiment of the invention.

[0040] Figure 2 shows a topology of a high frequency multilevel inverter according to various embodiments.

[0041] Figure 3A to Figure 3H show topological stages of a seven level switched-capacitor multilevel inverter according to various embodiments.

[0042] Figure 4 shows a simulation model according to various embodiments.

[0043] Figure 5 shows a diagram illustrating a 50 kHz multilevel (seven) staircase output voltage of an inverter according to various embodiments.

[0044] Figure 6 shows a nine level switched–capacitor based multilevel inverter (MLI) according to various embodiments.

[0045] Figure 7 shows a nine level switched–capacitor based MLI according to various embodiments.

[0046] Figure 8 shows an illustration of a generalized topology for a switched capacitor based multilevel inverter (SCMLI) according to various embodiments.

[0047] Figure 9 shows a topology of a high frequency multilevel inverter according to various embodiments.

[0048] Figure 10A to Figure 10H show illustrations of topological stages of a seven level switched–capacitor multilevel inverter according to various embodiments.

[0049] Figure 11 shows a simulation model according to various embodiments.

[0050] Figure 12 shows a diagram illustrating a 50 kHz multilevel (seven) staircase output voltage of an inverter according to various embodiments.

[0051] Figure 13A shows a nine level switched–capacitor based MLI according to various embodiments.

[0052] Figure 13B and Figure 13C show higher level switched-capacitor multilevel inverters according to various embodiments.

[0053] Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been depicted to scale. For example, the dimensions of some of the elements in the block diagrams or steps in the flowcharts may be exaggerated in respect to other elements to help improve understanding of the present embodiment.

DETAILED DESCRIPTION

[0054] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any theory presented in the preceding background of the invention or the following detailed description. It is the intent of the preferred embodiments to disclose a method and system which is able to efficiently generate AC (alternating current) voltages.

[0055] Power distribution systems with frequencies above utility frequency (50 Hz or 60 Hz) are traditionally referred to as high frequency AC power distribution systems (HFAC PDS). HFAC PDS find application for example in aerospace, telecommunication, lighting, computer

power supply, micro-grids and auxiliary power supply units for automotive. HFAC PDS offer significant advantages over conventional direct current (DC) PDS and low frequency alternating current PDS. An advantage of HFAC PDS over DC PDS is that HFAC PDS eliminate the need for a rectifier stage in the front end power supply system, and the need for an inverter in the point of load power supply. Advantageously, this reduction in the number of power conversion stages translates to fewer components, higher efficacy/ efficiency, lower cost and better reliability.

[0056] Multilevel inverters (MLIs) are used in the power industry owing to benefits they present. With MLIs, it is easier to produce a high power, high voltage AC output with a multilevel topology as the voltage stress on the individual device is controlled. Advantageously, it is furthermore possible to obtain higher voltages with low harmonics without employing transformers. The harmonic content may be mitigated by increasing the number of voltage levels in the AC output. Multilevel inverters are generally classified into diode–clamped, flying–capacitors (also called capacitor–clamped) and cascaded types. Popular PWM (pulse width modulation) strategies include space vector modulation, multilevel selective harmonic elimination and multilevel sinusoidal pulse width modulation.

[0057] Switched–capacitor converters have drawn attention due to their simplicity, low weight and low cost features. They employ switches and capacitors to achieve voltage conversion. Since they eliminate the need for bulky inductors, they are usually small in size and extremely lighter. These features allow switched–capacitor converters to be also fabricated into ICs (integrated circuits).

[0058] According to various embodiments, a switched–capacitor converter (in other words: a switched-capacitor inverter) may be provided in a multilevel inverter to realize a circuitry that outputs a staircase high frequency AC waveform. According to various embodiments, a switched–capacitor based front end DC level shifter may enable a system to obtain multiple voltage levels to realize a multilevel inverter.

[0059] Advantageously, according to various embodiments, an inverter is provided which uses a reasonable number of capacitors, and can be operated without relying on PWM (pulse width modulation), in contrast to commonly used inverters which use a high number of switches and which use complex PWM techniques.

[0060] According to various embodiments, a topology of multilevel inverters for high frequency AC applications may be provided. The multilevel inverters according to various embodiments may employ a switched–capacitor technique. Advantageously, the multilevel inverters according to various embodiments may include an inverter front end including a switched–capacitor based DC (direct current) level shifter that produces multiple DC levels at the DC bus of the inverter. Advantageously, the multilevel inverters according to various embodiments may further include a full bridge inverter which obtains different voltage levels at the output.

[0061] Figure 1 shows a multilevel inverter 100 according to various embodiments. The multilevel inverter 100 may include a switched capacitor inverter 102 configured to output a unipolar sequence of DC voltages. The multilevel inverter 100 may further include a full bridge inverter 104 configured to receive the unipolar sequence of DC voltages and to output a bipolar sequence of DC voltages. The switched capacitor inverter 102 and the full bridge inverter 104 may be connected, like illustrated by line 106, for example electrically connected.

[0062] In other words, advantageously, the full bridge inverter 104 of the multilevel inverter 100 receives a sequence of DC voltages of a single polarity from the switched capacitor inverter 102, and generates a sequence of DC voltages of two different polarities based on (in other words: from) the received sequence of DC voltages of the single polarity. In other words, the full bridge inverter 104 of the multilevel inverter 100 converts a sequence of DC voltages of a single polarity received from the switched capacitor inverter 102 into a sequence of DC voltages of two different polarities.

[0063] According to various embodiments, the unipolar sequence may include or may be a periodic sequence.

[0064] According to various embodiments, the unipolar sequence may include or may be a rising sub-sequence and a falling sub-sequence.

[0065] According to various embodiments, the unipolar sequence may include or may be DC voltages of a single pre-determined polarity.

[0066] According to various embodiments, the bipolar sequence may include or may be a periodic sequence.

[0067] According to various embodiments, the bipolar sequence may include or may be a rising sub-sequence and a falling sub-sequence.

[0068] According to various embodiments, the bipolar sequence may include or may be DC voltages of two different polarities.

[0069] According to various embodiments, the switched capacitor inverter 102 may include or may be a charge pump.

[0070] According to various embodiments, the switched capacitor inverter 102 may include a plurality of capacitors.

[0071] According to various embodiments, the switched capacitor inverter 102 may be free from inductors.

[0072] According to various embodiments, the unipolar sequence may be free from pulse width modulation signals.

[0073] According to various embodiments, the bipolar sequence may be free from pulse width modulation signals.

[0074] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a single voltage source. Advantageously, generating the multilevel voltages from a single voltage source reduces complexity of the input to the multilevel inverter

[0075] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a plurality of voltage sources.

[0076] According to various embodiments, the full bridge inverter 104 may be configured to selectively pass through the DC voltages of the unipolar sequence or to negate the DC voltages of the unipolar sequence.

[0077] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a first voltage source and to a second voltage source. According to various embodiments, the switched capacitor inverter 102 may include a first switched capacitor inverter switch, a second switched capacitor inverter switch, a third switched capacitor inverter switch, a first diode, a second diode and a capacitor.

[0078] According to various embodiments, the first switched capacitor inverter switch may be connected to the second voltage source, the second diode, and the second switched capacitor inverter switch; the second switched capacitor inverter switch may be connected to the first switched capacitor inverter switch, the second diode, the capacitor, and the third switched capacitor inverter switch; the third switched capacitor inverter switch may be connected to the first voltage source, the second voltage source, the second switched capacitor inverter switch, the capacitor, and the full bridge inverter 104; the first diode may be connected to the first voltage source and the second diode; the second diode may be connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the first diode, and the capacitor; and the capacitor may be connected to the second switched capacitor inverter switch, the third switched capacitor inverter switch, the first diode, the second diode, and the full bridge inverter 104.

[0079] According to various embodiments, the unipolar sequence may include or may be DC voltages of four different levels corresponding to a zero voltage, a voltage of the first voltage source, a voltage of the second voltage source, and a sum of the voltage of the first voltage source and the voltage of the second voltage source. According to various embodiments, the bipolar sequence may include or may be DC voltages of seven different levels corresponding to a zero voltage, the voltage of the first voltage source, the voltage of the second voltage source, the sum of the voltage of the first voltage source and the voltage of the second voltage source, an inverted voltage of the first voltage source, an inverted voltage of the second voltage source, and an inverted sum of the voltage of the first voltage source and the voltage of the second voltage source.

[0080] According to various embodiments, the switched capacitor inverter 102 may be configured to output a voltage of the first voltage source to the full bridge inverter 104 if the third switched capacitor inverter switch is in an on state and the first switched capacitor inverter switch and the second switched capacitor inverter switch are in an off state.

[0081] According to various embodiments, the switched capacitor inverter 102 may be configured to output a voltage of the second voltage source to the full bridge inverter 104 if the first switched capacitor inverter switch is in an on state and the second switched capacitor inverter switch and the third switched capacitor inverter switch are in an off state.

[0082] According to various embodiments, the switched capacitor inverter 102 may be configured to output a voltage corresponding to a sum of the voltage of the first voltage source and the voltage of the second voltage source to the full bridge inverter 104 if the first switched capacitor inverter switch and the second switched capacitor inverter switch are in an on state and the third switched capacitor inverter switch is in an off state.

[0083] According to various embodiments, the switched capacitor inverter 102 may include or may be a voltage increaser configured to selectively increase a voltage of at least one of the first voltage source or the second voltage source.

[0084] According to various embodiments, the switched capacitor inverter 102 may include or may be a voltage doubler configured to selectively double a voltage of at least one of the first voltage source or the second voltage source.

[0085] According to various embodiments, the switched capacitor inverter 102 may include or may be a voltage reducer configured to selectively reduce a voltage of at least one of the first voltage source or the second voltage source.

[0086] According to various embodiments, the switched capacitor inverter 102 may include or may be a voltage reducer configured to selectively half a voltage of at least one of the first voltage source or the second voltage source.

[0087] According to various embodiments, the unipolar sequence may include or may be DC voltages of five different levels; and the bipolar sequence may include or may be DC voltages of nine different levels.

[0088] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to at least three voltage sources; and the switched capacitor

inverter 102 may be configured to selectively output voltages corresponding to combinations of voltages of the three voltage sources to the full bridge inverter 104.

[0089] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a relay.

[0090] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a transistor.

[0091] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a bipolar junction transistor.

[0092] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be an insulated-gate bipolar transistor.

[0093] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch may include or may be a metal–oxide–semiconductor field-effect transistor.

[0094] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a single voltage source; and the switched capacitor inverter 102 may include or may be a first switched capacitor inverter switch, a second switched capacitor inverter switch, a third switched capacitor inverter switch, a fourth switched capacitor inverter switch, a first diode, a second diode, a first capacitor, and a second capacitor.

[0095] According to various embodiments, the first switched capacitor inverter switch may be connected to the voltage source, the first diode, the first capacitor, the second switched capacitor inverter switch, and the fourth switched capacitor inverter switch; the second

switched capacitor inverter switch may be connected to the voltage source, to the first switched capacitor inverter switch, to the first capacitor, to the fourth switched capacitor inverter switch, and to the full bridge inverter 104; the third switched capacitor inverter switch may be connected to the fourth switched capacitor inverter switch, the first diode, the second diode, the first capacitor, and the second capacitor; the fourth switched capacitor inverter switch may be connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, the first capacitor, and the second capacitor; the first diode may be connected to the voltage source, the first switched capacitor inverter switch, the third switched capacitor inverter switch, and the second diode; the second diode may be connected to the third switched capacitor inverter switch, the first diode, the first capacitor, the second capacitor, and the full bridge inverter 104; the first capacitor may be connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, the fourth switched capacitor inverter switch, the first diode, and the second diode; and the second capacitor may be connected to the third switched capacitor inverter switch, the fourth switched capacitor inverter switch, the second diode, and the full bridge inverter 104.

[0096] According to various embodiments, the unipolar sequence may include or may be DC voltages of four different levels corresponding to a zero voltage, a voltage of the voltage source, a doubled voltage of the voltage source, and a tripled voltage of the voltage source; and the bipolar sequence may include or may be DC voltages of seven different levels corresponding to a zero voltage, a voltage of the voltage source, a doubled voltage of the voltage source, and a tripled voltage of the voltage source, an inverted voltage of the voltage source, an inverted doubled voltage of the voltage source, and an inverted tripled voltage of the voltage source.

[0097] According to various embodiments, the switched capacitor inverter 102 may be configured to output a voltage of the voltage source to the full bridge inverter 104 if the second switched capacitor inverter switch and the fourth switched capacitor inverter switch are in an on state and the first switched capacitor inverter switch and the third switched capacitor inverter switch are in an off state.

[0098] According to various embodiments, the switched capacitor inverter 102 may be configured to output a doubled voltage of the voltage source to the full bridge inverter 104 if

the first switched capacitor inverter switch is in an on state and the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch are in an off state.

[0099] According to various embodiments, the switched capacitor inverter 102 may be configured to output a tripled voltage of the voltage source to the full bridge inverter 104 if the first switched capacitor inverter switch and the third switched capacitor inverter switch are in an on state and the second switched capacitor inverter switch and the fourth switched capacitor inverter switch are in an off state.

[00100] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a relay.

[00101] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a transistor.

[00102] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a bipolar junction transistor.

[00103] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be an insulated-gate bipolar transistor.

[00104] According to various embodiments, one or more (for example all) of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch may include or may be a metal–oxide–semiconductor field-effect transistor.

[00105] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a single voltage source; and the switched capacitor inverter 102 may include or may be a plurality of voltage increasers configured to selectively increase a voltage of the voltage source.

[00106] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a single voltage source; and the switched capacitor inverter 102 may include or may be a plurality of voltage doublers configured to selectively double a voltage of the voltage source.

[00107] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a single voltage source; and the switched capacitor inverter 102 may include or may be a plurality of voltage reducers configured to selectively reduce a voltage of the voltage source.

[00108] According to various embodiments, the switched capacitor inverter 102 may be configured to be connected to a single voltage source; and the switched capacitor inverter 102 may include or may be a plurality of voltage reducers configured to selectively half a voltage of the voltage source.

[00109] According to various embodiments, the full bridge inverter 104 may include a first full bridge inverter switch, a second full bridge inverter switch, a third full bridge inverter switch, and a fourth full bridge inverter switch.

[00110] According to various embodiments, the first full bridge inverter switch may be connected to the switched capacitor inverter 102, the second full bridge inverter switch, the fourth full bridge inverter switch, and an output of the full bridge inverter; the second full bridge inverter switch may be connected to the switched capacitor inverter 102, the first full bridge inverter switch, the third full bridge inverter switch, and the output; the third full bridge inverter switch may be connected to the switched capacitor inverter 102, the second full bridge inverter switch, the fourth full bridge inverter switch, and the output; and the fourth full bridge inverter switch may be connected to the switched capacitor inverter 102, the first full bridge inverter switch, the third full bridge inverter switch, and the output.

[00111] According to various embodiments, the full bridge inverter 104 may be configured to output a voltage received from the switched capacitor inverter 102 if the first full bridge inverter switch and the third full bridge inverter switch are in an on state and the second full bridge inverter switch and the fourth full bridge inverter switch are in an off state.

[00112] According to various embodiments, the full bridge inverter 104 may be configured to invert a voltage received from the switched capacitor inverter 102 and output the inverted voltage if the second full bridge inverter switch and the fourth full bridge inverter switch are in an on state and the first full bridge inverter switch and the third full bridge inverter switch are in an off state.

[00113] According to various embodiments, the full bridge inverter 104 may be configured to output a zero voltage after having output a positive voltage with the first full bridge inverter switch in an on state and the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch in an off state.

[00114] According to various embodiments, a body diode associated with the second full bridge inverter switch may be configured to provide freewheeling.

[00115] According to various embodiments, the full bridge inverter 104 may be configured to output a zero voltage after having output a negative voltage with the fourth full bridge inverter switch in an on state and the first full bridge inverter switch, the second full bridge inverter switch, and the third full bridge inverter switch in an off state.

[00116] According to various embodiments, a body diode associated with the fourth full bridge inverter switch may be configured to provide freewheeling.

[00117] According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be a relay.

[00118] According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be a transistor.

[00119] According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be a bipolar junction transistor.

[00120] According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be an insulated-gate bipolar transistor.

[00121] According to various embodiments, one or more (for example all) of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch may include or may be a metal–oxide–semiconductor field-effect transistor.

[00122] According to various embodiments, a switched capacitor based multilevel inverter for high frequency AC power distribution systems may be provided. According to various embodiments, a dual input switched capacitor based multilevel inverter for high frequency AC power distribution systems may be provided.

[00123] According to various embodiments, a front end DC level shifter with two (voltage) sources, three transistors, two diodes and a capacitor may be provided. Advantageously, providing to voltage sources reduces complexity of the circuit of the multilevel inverter.

[00124] According to various embodiments, a front end DC level shifter with a single voltage source, four transistors, two diodes and two capacitors may be provided.

[00125] According to various embodiments, a family of circuits may be provided. Each circuit of the family of circuits may use a low (for example a minimum) number of switches to obtain multiple DC voltage levels.

[00126] According to various embodiments, a multilevel inverter (or a topology of multilevel inverters), for example a multilevel inverter circuit, for high frequency AC applications may employ a switched–capacitor technique. The inverter front end may include a switched–capacitor based DC to DC converter (for example a DC level shifter) that produces multiple DC levels at the DC bus of the inverter. A full bridge inverter may receive the multiple DC levels and may obtain different voltage levels at the output.

[00127] For example, a multilevel inverter (which may use a plurality of DC input sources, or which may use a single DC input source and) may output for example a seven level (for example three positive levels, three negative levels and a zero level) staircase voltage waveform. Utilizing a switched–capacitor technique according to various embodiments, the need to use heavy magnetic components, which may also occupy large space, may be eliminated. Thus, an inverter according to various embodiments may be lighter, may be smaller in size and/ or may be cheaper.

[00128] According to various embodiments, a multilevel inverter may include a front end multi-level generator, which is realized by a switched-capacitor DC level shifter, and an H-bridge converter.

[00129] According to various embodiments, the front end switched–capacitor converter may be configured to produce multiple DC levels at the DC bus of the inverter. The front end converter may employ two voltage sources, two diodes, three transistors and one capacitor for voltage conversion.

[00130] Figure 2 shows an illustration 200 of a high frequency multilevel inverter (HF MLI) according to various embodiments, which may output a seven level staircase voltage waveform (three positive, zero and three negative). The HF MLI may include two cascaded stages: a switched capacitor based front end DC level shifter 202 and a full bridge inverter 204. The front end switched capacitor DC level shifter 202 may include (or employ) three (switched capacitor inverter) switches (for example MOSFETs): a first switch S_1 214, a second switch S_2 216 and a third switch S_3 220. The front end switched capacitor DC level shifter 202 may furthermore include two diodes: a first diode D_1 208 and a second diode D_2 210. The front end switched capacitor DC level shifter 202 may furthermore include two voltage sources: a first voltage source V_{IN1} 206 and a second voltage source V_{IN2} 218. The front end switched capacitor DC level shifter 202 may furthermore include a capacitor C 212. The different DC levels obtained at the V_{DCbus} 230 include V_{IN1}, V_{IN2} and $V_{IN1} + V_{IN2}$. The full

bridge inverter 204 employs four MOSFETs Q_1 222, Q_2 224, Q_3 226 *and* Q_4 228. Full bridge inverter operation effectively produces seven levels, i.e., *0*, $\pm V_{IN1}$, $\pm V_{IN2}$ and $\pm(V_{IN1} + V_{IN2})$, which for example are available to a load 232. For analysis, it may be assumed that the size of the capacitor 212 is large enough for the voltage ripple to be negligible, and that the switching devices (the MOSFETS 214, 216, 220, 222, 224, 226, and 228, and the diodes 208, 210) and the input voltage sources 206, 218 are ideal. The working states will be explained in more detail with reference to Figure 3A to Figure 3H.

[00131] Figure 3A shows an equivalent circuit 300 of the multilevel inverter according to various embodiments for $V_0 = +V_{IN1}$. Figure 3B shows an equivalent circuit 302 of the multilevel inverter according to various embodiments and $V_0 = -V_{IN1}$. For a $V_0 = \pm V_{IN1}$ state (which may be understood as to be a short form of a state in which $V_0 = +V_{IN1}$ or $V_0 = -V_{IN1}$), the capacitor C 212 is charged to V_{IN1} 206 through the first diode D_1 208 and by turning ON S_3 220, while S_1 214 and S_2 216 remain turned OFF, in the front end DC level shifter 202. In the full bridge inverter 204, to obtain $+V_{IN1}$ across the load 232, Q_1 222 and Q_3 226 are turned ON, while Q_2 224 and Q_4 228 remain turned OFF. To obtain $-V_{IN1}$ across the load 232, Q_2 224 and Q_4 228 are turned ON, while Q_1 222 and Q_3 226 remain turned OFF. D_2 210 remains turned OFF for both the states ($+V_{IN1}$ across the load 232 and $-V_{IN1}$ across the load 232). V_{IN2} 218 is blocked from appearing at the output by turning OFF S_1 214 and S_2 216.

[00132] Figure 3C shows an equivalent circuit 304 of the multilevel inverter according to various embodiments for $V_0 = +V_{IN2}$. Figure 3D shows an equivalent circuit 306 of the multilevel inverter according to various embodiments for and $V_0 = -V_{IN2}$. According to various embodiments, for normal operation, i.e., to produce a seven level staircase output, an input voltage condition $V_{IN2} > V_{IN1}$ may be provided. For a $V_0 = \pm V_{IN2}$ state, in the frontend DC level shifter 202, when S_1 214 is turned ON, while S_2 216 and S_3 220 remain turned OFF, D_2 210 is forward biased by V_{IN2} 218, and D_1 208 is reverse biased ($V_{IN2} > V_{IN1}$). Under this condition, V_{IN2} 218 is directly connected to the V_{DCbus} 230. In the full bridge inverter 204, to obtain $+V_{IN2}$ across the load 232, Q_1 222 and Q_3 226 are turned ON, while Q_2 224 and Q_4 228 remain turned OFF. To obtain $-V_{IN2}$ across the load 232, Q_2 224 and Q_4 228 are turned ON, while Q_1 222 and Q_3 226 remain turned OFF. Voltage across the capacitor C 212 still remains at V_{IN1}.

[00133] Figure 3E and shows an equivalent circuit 308 of the multilevel inverter according to various embodiments for $V_0 = +(V_{IN1} + V_{IN2})$. Figure 3F shows an equivalent circuit 310 of

the multilevel inverter according to various embodiments for $V_0 = -(V_{IN1} + V_{IN2})$. For a $V_0 = \pm(V_{IN1} + V_{IN2})$ state, the voltage across the capacitor C 212 remains at V_{IN1}. In the frontend DC level shifter 202, when S_1 214 and S_2 216 are turned ON, while S_3 220 remains turned OFF, D_1 208 and D_2 210 are reverse biased. Under this condition, the capacitor C 212 is connected in series to V_{IN2} 218. This connection ensures $V_0 = V_{IN1} + V_{IN2}$. In the full bridge inverter 204, to obtain $+(V_{IN1} + V_{IN2})$ across the load 232, Q_1 222 and Q_3 226 are turned ON, while Q_2 224 and Q_4 228 remain turned OFF. To obtain $-(V_{IN1} + V_{IN2})$ across the load 232, Q_2 224 and Q_4 228 are turned ON, while Q_1 222 and Q_3 226 remain turned OFF.

[00134] Figure 3G shows an equivalent circuit 312 of the multilevel inverter according to various embodiments for generating a zero level after a positive half cycle. Figure 3H shows an equivalent circuit 316 of the multilevel inverter according to various embodiments for generating a zero level after a negative half cycle. For a $V_0 = 0$ state, to obtain zero volt at the output (V_0) 232 after a positive half cycle, only Q_1 222 is turned ON, while all the other switches in the full bridge inverter 204 remain turned OFF, and the body diode D_{Q2} 314 (of the switch Q_2 224) is employed for freewheeling. To obtain zero volt at the output (V_0) 232 after the negative half cycle, only Q_4 224 is turned ON, while all the other switches in the full bridge inverter remain turned OFF, and the body diode D_{Q3} 318 (of the switch Q_3 226) is employed for freewheeling. The switches in the front end DC level shifter 202 remain in their previous states.

[00135] Table 1 shows a summary of the working states logic as described with reference to Figure 3A to Figure 3H for the multilevel inverter according to various embodiments.

S_1	S_2	S_3	Q_1	Q_2	Q_3	Q_4	V_0
1	1	0	1	0	1	0	V_1+V_2
1	0	0	1	0	1	0	V_2
0	0	1	1	0	1	0	V_1
0	0	1	1	0	0	0	0
0	0	1	0	1	0	1	$-V_1$
1	0	0	0	1	0	1	$-V_2$
1	1	0	0	1	0	1	$-(V_1+V_2)$
0	0	1	0	0	0	1	0

Table 1.

[00136] As described above, and as illustrated in Table 1, by turning on different transistors at different instants may result in obtaining different DC levels. In the front–end converter, turning ON only S1 and S2 provides VIN1 + VIN2 at the DC bus, turning ON only S1

provides VIN2 at the DC bus and turning ON only S3 provides VIN1 at the DC bus. As described above, the H-bridge converter (which may include or may consist of four transistors) may provide a bipolar waveform from a unipolar waveform at the DC bus. Figures 3A to 3H and Table 1 explain in detail and show the seven levels, i.e., 0, ±VIN1, ±VIN2 and ±(VIN1 + VIN2). For example, turning ON Q1 and Q3, a positive cycle of AC is obtained at the output. Turning ON, Q2 and Q4, a negative cycle of AC is obtained at the output.

[00137] Figure 4 shows an illustration 400 of a simulation model of a multilevel inverter (for example the multilevel inverter 200 of Figure 2) according to various embodiments. A circuitry 402 for controlling the switches may be provided.

[00138] Figure 5 shows an illustration 500 of an output of the inverter (for example of the simulation model of Figure 4), for example a 50 kHz multilevel (for example seven-level) staircase output voltage).

[00139] Figure 6 shows a nine level inverter 600 according to various embodiments, and based on the seven level circuit of Figure 2, so that the same reference signs may be used, and some reference signs may be omitted for ease of readability of Figure 6. The nine level inverter 600 may employ a voltage doubler 604 (for double the voltage V_{IN1} of the voltage source 206) as one of the voltage inputs to the front end DC level shifter 602. Therefore, the inverter 600 may output $\pm V_{IN1}$, $\pm 2V_{IN1}$ $\pm V_{IN2}$ and $\pm(V_{IN1} + V_{IN2})$. The voltage double 604 may include switches S_1 610 and S_2 612, a diode 606, and a capacitor 608.

[00140] Figure 7 shows a nine level inverter 700 according to various embodiments, and based on the seven level circuit of Figure 2, so that the same reference signs may be used, and some reference signs may be omitted for ease of readability of Figure 7. The nine level inverter 700 may employ a circuit 704 which reduces the input voltage V_{IN1} of the voltage source 206 by half as one of the voltage inputs to the front end DC level shifter 702. This enables the inverter 700 to output $\pm(V_{IN1}/2)$, $\pm V_{IN1}$, $\pm V_{IN2}$ and $\pm(V_{IN1}/2 + V_{IN2})$. The circuit 704 may include switches S_1 712 and S_2 714, a capacitor C 706, and diodes D_1 708 and D_2 710.

[00141] Figure 8 shows an illustration 800 of a switched–capacitor based multilevel inverter (SCMLI) according to various embodiments. The switched–capacitor based multilevel inverter may be based on the seven level circuit of Figure 2, so that the same reference signs may be used, and some reference signs may be omitted for ease of readability of Figure 8. The dotted lines 804 illustrate portions where further circuit elements may be provided for a higher

level inverter based on a basic cell 812 of the switched-capacitor based front end DC level shifter 802 (in which the basic cell 812 (in other words: single unit) corresponds to the switched capacitor based front end DC level shifter 202 of the seven level circuit 200 of Figure 2). For an integer number i independent input voltage sources 806, 808, 810, the number of levels may be $n = 2^{(i+1)} - 1$. Table 2 shows a switching logic for the generalized topology of the SCMLI.

S_1	S_2	S_3	S_4	S_{i+2}	V_{DCbus}
0	0	1	0	1	V_3
0	0	1	0	0	V_2
1	0	0	0	0	V_1
0	0	1	1	0	V_3+V_2
1	0	0	1	0	V_1+V_3
1	1	0	0	0	V_2+V_1
1	1	0	1	0	$V_1+V_2+V_3$

Table 2.

[00142] According to various embodiments, a multilevel converter may be provided with a front end converter which include one voltage sources, two diodes, four transistors and two capacitors for voltage conversion.

[00143] Figure 9 shows a high frequency multilevel inverter (HF MLI) 900 according to various embodiments. The high frequency multilevel inverter (HF MLI) 900 may output a seven level staircase voltage waveform (for example three positive, one zero and three negative voltages). The high frequency multilevel inverter (HF MLI) 900 may include (or consist of) two cascaded stages: a switched capacitor based front end DC to DC converter 902 and a full bridge inverter 904. The switched capacitor based front end DC to DC converter 902 may be a front end switched capacitor DC level shifter, and may include four (switched-capacitor) switches (a first switch G_1 916, a second switch G_2 918, a third switch G_3 920 and fourth switch G_4 922), which may for example be MOSFETs, two diodes (a first diode D_1 908 and a second diode D_2 910), a voltage sources V_{IN} 906, and two capacitors (a first capacitor C_1 *910* and a second capacitor C_2 914). The different DC levels obtained at the V_{DCbus} 924 may include V_{IN}, $2V_{IN}$ *and* $3V_{IN}$. The full bridge inverter 904 may include switches S_1 926, S_2 928, S_3 930, S_4 932, and may produce seven levels of voltages V_0, for example, *0,* $\pm V_{IN}$, $\pm 2V_{IN}$ *and* $\pm 3V_{IN}$, which for example may be output or provided to a load 934. For analysis, it may be assumed that the size of the capacitors 912, 914 is large enough for the voltage ripple to be negligible, and that the switching devices 916, 918, 920, 922, 926, 928, 930, 932 and the input voltage sources 906 are ideal. The working states of the HF MLI 900 will be described in

more detail with reference to Figure 10A to Figure 10H. It will be understood that the numbering of the switches S_i (in other words: the index i in the switch name S_i) in the full bridge inverter 904 shown in Figure 9 may be different from the numbering of the switches Q_i in the full bridge inverter 204 shown in Figure 2; for example, while the first (full bridge inverter) switch is Q_1 in Figure 2 and S_1 in Figure 9 (i.e. same index 1), the second (full bridge inverter) switch is Q_2 in Figure 2 and S_3 in Figure 9 (i.e. different indexes 2 and 3, respectively); likewise, the third (full bridge inverter) switch is Q_3 in Figure 2 and S_4 in Figure 9; and the fourth (full bridge inverter) switch is Q_4 in Figure 2 and S_2 in Figure 9.

[00144] Figure 10A shows an equivalent circuit 1000 of the multilevel inverter according to various embodiments for $V_0 = +V_{IN1}$. Figure 10B shows an equivalent circuit 1002 of the multilevel inverter according to various embodiments for $V_0 = -V_{IN1}$. For the $V_0 = \pm V_{IN}$ state, the capacitor C_1 912 and C_2 914 may be charged to V_{IN} through the diodes D_1 908 and D_2 910, respectively, by turning ON the switches G_2 918 and G_4 922, while the switches G_1 918 and G_3 920 remain turned OFF, in the front end DC level shifter 902. In the full bridge inverter 904, to obtain $+V_{IN1}$ across the load 934, switches S_1 926 and S_4 932 may be turned ON, while switches S_2 928 and S_3 930 remain turned OFF. To obtain $-V_{IN1}$ across the load 934, switches S_2 928 and S_3 930 may be turned ON, while switches S_1 926 and S_4r932 remain turned OFF.

[00145] Figure 10C shows an equivalent circuit 1004 of the multilevel inverter according to various embodiments for $V_0 = +V_{IN2}$. Figure 10D shows an equivalent circuit 1006 of the multilevel inverter according to various embodiments for $V_0 = -V_{IN2}$ respectively. For the $V_0 = \pm 2V_{IN}$ state, in the frontend DC level shifter 902, when the switch G_1 916 is turned ON, while switches G_2 918, G_3 920 and G_4 930 remain turned OFF, diode D_2 910 is forward biased, and diode D_1 908 is reverse biased. Under this condition, the voltage source V_{IN} 906 is in series with capacitor C_1 912 (which is charged to V_{IN}) and is directly connected to the V_{DCbus} 924. In the full bridge inverter 904, to obtain $+2V_{IN}$ across the load 934, switches S_1 926 and S_4 932 may be are turned ON, while switches S_2 928 and S_3 930 remain turned OFF. To obtain $-2V_{IN}$ across the load 934, switches S_2 928 and S_3 930 are turned ON, while switches S_1 926 and S_4 932 remain turned OFF. The voltage across both capacitors 912, 914 may remain at V_{IN}.

[00146] Figure 10E shows an equivalent circuit 1008 of the multilevel inverter according to various embodiments for $V_0 = +3V_{IN1}$. Figure 10F shows an equivalent circuit 1010 of the multilevel inverter according to various embodiments for $V_0 = -3V_{IN1}$. For the $V_0 = \pm 3V_{IN}$ state, a voltage across both capacitors 912, 914 may remain at V_{IN}. In the frontend switched–

capacitor DC level shifter 902, when switches G_1 916 and G_3 920 are turned ON, while switches G_2 918 and G_4 922 remain turned OFF, diodes D_1 908 and D_2 910 may be reverse biased. Under this condition, both the capacitors 912, 914 are connected in series to V_{IN} 906. This connection may provide that $V_{DCbus} = 3V_{IN1}$. In the full bridge inverter 904, to obtain $+3V_{IN}$ across the load 934, switches S_1 926 and S_4 932 may be turned ON, while switches S_2 928 and S_3 930 may remain turned OFF. To obtain $-3V_{IN}$ across the load 934, switches S_2 928 and S_3 930 may be turned ON, while switches S_1 926 and S_4 932 may remain turned OFF.

[00147] Figure 10G shows an equivalent circuit 1012 of the multilevel inverter according to various embodiments for generating the zero level after a positive half cycle. Figure 10H shows an equivalent circuit 1016 of the multilevel inverter according to various embodiments for generating the zero level after a negative half cycle. For the V_0 = '0' state, to obtain zero volt at the output V_0 after the positive half cycle, only the switch S_1 926 may be turned ON, while all the other switches 928, 930, 932 in the full bridge inverter 904 remain turned OFF, and a body diode D_{S3} 1014 associated with the switch S_3 930 is employed for freewheeling. To obtain zero volt at the output V_0 after the negative half cycle, only the switch S_2 928 is turned ON, while all the other switches 926, 930, 932 in the full bridge inverter 904 may remain turned OFF, and a body diode D_{S4} 1018 associated with the switch S_4 932 is employed for freewheeling. The switches 916, 918, 920, 922 in the front end DC level shifter 902 may remain in their previous states.

[00148] Table 3 shows a summary of the working states logic for the multilevel inverter like described with reference to Figure 10A to Figure 10H above.

G_1	G_2	G_3	G_4	S_1	S_2	S_3	S_4	V_0
1	0	1	0	1	0	0	1	$3V_1$
1	0	0	0	1	0	0	1	2V1
0	1	0	1	1	0	0	1	V1
0	1	0	1	1	0	0	0	0
0	1	0	1	0	1	1	0	-V1
1	0	0	0	0	1	1	0	-2V1
1	0	1	0	0	1	1	0	-3V1
0	1	0	1	0	1	0	0	0

Table 3.

[00149] As described above, the voltage levels at the DC bus 924 of the inverter 902 may include V_{IN}, $2V_{IN}$ and $3V_{IN}$. As highlighted in Figures 10A to 10H and Table 3, turning on different transistors 916, 918, 920, 922 at different instants may provide obtaining the mentioned DC levels. In the front–end converter 902, turning ON only G_1 916 and G_2 918

may provide $3V_{IN}$ at the DC bus 924. Turning ON only G_1 916 may provide $2V_{IN}$ at the DC bus 924. Turning ON only G_2 918 and G_4 922 provides V_{IN} at the DC bus 924. Figure 10A to Figure 10H above describe in more detail how seven levels, i.e., *0*, $\pm V_{IN1}$, $\pm 2V_{IN}$ and $\pm 3V_{IN}$., are obtained. Turning ON switch S_1 926 and S_4 932, a positive cycle of AC (for example a sequence of piecewise DC voltages) may be obtained at the output 934. Turning ON switch S_2 928 and S_3 930, a negative cycle of AC may be obtained at the output 934.

[00150] Figure 11 shows an illustration 1100 of a simulation model of a multilevel inverter (for example the multilevel inverter 900 of Figure 9) according to various embodiments. A circuitry 1102 for controlling the switches may be provided.

[00151] Figure 12 shows an illustration 1200 of the states of the switches of the multilevel inverter 900 of Figure 9 (wherein for example Vs1 indicates the state of the switch S_1 926, wherein a higher value (i.e. a line closer to the top of the diagram) indicates an 'on' state, and a lower value (i.e. a line closer to the bottom of the diagram) indicates an 'off' state) in a sub-diagram 1202, and the resulting voltage V_0 in a sub-diagram 1204.

[00152] Figure 13A shows a nine level inverter 1300, which is based on the five level inverter shown in Figure 9 (including the switched capacitor inverter 902 and the full bridge inverter 904), with additional two switches 1308, 1310 (for example transistors), an additional diode 1304, and an additional capacitor 1306. The additional two switches 1308, 1310, the additional diode 1304, and the additional capacitor 1306 may form a (further) voltage doubler 1302, so that the following voltages may be provided to the load 934: *0*, $\pm V_{IN}$, $\pm 2V_{IN}$, $\pm 3V_{IN}$., and $\pm 4V_{IN}$. (in other words: $-4V_{IN}$, $-3V_{IN}$, $-2V_{IN}$., $-V_{IN}$, 0, V_{IN}, $2V_{IN}$, $3V_{IN}$., and $4V_{IN}$).

[00153] Figure 13B shows a multilevel inverter 1310, which includes a plurality of voltage doublers 1302. Like indicated by lines 1312, further voltage doublers may be added.

[00154] Figure 13C shows a multilevel inverter 1314. Like indicated by lines 1316, further voltage doublers may be added.

[00155] It will be understood that in the various front end DC level shifters described herein, one or more voltage sources may or may not be a part of the front end DC level shifter. According to various embodiments, the front end DC level shifter may include one or more voltage sources. According to various embodiments, the front end DC level shifter may be connected to one or more voltage sources.

[00156] The multilevel inverters according to various embodiments may be configured to provide either a high frequency AC output, for example 400 Hz, or 50 kHz, or a low frequency AC output, for example 50 Hz or 60 Hz.

[00157] According to various embodiments, a lower number of switches (for example compared to commonly used inverters) may be used.

[00158] According to various embodiments, different topologies may be provided based on a basic topology (for example based on one of the topologies described above).

[00159] According to various embodiments, a small capacitor size may be sufficient for high frequency applications (or high frequency operation).

[00160] According to various embodiments, an intelligent placement of switches may be provided.

[00161] According to various embodiments, a modular design may be provided which may ensure extension of the topologies (for example extension to a higher number of voltage levels in the multilevel output).

[00162] Various embodiments may solve (in other words: overcome; in other words: eliminate) the need to use excessive devices, power sources and passive components. Various embodiments may eliminate the need to employ bulky inductors.

[00163] Various embodiments may provide a multilevel output which may reduce harmonic content.

[00164] Various embodiments may be applied in aerospace industry, telecommunications industry, lighting industry, and automotive industry.

[00165] It will be understood that a switched capacitor inverter switch is a switch, and that a full bridge inverter switch is a switch, and that the terms 'switched capacitor inverter' switch and 'full bridge inverter' switch are merely used to describe where the respective switch is provided, without necessarily requiring any specific property of the switch.

[00166] It will be understood that the name of a voltage source and the voltage it provides may be denoted with the same reference. For example, 'V' may refer to a voltage source as a

circuit element, and at the same time, 'V' may refer to the voltage that the voltage source 'V' provides.

[00167] According to various embodiments, a switch may be illustrated in the drawings as a transistor and a diode, and may be provided as a transistor and a diode accordingly.

[00168] According to various embodiments, transistors provided in the multilevel inverter may be any controllable switch, such as bipolar junction transistor, IGBT (Insulated-gate bipolar transistor), MOSFET (metal–oxide–semiconductor field-effect transistor) or a relay.

[00169] While exemplary embodiments have been presented in the foregoing detailed description of the invention, it should be appreciated that a vast number of variations exist.

[00170] It should further be appreciated that the exemplary embodiments are only examples, and are not intended to limit the scope, applicability, operation, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing an exemplary embodiment of the invention, it being understood that various changes may be made in the function and arrangement of elements and method of operation described in an exemplary embodiment without departing from the scope of the invention as set forth in the appended claims.

CLAIMS

1. A multilevel inverter comprising:

a switched capacitor inverter configured to output a unipolar sequence of DC voltages; and

a full bridge inverter configured to receive the unipolar sequence of DC voltages and to output a bipolar sequence of DC voltages.

2. The multilevel inverter of claim 1,

wherein the unipolar sequence comprises a periodic sequence.

3. The multilevel inverter of claim 2,

wherein the bipolar sequence comprises a periodic sequence.

4. The multilevel inverter of any one of claims 1 to 3,

wherein the unipolar sequence comprises a rising sub-sequence and a falling sub-sequence.

5. The multilevel inverter of claim 4,

wherein the bipolar sequence comprises a rising sub-sequence and a falling sub-sequence.

6. The multilevel inverter of any one of claims 1 to 5,

wherein the switched capacitor inverter comprises a charge pump.

7. The multilevel inverter of any one of claims 1 to 6,

wherein the switched capacitor inverter is configured to be connected to a single voltage source.

8. The multilevel inverter of any one of claims 1 to 6,

wherein the switched capacitor inverter is configured to be connected to a plurality of voltage sources.

9. The multilevel inverter of any one of claims 1 to 8,

wherein the full bridge inverter is configured to selectively pass through the DC voltages of the unipolar sequence or to negate the DC voltages of the unipolar sequence.

10. The multilevel inverter of any one of claims 1 to 9,

wherein the switched capacitor inverter is configured to be connected to a first voltage source and to a second voltage source; and

wherein the switched capacitor inverter comprises a first switched capacitor inverter switch, a second switched capacitor inverter switch, a third switched capacitor inverter switch, a first diode, a second diode and a capacitor.

11. The multilevel inverter of claim 10,

wherein the first switched capacitor inverter switched capacitor inverter switch is connected to the second voltage source, the second diode, and the second switched capacitor inverter switch;

wherein the second switched capacitor inverter switch is connected to the first switched capacitor inverter switch, the second diode, the capacitor, and the third switched capacitor inverter switch;

wherein the third switched capacitor inverter switch is connected to the first voltage source, the second voltage source, the second switched capacitor inverter switch, the capacitor, and the full bridge inverter;

wherein the first diode is connected to the first voltage source and the second diode;

wherein the second diode is connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the first diode, and the capacitor; and

wherein the capacitor is connected to the second switched capacitor inverter switch, the third switched capacitor inverter switch, the first diode, the second diode, and the full bridge inverter.

12. The multilevel inverter of any one of claims 10 to 11,

wherein the unipolar sequence comprises DC voltages of four different levels corresponding to a zero voltage, a voltage of the first voltage source, a voltage of the second voltage source, and a sum of the voltage of the first voltage source and the voltage of the second voltage source; and

wherein the bipolar sequence comprises DC voltages of seven different levels corresponding to a zero voltage, the voltage of the first voltage source, the voltage of the

second voltage source, the sum of the voltage of the first voltage source and the voltage of the second voltage source, an inverted voltage of the first voltage source, an inverted voltage of the second voltage source, and an inverted sum of the voltage of the first voltage source and the voltage of the second voltage source.

13. The multilevel inverter of any one of claims 10 to 12,

wherein the switched capacitor inverter is configured to output a voltage of the first voltage source to the full bridge inverter if the third switched capacitor inverter switch is in an on state and the first switched capacitor inverter switch and the second switched capacitor inverter switch are in an off state.

14. The multilevel inverter of any one of claims 10 to 13,

wherein the switched capacitor inverter is configured to output a voltage of the second voltage source to the full bridge inverter if the first switched capacitor inverter switch is in an on state and the second switched capacitor inverter switch and the third switched capacitor inverter switch are in an off state.

15. The multilevel inverter of any one of claims 10 to 14,

wherein the switched capacitor inverter is configured to output a voltage corresponding to a sum of the voltage of the first voltage source and the voltage of the second voltage source to the full bridge inverter if the first switched capacitor inverter switch and the second switched capacitor inverter switch are in an on state and the third switched capacitor inverter switch is in an off state.

16. The multilevel inverter of any one of claims 10 to 15,

wherein the switched capacitor inverter comprises a voltage increaser configured to selectively increase a voltage of at least one of the first voltage source or the second voltage source.

17. The multilevel inverter of any one of claims 10 to 16,

wherein the switched capacitor inverter comprises a voltage doubler configured to selectively double a voltage of at least one of the first voltage source or the second voltage source.

18. The multilevel inverter of any one of claims 10 to 17,

wherein the switched capacitor inverter comprises a voltage reducer configured to selectively reduce a voltage of at least one of the first voltage source or the second voltage source.

19. The multilevel inverter of any one of claims 10 to 18,

wherein the switched capacitor inverter comprises a voltage reducer configured to selectively half a voltage of at least one of the first voltage source or the second voltage source.

20. The multilevel inverter of any one of claims 16 to 19,

wherein the unipolar sequence comprises DC voltages of five different levels; and

wherein the bipolar sequence comprises DC voltages of nine different levels.

21. The multilevel inverter of any one of claims 1 to 20,

wherein the switched capacitor inverter is configured to be connected to at least three voltage sources;

wherein the switched capacitor inverter is configured to selectively output voltages corresponding to combinations of voltages of the three voltage sources to the full bridge inverter.

22. The multilevel inverter of any one of claims 10 to 21,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch comprises a relay.

23. The multilevel inverter of any one of claims 10 to 22,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch comprises a transistor.

24. The multilevel inverter of claim 23,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch comprises a bipolar junction transistor.

25. The multilevel inverter of any one of claims 23 to 24,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch comprises an insulated-gate bipolar transistor.

26. The multilevel inverter of any one of claims 23 to 25,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch comprises a metal–oxide–semiconductor field-effect transistor.

27. The multilevel inverter of any one of claims 1 to 9,

wherein the switched capacitor inverter is configured to be connected to a single voltage source; and

wherein the switched capacitor inverter comprises a first switched capacitor inverter switch, a second switched capacitor inverter switch, a third switched capacitor inverter switch, a fourth switched capacitor inverter switch, a first diode, a second diode, a first capacitor, and a second capacitor.

28. The multilevel inverter of claim 27,

wherein the first switched capacitor inverter switch is connected to the voltage source, the first diode, the first capacitor, the second switched capacitor inverter switch, and the fourth switched capacitor inverter switch;

wherein the second switched capacitor inverter switch is connected to the voltage source, to the first switched capacitor inverter switch, to the first capacitor, to the fourth switched capacitor inverter switch, and to the full bridge inverter;

wherein the third switched capacitor inverter switch is connected to the fourth switched capacitor inverter switch, the first diode, the second diode, the first capacitor, and the second capacitor;

wherein the fourth switched capacitor inverter switch is connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, the first capacitor, and the second capacitor;

wherein the first diode is connected to the voltage source, the first switched capacitor inverter switch, the third switched capacitor inverter switch, and the second diode;

wherein the second diode is connected to the third switched capacitor inverter switch, the first diode, the first capacitor, the second capacitor, and the full bridge inverter;

wherein the first capacitor is connected to the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, the fourth switched capacitor inverter switch, the first diode, and the second diode; and

wherein the second capacitor is connected to the third switched capacitor inverter switch, the fourth switched capacitor inverter switch, the second diode, and the full bridge inverter.

29. The multilevel inverter of any one of claims 27 to 28,

wherein the unipolar sequence comprises DC voltages of four different levels corresponding to a zero voltage, a voltage of the voltage source, a doubled voltage of the voltage source, and a tripled voltage of the voltage source; and

wherein the bipolar sequence comprises DC voltages of seven different levels corresponding to a zero voltage, a voltage of the voltage source, a doubled voltage of the voltage source, and a tripled voltage of the voltage source, an inverted voltage of the voltage source, an inverted doubled voltage of the voltage source, and an inverted tripled voltage of the voltage source.

30. The multilevel inverter of any one of claims 27 to 29,

wherein the switched capacitor inverter is configured to output a voltage of the voltage source to the full bridge inverter if the second switched capacitor inverter switch and the fourth switched capacitor inverter switch are in an on state and the first switched capacitor inverter switch and the third switched capacitor inverter switch are in an off state.

31. The multilevel inverter of any one of claims 27 to 30,

wherein the switched capacitor inverter is configured to output a doubled voltage of the voltage source to the full bridge inverter if the first switched capacitor inverter switch is in an on state and the first switched capacitor inverter switch, the second switched capacitor inverter switch, and the third switched capacitor inverter switch are in an off state.

32. The multilevel inverter of any one of claims 27 to 31,

wherein the switched capacitor inverter is configured to output a tripled voltage of the voltage source to the full bridge inverter if the first switched capacitor inverter switch and the

third switched capacitor inverter switch are in an on state and the second switched capacitor inverter switch and the fourth switched capacitor inverter switch are in an off state.

33. The multilevel inverter of any one of claims 27 to 32,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch comprises a relay.

34. The multilevel inverter of any one of claims 27 to 33,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch comprises a transistor.

35. The multilevel inverter of claim 34,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch comprises a bipolar junction transistor.

36. The multilevel inverter of any one of claims 34 to 35,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch comprises an insulated-gate bipolar transistor.

37. The multilevel inverter of any one of claims 34 to 36,

wherein at least one of the first switched capacitor inverter switch, the second switched capacitor inverter switch, the third switched capacitor inverter switch, and the fourth switched capacitor inverter switch comprises a metal–oxide–semiconductor field-effect transistor.

38. The multilevel inverter of any one of claims 1 to 37,

wherein the switched capacitor inverter is configured to be connected to a single voltage source; and

wherein the switched capacitor inverter comprises a plurality of voltage increasers configured to selectively increase a voltage of the voltage source.

39. The multilevel inverter of any one of claims 1 to 38,

wherein the switched capacitor inverter is configured to be connected to a single voltage source; and

wherein the switched capacitor inverter comprises a plurality of voltage doublers configured to selectively double a voltage of the voltage source.

40. The multilevel inverter of any one of claims 1 to 39,

wherein the switched capacitor inverter is configured to be connected to a single voltage source; and

wherein the switched capacitor inverter comprises a plurality of voltage reducers configured to selectively reduce a voltage of the voltage source.

41. The multilevel inverter of any one of claims 1 to 40,

wherein the switched capacitor inverter is configured to be connected to a single voltage source; and

wherein the switched capacitor inverter comprises a plurality of voltage reducers configured to selectively half a voltage of the voltage source.

42. The multilevel inverter of any one of claims 1 to 41,

wherein the full bridge inverter comprises a first full bridge inverter switch, a second full bridge inverter switch, a third full bridge inverter switch, and a fourth full bridge inverter switch.

43. The multilevel inverter of claim 42,

wherein the first full bridge inverter switch is connected to the switched capacitor inverter, the second full bridge inverter switch, the fourth full bridge inverter switch, and an output of the full bridge inverter;

wherein the second full bridge inverter switch is connected to the switched capacitor inverter, the first full bridge inverter switch, the third full bridge inverter switch, and the output;

wherein the third full bridge inverter switch is connected to the switched capacitor inverter, the second full bridge inverter switch, the fourth full bridge inverter switch, and the output; and

wherein the fourth full bridge inverter switch is connected to the switched capacitor inverter, the first full bridge inverter switch, the third full bridge inverter switch, and the output.

44. The multilevel inverter of any one of claims 42 to 43,

wherein the full bridge inverter is configured to output a voltage received from the switched capacitor inverter if the first full bridge inverter switch and the third full bridge inverter switch are in an on state and the second full bridge inverter switch and the fourth full bridge inverter switch are in an off state.

45. The multilevel inverter of any one of claims 42 to 44,

wherein the full bridge inverter is configured to invert a voltage received from the switched capacitor inverter and output the inverted voltage if the second full bridge inverter switch and the fourth full bridge inverter switch are in an on state and the first full bridge inverter switch and the third full bridge inverter switch are in an off state.

46. The multilevel inverter of any one of claims 42 to 45,

wherein the full bridge inverter is configured to output a zero voltage after having output a positive voltage with the first full bridge inverter switch in an on state and the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch in an off state.

47. The multilevel inverter of claim 46,

wherein a body diode associated with the second full bridge inverter switch is configured to provide freewheeling.

48. The multilevel inverter of any one of claims 42 to 47,

wherein the full bridge inverter is configured to output a zero voltage after having output a negative voltage with the fourth full bridge inverter switch in an on state and the first full bridge inverter switch, the second full bridge inverter switch, and the third full bridge inverter switch in an off state.

49. The multilevel inverter of claim 48,

wherein a body diode associated with the fourth full bridge inverter switch is configured to provide freewheeling.

50. The multilevel inverter of any one of claims 42 to 49,

wherein at least one of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch comprises a relay.

51. The multilevel inverter of any one of claims 42 to 50,

wherein at least one of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch comprises a transistor.

52. The multilevel inverter of claim 51,

wherein at least one of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch comprises a bipolar junction transistor.

53. The multilevel inverter of any one of claims 51 to 52,

wherein at least one of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch comprises an insulated-gate bipolar transistor.

54. The multilevel inverter of any one of claims 51 to 52,

wherein at least one of the first full bridge inverter switch, the second full bridge inverter switch, the third full bridge inverter switch, and the fourth full bridge inverter switch comprises a metal–oxide–semiconductor field-effect transistor.

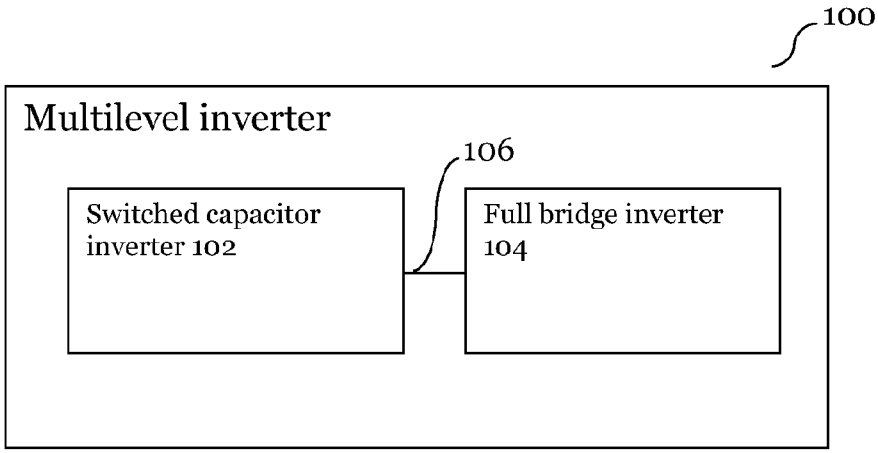


Figure 1

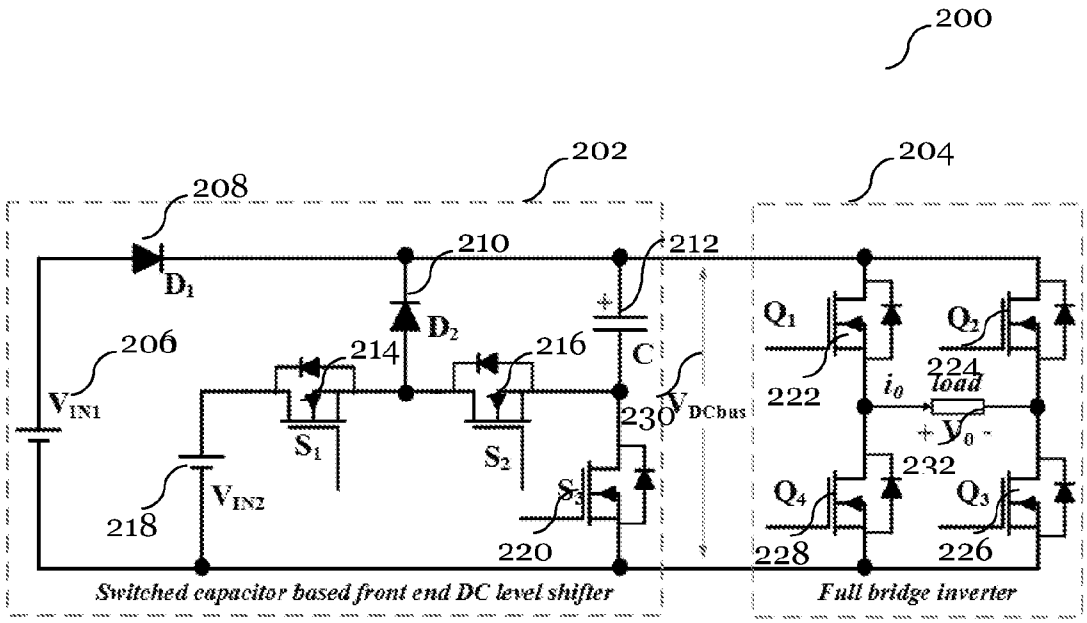


Figure 2

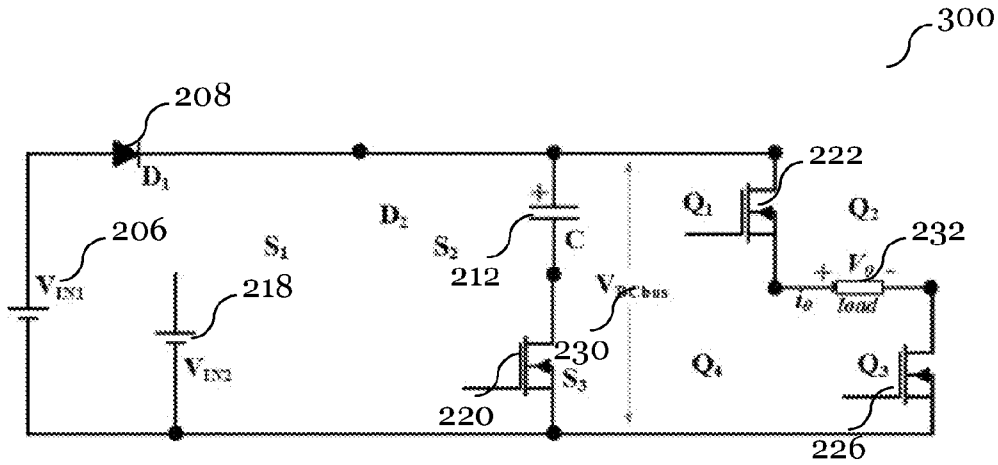


Figure 3A

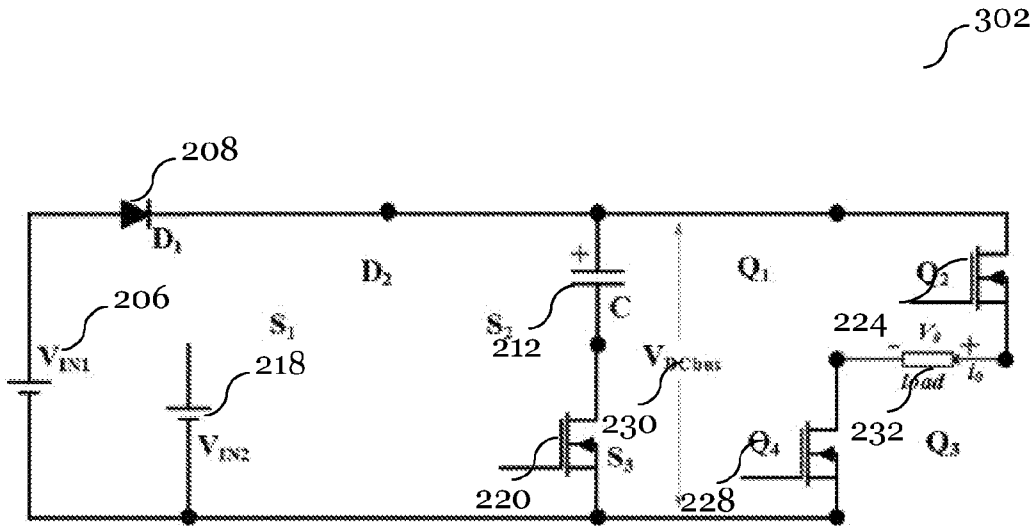


Figure 3B

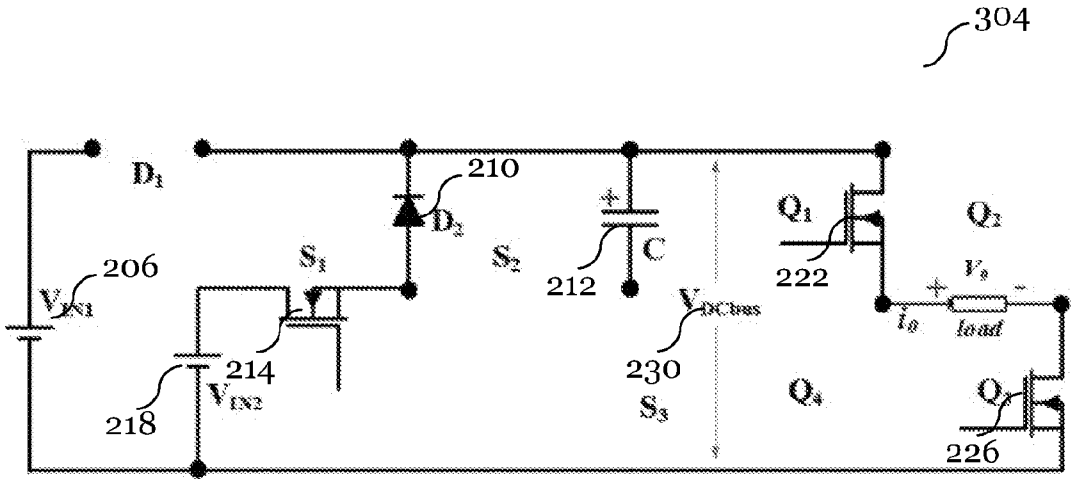


Figure 3C

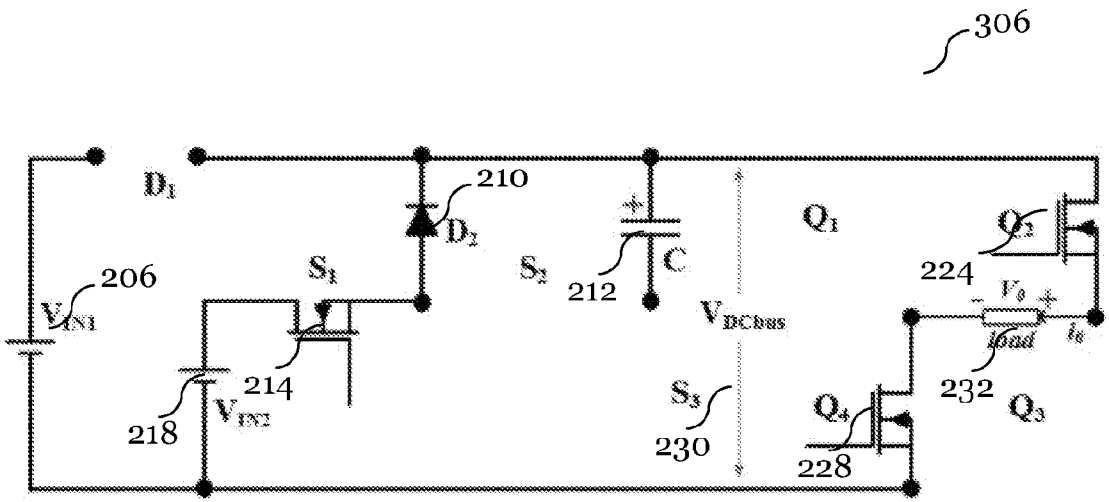


Figure 3D

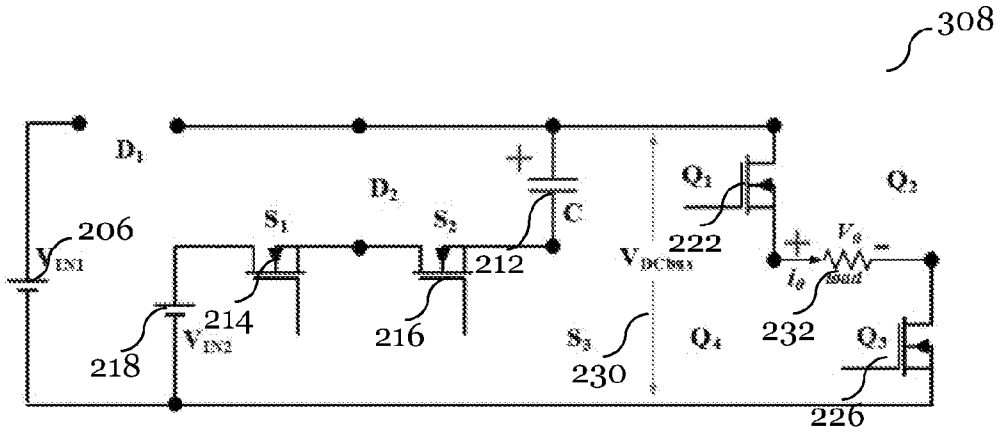


Figure 3E

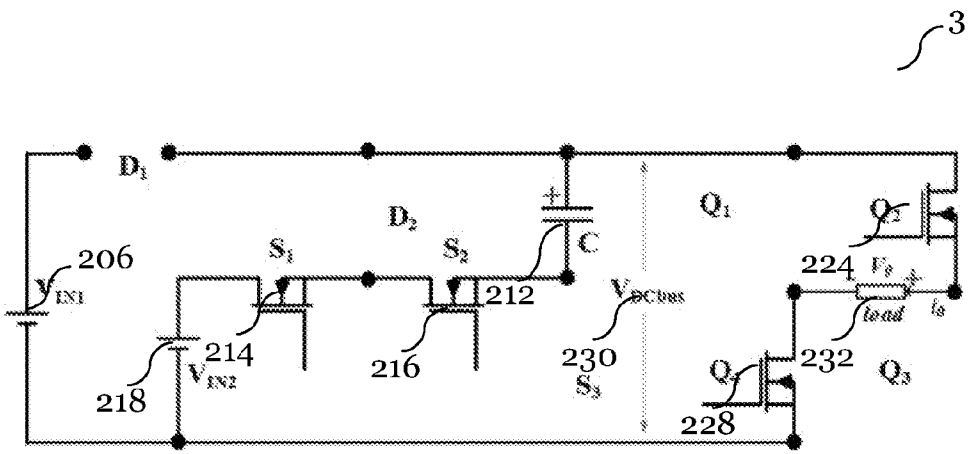


Figure 3F

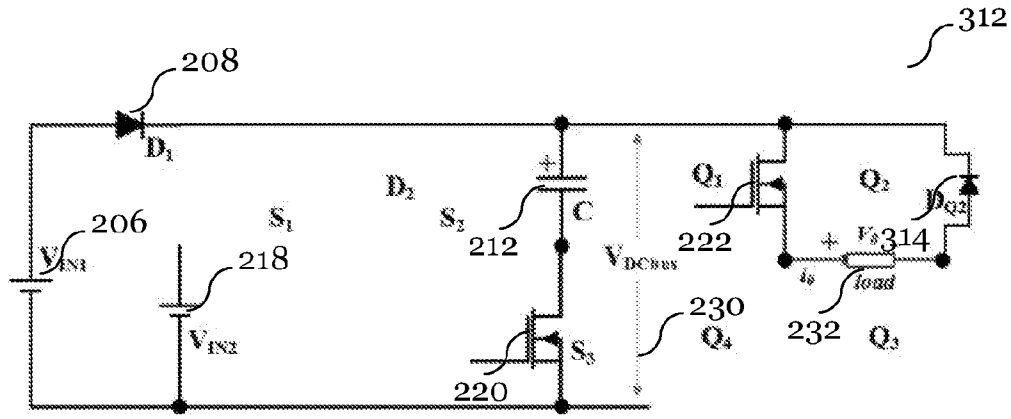


Figure 3G

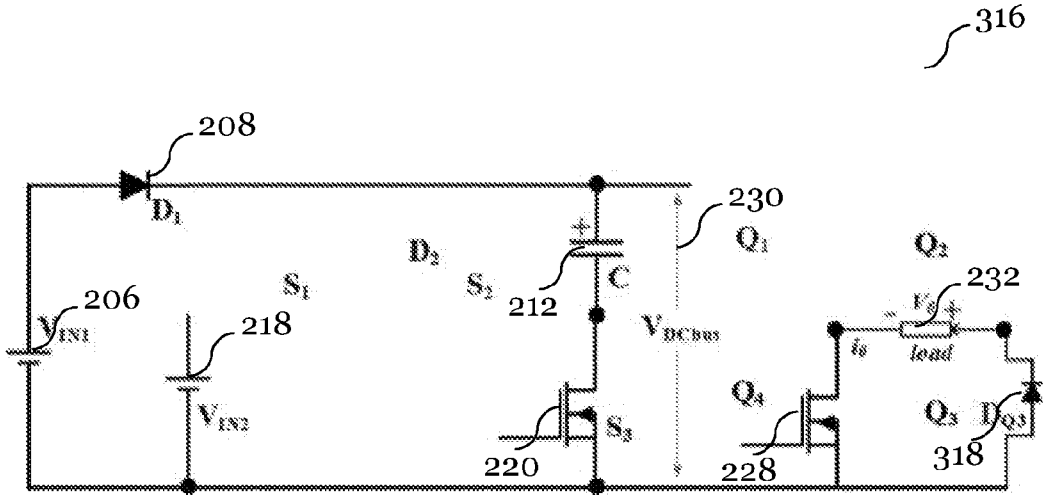


Figure 3H

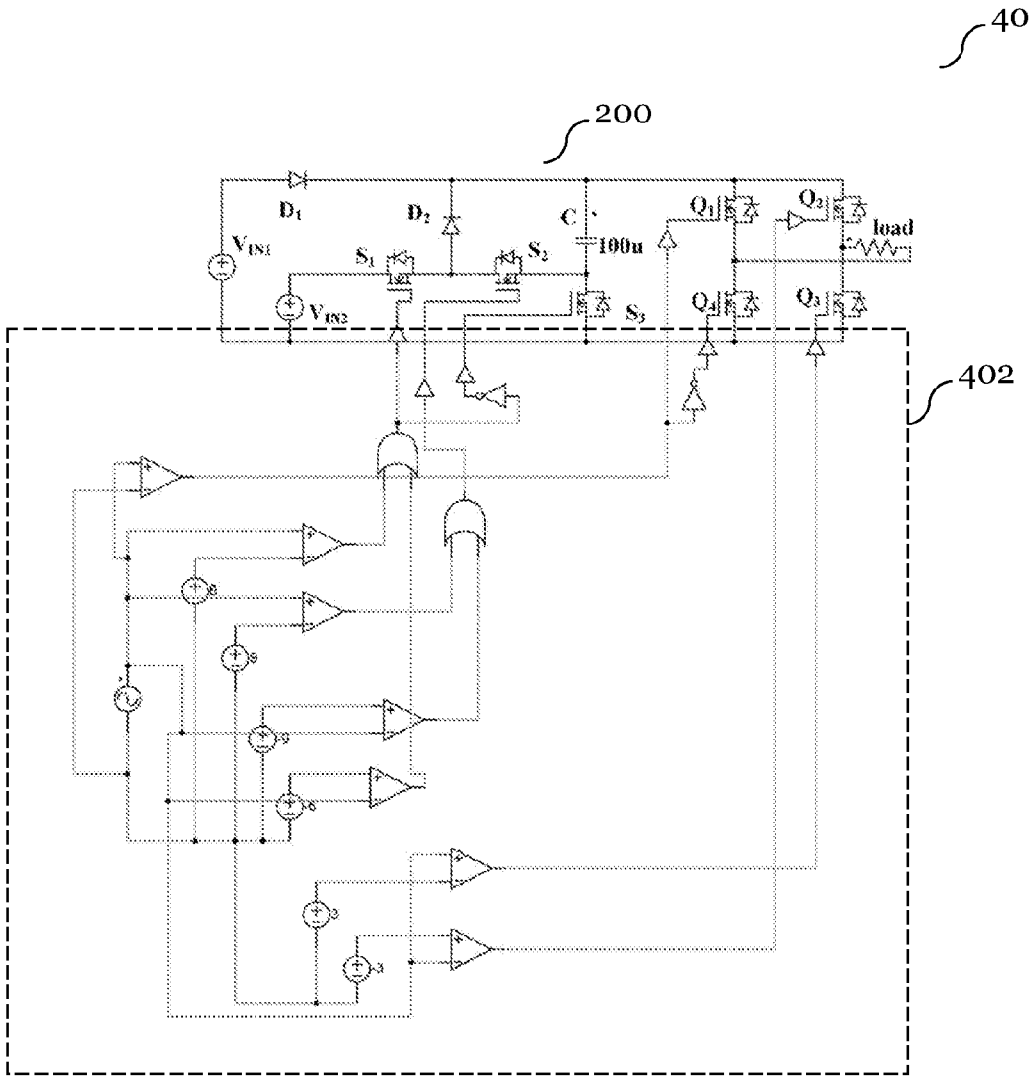


Figure 4

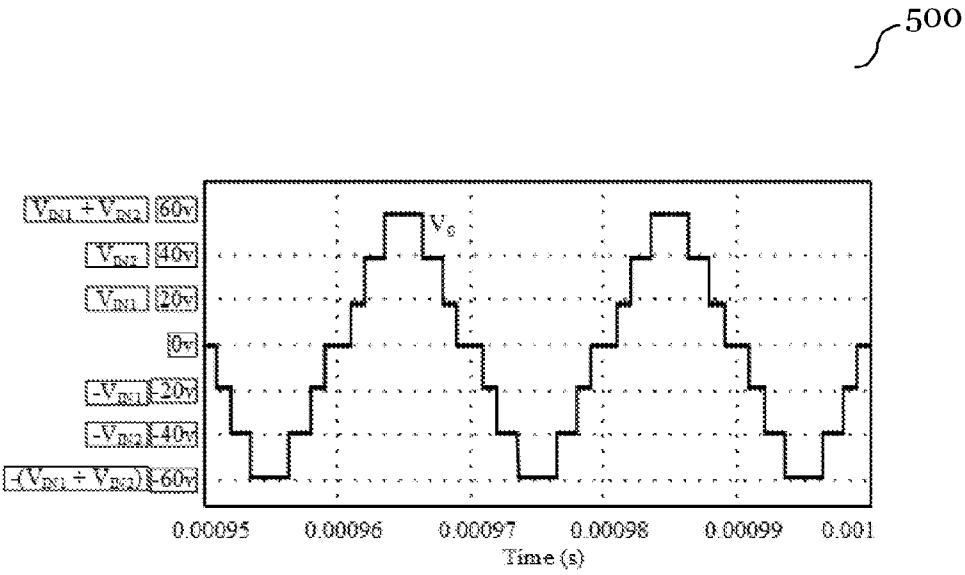


Figure 5

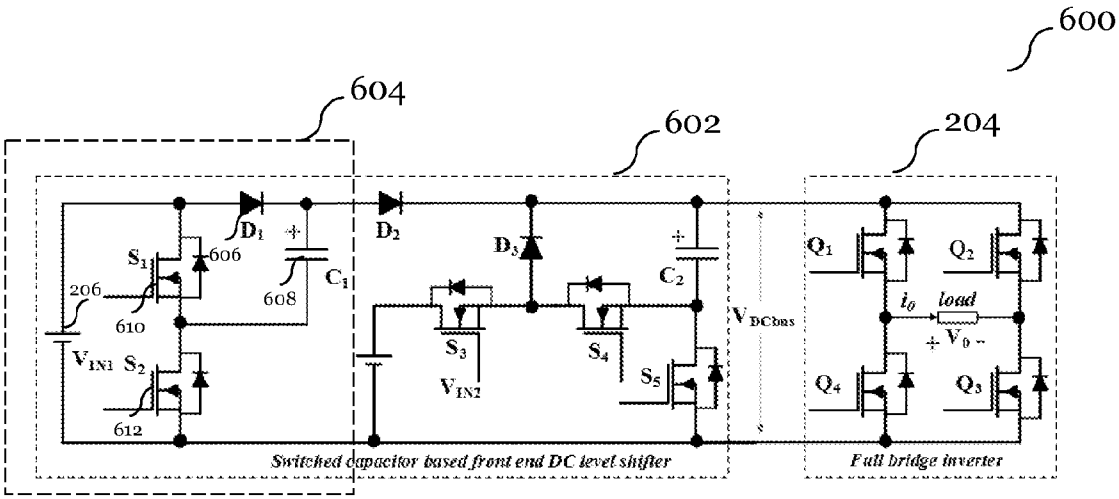


Figure 6

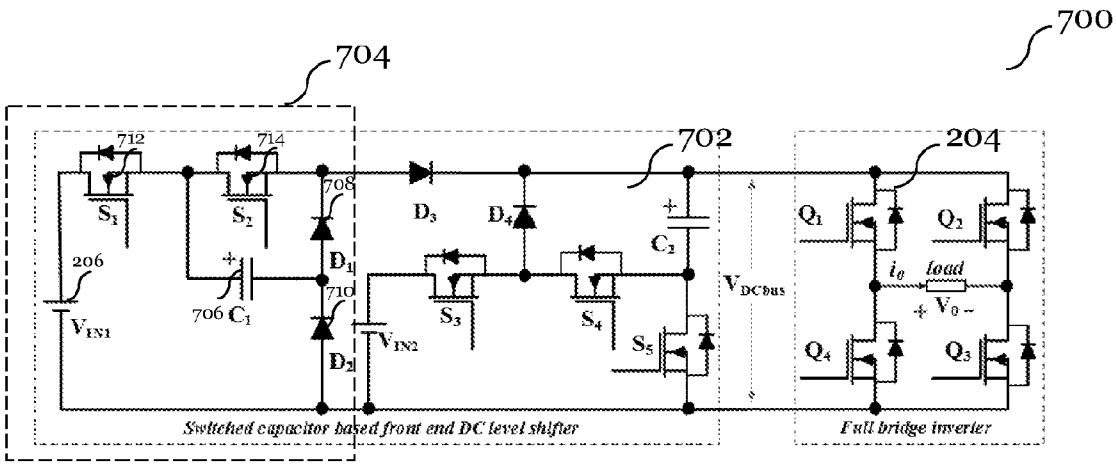


Figure 7

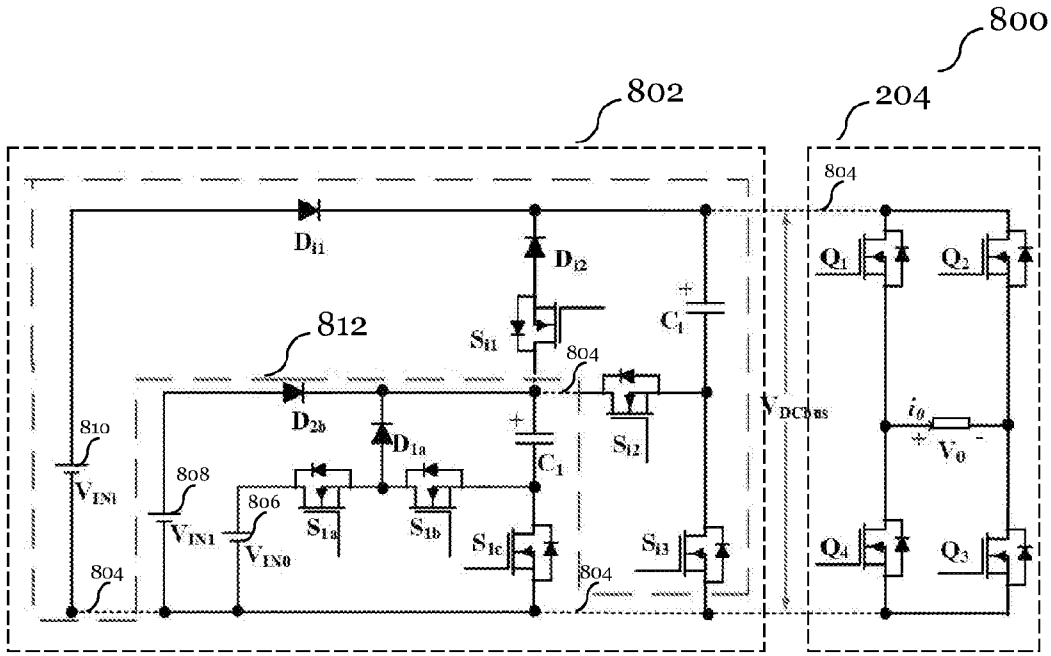
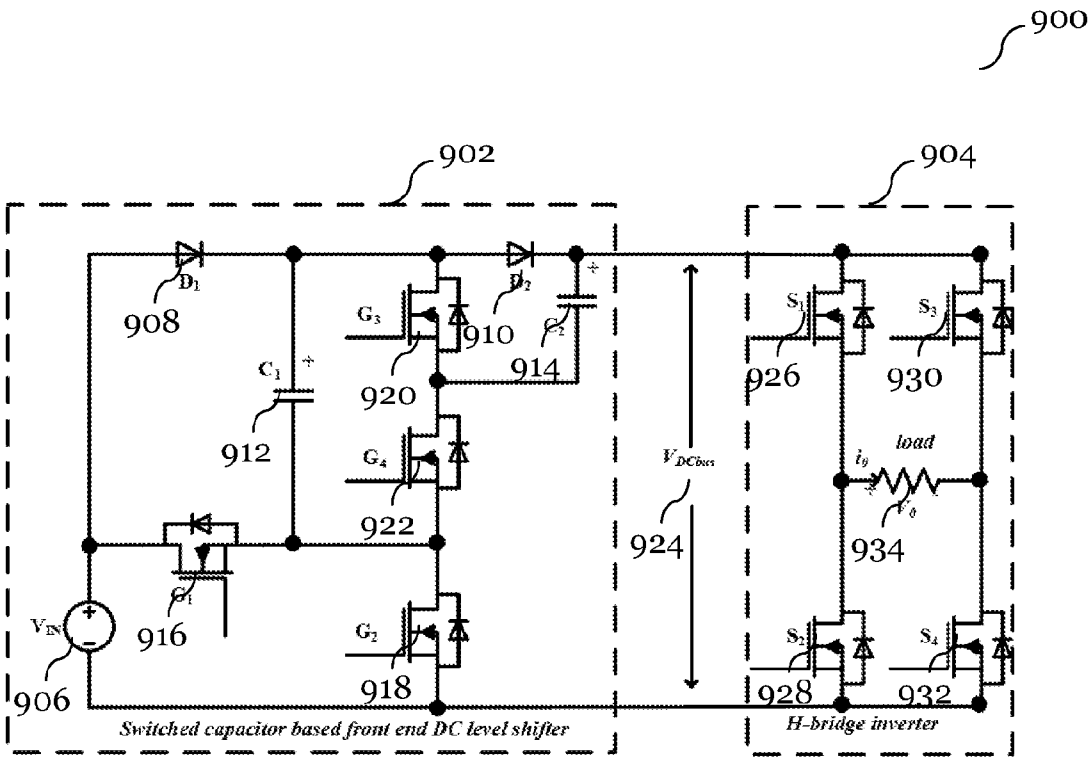


Figure 8


900
902
904
908
910
912
914
916
918
920
922
924
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928
930
932
934
load
Switched capacitor based front end DC level shifter
H-bridge inverter

Figure 9

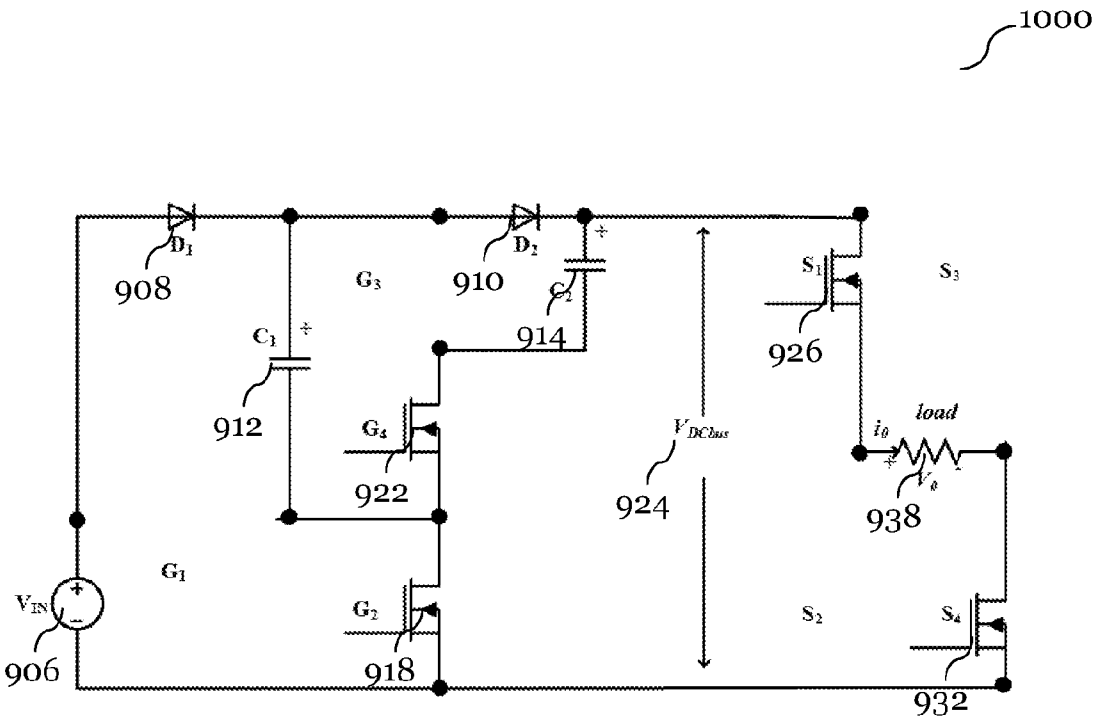
1000
D1
908
G3
D2
910
C2
914
S1
S3
926
C1
912
G4
922
VDCbus
924
load
io
Vo
938
G1
VIN
906
G2
918
S2
S4
932

Figure 10A

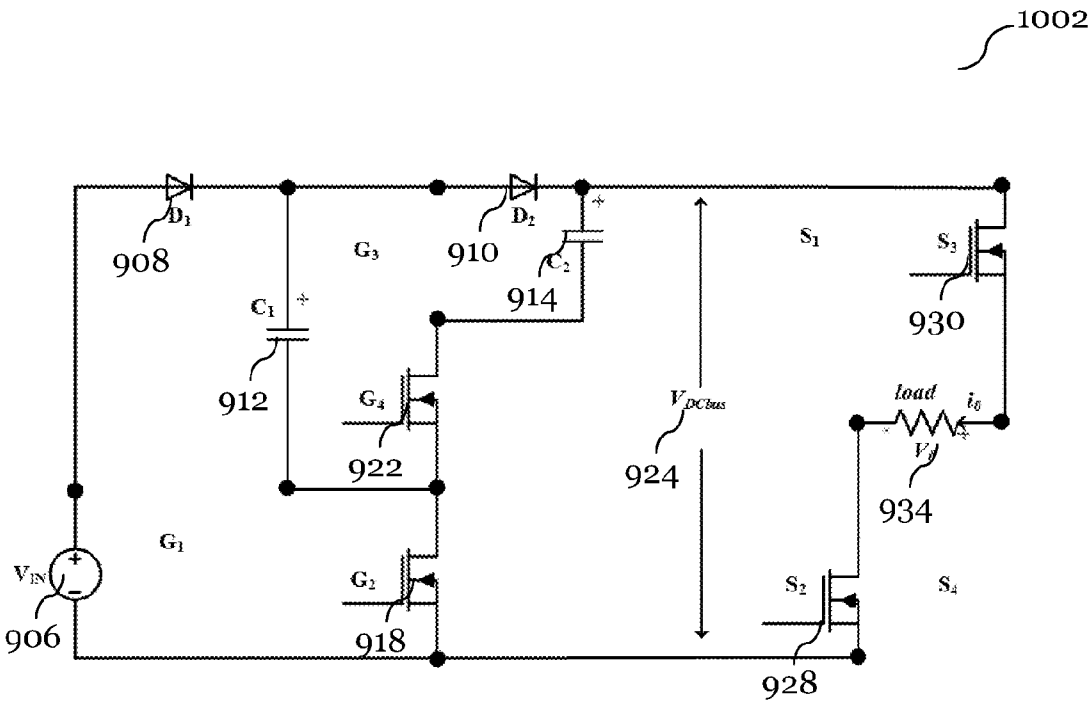
1002
D1
908
D2
910
G3
C2
914
C1
912
S1
S3
930
G4
922
VDCbus
924
load
io
Vo
934
G1
VIN
906
G2
918
S2
S4
928

Figure 10B

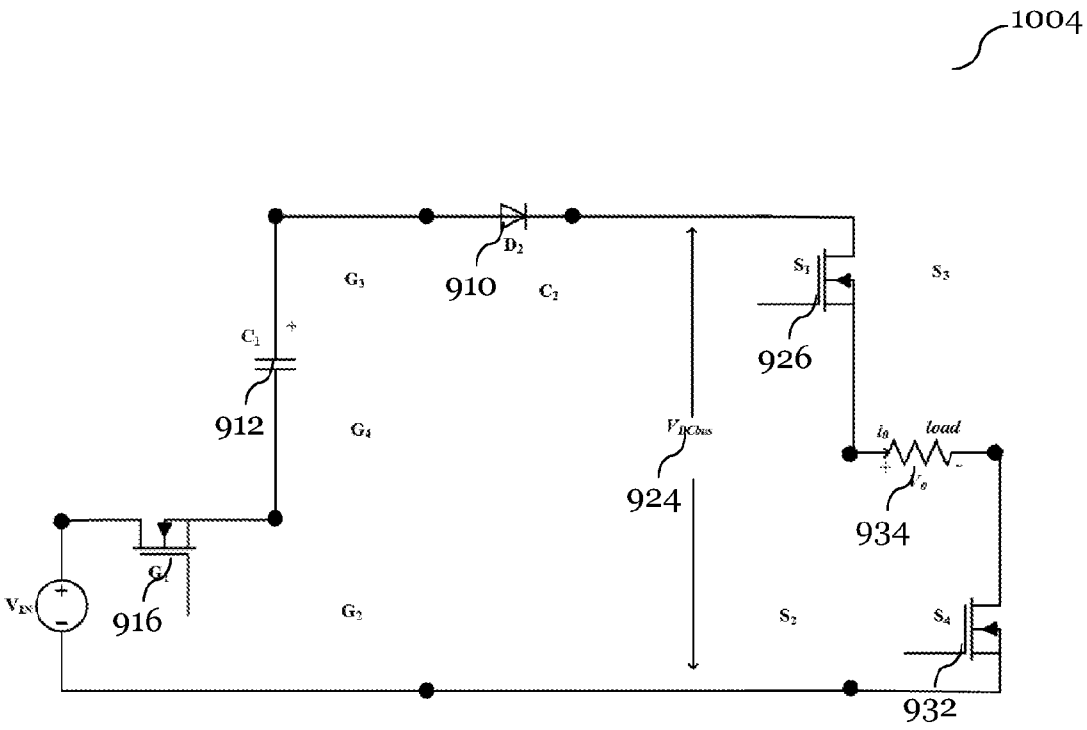
1004
D2
910
G3
C2
S1
S3
C1
912
926
G4
VDCbus
924
io
load
934
G1
916
VIN
G2
S2
S4
932

Figure 10C

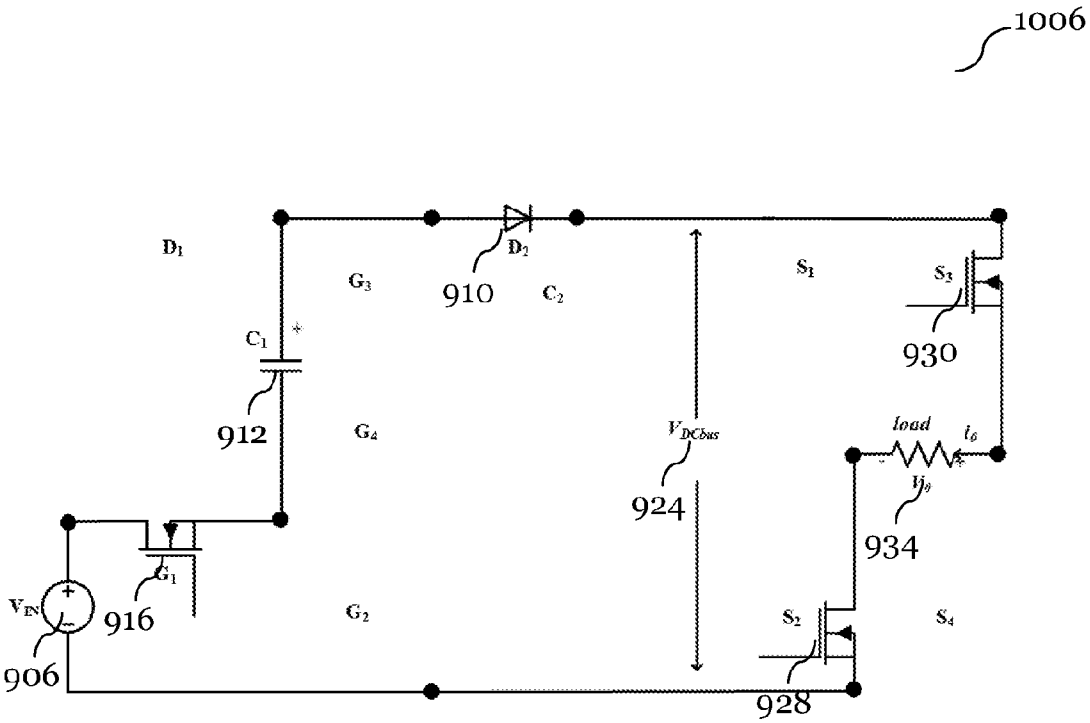
1006
D1
D2
910
G3
C2
S1
S3
930
C1
912
G4
VDCbus
924
load
io
934
G1
VIN
916
906
G2
S2
S4
928

Figure 10D

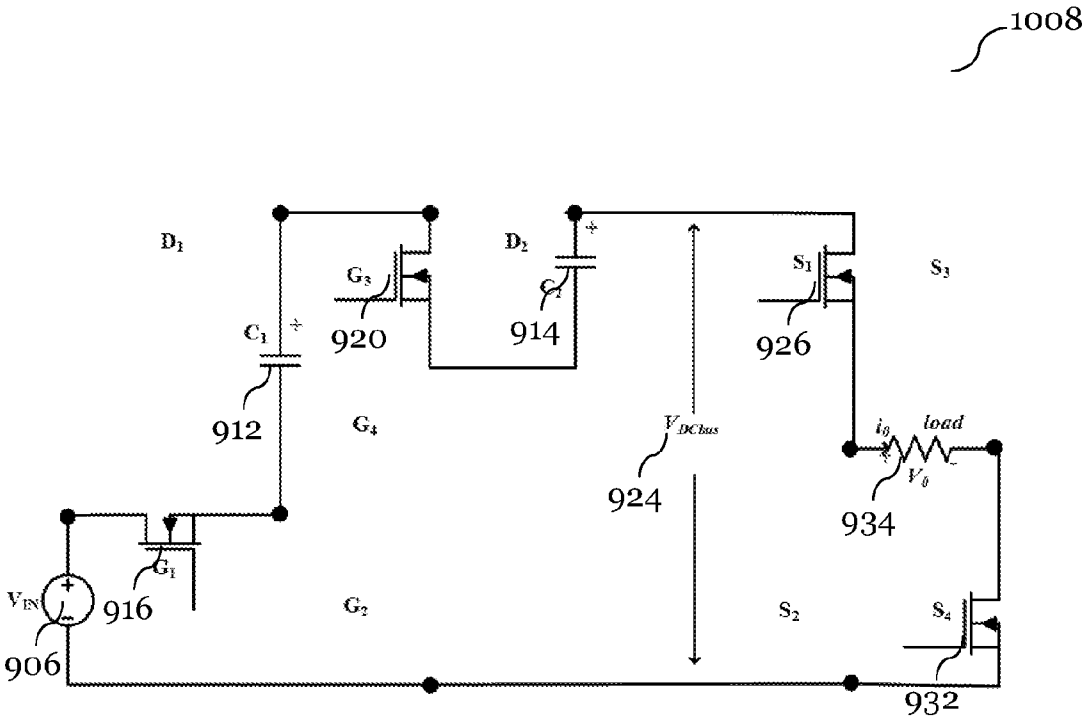
1008
D1
D2
G3
920
914
S1
S3
926
C1
912
G4
VDCbus
924
load
io
Vo
934
VIN
906
G1
916
G2
S2
S4
932

Figure 10E

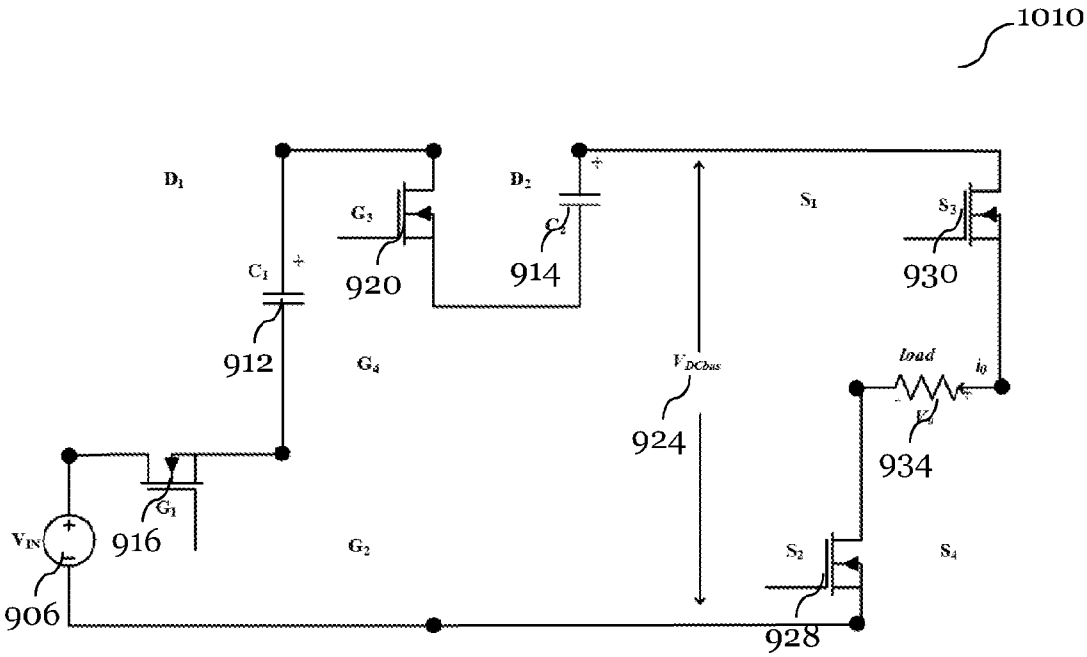
1010
D1
D2
G3
C2
914
S1
S3
930
C1
912
920
G4
VDCbus
924
Load
io
934
VIN
906
G1
916
G2
S2
S4
928

Figure 10F

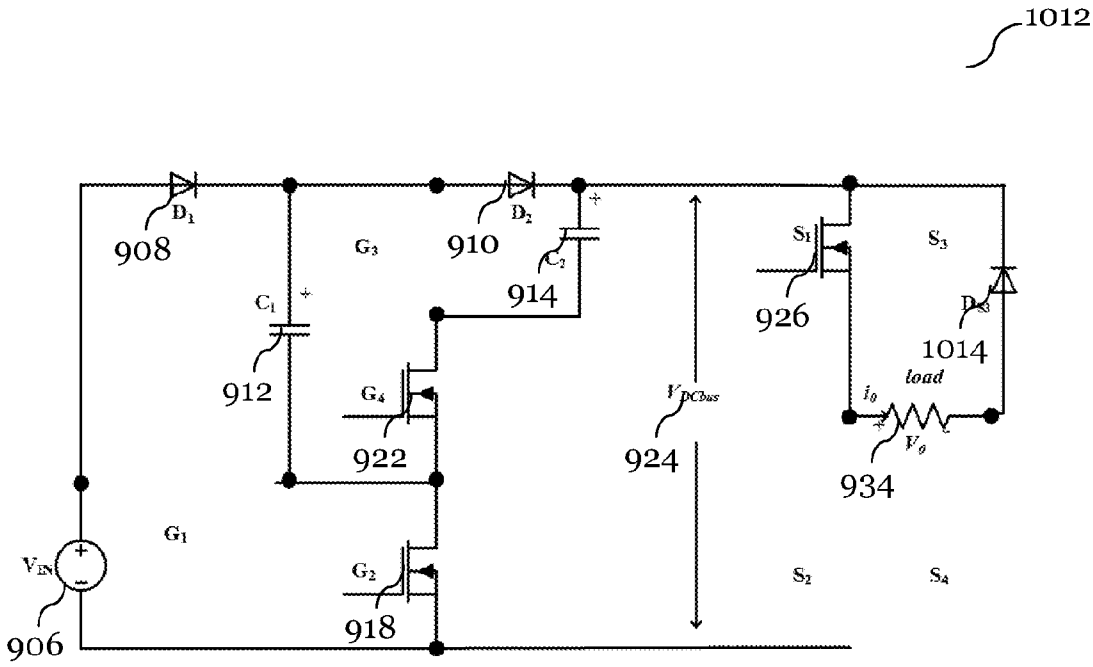
1012
D1
908
G3
D2
910
C2
914
S1
926
S3
1014
load
C1
912
G4
922
VPCbus
924
io
Vo
934
G1
VIN
906
G2
918
S2
S4

Figure 10G

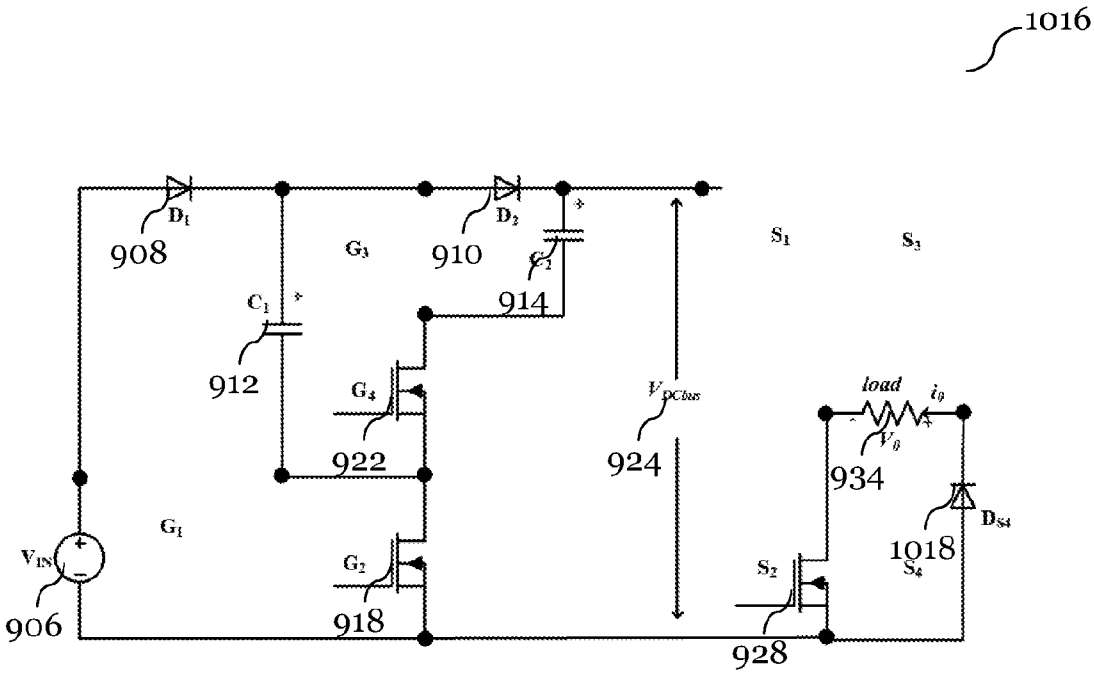
1016
D1
908
G3
D2
910
C2
914
S1
S3
C1
912
G4
922
VDCbus
924
load
io
Vo
934
G1
VIN
906
G2
918
S2
S4
DS4
1018
928

Figure 10H

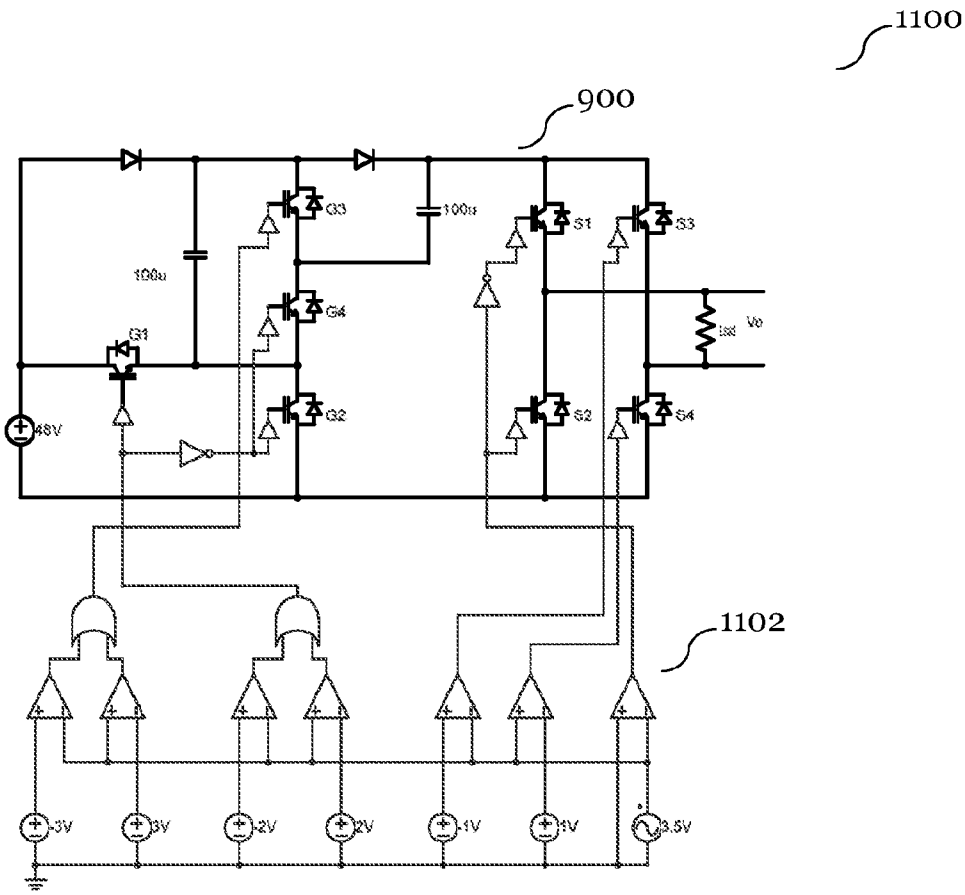
1100
900
G3
100u
S1
S3
100u
G4
Vo
G1
48V
G2
S2
S4
1102
3V
3V
2V
2V
1V
1V
3.5V

Figure 11

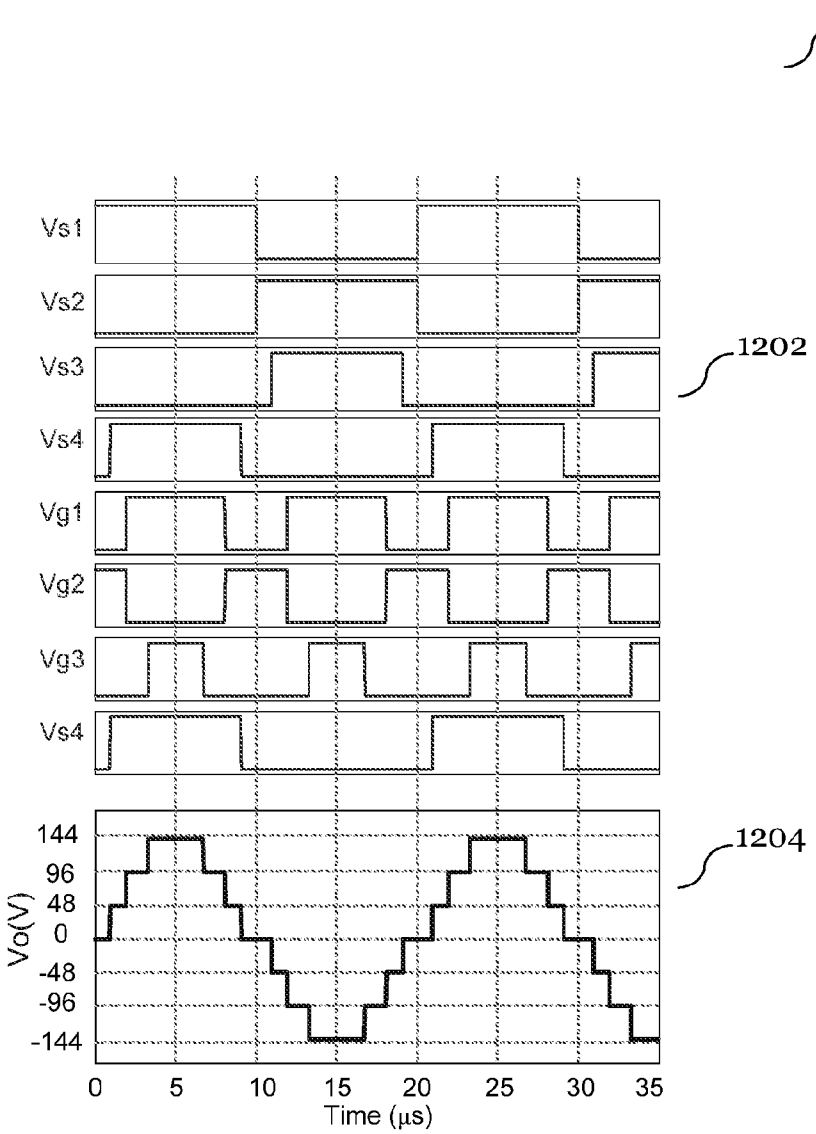
1200
Vs1
Vs2
Vs3
Vs4
Vg1
Vg2
Vg3
Vs4
1202
144
96
48
0
-48
-96
-144
Vo(V)
1204
0
5
10
15
20
25
30
35
Time (μs)

Figure 12

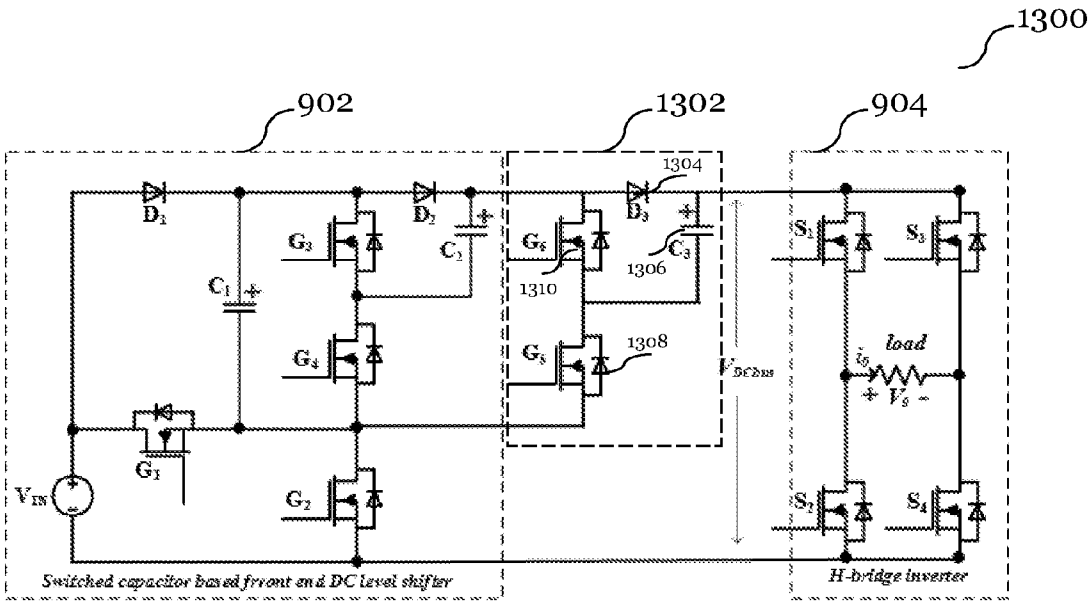

Figure 13A

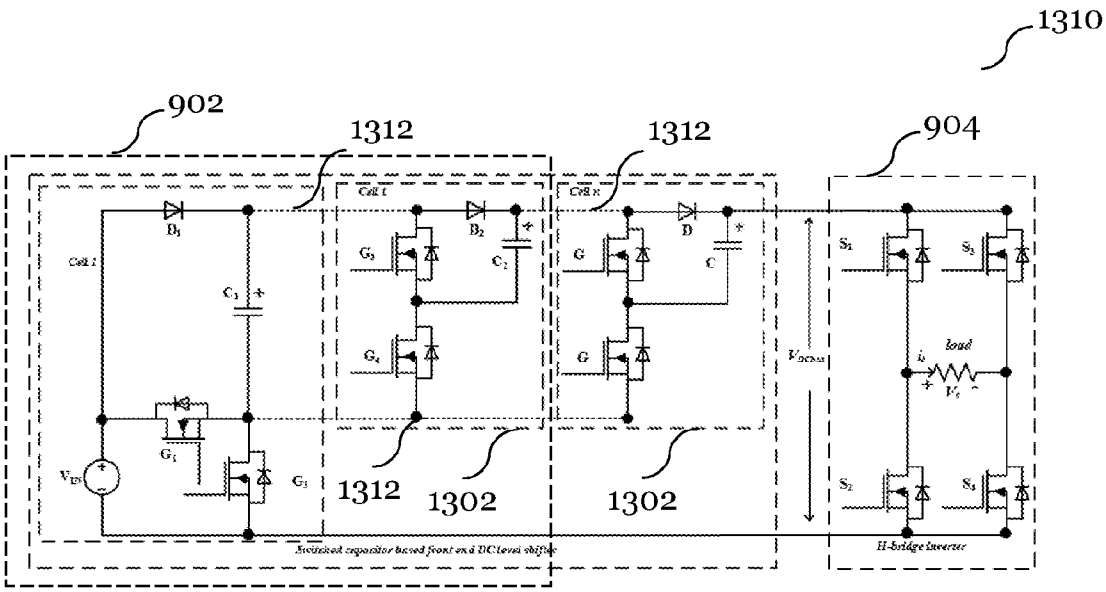

Figure 13B

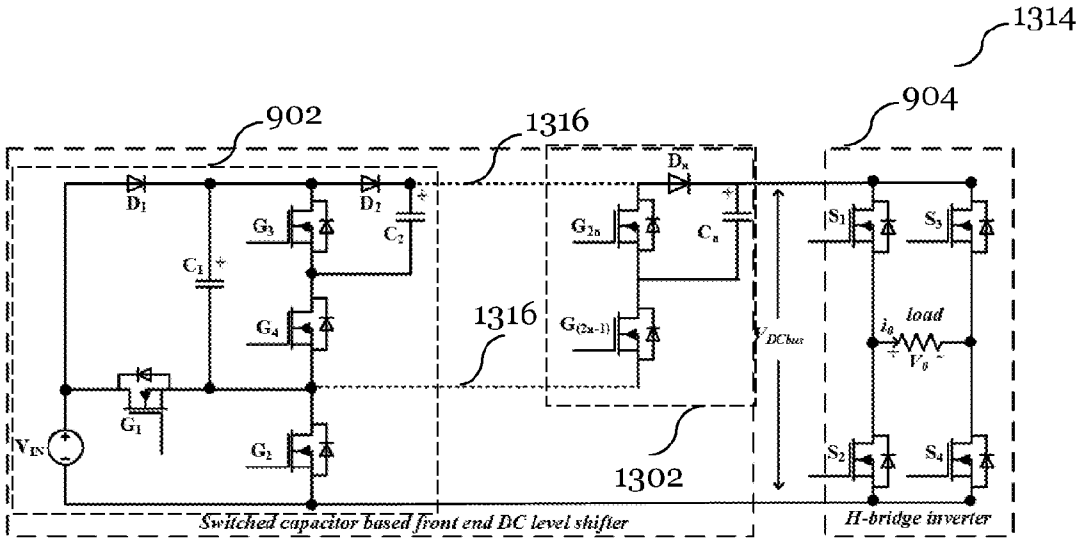
1314
902
1316
904
1316
1302
load
Switched capacitor based front end DC level shifter
H-bridge inverter

Figure 13C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/076559

A. CLASSIFICATION OF SUBJECT MATTER

H02M 7/483(2007.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI, CNPAT, EPODOC, WPI: multi w level, inverter?, switch??, capacit+, DC, direct current, diode, input, double, reduce

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 106301042 A (EAST CHINA JIAOTONG UNIVERSITY) 04 January 2017 (2017-01-04) description, paragraphs[0018]-[0030], figure 1	1, 27, 28, 30, 31, 32, 34, 36, 37, 42-49, 51, 53, 54
X	CN 205160401 U (SOUTH CHINA UNIVERSITY OF TECHNOLOGY) 13 April 2016 (2016-04-13) description, paragraphs[0015]-[0025], figure 1	1-9, 27, 33-37, 42-45, 50-54
A	CN 101262180 A (TSINGHUA UNIVERSITY) 10 September 2008 (2008-09-10) the whole document	1-54
A	CN 103259433 A (NANJING UNIVERSITY OF SCIENCE AND TECHNOLOGY) 21 August 2013 (2013-08-21) the whole document	1-54
A	US 2013221752 A1 (KABUSHIKI KAISHA TOSHIBA) 29 August 2013 (2013-08-29) the whole document	1-54

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 June 2017	**14 June 2017**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**WANG,Xiaohan**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)61648118**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/076559

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015263644 A1 (FUTUREWEI TECHNOLOGIES, INC.) 17 September 2015 (2015-09-17) the whole document	1-54

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/076559

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	106301042	A	04 January 2017	None			
CN	205160401	U	13 April 2016	None			
CN	101262180	A	10 September 2008	CN	101262180	B	14 September 2011
CN	103259433	A	21 August 2013	CN	103259433	B	13 May 2015
US	2013221752	A1	29 August 2013	JP	2013212042	A	10 October 2013
				JP	2016007134	A	14 January 2016
				JP	6030202	B2	24 November 2016
				FR	2987522	A1	30 August 2013
				GB	2499653	A	28 August 2013
				GB	201203281	D0	11 April 2012
				GB	2499653	B	29 January 2014
				FR	2987522	B1	25 November 2016
US	2015263644	A1	17 September 2015	US	9385628	B2	05 July 2016
				WO	2015139570	A1	24 September 2015
				EP	3103189	A1	14 December 2016
				CN	106031010	A	12 October 2016
				EP	3103189	A4	08 March 2017
				JP	2017508433	W	23 March 2017