ABSTRACT

Timekeeping apparatus in which a precision crystal oscillator is used as a frequency reference, the output of which is divided in frequency by a multi-stage binary divider before being converted to effect mechanical movement of a time display, the reference frequency and number of divider stages being chosen to produce a low divider output frequency to allow the display to be advanced with inexpensive mechanical parts. The intermediate stages of the divider chain are tapped to produce output signals for driving an alarm speaker associated with the primary time display.

9 Claims, 6 Drawing Figures
CRYSTAL CONTROLLED MOVEMENT WITH FREQUENCY DIVIDING CIRCUITRY

Clocks and watches produced for the consumer market are subject to a number of constraints in their design and manufacture. They must provide accuracy over long periods of time, require a minimum number of parts, be easily assembled, and be inherently inexpensive. D-C operated clocks and watches additionally require that the power consumption be very low to avoid the expense and inconvenience of charging or replacement of batteries. Electronic watches in particular impose a severe space restriction while requiring a high degree of accuracy and lowest possible battery drain.

Accuracy in an electric clock is primarily dependent upon the accuracy and stability of the oscillator which is employed as a frequency base. However, oscillators running at low clock frequencies, such as one cycle per second, are inherently large, relatively inaccurate and expensive. One known technique for overcoming this problem involves using an electro-mechanical oscillator operating in the 200-500 Hz frequency range with speed reduction gearing to divide down to clock hand speed. But it has been found difficult to convert electronic oscillations into rotary motion at such high oscillator frequencies.

It is the main object of the invention to satisfy numerous design constraints such as those noted above and to overcome the drawbacks and inadequacies of previous clock and watch drives incident to producing an electrical drive signal at a low frequency to achieve economy in the choice of mechanical parts and reducing the speeds at which such parts must move to optimize overall performance.

It is a general object of the present invention to provide a precision electronic timepiece having a high degree of accuracy and stability, on the order of a few parts per million, over long periods of time and over normally encountered temperature variations.

It is another object of the present invention to provide a drive for an electric timepiece which may be powered by a small storage battery, about the size of a small coin, and which is inherently compact for use universally in watches.

A further object of the present invention is the provision of electronic timekeeping apparatus providing an accurate and stable time display while at the same time providing a plurality of synchronized signals at audio frequency for application to peripheral apparatus, especially a time triggered alarm.

Other objects and advantages of the present invention will become evident upon reading the attached detailed description and upon reference to the drawings in which:

FIG. 1 is a perspective view, simplified and partially diagrammatic, of an alarm clock mechanism for use in the present invention;

FIG. 1a shows a "friction" forming a part of the mechanism of FIG. 1;

FIG. 2 is a horizontal section taken through the mechanism of FIG. 1;

FIG. 3 is a schematic diagram, partially in block form, of the circuitry used in the oscillator, shaper and divider portions of the circuit;

FIG. 4 is a schematic diagram of the auxiliary circuitry used in the alarm version of the present invention; and

FIG. 5 shows application of the invention to the driving of a timing train in a watch.

While the invention has been described in connection with the preferred embodiment, it will be understood that I do not intend to be limited to the particular embodiments set forth, but intend, on the contrary, to cover the various alternatives, modifications and equivalents as may be included within the spirit and scope of the invention.

Turning now to the drawings, there is shown in FIGS. 1 and 2 an alarm clock mechanism 20 which may be used in practicing the invention and having a face 21. The first gear in the timing train is a "seconds" wheel 3 which is driven, by means to be described, at the average rate of 1 r. p. m. The seconds wheel 30 has a shaft 31, at the forward end of which is mounted a seconds hand 32. The "seconds" wheel also has a pinion 33 which meshes with a step-down gear 34 having a pinion 35. The pinion is rotatable with respect to the gear and is drivingly coupled to it by means of a friction, illustrated in FIG. 1a, which includes a star wheel 36, which is directly coupled to the pinion 35, and pawls 37, three in number, and each of which is anchored to the gear at 38 so as to bias the tip 39 resiliently inward into engagement with the star wheel.

The result is a detent or "click" type of friction which provides sufficient torque for normal driving but which may be readily overpowered during manual setting of the hands.

Meshing with the pinion 35 is a minute wheel 40 connected to a shaft 41 having a minute hand 42. A further 12:1 reduction is brought about by a pinion 43 on the minute wheel meshing with a step down gear 44 having a pinion 45 driving an hour wheel 50. The latter has a forwardly projecting shaft 51 which amounts the hour hand 52.

For the purpose of triggering the alarm, the hour wheel 50 is slidable axially and has cams 53 formed on the face thereof. Arranged adjacent the hour wheel is an alarm set wheel 60 having a hollow shaft 61 and hand 62 and carrying a corresponding set of cams 63 opposed to the cams 53. When the cams 53, 63 ride up upon one another at a pre-set "alarm" time, the inward axial movement of the hour wheel 50 serves to trigger an alarm (to be described shortly) by closing a pair of switches 70, 71 in the alarm circuitry. A manual alarm control knob 72 is provided, which, when pushed forward, disables the alarm circuitry via a mechanical connection to a pair of switches 73, 74 respectively in series with the switches 70, 71. To change the phase position of the alarm set wheel 60, a setting shaft 65 is provided having a spade lug 66 thereon which, when the shaft 65 is pushed inwardly, engages a slot 67 formed in an alarm set pinion 68 (see FIG. 2). The alarm set pinion rotates the alarm set wheel 60 which repositions the cams 63 and the alarm set hand 62.

For setting the indicated time, the pinion 35 on the reduction gear 34 is provided with a slot 69 which may be engaged by the lug 66 when the shaft 65 is pulled outwardly prior to rotation. Idle clicking occurs at the star wheel 36 so that the gear train leading to the motor remains stationary during setting of the time.

In accordance with the present invention, a crystal controlled oscillator is provided operating at a relatively high super audio frequency on the order of 262, 144 Hz. Also provided are divider stages in the form of flip-
flop devices for dividing the oscillator signal down to a frequency on the order of 1 Hz, and suitable for pulsing a stepping motor or the like for driving of a slow speed wheel in a clock train, with a signal at an audio frequency being tapped from one of the intervening divider stages to be connected to a transducer for sounding the alarm at the pre-set time.

Referring to FIG. 3, there is shown a highly precise and stable pulse source including a crystal oscillator 75 and a pulse shaper 76. The crystal oscillator shown in FIG. 3 is only intended to be illustrative of the high frequency oscillators which may be used to produce the reference pulses and is not claimed to be inventive per se. It includes a single stage comprised of an NPN transistor 78 biased by a pair of base resistors 79, 80 respectively connected to a positive voltage supply terminal 81 and ground 82. The emitter of the transistor 78 is connected to ground through an emitter resistor 84 shunted by a capacitor 85. A dropping resistor 87 connects the collector of the transistor 78 to the positive supply. A form of inductance-capacitance tuning is provided by a resonance circuit 88 connected to the collector of the transistor 78. The resonance circuit includes the quartz crystal C in parallel with a voltage divider consisting of a pair of capacitors 89, 90, the junction between the capacitors being grounded via a line 91. The necessary regenerative feedback is provided by a connection between the resonance circuit 88 and the base of the transistor 78.

In operation, the single stage, acting as a common-emitter amplifier, drives the resonance circuit 88 utilizing the parallel resonance mode of the crystal C. The voltage developed across the capacitor 90 is 180 degrees out of phase with the voltage at the collector of the transistor 78. This out of phase voltage is applied as a feedback signal between the base of the transistor 78 and ground for sustaining oscillation. The oscillating frequency of this circuit is determined by the resonant frequency of the crystal C and the value of the capacitors 89, 90 and preferably is on the order of 262,144 Hz. A more thorough explanation of the operational characteristics of this crystal oscillator can be found in U.S. Army Technical Manual No. 11-690 "Basic Theory and Application of Transistors". A coupling capacitor 94 is provided to block the D-C component of the amplified signal at the collector of the transistor 78 from the output of the oscillator.

For converting the output of the crystal oscillator, which is sinusoidal, into a series of pulses having sharply defined rising and trailing edges, a pulse shaper 76 is provided which includes a pair of transistors 100, 101. A ground reference resistor 102 insures that the output of the oscillator 75 swings symmetrically above and below ground, and an input resistor 103 applies this signal to the transistor 100. The emitter of the transistor 100 is grounded so that the transistor conducts only during the positive half cycles of the oscillator output signal. The amplified signal is fed from the collector of the transistor 100 to the base of the transistor 101 through a coupling resistor 105, while a bias resistor 106 connects the base to the positive supply terminal 81 to insure that the transistor 101 is not rendered conductive by collector-to-base leakage current. A dropping resistor 108 references the collector of the transistor 101 to ground when the transistor is not conducting. In operation, the positive half cycle from the crystal oscillator renders the transistor 100 conductive, drawing a greatly amplified current through the resistor 105 and the base-emitter junction of the transistor 101, which current in turn is amplified in the collector-emitter circuit of the transistor 101 to cause a step rise in the voltage across the resistor 108. A negative half cycle at the oscillator output quickly pulls the first transistor 100 out of conduction, depriv ing the transistor 101 of base current and rendering it non-conductive. The result is an abrupt decrease in the voltage across the resistor 108. The resulting signal at the shaper output is a sharply defined square wave having the same frequency and phase as the output from the crystal oscillator 75.

Crystal-controlled oscillators characteristically have an extremely high Q (narrow band width) and good frequency stability over a given temperature range. In carrying out the present invention a crystal frequency is chosen in excess of 8 kHz and preferably above 100 kHz and less than 300 kHz, with tandem divider stages being utilized to divide the frequency down to a low frequency on the order of 1 Hz. While it has been found that crystals having resonant frequencies as low as 8 kHz will provide the necessary stability when the present invention is used in a clock, it is preferred, for both clocks and watches, to use a crystal frequency of 262,144 Hz, with division by 24 to produce the 1 Hz output signal. To this end, the embodiment of FIG. 3 includes a series of binary division elements FF1–FF18 which can typically take the form of conventional divide-by-two flip-flops. Each of these flip-flops receives an input signal at a clock, or toggle, terminal T and produces output signals at a pair of output terminals Q, Q which are mutually opposite in phase and at one half the frequency of the input signal. The Q output terminal of each flip-flip is connected to the toggle terminal T of the succeeding flip-flop so that, assuming a reference pulse frequency of 262,144 Hz, the eighteen stages of the divider will respectively have outputs at 131,072 – 65,536 – 32,768 – 16,384 – 8,192 – 4,096 – 2,048 – 1,024 – 512 – 256 – 128 – 64 – 32 – 16 – 8 – 4 – 2 and 1 Hz.

For the purpose of utilizing the 1 Hz. square output wave from the final divider stage an amplifier and single stepping type, or ratchet, motor are used, coupled to the "seconds" wheel 30 of the clock train shown in FIGS. 1 and 2. The amplifier indicated at 115 is a high gain NPN stage having an input resistor 116. The motor is in the form of an electromagnet, preferably a solenoid, having a coil 118 and an armature 119 carrying a pawl 120 which acts upon ratchet teeth 121 formed on the periphery of the seconds wheel 30. The ratchet teeth are 60 in number so that the seconds hand 32 is advanced one division on the clock dial for each impulse. A return spring 122 returns the pawl 120 after each power stroke. A keeper pawl 123 prevents retrograde movement.

For illustrating the circuit, the first binary divider stage FF-1 is set forth in schematic form to show a typical dividing flip-flop. This circuit includes a pair of NPN transistor stages 130, 131 with their emitters tied to a common ground terminal 132. The circuitry associated with each of these transistors 130, 131 forms a symmetric configuration. A pair of collector resistors
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134, 135 form the respective loads for the transistors 130, 131. The collector of transistor 130 is coupled to the base of the transistor 131 through a resistor 136 which is shunted by an accelerating capacitor 137. Similarly, the collector of the transistor 131 is connected to the base of the transistor 130 through a resistor 138 and an accelerating capacitor 139.

One skilled in the art will readily appreciate that, in the stable state, one of the transistors 130 or 131 will be saturated while the other transistor is cut-off. Thus, there are two possible stable states, depending upon which transistor is conducting. For switching the circuit from one stable state to the other, there is provided a "steering" network including an input path to the base of the transistor 130 which includes an input resistance 142, a differentiating capacitor 143 and a diode 144 connected in series. Similarly, an input path to the base of the transistor 131 includes an input resistor 146, a differentiating capacitor 147 and a diode 148. The input paths are tied together at the toggle terminal T of the flip-flop FF-1. A blocking diode 150 connects the collector of transistor 130 to the connection between the input resistor 142 and the differentiating capacitor 143 to prevent a positive input pulse applied at the toggle terminal T from reaching the base of the transistor 130 when that transistor is already conducting. Similarly, a blocking diode 151 connects the collector of the transistor 131 to the junction between the input resistor 146 and the differentiating capacitor 147 to block an input pulse from the base of the transistor 131 when that transistor is conducting.

To understand the operation of this circuit, first assume that the transistor 130 is conducting and saturated while transistor 131 is at cut-off. A positive pulse applied at the toggle terminal T causes current to pass through both input resistors 142 and 146. However, the current through resistor 142 is shunted to ground through the diode 150 and the saturated collector-emitter junction of the transistor 130. Since the transistor 131 is originally at cut-off, the voltage at its collector, and at the cathode of diode 151, is high, and the input pulse applied through the resistor 146 passes freely to be differentiated by the capacitor 147 and applied to the base of the transistor 131 through the diode 148, rendering the transistor 131 conductive. As the voltage at the collector of the transistor 131 falls, a corresponding voltage decrease is applied to the base of the transistor 130 through the previously charged accelerating capacitor 139, sharply turning off the transistor 130. As a result, the collector voltage of the transistor 130 rises sharply and is applied to the base of transistor 131 as regenerative feedback through the capacitor 137 and coupling resistor 136. Thus, an abrupt change of state has taken place and the output Q is now effectively at ground voltage. The negative half cycle of the pulse at the toggle terminal T has no effect on the circuit because of the polarity of the diodes 144, 148, 150 and 151. The next positive input pulse is blocked from the now-conducting transistor 131 by the diode 151 while being differentiated by the capacitor 143 to apply a current spike to the base of the transistor 130. The whole process begins over again in the opposite direction from that described previously. The charged capacitor 137 couples the decreasing collector voltage from the transistor 130 to turn off the transistor 131, which, in turn, applies an increasing voltage from the collector of the transistor 131 to the base of the transistor 130 in a regenerative fashion. The circuit abruptly changes states to render the output Q low in voltage and the output Q high in voltage. Thus, it is seen that a positive pulse results at the output terminal Q with every second positive pulse at the toggle terminal T, producing division by two.

In carrying out the present invention, an alarm device is provided in the form of a small transducer, or speaker, energized at the pre-set time by an audio signal from one of the intermediate stages of the binary divider. More specifically, audio signals are taken from two of the divider stages and combined in such a way as to produce a pleasing wake-up sound. To this end, the embodiment shown in FIG. 4 includes an alarm circuit 176, with the crystal oscillator 75 and pulse shaper 76 being shown in block form, and the series of divide-by-two flip-flops FF1–FF18 being represented by the binary divider 171. In this instance, two audio outputs 172, 173 are taken from divider stages FF8 and FF9 respectively, the selected frequencies being preferably 1024 Hz. and 512 Hz., in addition to the regular 1 Hz. output 174. An output speaker 177 has a drive coil 178 forming the load for a single stage transistor amplifier 179. The amplifier 179 includes a PNP transistor 180 having its emitter lead connected to the positive supply terminal 181. A bias resistor 182 and an input resistor 183 are connected to the base of the transistor 180. Any of the audio frequency signals produced by the binary divider may be applied to the amplifier 179 to drive the speaker 177, however, of the frequencies present in this divider arrangement, the 512 and 1024 Hz. signals have been found to produce a most pleasing effect. For control of the alarm means by the clock mechanism there is provided a mechanical switch 185 having a first contact arm 186 inserted in series with the input resistor 183 to the transistor 180 and which is coupled to the hour wheel 50 (FIG. 1) by means of a mechanical connection 187 to make contact at the preset wake-up time.

Further in accordance with the teachings of the present invention, I provide a commutating means for alternately connecting the selected audio frequency signals from the frequency divider to the alarm speaker 177. To this end, the alarm circuit 170 of FIG. 4 includes a commutating relay 190 having an energization coil 191, a normally open contact 192 and a normally closed contact 193. The contacts 192, 193 are respectively inserted in series with the 512 Hz. output 173 and the 1024 Hz. output 172 of the binary divider 171. The energization coil 191 is pulsed intermittently by a transistor 195 responding to a signal applied thereto.

The emitter of the transistor 195 is connected to ground while the collector is connected to the positive supply terminal 181 through the coil 191. An input resistor 196 connects the base of the transistor 195 to an input line 197. Any one of a number of different commutating frequencies are available from the binary divider 171. In this instance, the input line 197 to the commutating circuit is driven from the 1 Hz. divider output 174. A second contact arm 188 of the mechanical switch 185 controls the application of the 1 Hz. signal to the commutator input line 197 and insures that the commutator circuit draws power from the
supply terminal 181 only when the alarm mechanism of the time display is actuated.

When the set time is reached for sounding the alarm, the mechanical connection 187 closes the contact arms 186, 188 of the switch 185. The positive-going pulse from the 1 Hz divider output 174 renders the transistor 195 conductive to energize the relay 190, causing the contact 192 to close and contact 193 to open. A burst of pulses at 512 Hz. will be fed through the now-closed circuit to the alarm amplifier 179, energizing coil 178 and speaker 177 at 512 Hz. One-half second later the 1 Hz. output 174 falls to 0 volts and the transistor 195 is rendered non-conductive. As the relay 190 is de-energized, the contact 192 opens while the contact 193 closes. The 1024 Hz. output 172 is connected to drive the alarm amplifier 179 and to thereby excite the speaker coil 178 and the speaker 177 at 1024 Hz. The commutating action will continue until the alarm is shut off, which may be accomplished by the alarm control knob 72 coupled to switches 73 and 74 in the manner shown in FIG. 1 and 4.

Another feature of the embodiment shown in FIG. 4 is the provision of a three-position switch 205 for selectively applying either a steady 512 Hz. signal, a steady 1024 Hz. signal or the aforementioned commutated signal to the alarm amplifier 179 when the alarm goes off. With this provision the user manually dial his preferred alarm sound.

Since the divider output signals are all in the form of square-wave pulse trains, the signal applied to the speaker 177 will not produce a pure single-frequency tone. A square wave includes many harmonics of the fundamental frequency, and a certain amount of higher frequency components will exist in the output sound from the speaker 177 in addition to the fundamental 512 or 1024 Hz. signal. It has been found that this does not make the sound any less pleasing, but, on the contrary, it seems to add a fullness pleasing to the ears of most listeners. However, if it is desired to eliminate the higher frequency components from the speaker signals, a band pass filter may be inserted somewhere between the binary divider outputs and the speaker coil 178.

One of the primary advantages of utilizing frequency division circuitry in the present invention lies in the adaptability of such circuitry to fabrication in an integrated circuit. In a practiced form of the invention, the crystal oscillator 75, the pulse shaper 76 and the binary divider 171 are all incorporated into a single integrated circuit having output terminals for connecting to ground, a D-C. power source, the clock train drive mechanism, and a suitable reference crystal. One of the benefits of integrating the electrical circuitry is illustrated in FIG. 5, which shows the primary elements of the present invention embodied in a wristwatch. In this form, the electronic time piece consists of a watch housing 210 having a face 211 which is partially cut away to reveal the internal parts arrangement. The electronics portion of the present invention is fabricated into a single integrated circuit 214. D-C. power for the integrated circuit is applied by two small storage batteries 216, 217 connected in series and adapted to supply the circuit via a ground line 218 and a B+ line 219. The frequency reference is provided by a crystal 222 connected to the integrated circuit via a pair of connecting lines 223, 224. The 1 Hz output from the divider section of the integrated circuit is brought out on a terminal 228 and connected to energize a stepping motor indicated generally at 230. For purposes of illustration, the stepping motor 230 set forth here is in the form of a ratchet-wheel-escapement mechanism comprised of a pallet 231 having a pair of pallet pins 232 adapted to cooperate with a series of cam-teeth 234 of a second drive wheel 235. The pallet 231 is pivotable in oscillatory fashion about a pivot pin 237 and is adapted to be controlled through a L-shaped lever arm 238 which cooperates with a stepping solenoid 239. The stepping solenoid 239 is grounded at one end while having its other end connected for energization by the 1 Hz. output 228 of the integrated circuit. The lever arm 238 is biased against the force of the solenoid 239 by a return spring 240. The ratchet wheel 235 will preferably have 60 cam-teeth equally spaced around its periphery so as to properly advance a seconds hand 236 to which it is attached.

As the voltage at the 1 Hz. output terminal 228 of the integrated circuit 214 rises, the solenoid 239 will become energized to advance the seconds hand 236 over a one-half second increment via the camming action of the lower pallet pin 232 on one of the ratchet teeth 234. When the 1 Hz. output 228 falls to a low voltage, the pallet 231 will rotate clockwise under the force of the return spring 240 to advance the seconds hand 236 over another one-half second increment by way of the camming action of the upper pallet pin 232 on another one of the ratchet teeth 234. Therefore, it is seen that the seconds hand 236 is directly advanced by the stepping motor 238, an arrangement which eliminates the need for reduction gearing.

The embodiments of FIGS. 1-3 show only a few of the many possible variations of the present invention. The multiplicity of output signals at different frequencies which are available from the binary divider 171 may be used for driving a number of auxiliary devices which are housed in the same environment as the time display. For instance, if the time display is in the form of an automobile clock, a number of intermediate frequency signals can be tapped from the binary divider 171 to provide reference frequencies for such devices as the turn signals, flasher signals, a speed governor and the automobile horn.

Also within the scope of the present invention is the provision of two or more frequencies from the binary divider 171 to provide a number of different time references for the same time display. For instance, the addition of six more flip-flop stages to the embodiment shown in FIGS. 1 and 2 would provide a signal suitable for driving the “minutes” hand of a time display with a minimum of speed conversion gearing. It has proven economical in many consumer products to use a small motor to drive the time display of a clock, and the divider circuitry of the present invention could provide an alternating drive for such a motor.

It is further within the scope of this invention to use a frequency divider employing interstage feedback so as to achieve non-binary division. One skilled in the art will recognize that any possible integer division factor may be obtained from such a divider. The straight binary division is shown only because it is the most economical to fabricate on a semi-conductor chip.
A reference crystal having a resonant frequency on the order of 266,144 Hz will provide optimum performance with acceptable power drain in most applications. However, when the cost of the binary divider is a factor, it will be advantageous to use a much lower frequency, on the order of 8,192 Hz, as the reference frequency. With this lower reference frequency, a 13-stage binary divider can be used to provide a 1 Hz clock drive as well as suitable audio frequencies such as 512, 1024 Hz, for driving an alarm as in the embodiment of FIG. 3.

A further variation of the present invention is illustrated at the bottom of FIG. 3, where an alternative display drive takeoff 250 is shown as taken from FF 12. The 64 Hz signal available at that point is used to drive a conventional clock drive mechanism illustrated by a synchronous motor 251 coupled to drive a clock train 252. As a practiced example, the motor can be a 15-pole-pair synchronous motor producing a mechanical output at 256 RPM. With speed reduction gearing in the clock train such an arrangement can result in a very high precision movement at the lowest possible cost.

I claim as my invention:
1. An electronic timepiece comprising:
a crystal oscillator for producing pulses at a predetermined super-audible reference frequency,
means including a series of frequency divider stages connected to the oscillator and responsive to said pulses having terminals for producing a drive signal at a super-audible frequency and an alarm signal at an audible frequency,
time display means including a stepping motor and an electro-mechanical transducer, the stepping motor being coupled to the drive signal terminal and the transducer being coupled to the alarm signal terminal,
said time display means having an alarm switch and means for triggering the same at a pre-set time, the switch being effectively interposed between the alarm terminal and the transducer so that an audible alarm is produced at the pre-set time.
2. An electronic timepiece according to claim 1 wherein said time display means includes time indicating elements advanced by said stepping motor and wherein said sub-audible drive signal is at a frequency corresponding to a standard unit of time, said signal being directly coupled to advance an indicating element of said time display means representing said standard unit of time.
3. An electronic timepiece according to claim 2 wherein said drive signal has a frequency of 1 Hz and wherein said directly advanced indicating element is a seconds hand.
4. An electronic timepiece according to claim 1 wherein said crystal oscillator produces pulses at a super-audible reference frequency which is an exact binary multiple of 1 Hz.
5. An electronic timepiece according to claim 1 wherein said reference frequency is at least a binary magnitude above the audio frequency range and wherein said frequency divider stages comprise divide-by-two flip-flops connected in a series chain, each of said flip-flops having a pair of mutually complimentary outputs delivering signals at one half the frequency of the previous flip-flop output.
6. Timekeeping apparatus comprising:
display means including a stepping motor and indicator elements for providing a visual time indication, alarm means operatively associated with said display means and including a signal amplifier and a speaker,
a precision pulse source producing pulses at a super-audible reference frequency which is an exact binary multiple of a unit of time,
a binary division unit responsive to said pulses and operative to divide said reference frequency by a plurality of binary factors for providing a signal at a sub-audible frequency for driving said display means and at least one signal at an audible frequency for driving said alarm means.
7. Timekeeping apparatus according to claim 6 further including commutating means controlling the application of at least two of said audible frequency signals to said alarm means and controlled by one of said signals at a sub-audible frequency, said sub-audible signal effecting connection of said audible range signals in alternating sequence to drive said speaker when said alarm means is actuated.
8. An electronic timepiece comprising in combination
a precision source of pulses including a crystal oscillator operating at a reference frequency of at least 8 kHz,
frequency division means mounted on a semiconductor chip and being responsive to said pulses for providing a plurality of available output signals at frequencies which are sub-multiples of said reference frequency, including a 64 Hz display drive signal, said means including a plurality of binary divider circuits in series,
a multi-pole synchronous motor responsive to said display drive signal, and
time display means driven by said motor and operative to advance at a rate proportional to said reference frequency.
9. An electronic timepiece comprising in combination,
a precision source of pulses including a crystal oscillator operating at a reference frequency of at least 8 kHz,
frequency division means mounted on a semiconductor chip and being responsive to said pulses for providing a plurality of available output signals at frequencies which are sub-multiples of said reference frequency, said reference frequency being an exact binary multiple of 1 cycle per second, and said means including a plurality of binary divider circuits in series,
time display means responsive to at least one of said available output signals and operative to advance at a rate proportional to said reference frequency, and
an alarm means including a speaker and an amplifier, said divided output signals including at least one audio signal coupled to said amplifier for driving said speaker at a predetermined alarm time.
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