Abstract: Stacked die arrangements are implemented using a variety of methods. Using one such method, a first (108) and second (104) die are bonded to a support structure (106) that substantially circumscribes an interface region (114). The interface region includes a material having a pliability that is consistent with the thermal coefficient of expansion of the dies and that is greater than the pliability of support structure (106).
For two-letter codes and other abbreviations, refer to the “Guidance Notes on Codes and Abbreviations” appearing at the beginning of each regular issue of the PCT Gazette.
METHOD AND SYSTEM FOR STACKED DIES

The present invention relates generally to stacked dies and, more particularly, to implementing stacked dies having different thermal characteristics.

Electrical circuit designs require a number of different considerations. In many applications, the physical size of the circuit is critical. For instance, portable devices, such as cellular phones, personal digital assistants (PDAs), gaming devices and music players, require increasingly more functionality in the same or reduced physical form factors. One solution to such portable devices is to use stacked die integrated circuits (ICs). Stacked die ICs provide the benefit of allowing both die to be located within the same IC package without necessitating significant increases in either the footprint or height of the IC.

In certain stacked die ICs, the dies have noticeable differences in their thermal characteristics. For example, dies which exhibit sufficient differences in their dielectric constant (k) also have differences in their thermal coefficient of expansion (TCE). A material with a larger TCE is restricted from expanding by a material with smaller TCE, thereby exerting a force upon the material with smaller TCE to expand more than its TCE predicts. The interconnection between the dies, therefore, is subject to stress due to the different thermal properties. This stress can reduce the useful life of the IC and cause structural failures in the IC due to cracking or otherwise damaging the dies or their interconnection.

Attempts have been made to lessen the thermal stress between the dies using silicon, Teflon® and adhesive films between the dies; however, such methods can be costly, difficult to implement, and still subject to an unsatisfactory level of thermal failures. One such attempt is described in Taiwanese patent number TW504818B to Su, Spencer, et al, issued on February 18, 2003 and entitled "Multi-chip package." This patent teaches using two interposers with an interval between the interposers but leaves room for improvement.

These and other limitations present challenges to the implementation of stacked die ICs.

Various aspects of the present invention are directed to methods and arrangements for implementing in a manner that addresses and overcomes the above-mentioned issues.
Consistent with one example embodiment, the present invention is directed to a stacked die integrated circuit arrangement having a first silicon die that is subject to a first variation in a physical dimension due to a thermal change. The circuit arrangement also contains a second silicon die that is subject to a second variation in the physical dimension due to the thermal change. The variation in a physical dimension produces a force upon the integrated circuit arrangement. In addition, the circuit arrangement includes a support structure bonded to each die and substantially circumscribing an interface region. The interface region contacts a portion of each die and has a pliability factor greater than the support structure. The pliability factor is a function of a difference between the first and second variations in the physical dimension.

Consistent with a further example embodiment, a method for creating a stacked die integrated circuit arrangement having a first and second silicon die is employed. A pliability factor is determined for an interface region as function of a difference between the first and second dies TCE. From the pliability factor, a material is selected for use in the interface region. The first silicon die is bonded to a support structure. The support structure substantially circumscribes the interface region. The second die is bonded to the support structure such that the interface region contacts a portion of each die and the dies are orthogonal to each other.

The above summary of the present invention is not intended to describe each embodiment or every implementation of the present invention. Advantages and attainments, together with a more complete understanding of the invention, will become apparent and appreciated by referring to the following detailed description and claims taken in conjunction with the accompanying drawings.

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 is block diagram depicting a stacked die arrangement, according to an example embodiment of the present invention;

FIG. 2 shows multiple stacked die arrangement creation methods, according to an example embodiment of the present invention; and

FIG. 3 is a diagram illustrating an example method for creating a stacked die arrangement, according to an example embodiment of the present invention.
While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the scope of the invention as defined by the appended claims.

The present invention is believed to be applicable to a variety of integrated circuits and approaches involving stacked die construction. While the present invention is not necessarily limited to such applications, an appreciation of various aspects of the invention is best gained through a discussion of examples in such an environment.

Consistent with an example embodiment of the present invention, a layer of plastic or similar spacing material is applied to a first die. The spacing material is applied such that it substantially circumscribes an interface region. A second die is positioned above the first die such that the spacing material is between the first and second die. The first and second dies are bonded to the spacing material and separated from each other by the spacing material and the interface region. The spacing material provides structural support to the resulting stacked die arrangement.

Another example embodiment of the present invention includes two die each bonded to a layer of spacing material such that the layer of spacing material separates the two die. The layer of spacing material substantially circumscribes an interface region that contains air and extends between the two die. The particular type of spacing material used varies, but may include thermoplastics (plastics that may be repeatedly reformed by melting) or adhesives, such as Teflon®. In a preferred embodiment, the adhesives may be either Hysol® QMI536™ or ABLESTIK™ 2025D. Teflon® is a trademark of the du Pont de Nemours and Company Corporation. The ABLESTIK Logo is a trademark of National Starch and Chemical Company. Hysol and QMI536 are trademarks of the Henkel Corporation.

The spacing material provides structural support and also prevents encapsulant from entering the interface region by substantially circumscribing the interface region. Thus, the spacing material must be of sufficient strength to support the dies and must surround the interface region sufficiently as related to the encapsulant. For instance, the spacing material can be applied to have small pathways into the interface region for an encapsulant that is relatively thin (in terms
of fluidity) when applied to the dies and larger pathways for an encapsulant that is relatively thick. Moreover, the spacing material has enough structural strength to support stress on the dies due to thermal and other forces and is able to maintain the structural support at the temperature at which the encapsulant is applied.

In one embodiment, the interface region consists of the gas present in the atmosphere at the time the dies are bonded to the spacing material. In such an embodiment, the gas allows the dies to expand and contract from a thermal change without excess force exerted upon die. Other materials are also envisioned to be within the interface region. An important characteristic of such a material is the viscosity or pliability of the material. Ideally, the material should have low viscosity or high pliability to minimize the force applied to the dies due to physical changes due to a thermal change. The required viscosity or pliability can be determined by subjecting stacked die arrangements, with different interface materials, to the thermal change and determining the interface materials for which the dies are subject to cracking or similar undesirable issues. The required viscosity or pliability can also be determined as a function of the different TCEs between the dies because the potential stress between the dies is increased as the difference in TCEs is increased.

Turning now to the figures, FIG. 1 shows a block diagram depicting a cross-section of a stacked die arrangement, according to an example embodiment of the present invention. FIG. 1 shows a first die 108, a second die 104, a plastic layer 106, an interface region 114, bond-wires 110, substrate or lead frame 112, and encapsulant 102.

The first and second dies are integrated circuits that typically perform different functions. For example, the first die 108 may be a complementary metal-oxide-semiconductor (CMOS) die having a relatively low dielectric constant, while the second die 104 has relatively high dielectric constant. More specifically, the first die may be a CMOS die using 60nm or 90nm technology with a low dielectric constant. Thus, the dies may have significant differences in their TCE.

Layer 106 is shown between the first and second dies. Layer 106 can be a nonconductive plastic or adhesive material that is positioned near the exterior of the opposing faces of the stacked dies. In this manner, layer 106 creates an interface region 114 between the dies. Typically, this gap contains a gas (e.g., an atmospheric
or other gas mixture); however, other substances that have a low viscosity and are nonconductive can also be contained within the interface region 114.

In one instance, the stacked die arrangement is encased by an encapsulant 102. The encapsulant 102 is generally more rigid than either the layer 106 or the substance within the interface region 114. For this reason, it is preferred that the layer 106 be arranged to prevent the encapsulant 102 from entering the interface region 114 and to reduce the area between the layer 106 and the edge of the dies, as shown by arrow 116. Moreover, the area 116 can be controlled by the application of layer 106 so as to limit coverage of the encapsulant 102 to areas of the dies that are less susceptible to thermal stress.

FIG. 2 shows multiple stacked die arrangement creation methods, according to various example embodiment of the present invention. FIG. 2 depicts spacer materials 204 and 208, dies 202 and 210, and needle 206.

Spacer 204 is a preformed material that is applied to die 202. In one instance, the spacer material is a thermoplastic or adhesive (e.g., B stage epoxy) material. The material is preformed so that it sufficiently holds its shape while being placed upon die 202. In the case of a thermoplastic, the second die is placed upon the thermoplastic after the thermoplastic is placed upon the first die. The thermoplastic is then heated to form a bond between the dies and the thermoplastic. The heat also helps to shape the thermoplastic to better enclose the space between the dies. In the case of an adhesive, the second die is placed upon the adhesive after the adhesive is placed upon the first die. The die arrangement is then cured using heat or other methods to bond the dies to the adhesive.

Alternatively, the spacer material is applied without being preformed. For example, spacer material 208 is shown as being applied to die 210 using needle 206. Needle 206 applies spacer material 208 to enclose a portion of die 210. A second die is then placed on the applied spacer material 208, and the dies are bonded to the spacer material 208.

Using either method discussed above, the dies are separated by the spacer material and a gap having air or low viscosity material enclosed by the spacer material. In addition to enclosing a portion of the dies, the area of the dies that is not enclosed or covered by the spacer material can be minimized to reduce the amount of encapsulant that is located between the dies.
FIG. 3 is a diagram illustrating an example method for creating a stacked die arrangement, according to an example embodiment of the present invention. In particular, FIG. 3 shows a series of steps for creating a stacked die arrangement according to an embodiment of the present invention.

Block 302 depicts the placement of the spacing material on the first die. Different methods of placement may be implemented. For example, the spacing material may be preformed into an enclosed shape, such as a circle, triangle, rectangle, or other shape. Alternatively, the spacing material can be applied to the first die so as to form an enclosed shape using a needle or similar application means.

After applying the spacing material, the material can optionally be bonded to the first die, as shown by block 304. For instance, an adhesive may be bonded using a chemical reaction, heat or pressure. This bonding may be advantageous in maintaining the position and shape of the spacing material prior to and during the placement of the second die. If the bonding shown by block 304 is not implemented or upon completion of the bonding of block 304, the process continues with the next step shown by block 306.

Block 306 represents the placement of the second die. In particular, the second die is placed such that the spacing material is positioned between the first and second dies. Generally, the spacing material has a consistent height relative to the face of the first die. In one instance, the height is near 30um to 50um. Thus, first and second dies are positioned perpendicular to each other and separated by the height of the spacing material.

After placement in block 306, the dies are bonded to the spacing material as depicted in block 308. The bonding may be accomplished a number of ways including using temperature, chemical reactions and pressure. The resulting die stacked arrangement can then optionally be encapsulated as shown by step 310.

The various embodiments described above and shown in the figures are provided by way of illustration only and should not be construed to limit the invention. Based on the above discussion and illustrations, those skilled in the art will readily recognize that various modifications and changes may be made to the present invention without strictly following the exemplary embodiments and applications illustrated and described herein. For instance, applications other than CMOS stacked dies may be amenable to implementation using similar approaches.
Such modifications and changes do not depart from the true scope of the present invention that is set forth in the following claims.
CLAIMS:

1. A stacked die integrated circuit arrangement comprising:
   a first silicon die (108) subject to a first variation in a physical dimension due to a thermal change;
   a second silicon die (104) subject to a second variation in the physical dimension due to the thermal change, the variation in a physical dimension producing a force upon the integrated circuit arrangement; and
   a support structure (106) bonded to each die and substantially circumscribing an interface region (114), the interface region (114) contacting a portion of each die and having a pliability factor that is greater than the support structure (106) and that is a function of a difference between the first and second variations in the physical dimension.

2. The integrated circuit arrangement of claim 1, wherein the support structure (106) is a thermoplastic of about 30 to 50 micrometers thickness between the dies.

3. The integrated circuit arrangement of claim 1, wherein the support structure (106) is a nonconductive adhesive.

4. The integrated circuit arrangement of claim 1, wherein the first die (108) is a complementary metal-oxide-semiconductor having a dielectric constant that is lower than the second die’s dielectric constant and the dies are orthogonal to each other.

5. The integrated circuit arrangement of claim 1, further comprising an encapsulant (102) surrounding the dies and the support structure (106).

6. The integrated circuit arrangement of claim 1, wherein the interface region (114) is mainly comprised of a gas of about 30 to 50 micrometers thickness between the dies.
7. The integrated circuit arrangement of claim 4, wherein the first die (108) is a complementary metal-oxide-semiconductor constructed using less than about 90 nanometers lithography.

8. A method of creating a stacked die integrated circuit arrangement having a first (108) and second (104) silicon die each having a thermal coefficient of expansion, the method comprising:
   determining a pliability factor for an interface region (114) as function of a difference between the first and second dies thermal coefficient of expansion;
   selecting at least one material for use in the interface region (114) in response to the determination;
   bonding the first silicon die (108) to a support structure (106) that substantially circumscribes the interface region (114), the first silicon die (108) subject to a force due to a thermal change; and
   bonding the second silicon die (104) to the support structure (106) such that the interface region (114) contacts both dies and the dies are orthogonal to each other.

9. The method of claim 8, wherein the bonding is accomplished by heat.

10. The method of claim 8, wherein the support structure (106) is a thermoplastic of about 30 to 50 micrometers thickness between the dies.

11. The method of claim 8, wherein the support structure (106) is a preformed plastic structure.

12. The method of claim 10, further comprising placing the support structure (106) on the first silicon die using a needle.
13. The method of claim 8, wherein the support structure (106) is a B stage epoxy of about 30 to 50 micrometers thickness between the dies.

14. The method of claim 8, wherein the bonding of the support structure (106) is arranged to prevent an encapsulant (102) from entering the interface region.