



- (51) International Patent Classification: Not classified
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- (21) International Application Number: PCT/US20 12/032648
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (22) International Filing Date: 6 April 2012 (06.04.2012)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:

61/473,076	7 April 2011 (07.04.2011)	US
61/505,037	6 July 2011 (06.07.2011)	US
61/537,488	21 September 2011 (21.09.2011)	us
13/441,659	6 April 2012 (06.04.2012)	us
13/441,730	6 April 2012 (06.04.2012)	us
- (63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

US	61/473,076 (CON)
Filed on	7 April 2011 (07.04.2011)
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- Published:
 - without international search report and to be republished upon receipt of that report (Rule 48.2(g))

WO 2012/139079 A2

(54) Title: TUNABLE IMPEDANCE SURFACES

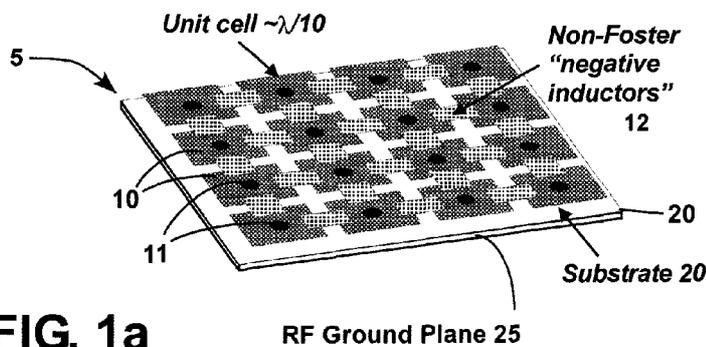


FIG. 1a RF Ground Plane 25

(57) Abstract: A tunable impedance surface, the tunable surface including a plurality of elements disposed in a two dimensional array; and an arrangement of variable negative reactance circuits for controllably varying negative reactance between at least selected ones of adjacent elements in the aforementioned two dimensional array.

Tunable Impedance Surfaces

Cross Reference to Related Applications

[0001] This application claims the benefit of the following US provisional applications: (i) US Provisional Patent Application Serial No. 61/537,488 entitled "Wideband Tunable Impedance Surfaces", filed September 21, 2011; (ii) US Provisional Patent Application Serial No. 61/473,076 entitled "Wideband Adaptable Artificial Impedance Surface", filed April 7, 2011; and (iii) US Provisional Patent Application Serial No. 61/505,037 entitled "Differential Negative Impedance Converters and Inverters with Tunable Conversion Ratios" filed July 6, 2011, all of which are hereby incorporated herein by reference.

[0002] This application is also related to US Patent Application Serial No. 12/768,563 entitled "Non-Foster Impedance Power Amplifier", filed April 27, 2010, the disclosure of which is hereby incorporated herein by reference.

[0003] This application is also related to US Patent Application Serial No. 13/441,730 filed on the same date as this application and entitled "Differential Negative Impedance Converters and Inverters with Tunable Conversion Ratios" (attorney docket 626614-1), the disclosure of which is hereby incorporated herein by reference.

Technical Field

[0004] This disclosure relates to wideband tunable impedance surfaces. Otherwise, this disclosure relates to tunable impedance surfaces having improved bandwidths. The term, "tunable impedance surface" is meant to refer to a class of surfaces called Artificial Impedance Surfaces (AISs), Artificial Magnetic Conductors (AMCs) and Frequency Selective Surfaces (FSSs), and this disclosure relates to the use of circuits with variable negative inductance in order provide not only tunability but also a wider bandwidth than known in the prior art. In the tunable impedance surface, the impedance which a wave sees, either a free-space plane wave or an attached surface wave, is variable and has wider bandwidth performance than traditional passive

artificial impedance surfaces and prior art passive artificial impedance surfaces loaded with varactors. In particular, this disclosure relates to the loading of a traditional passive AIS/AMC/FSS with tunable negative inductors realized with Non-Foster Circuit (NFC) technology.

Background

[0005] Conformal and hidden antennas are desirable on many mobile platforms for reasons of aerodynamics and styling, among others. Such antennas have been implemented as or on Artificial Impedance Surfaces (AIS) and have been associated with Frequency Selective Surfaces (FSS). AIS can also be referred to as Artificial Magnetic Conductors (AMC), particularly when a separate antenna is disposed on it. AMC, AIS and FSS are all well known in the art and look very similar to each other which means that persons skilled in the art have not always maintained bright lines of distinction between these terms. AMC, AIS and FSS are generically referred to as impedance surfaces and if they are tunable, as tunable impedance surfaces herein.

[0006] AIS and AMC tend to have a ground plane which is closely spaced from an array of small, electrically conductive patches. The AIS can serve as an antenna itself whereas an AMC tends to have, in use, a separate antenna disposed on it. Other than the manner of use (and where an antenna is specifically mounted on one), an AIS and a AMC are otherwise basically pretty much identical. The FSS, on the other hand, tends to have no ground plane and therefor it can be opaque (reflective) at certain frequencies and transmissive at other frequencies, much like an optical filter. The FSS look much like a AMC or a AIS, except that there is typically no ground plane. All of these devices (AMC, AIS and FSS) operate at RF frequencies and have many applications at UHF and higher frequencies. Typical prior art AMC, AIS and FSS are either completely passive in nature or utilize varactors (for example) to tune the AMC/AIS/FSS as desired. See, for example:

[0007] B. H. Fong, J. S. Colburn, J. J. Ottusch, J. L. Visher and D. F. Sievenpiper; "Scalar and Tensor Holographic Artificial Impedance Surfaces", *Trans. Antennas and Propag.*, vol. 58, pp. 3212-3221, Oct. 2010, which discusses a passive AIS. The disclosure of this document is hereby incorporated herein by reference.

[0008] J. S. Colburn, A. Lai, D. F. Sievenpiper, A. Bekaryan, B. H. Fong, J. J. Ottusch and P. Tulythan; "Adaptive Artificial Impedance Surface Conformal Antennas", in *Proc. IEEE Antennas and Propagation Society Int. Symp.*, 2009, pp 1-4, which discusses tunable AIS.

[0009] D. Sievenpiper, G. Tangonan, R.Y. Loo, and J.H. Schaffner, US Patent No. 6,483,480 issued November 19, 2002 and entitled "Tunable Impedance Surface".

[0010] D. Sievenpiper, G. Tangonan, R.J. Harvey, R.Y. Loo, and J.H. Schaffner, US Patent No. 6,538,621 issued March 25, 2003 and entitled "Tunable Impedance Surface".

[0011] At VHF and UHF frequencies, however, many relevant platforms which might use AIS/FSS antenna technology are on the order of one wavelength or less in size, which dictates that the antennas be electrically small. Therefore, the performance is limited by the fundamental bandwidth-efficiency tradeoff given by the Chu limit when passive matching is employed.

[0012] A wideband artificial magnetic conductor (AMC), a special case of an AIS, can be realized by loading a passive artificial magnetic conductor structure with NFCs (i.e. negative inductance and negative capacitance) as suggested by D. J. Kern, D. H. Werner and M. J. Wilhelm, "Active Negative Impedance Loaded EBG Structures for the Realization of Ultra-Wideband Artificial Magnetic Conductor", in *Proc. IEEE Antennas and Propagation Society Int. Symp.*, 2003, pp 427-430. Only simulation results were presented in this paper with ideal NFCs; no details are provided of how to realize the stable NFCs needed in such an application.

[0013] NFCs (non-foster circuits) are so named because they violate Foster's reactance theorem and overcome these limitations by canceling the antenna or surface immittance over broad bandwidths with negative inductors or negative capacitors. See the article by Kern mentioned above and also S. E. Sussman-Fort and R. M. Rudish, "Non-Foster impedance matching of electrically-small antennas, *IEEE Trans. Antennas and Propagat.*", vol. 57, no, 8, Aug. 2009. These non-passive reactive elements are synthesized using Negative Impedance Converters (NICs) or Negative Impedance Inverters (Nils). NICs are feedback circuits that convert a passive capacitor to a negative capacitor while Nils are feedback circuits which

convert a passive capacitor to a negative inductor. It is also possible to use passive inductors to make negative capacitors and negative inductors using these circuits, but since a passive capacitor is easier to make using semiconductor fabrication techniques, it is assumed herein that a passive capacitor is preferably used to generate a negative inductance (using a Nil) or a negative capacitance (using a NICO as needed herein).

[0014] The main challenge in realizing NFCs is stability; NICs and Nils are conditionally stable, and the stability margin typically approaches zero as immittance cancellation becomes more complete. For this reason, few stable demonstrations are reported in the literature at and above VHF frequencies. Sussman-Fort and Rudish noted above and K. Song and R. G. Rojas, "Non-Foster impedance matching of electrically small antennas," *Proc. IEEE Ant. Prop. Int. Symp.*, Jul. 2010 have reported negative-capacitance circuits and measured improvement in the realized gain of electrically small monopole antennas.

[0015] A well-known class of AIS consists of printed metallic patterns on an electrically thin, grounded dielectric substrate. They can be used to synthesize narrow-band Artificial Magnetic Conductors (AMC) for the realization of low profile antennas as well as suppress surface waves over a narrow bandwidth. They can be made tunable. See, for example, US Patent 6,538,621 to Sievenpiper et al mentioned above. Furthermore, HRL has shown that they can be used to build directional antennas with arbitrary radiation patterns and direct incident energy around obstacles using conformal surfaces with a holographic patterning technique. See the paper noted above by B. H. Fong, et al. entitled "Scalar and Tensor Holographic Artificial Impedance Surfaces". The main issue with prior art AISs is their useful bandwidth, i.e. the frequency range in which their impedance is maintained near a prescribed value. This invention addresses that issue by increasing the bandwidth of AISs (and thus also synthesized AMCs). The invention can also be used to increase the bandwidth of FSSs.

Brief description

[0016] The present technology can be used to modify prior art AMCs, AISs and FSSs to increase their bandwidths, but it is described primarily with reference to tunable AISs (and AMCs are considered to be a subset of AISs, since an AIS can perform as a AMC when operated

as such). Less description is given a tunable FSS embodiment since there is probably less of a need for a wideband adaptable FSS than a wideband adaptable AIS/AMC. Given the fact that this invention can be used to increase the bandwidth of prior art tunable AMCs, AISs and FSSs, those surfaces are generically referred to as simply tunable impedance surfaces herein.

[0017] In one aspect the present invention provides a tunable impedance surface, the tunable surface comprising: (a) a plurality of elements disposed in a two dimensional array; and (b) an arrangement of variable negative inductance circuits for controllably varying negative inductance between at least selected ones of adjacent elements in said two dimensional array.

Brief Description of the Drawings

[0018] Fig. 1a depicts a passive AIS where the traditional capacitive elements disposed between adjacent conductive patches are replaced by negative inductive loading using a Nil (an active non-Foster circuit) for broadband reactance match.

[0019] Fig. 1b shows a top view of the embodiment in Fig. 1a illustrating the connections between the components; only a few of the patches and Nils are shown for ease of illustration.

[0020] Fig. 1c shows a cut-away perspective view of a section of the embodiment in Fig. 1a.

[0021] Fig. 1d shows the underside of the embodiment of Fig. 1a.

[0022] Fig. 2 is a schematic diagram of the negative inductance integrated circuit, which circuit transforms the load capacitance C_L into a negative inductance at the terminals, and has been implemented as a IC using in the IBM 8HP SiGe process.

[0023] Fig. 3 depicts a $1 \times 1 \text{ mm}^2$ die of the negative-inductance circuit. There are two RF contacts, two power supply contacts, and two control contacts.

[0024] Fig. 4 is a schematic of the equivalent circuit of Figs. 2 and 3.

[0025] Fig. 5 is a plot the equivalent circuit parameters of Fig. 4 as a function of control voltage V_R .

[0026] Fig. 6 is a graph showing the circuit admittance when $V_R = 2.2 \text{ V}$ for both the third IC tested and the simulation.

[0027] Figs. 7 and 8 contain plots of the simulated reflection coefficient for a normal-incidence plane wave off an AIS loaded with a tunable negative inductance circuit.

[0028] Fig. 9 is a design schematic of the negative inductance circuit showing more details than the more simplified schematic of Fig. 2.

Detailed Description

[0029] Non-Foster circuits provide a way to increase the bandwidth of electrically small antennas beyond the Wheeler/Chu limit. See US Patent Application Serial No. 12,768,563 entitled "Non-Foster Impedance Power Amplifier" filed April 27, 2010. In the embodiments disclosed herein, Non-Foster circuits are utilized to create wideband Artificial Impedance Surfaces (AISs) and wideband Frequency Selective Surfaces (FSSs). Non-Foster circuits are named for the fact that they violate Foster's theorem for passive networks, and may have a pure reactance that is a decreasing function of frequency. They enable one to create effective negative capacitors or negative inductors over decade bandwidths. In embodiments according to the principles of the present invention, non-Foster negative inductors are used with an otherwise passive AIS 5 to achieve a wideband impedance surface with a reflection coefficient that varies slowly with frequency, see Fig. 7.

[0030] Comparing Fig. 1a with a prior art tunable AIS/AMC/FSS (see, for example, the Sievenpiper patents noted above), the capacitive elements which were used in the prior art between adjacent conductive patches 10 (which form unit cells in a tunable AIS/AMC/FSS) are replaced with a variable negative inductive load using a Nil 12 in this embodiment. The patches 10 are typically metallic geometric patches having a dimension on each side equal to about one tenth of the frequency of interest (which may be the center of the frequency band of interest).

Without implying a limitation, the patches can have a square shape as indicated in Fig. 1a or they can have some other convenient, repeating geometric shape such as the hexagonal and triangular shapes depicted in US Patent No. 6,538,621 noted above. The particular shape selected for the patches will likely affect the number of tuning elements used between adjacent patches 10. The frequency of interest is (i) the frequency at which antennas (not shown), but which may be mounted on the AIS 5, operate when the AIS 5 functions as a AMC or (ii) the frequency at which the AIS is operated as when it functions as an antenna itself (see the paper by Fong). The patches 10 are mounted on a dielectric surface 20 which generally has an associated RF ground plane 25 and the patches are coupled to the RF ground plane in this embodiment by means of metallic via conductors 11 which couple each patch 10 to the underlying RF ground plane 25. If no RF ground plane 25 is present (and hence via conductors 11 are also not present) then the surface depicted by Fig. 1a would be called a FSS. If the RF ground plane 25 is present but no via conductors 11 are used, then the surface would be called a AIS. If both RF ground plane 25 and the via conductors 11 are present, then the surface is called a AMC. The patches 10 are connected to neighboring patches 10 by means of the Nils 12 (and in some embodiment NICs 12) located between neighboring patches 10 for FSSs, AISs and AMCs. The Nils provide a negative inductance between neighboring patches 10 while NICs can be used in some embodiments to provide a negative capacitance between neighboring patches 10. The NICs (or Nils if used) 12 may be mounted on a single, common surface 20 as depicted by Fig. 1a or in a stacked arrangement on multiple surfaces 20. The preferred embodiment disclosed herein uses Nils 12 and therefore the non-Foster circuits will be referred to as Nils in most of this disclosure, but it should be borne in mind that in some embodiments it will prove useful to substitute NICs for the Nils mentioned herein.

[0031] Fig. 1b illustrates a portion of the embodiment in Fig. 1a in greater detail. Fig. 1b shows that the Nils 12 are themselves preferably mounted on a printed circuit board 16. Only three Nils 12 are depicted in this view of ease of illustration, it being understood that additional Nils 12 would typically be employed laterally between neighboring patches 10 as depicted in the embodiment of Fig. 1a. The printed circuit board 16 comprises conductive traces 22 between thru pins 18 and connection terminals of the Nil 12 for supplying the control signals and voltages

described later. The negative inductance connections of the Nil 12 are connected to patches 10 by conductors 14 which may be solder or a combination of metal patches and solder.

[0032] Only six patches 10 are depicted in Fig. 1b and only sixteen patches 10 are depicted in Fig. 1a for ease of illustration. It should be understood that real life embodiments of this technology are likely to have hundreds or thousands or even more patches 10 and associated Nils 12 disposed on a common substrate 20.

[0033] Fig. 1c illustrates a cut-away perspective view of an embodiment shown in Figs. 1a and 1b. Not all components are shown for ease of illustration (for example, only one of the via conductors 11 used to connect each of the patches 10 to the RF ground plane 25 is shown in this view for ease of illustration). Without implying a limitation and with the understanding alternative embodiments consistent with the principles of the present invention illustrated in Figs. 1a -1d, Fig. 1c shows that the thru pins 18 preferably extend below the dielectric 20 through a layer 30 to make connection to a wiring layer 27 of a printed circuit board 28. The printed circuit board 28 may include the RF ground plane 25 on one of its surfaces and a DC ground plane 29 on the other of its surfaces. The thru pins 18 may be coupled to the RF ground plane 25 via bypass capacitors 26 shown in Fig. 1c, for example, and bypass capacitors 23 may also be used closer to Nil 12 to couple wires 23 to RF ground 25 (via plates 12 and via conductors 11). The layer 30 may comprise a dielectric or other material selected for reasons other than its electrical properties. For example, layer 30 may be electrically conductive with insulating vias provided (but not shown) to allow the thru pins 18 to pass through it without contacting it.

[0034] Fig. 1d shows the wiring layer 27 of the printed circuit board 28 of the embodiment of Fig. 1c and illustrates that the printed circuit board 28 may include conductive traces 31 between the thru pins 18 and the edge of the printed circuit board 28. Moreover, the printed circuit board 28 may also include a DC ground 29 covering all or part of the underside of the printed circuit board 28. If the DC ground 29 covers all of the underside of the printed circuit board 28, then conductive traces 31 are preferably sandwiched in a multi-layered printed

circuit board 28 between the DC ground 29 and the RF ground plane 25. The traces 31 may occur on a common layer or on multiple layers as needed to connect up the Nils 12.

[0035] The Nils 12 are preferably implemented as Integrated Circuits (ICs) which are disposed on the surface 20 of Fig. 1a as described above using the aforementioned printed circuit boards 16. Fig. 2 is a schematic diagram of a preferred embodiment of a negative inductance integrated circuit, which circuit transforms the load capacitance C_L into a negative inductance at the terminals Y_{NII} . Terminals Y_{NII} of each Nil 12 are connected to the neighboring conductive patches 10 shown in Fig. 1a by means of conductors 12. The core of the negative-inductance IC 12 is preferably a differential Nil (see Fig. 2), which preferably comprises two cross-coupled differential pairs of NPN transistors in this embodiment thereof. The Nil transforms the load admittance (connected between the collectors of Q1 and Q2) to its negative inverse-scaled by a conversion factor-at the RF terminals (between the collectors of Q3 and Q4). Neglecting parasitics at the output node:

$$Y_{NII} = -K^2 I Y_L$$

[0036] where to a first order:

$$K^2 = g_m^2 / [(2 + g_m R_1)(2 + g_m R_2)] \text{ and}$$

[0037] g_m is the transconductance of each transistor and is assumed to be identical for Q1 - Q4, R_1 is the resistance between the emitters of Q1 and Q2, and R_2 is the resistance between the emitters of Q3 and Q4. Neglecting all parasitics, the input inductance is given by

$L_{NII} = -C_L / K^2$. L_{NII} is tuned by varying R_2 , which is accomplished by varying the voltage V_R on the gate of NFET M1. In the embodiment of the Nil of Fig. 2, R_2 comprises the parallel combination of a 100 Ohm fixed resistor and NFET M1 which acts as a resistor with a resistance that depends on the voltage between the gate (V_R) and the source/drain. The parallel combination of M1 and the fixed resistor results in a variable resistance from 20 - 100 Ohms in this

embodiment. Control signal V_c can be used to adjust the transconductance gm by setting the bias current of the current sources CS1-CS4 and thus effects the value of K^2 noted above.

[0038] In this embodiment, current sources CS1-CS4 at the emitters of Q1 - Q4 set the quiescent current preferably to 2 mA per transistor (which current may be controlled by the control signal V_c), and the collector voltage is set by common-mode feedback circuits CMF B1 and CMF B2. The base voltages are equal to the collector voltages (except for the effects of device mismatch) because the differential pairs are DC coupled. The common-mode feedback circuits CMF B1 and CMF B2 are shown in greater detail in Fig. 9 along with other circuits details. The circuit of Fig. 2 has a V_{dd} and a DC ground connection in addition to v_R and V_c (in addition to the connections 12 to patches 10). The V_{dd} , DC ground, v_R and V_c connections account for the four thru pins 18 depicted by Fig. 1c. Since one of the pins is coupled to DC ground, it may be coupled directly to the DC ground plane 29 (if used) instead of being connected to DC ground via a wire 31 in the wiring layer 27. The V_c connection may be omitted in some embodiments since while the ability to control the current generators of Fig. 2 may be useful, it is expected that it will not be needed or necessary for many embodiments.

[0038] The circuit of Fig. 2 has been implemented on a $1 \times 1 \text{ mm}^2$ die (see Fig. 3) using the IBM 8HP SiGe BiCMOS process. C_L , in this particular implementation, is composed of two 2.5-pF Metal-Insulator-Metal (MIM) capacitors, connected in parallel, and M1, in this particular implementation, is a thick-oxide NFET with width and length 60 and $0.48 \mu\text{m}$, respectively. The RF pads are preferably disposed on the left and right sides of the IC and are preferably spaced $750 \mu\text{m}$ center to center. When used with the AIS 5 of Fig. 2, each RF pad is coupled to a neighboring patch 10. The DC pads are preferably provided on both the top and bottom: V_{dd} and GND supply power, while V_c controls the quiescent current and V_R tunes the negative inductance. The pads on top are redundant to the DC pads on bottom: V_R , V_{dd} , V_c , and GND from left to right. As a result, this implementation of the circuit is an IC which is preferably symmetric (in a 180 degree rotation), which may be advantageous for assembly in certain cases. Of course, if such symmetry is not needed, then the extra set of pads can be eliminated.

[0039] The embodiments of the Nil 12 of Figs. 2 and 3 realizes a stable tunable negative-inductance integrated circuit. The 1-port S-parameters of three of the SiGe ICs depicted by Fig. 3 (in parallel with a 43 nH inductor, which ensures circuit stability and approximates the loading of the AIS) were measured from 30 MHz to 3 GHz as a function of the tuning voltage V_R . Then in post processing, the 43 nH inductor was removed from the measured S-parameters with an Open-Short-Load calibration and the equivalent circuit model parameters of the negative inductance circuit were extracted. Fig. 4 is a schematic of the equivalent circuit of Figs. 2 and 3, and Fig. 5 plots the equivalent circuit parameters as a function of V_R . This equivalent circuit data shows a stable tunable negative inductance from -70 nH to about -43 nH for all three functional non-Foster IC dice tested. To our knowledge this is the first demonstration of a stable non-Foster IC.

[0040] In Fig. 4, L and R are negative inductance and resistance, respectively, which are primarily contributed by the negative inversion of Y_L . G and C are positive, and are primarily caused by shunt parasitics at the output nodes. The admittance of the model agrees very well with both the measured and simulated (Cadence Spectre) admittances from 10 MHz to 1 GHz. The case when $V_R = 2.2$ V is shown in Fig. 6 for both the third IC tested (NII3) and the simulation. In Fig. 5 depicts the extracted equivalent circuit values from the three functioning non-Foster IC dice tested. The inductance was tuned from -70 to -45 nH as V_R was varied from 1.5 to 2.6 V.

[0041] For additional information regarding the circuit of Figs. 2 and 3 and the testing of the three ICs mentioned above, see Appendix A: C.R. White, J.W. May and J.S. Colburn, "A Variable Negative-Inductance Integrated Circuit at UHF Frequencies", IEEE MWCL, Vol. 22, No. 1, Jan. 2012, which is hereby incorporated herein by reference, and Appendix A: D.J. Gregoire; C.R. White, and J.S. Colburn, "Non-Foster Metamaterials", which is also hereby incorporated herein by reference.

[0042] Figs. 7 and 8 contain plots of the simulated reflection coefficient for a normal-incidence plane wave off an AIS loaded with a tunable negative inductance circuit 12. The AIS unit cell geometry used is a 65 x 65 mm metal patch 10 with a 10 mm gap between patches 10

disposed on a 1 inch foam substrate. In these simulations, the AIS is modeled by a full-wave simulation assuming an infinite periodic structure at normal incidence and the negative inductance circuit is modeled as the full small-signal model that was used to design the circuit in Figs. 2 and 3. These reflection results indicate that slowly-varying impedance can be achieved over a relatively wide band. In addition, this slowly-varying impedance can be tuned by changing the tuning voltage V_R .

[0043] Another schematic of the negative inductance circuit is shown in Fig. 9 which includes legends providing additional information regarding the operation of the circuit of Fig. 2 and shows the suggested circuit in greater detail.

[0044] Having described the invention in connection with certain embodiments thereof, modification will now suggest itself to those skilled in the art. As such, the invention is not to be limited to the disclosed embodiments except as is specifically required by the appended claims.

[0045] All elements, parts and steps described herein are preferably included. It is to be understood that any of these elements, parts and steps may be replaced by other elements, parts and steps or deleted altogether as will be obvious to those skilled in the art.

[0046] Broadly, this writing discloses a tunable impedance surface, the tunable surface including a plurality of elements disposed in a two dimensional array; and an arrangement of variable negative reactance circuits for controllably varying negative reactance between at least selected ones of adjacent elements in the aforementioned two dimensional array.

[0047]Concepts

This writing discloses at least the following concepts.

Concept 1. A tunable impedance surface, the tunable surface comprising: (a) a plurality of elements disposed in a two dimensional array; and (b) an arrangement of variable negative reactance circuits for controllably varying negative reactance between at least selected ones of adjacent elements in said two dimensional array.

Concept 2. The tunable impedance surface of Concept 1 further including a substrate having first and second major surfaces, said substrate supporting a ground plane on the first major surface thereof and supporting said plurality of elements and the arrangement of variable negative reactance circuits on the second major surface thereof, the substrate having a thickness such that a distance between the ground plane and said plurality of elements is less than a wavelength of a radio frequency of interest.

Concept 3. The tunable impedance surface of Concept 2 wherein the arrangement of variable negative reactance circuits is adjustable in response to one or more control signals to spatially tune the tunable impedance surface.

Concept 4. The tunable impedance surface of Concept 3 wherein the plurality of elements each have an outside diameter which is less than the wavelength of the radio frequency of interest.

Concept 5. The tunable impedance surface of Concept 1 wherein the elements are directly or ohmically coupled to the ground plane by vias in a substrate supporting said ground plane, said plurality of elements and said arrangement of variable negative reactance circuits.

Concept 6. The tunable impedance surface of Concept 1 further including a substrate having two major surfaces, said substrate supporting supporting said plurality of elements and the arrangement of variable negative reactance circuits on a common major surface thereof.

Concept 7. The tunable impedance surface of Concept 6 wherein the arrangement of variable negative reactance circuits each have an adjustable negative reactance which is controlled by a control signal for spatially tuning the tunable impedance surface.

Concept 8. The tunable impedance surface of Concept 1 wherein the arrangement of variable negative reactance circuits comprises a plurality of negative reactance integrated circuits, each negative reactance integrated circuit of said plurality of negative reactance integrated circuits being coupled between adjacent ones of said plurality of elements.

Concept 9. The tunable impedance surface of Concept 1 wherein the negative reactance circuits in said arrangement of variable negative reactance circuits are each controlled by a control voltage.

Concept 10. The tunable impedance surface of Concept 1 wherein the negative reactance circuits in said arrangement of variable negative reactance circuits each comprise two pairs of differentially coupled transistors, a capacitor coupled between current carrying electrodes of a first pair of said two pairs of differentially coupled transistors with a negative reactance being realized between currently carrying electrodes of a second pair of said two pairs of differentially coupled transistors.

Concept 11. The tunable impedance surface of Concept 1 wherein the negative reactance circuits in said arrangement of variable negative reactance circuits each comprise:

two pairs of cross-coupled transistors;

a reactive load coupled to first current carrying electrodes of a first one of the pairs of cross-coupled transistors and a first control resistance coupled to second current carrying electrodes of said first one of the pairs of cross-coupled transistors;

a second control resistance coupled to current carrying electrodes current carrying electrodes of a second one of the pairs of cross-coupled transistors;

current sources for supplying a flow of current to at least one of the current carrying electrodes of each pair of cross-coupled transistors;

two common-mode feedback networks, each common-mode feedback network being coupled to current carrying electrodes of each pair of cross-coupled transistors; and

terminals coupled to current carrying electrodes of said second one of the pairs of cross-coupled transistors, a function of the product of the resistances of the first and second control resistances setting a conversion ratio between the reactive load and a load appearing across said terminals, said terminals being coupled to at least selected ones of said adjacent elements in said two dimensional array.

Concept 12. The tunable impedance surface of Concept 1 wherein the negative reactance is a negative inductance.

NON-FOSTER METAMATERIALS

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We examine the effects of non-Foster loading on the properties of metamaterials. Non-Foster circuits are characterized by their negative reactance. Artificial magnetic conductors (AMC) are a type of metamaterial with the boundary condition of $\vec{H} \times \hat{n} = 0$ on its surface. The image currents of a patch antenna on an AMC groundplane reinforce the antenna's currents and increase its gain. However, the AMC boundary condition is typically valid over only a narrow bandwidth, and limits an antenna's operational bandwidth. We show how loading an AMC with negative inductance will increase its bandwidth by factors exceeding 10. We present measurements of a non-Foster loaded, VHF-UHF, AMC with bandwidth greater than 150%. Those results are compared to an equivalent AMC that is capacitively loaded whose bandwidth is less than 20%.

1, Introduction

In this paper, we present what we believe to be the first demonstration of a non-Foster loaded AMC, also referred to here as an active AMC (AAMC). We have observed bandwidths in excess of 150% for a VHF-band AAMC.

Non-Foster circuits are active circuit elements that are used to create negative capacitors and negative inductors. Their name alludes to the fact that they circumvent Foster's reactance theorem [1] which states "the reactance of a passive, lossless two-terminal (one-port) network always monotonically increases with frequency". They can be used for many applications including canceling the reactance of electrically small antennas [2] or for creating wideband artificial magnetic conductors (AMC).

An AMC is a type of metamaterial that emulates a magnetic conductor over a limited bandwidth. A magnetic conductor is a hypothetical material that is the magnetic analog to the electric conductor. Its boundary conditions dictate that transverse components of magnetic field vanish at the boundary. As a result, image charges and parallel currents have the same polarity as their sources. Such a material, if it exists, would allow antennas to be placed with their radiation currents parallel to a surface, thus expanding the design space of low-profile conformal antennas [3]-[8].

AMC bandwidth is typically defined as that range where the phase of a reflected wave lies between -90° and 90° . The bandwidth scales with its substrate's inductance [3]. When a non-Foster negative inductor loads the AMC, its negative inductance in parallel

the substrate inductance result* in a net increase in the AMC inductance and consequently its bandwidth. The AAMC is conceptually represented in Fig. 1, and compared to passive capacitively-loaded AMC resonant at the same frequency. The AMC is composed of an array of metallic patches distributed on top of a thick grounded dielectric substrate. Reactive loading is electrically connected between the patches. Both Non-Foster and capacitive loading both lower the AMC resonant frequency. In this* example, the target frequency is 300 MHz. Capacitive loading results in a decrease in bandwidth while non-Foster loading results in an increase. This can be understood easily by examining the simple L-C parallel circuit model.

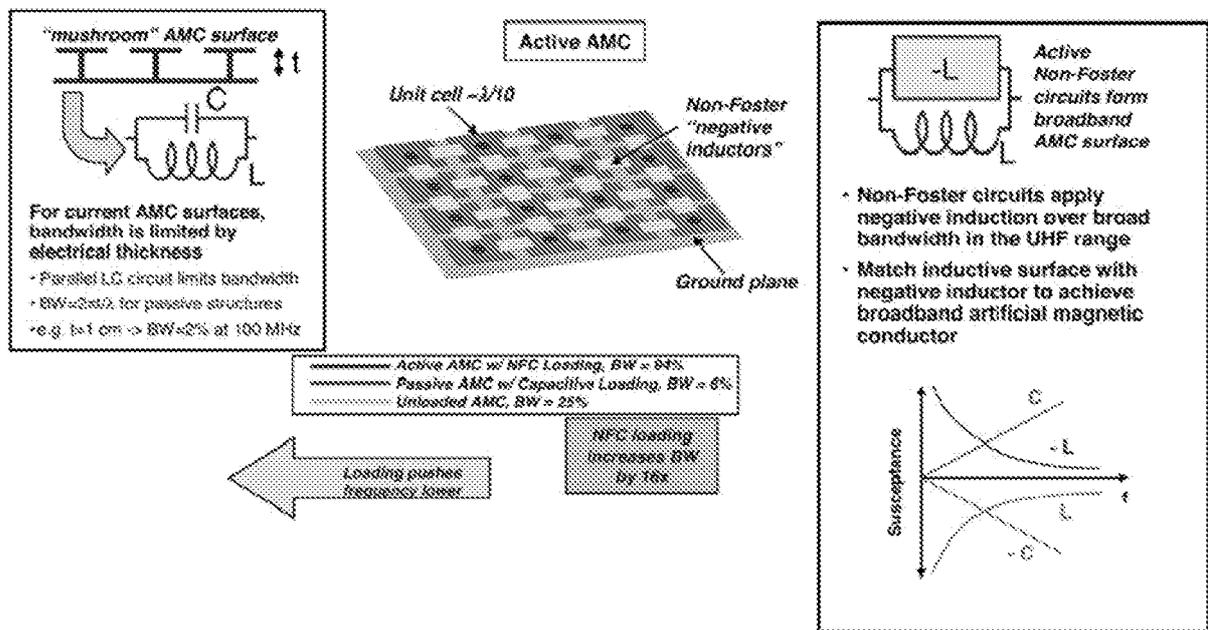


Figure 1: The AAMC concept is to increase the inductance and bandwidth of the traditional AMC structure with negative inductors to make VHF/UHF AMC a practical for integrated antenna application.

2. Non-Foster Circuits

The critical enabling element to the realization of an AAMC is the non-Foster circuit (NFC), which provides a negative inductance (a reactance that varies as ωL , where ω is the frequency in radians and L is the inductance in Henrys and is negative). This negative inductance can be realized using either a Negative Impedance Converter (NIC), or a Negative Impedance Inverter (NII), as shown in Fig. 2. The NIC is a two-port circuit whose input impedance at one port is the negative of the impedance connected across the other port; an inductor is converted into a negative inductor. The NII, on the other hand, is a two-port circuit whose input impedance at one port is the negative of the admittance connected across the other port; a capacitor is converted into a negative inductor. The NII is advantageous in integrated circuit embodiments of negative inductors because on-chip capacitors are small and of high quality, whereas on-chip inductors suffer from low quality factor (Q) and large area.

Fig. 3 gives the schematic of the AAMC architecture. This approach was developed to minimize the parasitics in the RF path which is critical for the stability of the non-Foster circuits while making it compatible with mass production processes. The non-Foster negative inductors are fabricated as an integrated circuit which is then mounted to a small carrier PCB using flip-chip technology. The ICs can be ordered from the foundry with the flip-chip bumps already installed. The small carrier PCBs are then attached to the metal pads of the top layer of the AAMC by soldering the RF pins to adjacent metal pads, with the bias being brought up from the bottom ground plane with pins which are also soldered to the carrier PCB geometry. This approach allows for the precision traces and assembly of the carrier PCBs to be completed separately from the fabrication of the metal patches which require less accuracy and need to be completed on a larger scale.

One realization of an NIC is shown Fig. 4a. The small-signal operation of the NIC can be understood by assuming ideal devices (no parasitic capacitance, no gate current, infinite drain-source resistance) with infinite transconductance. In this circuit, the voltage at the input is equal to the voltage across Z_L (which is an inductor for the negative inductor case), and the input current is equal to the current through Z_L scaled by the factor $-R_2/R_1$. Therefore input impedance, Z_{in} , is given by

$$Z_{in} = -\frac{R_2}{R_1} Z_L \Rightarrow L' = -\frac{R_2}{R_1} L_L \tag{6}$$

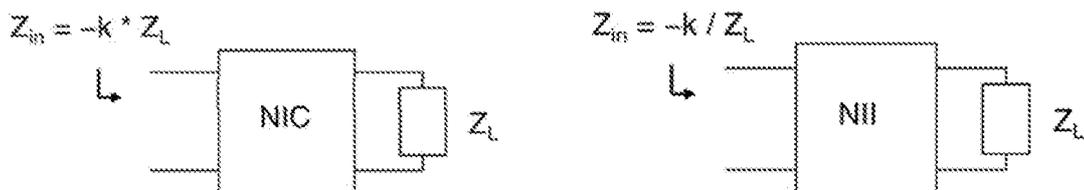
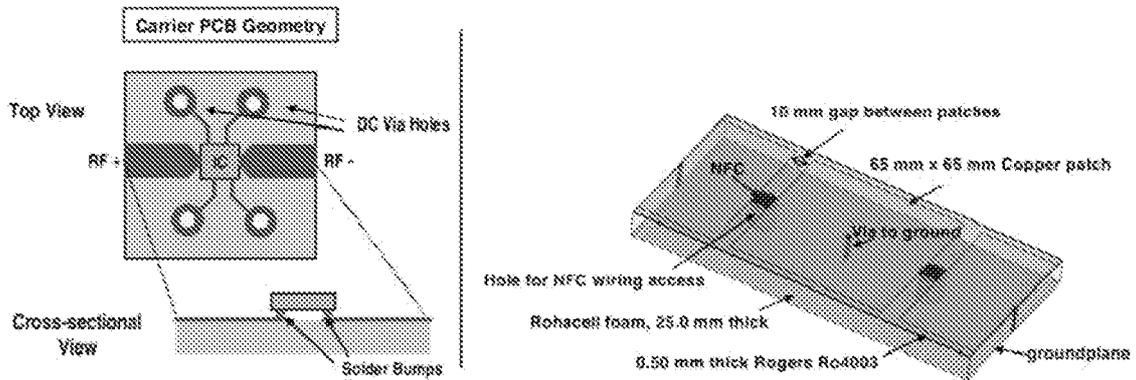


Figure 2 That NIC and NII are two-port circuit used to realize non-Foster Impedance.



Figures: AAMC Architecture. The left side details the carrier PCB board onto which the FET IC will be flipped chipped and the right side how the PCB carrier board is mounted on the AMC surface.

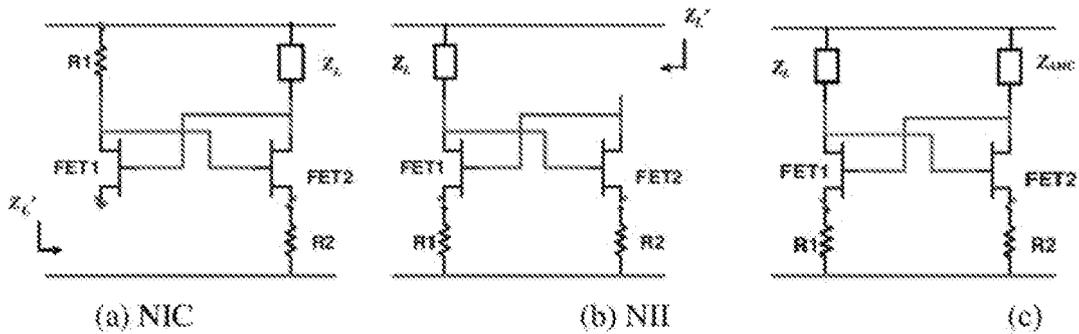


Figure 4: NIC and NU Circuit. (a) One realization of an NIC circuit; (b) the NII circuit derived from the NIC circuit in (a); (c) Z_{AMC} is the Impedance of the unit cell between the two NII terminate

The NIC can be converted to an NII by rearranging the placement of the ports and resistors. Swapping the input and load ports, and then swapping the load with R_1 gives the NII circuit in Fig. 4b. The input impedance of the NII is given by

$$Z_L' = -\frac{R_1 R_2}{Z_L} \Rightarrow L' = -R_1 R_2 C_L \tag{7}$$

All of the known NIC and NII circuits employ feedback and are conditionally stable. The stability of these circuits has been successfully predicted in simulation by the techniques of Middlebrook [9], and the circuit is stable for $\frac{3}{4}$ and Z_{AMC} such that the loop gain, T , is never negative-real and $< -j$ (this assumes negative feedback). The loop gain for this NII is:

$$T = -\frac{Z_L Z_{AMC}}{R_1 R_2} = \frac{Z_{AMC}}{Z_L} = \frac{Y_L'}{Y_{AMC}} = \frac{jB_L'}{G_{AMC} + jB_{AMC}} \tag{8}$$

which is -1 when $Z_{AMC} = -j\eta$. The zero-phase reflection associated with an AMC occurs when $B_{i1} = -B_{AMC}$, but the conductance due to radiation, G_{AMC} , prevents T from being negative real for an ideal negative inductance, Y_{L1} . B_{AMC} can be reduced at a given frequency by increasing the thickness of the AMC structure or by increasing the unit-cell size (which reduces the bandwidth).

The NFCs used in the AAMC [10] were designed with BiCMOS technology because it leads to superior analog performance, lower DC power consumption and greater flexibility to control conductance. A differential topology is used because it simplifies the circuit bias network and eliminates some components (e.g. DC blocking capacitors) that pose stability problems. The NFC negative inductance is tunable from -70 nH to -40 nH with application of a bias voltage.

NFC stability is a key issue, and extreme care was exercised to ensure that the circuits would be stable over the target range. For example, the circuit design is very sensitive to the series resistance of the output pins, so extra via holes were used in the IC layout to minimize the series resistance. Analysis indicated stable AAMC operation over 200 - 500 MHz if the pin resistance is kept less than 2 ohms. In order to minimize risk of instability from parasitics in the mounting structure, we used flip chip technology instead of wire bonding.

The NFCs were fabricated using the IBM 8HP process (130 nm BiCMOS). The NFCs were measured with direct probe testing for stability and equivalent circuit parameters. The observed stability and oscillation of these non-Foster ICs was consistent with simulations and design expectations. Fig. 5 shows an NFC mounted on a carrier board and the equivalent circuit model.

The equivalent circuit model parameters as a function of bias voltage were extracted using measured S-parameter data from 30 MHz to 1000 MHz. The parameters are plotted vs. bias voltage in Fig. 6 for ten of the NFCs. One of the ten is an obvious outlier

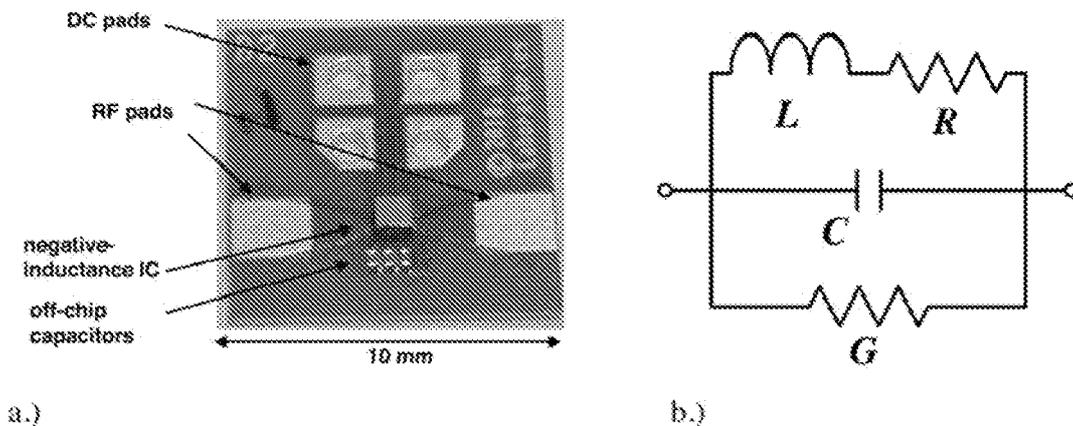


Figure 5: a.) AAMC carrier PCB board with negative inductance NFC and off chip capacitors attached B.) NFC equivalent circuit model. L and R are both negative and vary with tuning.

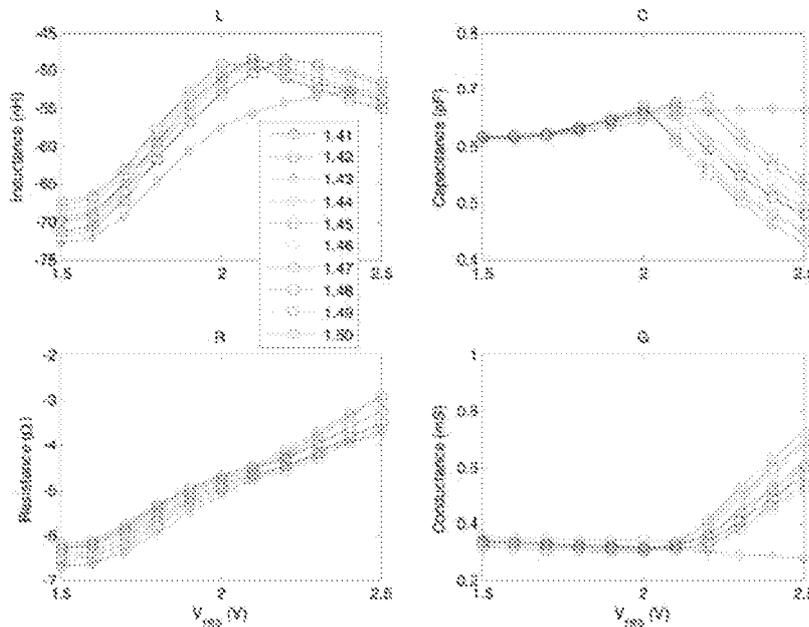


Figure 6. Equivalent circuit parameter* extracted from S^parameter data measured versus control voltage for 10 of the NFC*. NFC #1.43 is a rejected outlier.

and was rejected for use. The rest lie in a tight group. Overall, we realized better than 80% yield on over 100 NFCs. The negative inductance tune* from approximately -70 nH to -47 nH, very close to the design specifications. The range is limited at the high end by a 43 nH inductor placed in parallel across the measurement probes. Tuning the NFCs beyond this value results in circuit oscillation.

3. Artificial Magnetic Conductors

A magnetic conductor is a hypothetical material that is the magnetic analog to the electric conductor. Its boundary conditions dictate that transverse components of magnetic field vanish at the boundary. A typical AMC is realized with a laminated structure composed of a periodic grid of metallic patches distributed on a grounded dielectric layer. [3]–[8].

An AMC is most readily characterized by its resonant frequency, f_r , where an incident wave is reflected with 0° phase shift, and by its bandwidth as defined by the frequency range where the reflected phase is within the range $|\phi| < 90^\circ$. To first order, the AMC response can be determined with analytic expressions. Fig. 7 shows the reflection phase and magnitude as simulated for an example AMC with various capacitive loadings. AMC response can be accurately described over a limited frequency range using an equivalent parallel LRC circuit whose impedance is

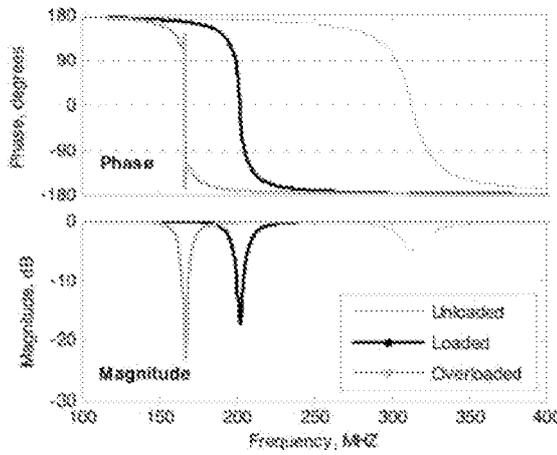


Figure 7: Reflection from a Capacitively-Loaded Lossy AMC.

$$Z = \frac{j\omega L}{1 - \omega^2 LC + j\omega L / R} \tag{1}$$

The resonant frequency and fractional bandwidth are

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \quad BW = \frac{\sqrt{LC}}{Z_0} \tag{2}$$

where Z_0 is the impedance of the incident wave. An AMC formed by a grounded dielectric substrate covered with a grid of loaded metallic squares loaded with lumped reactive elements can be represented by the transmission line model [13], [IJM 12] of Ftg. 8. The impedance seen by an incident wave is

$$Z = \frac{j(Z_0 + Z_{load})Z_0 \tan(k_z d)}{(Z_0 + Z_{load}) + jZ_0 \tan(k_z d)} \tag{3}$$

where Z_0 is the grid impedance, Z_{load} is the load impedance, $Z_0 = \eta_2 = \eta_0 \sqrt{\mu_2 / \epsilon_2}$ is the wave impedance in the dielectric, $k_z = k \sqrt{\mu_2 \epsilon_2}$ is the longitudinal wavenumber in the dielectric, d is the dielectric thickness, k is the free-space wavenumber, and ϵ , μ and η refer to relative permittivity, relative permeability and wave impedance respectively. The grid impedance of the metallic squares is capacitive, $Z_g = -j / (\omega C_g)$, and can be estimated analytically [11], [12]. Then, the simple LRC model can be used to estimate AMC reflection by equating the L, R and C of Eqn. 1 to quantities in the transmission line model of 3. If the load is capacitive, then the equivalent LRC circuit parameters are

$$L = Z_0 \tan(k_z d) / \omega, \quad C = C_g + C_{load} \quad \text{and} \quad R = R_{load} \tag{4}$$

If the load is inductive, then they are

$$L = \frac{L_{load} Z_0 \tan(k_z d)}{\omega L_{load} + Z_0 \tan(k_z d)}, \quad C = C_g \quad \text{and} \quad R = R_{load} \tag{5}$$

Loss in the substrate is not considered here, but it can be included in the circuit model as a resistor in series with the inductor [13].

When an NFC is used to load the AMC, it drives the net inductance of the AMC higher according to

$$L_{AMC} = L_{NFC} L_0 / (L_{NFC} + L_0) \tag{6}$$

where L_{NFC} , L_0 , and L_{AMC} are the inductances of the NFC, the unloaded AMC and the loaded AMC respectively. When $L_{NFC} < 0$ and $|L_{NFC}| > L_0 > 0$, then $L_{AMC} > L_0$, resulting in a decrease in the resonant frequency and an increase in the bandwidth according to

Eqn. (2), In the limit where $L_{NFC} \gg L_{\lambda}$, then $L_{AMC} \rightarrow \infty$. the resonant frequency goes to 0 and the bandwidth goes to infinity, in practice, losses within the circuit and the AMC materials limit the tuning and prevent this from happening.

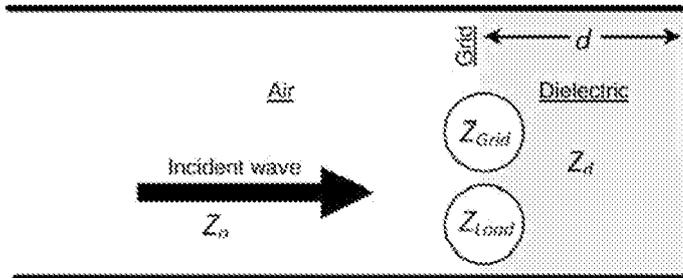


Figure 8. Loaded AMC Transmission Line Model.

4. AAMC Measurement

The AAMC test articles are fabricated using the architecture shown in Fig. 3 with an array of metallic patches on top of a grounded foam dielectric substrate. The NFCs are connected between the patches. Four control lines for ground, tuning bias, and power are connected from the NFC to a four-plane bias board behind the ground plane. Each NFC requires 32 mW of power. The bias lines pass through hole* in the ground plane, and are RF coupled to the ground plane with 100 pF capacitors to prevent RF coupling between neighboring unit cells. Vias from each patch to ground provide a ground at each terminal of the NFC. The AAMC only operate for a single polarization of incident waves because they are assembled with the MFCs along a single direction. A polarization^ independent AAMC could be made by installing NFCs along both directions.

It is desirable to measure AMC reflection properties with transverse electromagnetic (TEM) waves. We have measured the AAMC using both a large VHF-UHF parallel-plate TEM cell (LLTC) (Fig. 9a) and a compact coaxial TEM cell (Fig. 9b). The corresponding AAMC test articles for each TEM cell are shown in Fig. 10a and Fig. 10b respectively.

The AAMC tested in the PFTC is a 30 cm x 60 cm rectangular panel with 32 unit cells and 32 NPCs. Testing in the PFTC is desirable because it measures the AMC in a finite size that best represents how it will be used in antenna applications. The disadvantages of PFTC testing is that it is costly, labor intensive, and the panel AMC is more expensive to make since it requires 32 elements vs. 8 for the coaxial version. PFTC data extraction requires method-of-moments post processing that fits the data to a selected AMC circuit model.

We developed the coaxial TEM cell in order to make rapid measurements of the AAMC [13]. The coaxial TEM cell has an advantage over parallel plate waveguide TEM cell in that it produces direct real-time measurements of AMC phase and amplitude vs. frequency. The coax AMC appears to the incident wave in the coax as an infinite array of unit cells because of its radial periodicity and the PEC boundaries on coax walla. The

coax TEM cell is a tapered coaxial transmission line terminated by a standard 50-ohm coaxial connector at the small-diameter end and a straight coaxial section at the large* diameter end that accepts the device under test (DUT). The 40-cm long taper β formed with two concentric metal cones held in place by low-permittivity structural foam spacers at either end. The taper maintains the 50-ohm transmission line impedance from end to end.

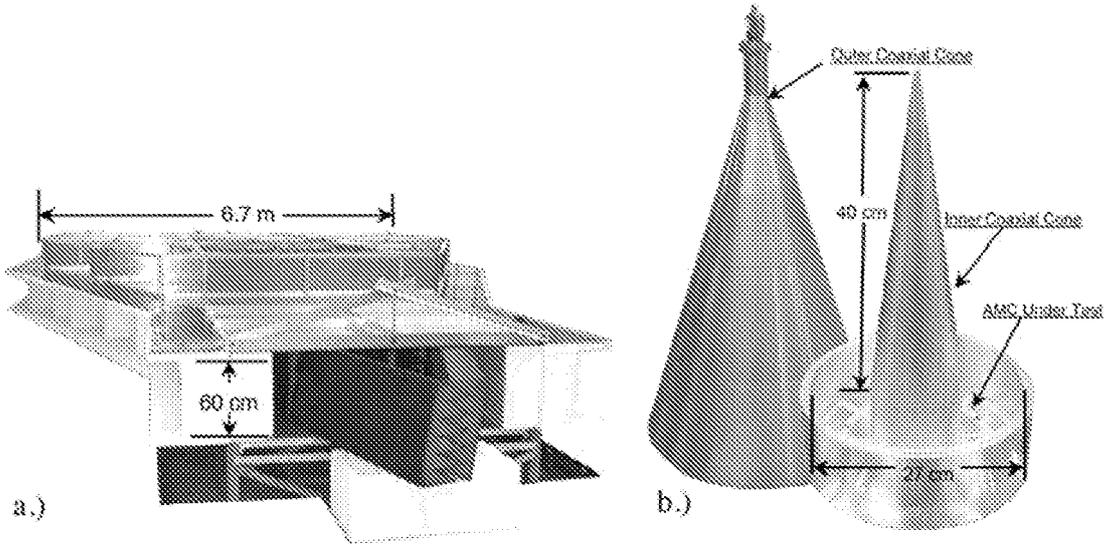


Figure 9. a.) VHF-UHF Parallel-Plate TEM Cell b.) Coaxial TEM cell

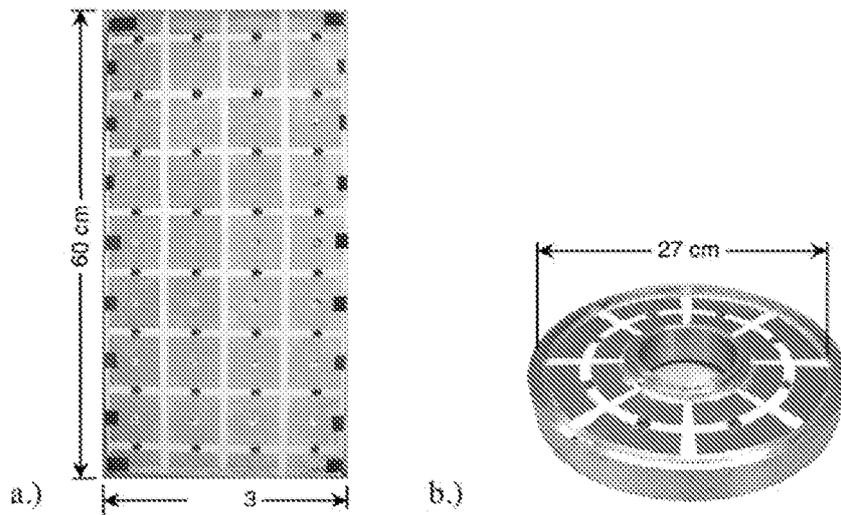


Figure 10. Rectangular and Coaxial AAMC test articles.

In order to validate the coax TEM cell as an accurate way to measure AMCs, we built several test coax AMCs loaded with passive capacitive elements whose behavior is easily predicted and compared to measurements. In the measurements, the reflection phase and amplitude are directly measured with a VNA and dc-coupled to the plane of the AMC. The test AMCs are based on the geometry used for the AAMC. Fig. 11a shows a measurement of a coax AMC loaded with a 12-pF fixed capacitor with 5% tolerance. The resonant frequency is 214 MHz and the $\pm 90^\circ$ degree bandwidth is 9.4%. These same values are obtained with a simulation using 12.4 pF loading and 1.03 ohms series resistance; both of those values are within the rated tolerance of the capacitors used for the loading. Similar results were obtained when the AMC is loaded with fixed capacitors, varying from 6 to 18 pF. The measured and simulated resonant frequencies and bandwidths of all these configurations are compared in Fig. 11b. The resonant frequency and bandwidth both decrease as the capacitive loading increases. This can be understood in terms of the circuit model of Section 3.

Fig. 12 shows measurements of a coax AAMC test article that confirms the predicted behavior and validates the NFC stability and operation. Fig. 12a shows several AMC phase curves for various NFC settings. When tuned to the target resonant frequency of 300 MHz (represented by the bold line in Fig. 12a), the $\pm 90^\circ$ bandwidth is more than 100% spanning the range from 200 to 450 MHz. A discontinuity in the phase curves between 450 and 600 MHz suggest the onset of coupling to the TBI mode in the coax AMC. The resonant frequency is tunable from 500 MHz down to a limit of 200 MHz before instability in the NFC dominates the performance. At resonant frequency less than 250 MHz, the instability is evident in the loss of smoothness in the phase curves. The instability has been confirmed by measuring radiation from the AMC surface in the extreme tuning range.

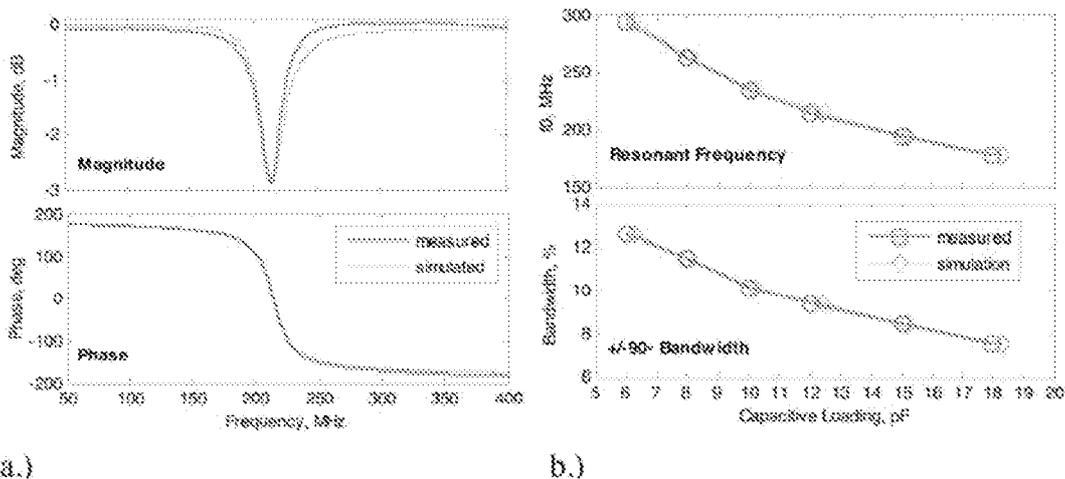


Figure 11. a.) Reflection from a Coax AMC Loaded with 12 pF Capacitors. b.) Resonant frequency and bandwidth of a varactor-loaded passive AMC.

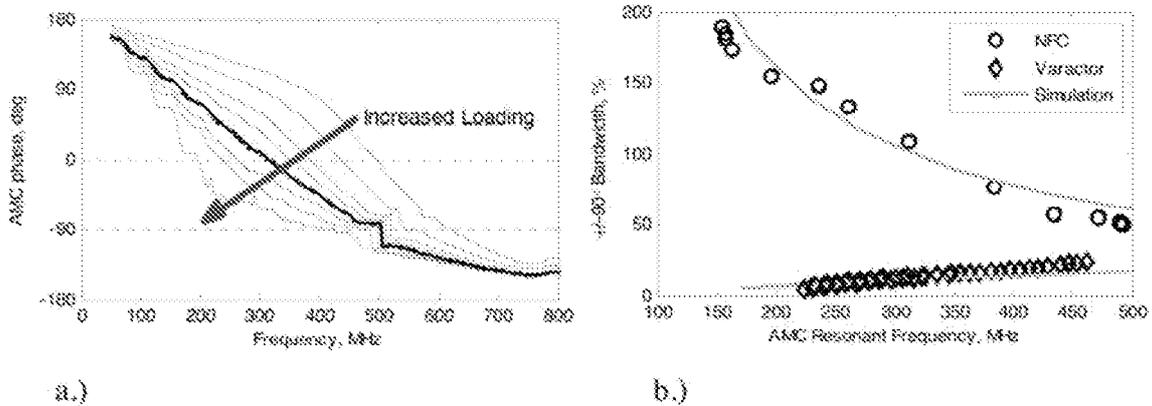


Figure 12. a.) The Phase Response of a Coax AMC Loaded With Non-Foster Negative-Inductance Circuits. b.) Comparison of $\pm 90^\circ$ Bandwidth for the AAMC and for a varactor-loaded AMC.

Figure 12b compares the $\pm 90^\circ$ bandwidth of the varactor-loaded AMC and the NFC-loaded AMC. As predicted by Eqns. 2, 4, and 6, the bandwidth of the varactor-loaded AMC decreases with resonant frequency while the NFC bandwidth increases significantly. The NFC AMC has better than ten times the bandwidth of the varactor-loaded AMC at high loading levels.

A second AAMC was fabricated using the NFCs whose equivalent circuit parameters are plotted in Fig. 6. The measurements are compared to simulations of the AAMC using the equivalent circuit parameters extracted in Fig. 13. The simulated resonant frequency is lower than the measured, but the character of the phase curves is similar. It's notable that the net reflection gain predicted for $f > 300$ MHz is confirmed by the measurements.

The rectangular panel AAMC seen in Fig. 10 was measured in the parallel-plate TEM cell. The preliminary results are shown in Fig. 14. The data shown here is extracted from a post-processing method that curve fits the measured data to an AAMC circuit model using a method of moments simulation of the scattering in the TEM cell by the AAMC. The results are similar in character to the coax AAMC results. It shows a controllable tuning of the AAMC over more than 100 MHz, and the phase curves show bandwidths as much as 50%. The reflection shows a net gain for $f < 400$ MHz for some bias levels. They differ in that the resonant frequency is higher and the tuning range is lower. The differences may be attributable to the effects of the finite size of the AAMC panel which may be presenting different AMC impedance to the NFCs on different locations on the panel. Another factor may be that the incident power used in the PPTC was too high and drove the NFCs into nonlinear response. Measurement in the coax TEM cell with different power levels confirm this behavior.

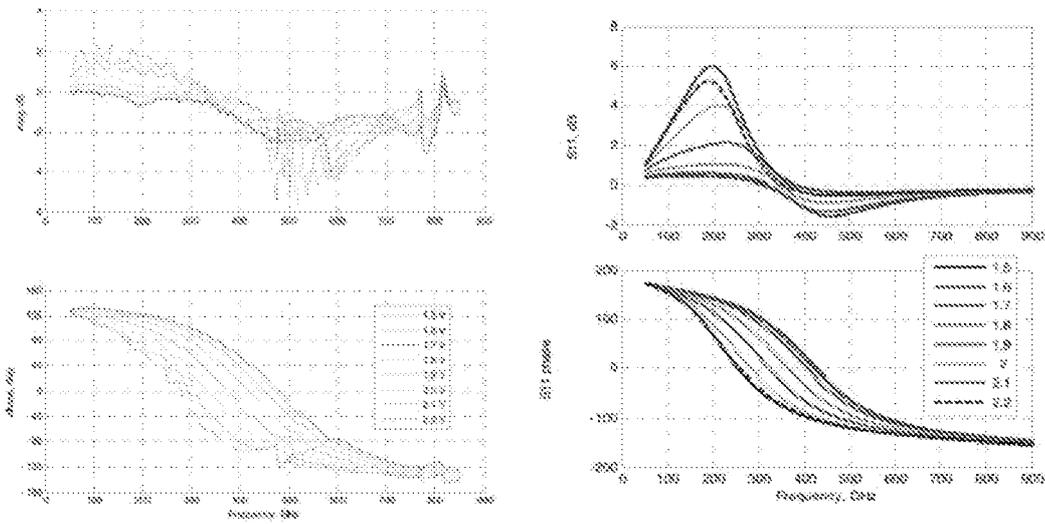


Figure 13. Coax AAMC #2 measurement (left) and simulation (right), Tit* simulations are made using the extracted NFC equivalent circuit parameters of Fig. 6. The tuning range* is lower for the simulated data. It is notable that the predicted gain for $f < 300$ MHz is confirmed by the measurements

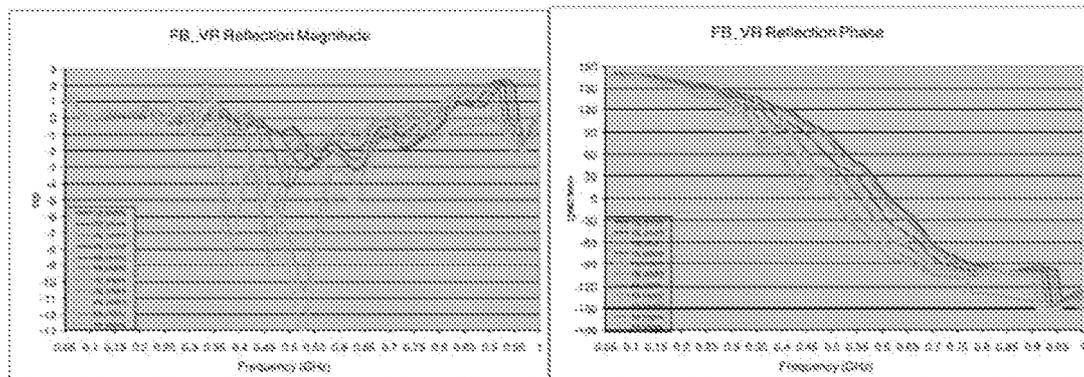


Figure 14: AAMC measurements in the parallel-plate TEM cell.

5. AAMC Ground Planes

AAMCs are touted as substrates that enable low-profile antennas [3]-[34] because of their magnetic boundary conditions. We tested that hypothesis with our coax AAMC being used as a ground plane for an antenna mounted 13 mm above it. We have demonstrated that the AAMC does indeed act as a magnetic conductor ground plane and facilitates the placement of antennas very close to its surface.

The antenna measurement setup is seen in Fig. 15. The antenna is a coaxial slot antenna that radiates into the TEM mode of the coax TEM cell. It is excited with the

conductors of a coaxial cable soldered to either side of the slot. The coax slot antenna's radiation in the coax TEM cell was characterized by measuring the two port S-parameters; port one is the feed coax cable of the slot antenna and port 2 is the coax output at the top of the coax TEM cell. When the same antenna is mounted 13 mm above a metal plate, no power at all radiates into the coax, and all of the power is reflected back into the feed port. Fig. 15b shows plots of the measured input reflection and the transmission coefficient for the coax slot antenna backed by the AAMC for different bias voltages. For each setting, there is a wide frequency band over which power is radiated efficiently through the coax TEM cell. At some points, the $S_{21} > 0$ dB because of net gain in the NFCs.

As the NFC bias is increased, the negative inductance is increased from -70 to -45 nH, and the AAMC's resonant frequency decreases accordingly. It's reasonable to assume, (although we haven't done rigid analysis on it yet) that the AAMC's resonant frequency is where the antenna's S_{11} is at a minimum. It's interesting to note that the apparent resonant frequency in this measurement ranges from 150 MHz to 300 MHz, while direct measurements of the AAMC range (see e.g. Fig. 12) from 250 MHz to 500 MHz for the same bias settings. This is because the presence of the large metal region of the antenna adds capacitive loading to the AAMC, resulting in the operating frequency band shifted lower in frequency. This is confirmed through simulations or application of the circuit model of section 3.

The antenna capacitance also shifts the range of NFC stability to a wider range of bias voltages (and more negative inductance). We hypothesize that the extra capacitance added to the AAMC by the antenna enhances the NFC stability.

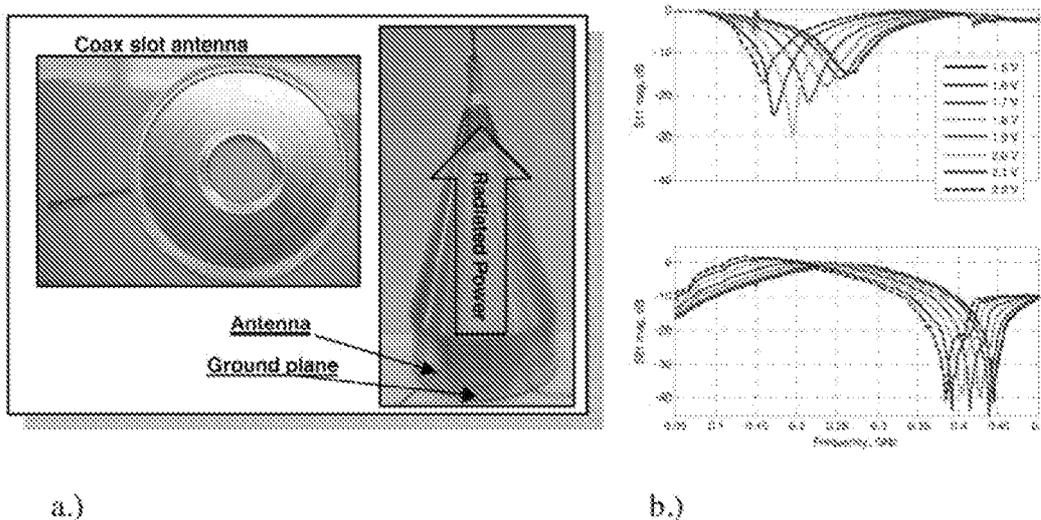


Figure 18: a.) The coax slot antenna and the measurement setup in the coax TEM cell, b.) The return loss (top) and the transmitted power of the coax slot antenna when mounted 19 mm above the AAMC ground plane for various AAMC bias settings*.

6. Conclusions

The work presented here represents what we believe to be the first demonstration of Active AMCs loaded with non-Foster circuits. The key challenge to realising this was in developing a stable negative inductor which was physically small, low power consuming was producible in large quantities, and capable of being integrating into a passive AMC structure without becoming unstable.

We have convincingly shown that AAMCs can be tuned over a large frequency range, have bandwidth* in excess of 100% and can be used as magnetic ground planes for low-profile antennas. We have also demonstrated a new method for direct measurement of AMC structures.

AAMC technology disclosed here is applicable applicability to a number antenna applications including including 1) Reducing finite ground plane edge affects for antennas mounted on structures to improve their radiation pattern or scattering properties, 2) Reducing coupling between closely spaced ($< 1 \lambda$) antenna elements on structures to mitigate co-site interference, 3) Enable radiation of energy polarized parallel to and directed along structural metal surfaces, and 4) Increase the bandwidth and efficiency of cavity-backed slot antennas while reducing cavity size.

While non-Foster circuit technology offers the potential to overcome fundamental limits on bandwidth and electrical size as demonstrated with the AAMC, it has many other electromagnetic applications (e.g. antenna matching, metamaterials). Of course, NFC stability will remain a large issue and needs to be addressed in detail for any application. We achieved stability through simultaneous circuit and AMC design that paid careful attention to parasitics in the circuit realization and the electromagnetic loading imposed by antenna geometry, metamaterial configuration, environment surrounding and bias network. This enabled stability robustness by enabling compensation for real world fabrication tolerance and uncontrollable surrounding environment loadings that must be compensated for in practical realizations.

Other applications for negative inductor non-Foster circuit developed on this project include 1) Wideband reactance cancellation of VHF/UHF slot antennas, 2) Realization of wideband adaptable VHF/UHF artificial impedance surfaces, both scalar and tensor, for holographic artificial impedance surface antennas or control of surface wave propagation on surfaces, and 3) Realization of wideband, thin, lightweight Salisbury screens/Jaumann absorbers.

Further research necessary general maturation of non-Foster technology 1) Study of the noise characteristic and ways to minimise it for receive applications, 2) Power handling for transmit applications, 3) Increased linearity, and 4) Self adaptive control to maintain stability in a changing environment, Solutions to these challenges will require more work in the area of optimum circuit topologies and consideration of III/V (e.g., InP and GaN) semiconductor technologies which offer inherent electrical property advantages (e.g., electron mobility, larger bandgaps) relative to Si.

7. Acknowledgements

The material in this paper is based upon work supported by the Air Force under AFRL Contract No. FA8718-10-C-0007. Any opinions, findings and conclusions or recommendations expressed in this material are those of the authors' and do not necessarily reflect the views of the AFRL.

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- [12] O. Luukkonen et al, "Simple and accurate analytical model of planar grids and high-impedance surfaces"*, IEEE Trans. Antennas Prop., vol. 56, 1624, 2008
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What is claimed is:

1. A tunable impedance surface, the tunable surface comprising: (a) a plurality of elements disposed in a two dimensional array; and (b) an arrangement of variable negative reactance circuits for controllably varying negative reactance between at least selected ones of adjacent elements in said two dimensional array.
2. The tunable impedance surface of claim 1 further including a substrate having first and second major surfaces, said substrate supporting a ground plane on the first major surface thereof and supporting said plurality of elements and the arrangement of variable negative reactance circuits on the second major surface thereof, the substrate having a thickness such that a distance between the ground plane and said plurality of elements is less than a wavelength of a radio frequency of interest.
3. The tunable impedance surface of claim 2 wherein the arrangement of variable negative reactance circuits is adjustable in response to one or more control signals to spatially tune the tunable impedance surface.
4. The tunable impedance surface of claim 3 wherein the plurality of elements each have an outside diameter which is less than the wavelength of the radio frequency of interest.
5. The tunable impedance surface of claim 1 wherein the elements are directly or ohmically coupled to the ground plane by vias in a substrate supporting said ground plane, said plurality of elements and said arrangement of variable negative reactance circuits.
6. The tunable impedance surface of claim 1 further including a substrate having two major surfaces, said substrate supporting supporting said plurality of elements and the arrangement of variable negative reactance circuits on a common major surface thereof.
7. The tunable impedance surface of claim 6 wherein the arrangement of variable negative reactance circuits each have an adjustable negative reactance which is controlled by a control signal for spatially tuning the tunable impedance surface.

8. The tunable impedance surface of claim 1 wherein the arrangement of variable negative reactance circuits comprises a plurality of negative reactance integrated circuits, each negative reactance integrated circuit of said plurality of negative reactance integrated circuits being coupled between adjacent ones of said plurality of elements.
9. The tunable impedance surface of claim 1 wherein the negative reactance circuits in said arrangement of variable negative reactance circuits are each controlled by a control voltage.
10. The tunable impedance surface of claim 1 wherein the negative reactance circuits in said arrangement of variable negative reactance circuits each comprise two pairs of differentially coupled transistors, a capacitor coupled between current carrying electrodes of a first pair of said two pairs of differentially coupled transistors with a negative reactance being realized between currently carrying electrodes of a second pair of said two pairs of differentially coupled transistors.
11. The tunable impedance surface of claim 1 wherein the negative reactance circuits in said arrangement of variable negative reactance circuits each comprise:
- two pairs of cross-coupled transistors;
 - a reactive load coupled to first current carrying electrodes of a first one of the pairs of cross-coupled transistors and a first control resistance coupled to second current carrying electrodes of said first one of the pairs of cross-coupled transistors;
 - a second control resistance coupled to current carrying electrodes current carrying electrodes of a second one of the pairs of cross-coupled transistors;
 - current sources for supplying a flow of current to at least one of the current carrying electrodes of each pair of cross-coupled transistors;
 - two common-mode feedback networks, each common-mode feedback network being coupled to current carrying electrodes of each pair of cross-coupled transistors; and
 - terminals coupled to current carrying electrodes of said second one of the pairs of cross-coupled transistors, a function of the product of the resistances of the first and second control resistances setting a conversion ratio between the reactive load and a load appearing across said

terminals, said terminals being coupled to at least selected ones of said adjacent elements in said two dimensional array.

12. The tunable impedance surface of claim 1 wherein the negative reactance is a negative inductance.

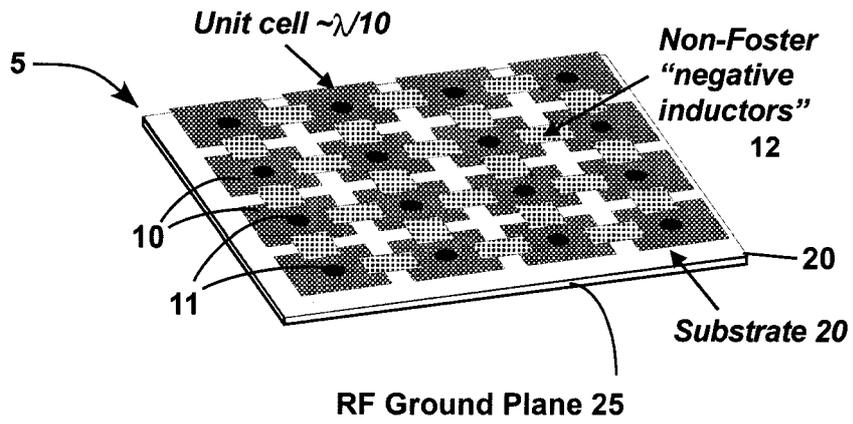


FIG. 1a

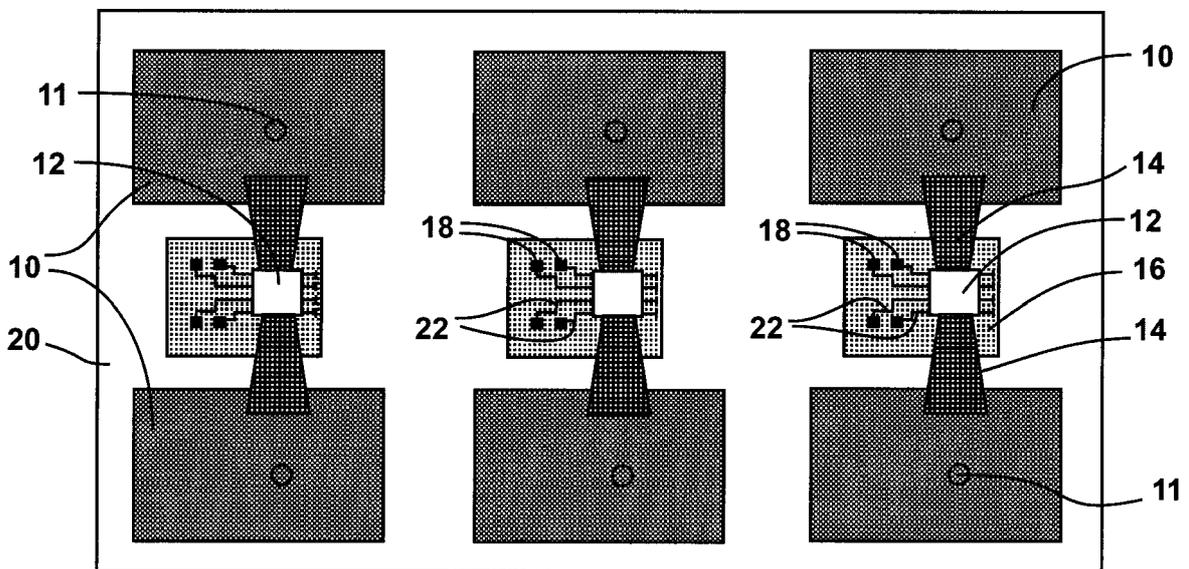


FIG. 1b

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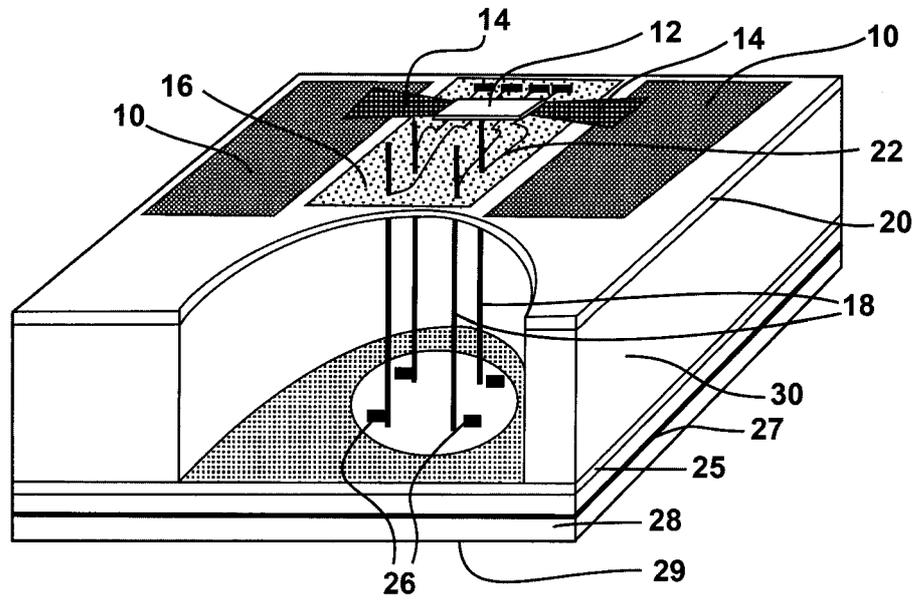


FIG. 1c

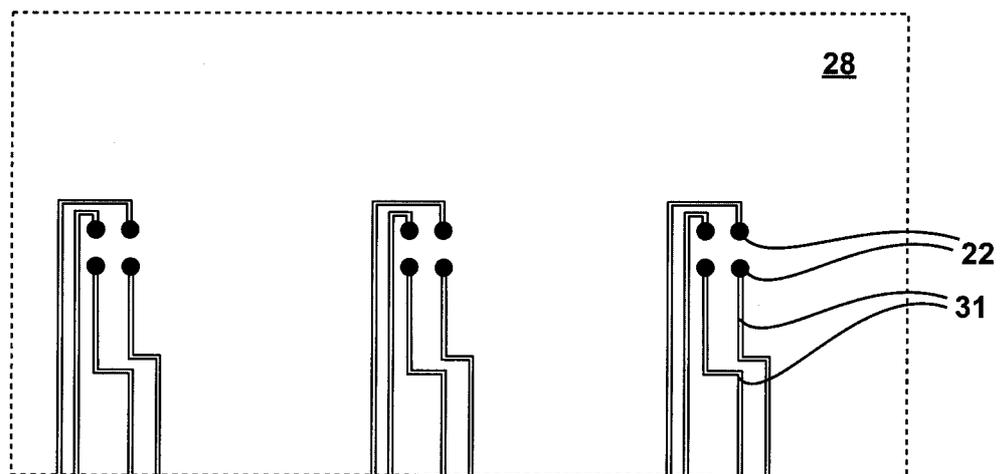


FIG. 1d

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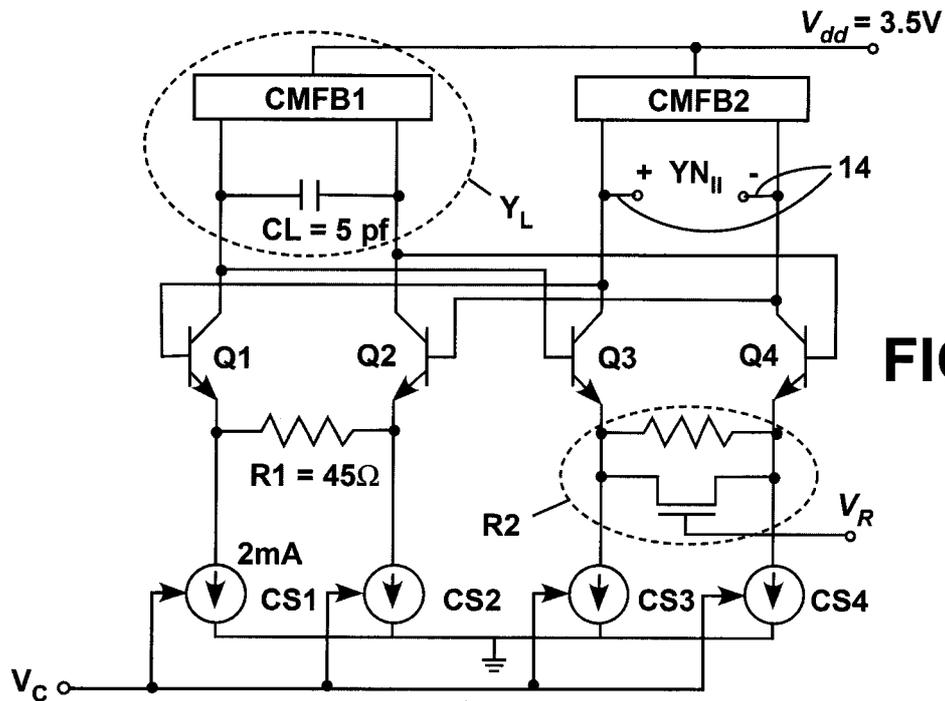


FIG. 2

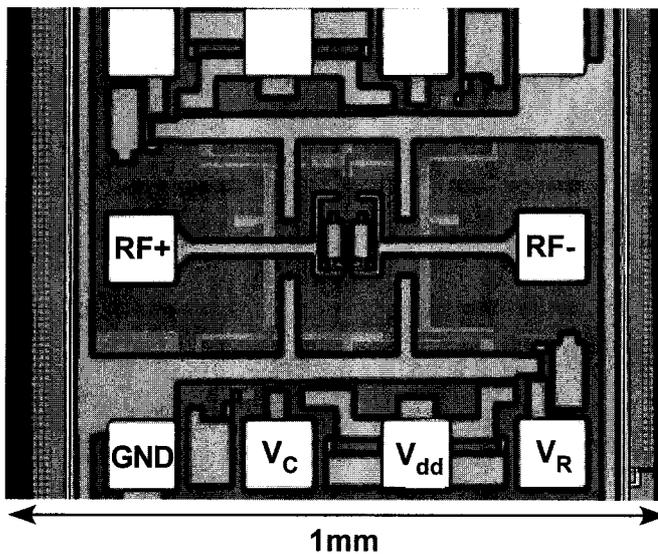


FIG. 3

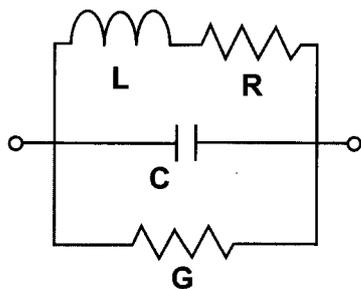


FIG. 4

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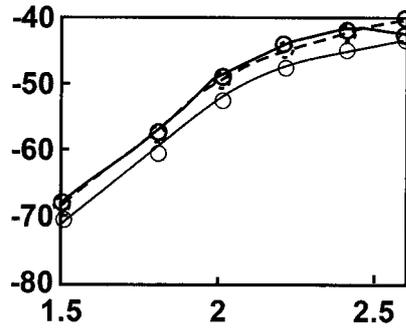


FIG. 5

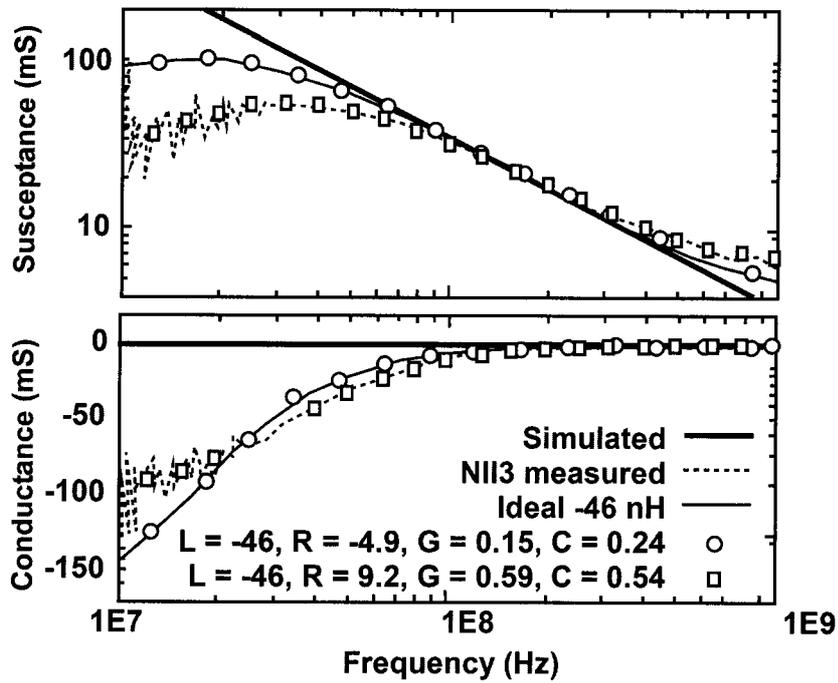


FIG. 6

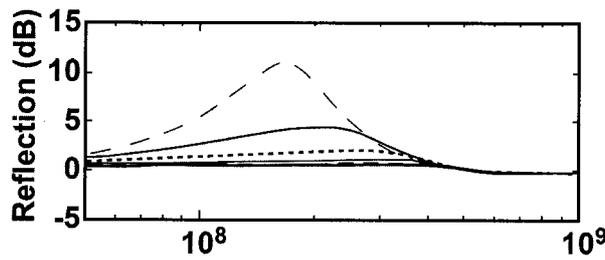


FIG. 7

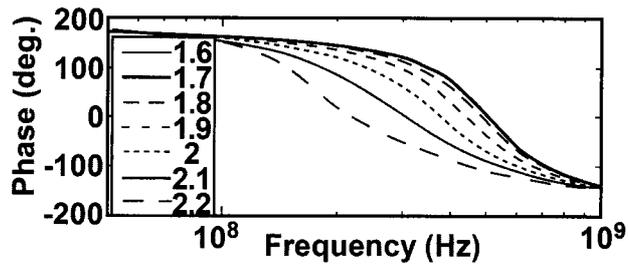


FIG. 8

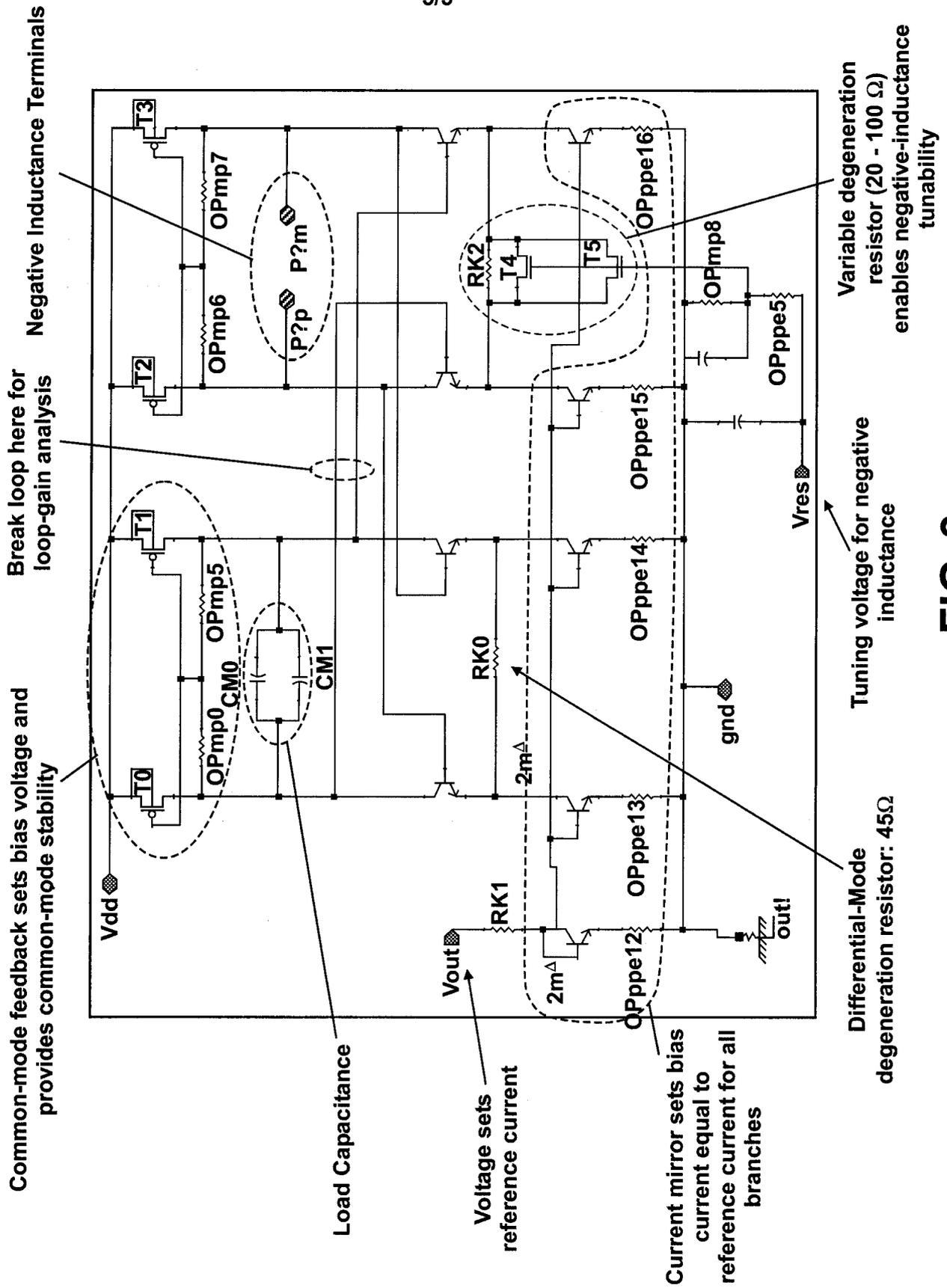


FIG. 9