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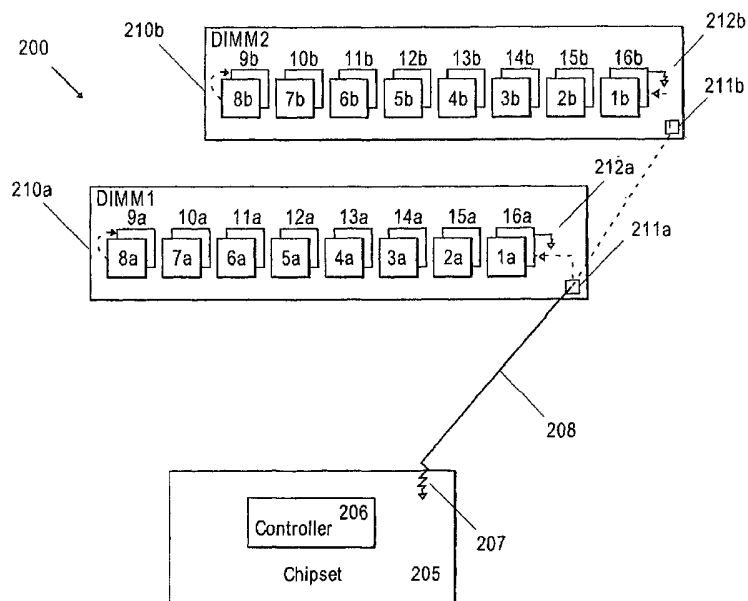
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[Continued on next page]

(54) Title: SPLIT T-CHAIN MEMORY COMMAND AND ADDRESS BUS TOPOLOGY



(57) Abstract: Embodiments of the invention provide a memory command and address (CA) bus architecture that can accommodate higher CA data output frequencies with reduced signal degradation. For one embodiment of the invention the CA is divided on the motherboard and a CA signal component routed to each of two dual in-line memory modules (DIMMs) of a two-DIMM/channel memory bus design. The CA signal component on each DIMM is then routed sequentially through each dynamic random access memory (DRAM) chip on the respective DIMM. In one embodiment, after routing through each DRAM, the CA signal is terminated on the DIMM. In an alternative embodiment, the CA signal is terminated on the die at the last DRAM of each respective DIMM.

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 02/084428 A (MICRON TECHNOLOGY, INC) 24 October 2002 (2002-10-24) page 5, line 13 - page 7, line 9 page 11, line 17 - page 12, line 2 figures 1,4	1-30
A	----- US 5 668 834 A (TAKEKUMA ET AL) 16 September 1997 (1997-09-16) figures 13,14	1-30
A	----- US 6 125 419 A (UMEMURA ET AL) 26 September 2000 (2000-09-26) figures 10,11 -----	1-30

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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