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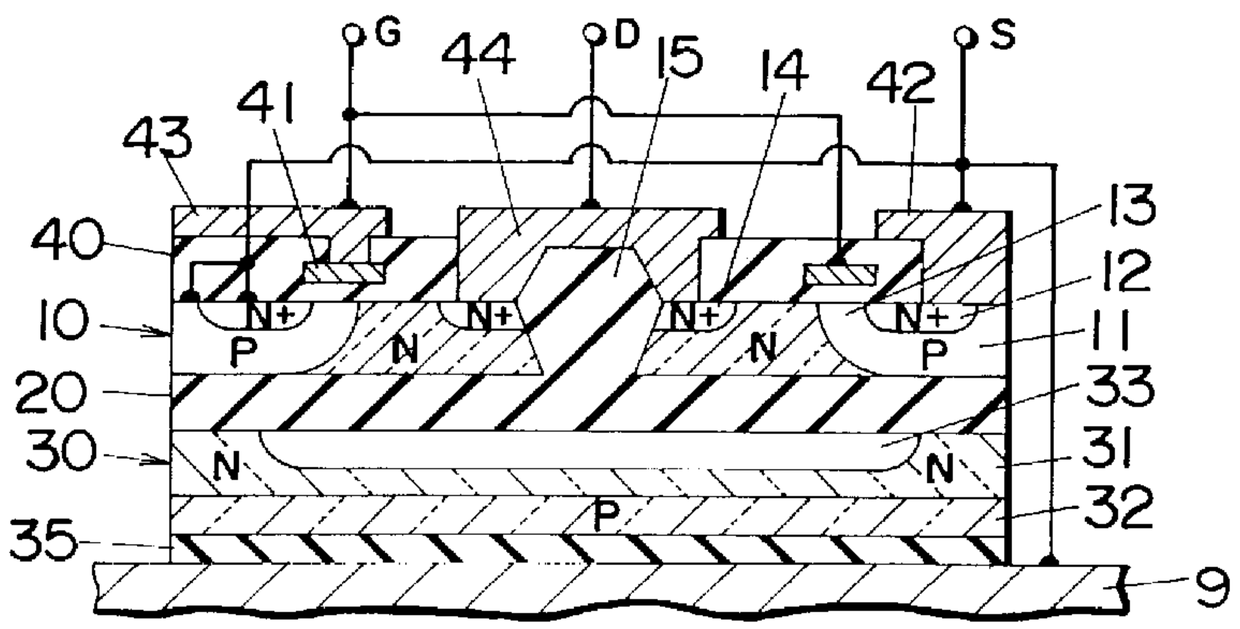

(57) Abrégé/Abstract:
A solid state relay composed of a series connected pair of LDMOSFETs has a minimized output capacitance. Each LDMOSFET is configured to have a silicon layer of a first conductive type, a drain region of the first conductive type diffused in the top surface of the silicon layer, a well region of a second conductive type diffused in the silicon layer in a laterally spaced relation from the drain region, and a source region of the first conductive type diffused within the well region to define a channel extending between the source region and a confronting edge of the well region along the top surface of the silicon layer. Each LDMOSFET is of an SOI (Silicon-On-Insulator) structure composed of a silicon substrate placed on a supporting plate, a buried oxide layer on the silicon substrate, and the silicon layer on the buried oxide layer. The well region is diffused over the full depth of the silicon layer to have its bottom in contact with the buried oxide layer, so that the well region forms with the silicon layer a P-N interface only at a small area adjacent the channel. Because of this reduced P-N interface and also because of the buried oxide layer exhibiting a much lower capacitance than the silicon layer, it is possible to greatly reduce a drain-source capacitance for minimizing the output capacitance of the relay in the non-conductive condition.

ABSTRACT

A solid state relay composed of a series connected pair of LDMOSFETs has a minimized output capacitance. Each LDMOSFET is configured to have a silicon layer of a first conductive type, a drain region of the first conductive type diffused in the top surface of the silicon layer, a well region of a second conductive type diffused in the silicon layer in a laterally spaced relation from the drain region, and a source region of the first conductive type diffused within the well region to define a channel extending between the source region and a confronting edge of the well region along the top surface of the silicon layer. Each LDMOSFET is of an SOI (Silicon-On-Insulator) structure composed of a silicon substrate placed on a supporting plate, a buried oxide layer on the silicon substrate, and the silicon layer on the buried oxide layer. The well region is diffused over the full depth of the silicon layer to have its bottom in contact with the buried oxide layer, so that the well region forms with the silicon layer a P-N interface only at a small area adjacent the channel. Because of this reduced P-N interface and also because of the buried oxide layer exhibiting a much lower capacitance than the silicon layer, it is possible to greatly reduce a drain-source capacitance for minimizing the output capacitance of the relay in the non-conductive condition.

SPECIFICATION

SOLID-STATE RELAY

TECHNICAL FIELDS

The present invention is directed to a solid-state relay, and more particularly to a solid-state relay having a pair of LDMOSFETs of which drains define output terminals for connection with a load to be controlled by the relay.

BACKGROUND ART

Solid-state relays have been widely utilized in place of mechanical relays in view of many advantages including miniaturized configuration, low-energy consumption, and high-speed switching performance. Because of the above advantages, the solid-state relay can be successfully incorporated in a small device, such as an automatic test equipment for testing LSI chips, for example. When utilized for the measurement of this kind, the relay is designed to provide a series of output signal as a testing signal. As the frequency of the output signal becomes higher, the relay is required to have a lower output capacitance developed across output terminals of the relay during off-periods of the output signal, i.e., the periods in which the output terminals are in non-conductive condition, in addition to minimizing on-state resistance between the output terminals during on-periods of the output signal. The output capacitance is the sum of a drain-source capacitance and a gate-drain capacitance at the non-conductive condition of the output terminals of the relay.

Japanese Patent Laid-Open Publication No. 9-312392 discloses a solid state relay which utilizes LDMOSFETs as switching elements in an attempt to reduce the output capacitance. The LDMOSFET has structure in which a well region and a drift region are diffused in the top

surface of a silicon layer with a source region being diffused within a confine of the well region and with a drain region being diffused within a confine of the drift region. However, since the drift region and the well region are formed in the top surface of the silicon layer, there is formed a P-N interface of extended area including the bottoms of the drift region and the well region. The P-N interface of such enlarged area is responsible for increasing a capacitance between the source and drain of LDMOSFET. Accordingly, the LDMOSFET of this structure is not satisfactory for minimizing the output capacitance between the output terminals of the relay.

DISCLOSURE OF THE INVENTION

The present invention has been accomplished in view of the above insufficiency to provide a solid state relay which is capable of minimizing an output capacitance across output terminals of the relay, while retaining a low on-state resistance across the output terminals. The solid-state relay in accordance with the present invention comprises a control unit which gives an electrical energy upon receipt of an input signal and a pair of LDMOSFETs (Lateral Double-diffused Metal Oxide Semiconductor Field Effect Transistors) mounted on a supporting plate of electrically conductive material. LDMOSFETs are arranged in circuit with individual gates commonly coupled to receive the electrical energy from the control unit so as to be driven thereby to turn on and off. Sources of LDMOSFETs are connected to each other in a series fashion so as to have individual drains connected to the output terminals, respectively. Each LDMOSFET is configured to have a silicon layer of a first conductive type, a drain region of the first conductive type diffused in the top surface of the silicon layer, a well region of a second

conductive type diffused in the silicon layer in a laterally spaced relation from the drain region, and a source region of the first conductive type diffused within the well region to define a channel extending between the source region and a confronting edge of the well region along the top surface of the silicon layer. The source region and the drain region define respectively the source and drain of LDMOSFET. Drain and source electrodes are placed respectively over the drain and source regions in electrically connected relation thereto. A gate electrode is connected to a gate layer of an electrically conductive material which is placed over the channel through a dielectric layer and which defines the gate of LDMOSFET. A characterizing feature of the solid-solid state relay resides in that each LDMOSFET is of an SOI (Silicon-On-Insulator) structure composed of a silicon substrate placed on said supporting plate, a buried oxide layer on the silicon substrate, and the silicon layer on the buried oxide layer, and that the well region extends the full depth of the silicon layer to have a bottom abutted against said buried oxide layer.

Since the well region is diffused over the full depth of the silicon layer to have its bottom abutted against the buried oxide layer, the well region of the second conductive type forms with the silicon layer of the first conductive type a P-N interface only at a small portion adjacent the channel. That is, only a side boundary of the well region laterally confronting the drain region forms the P-N interface. Because of this reduced P-N interface and also because of the buried oxide layer exhibiting much lower capacitance than the silicon layer, it is possible to greatly reduce a drain-source capacitance for minimizing the output capacitance of the relay in the non-conductive condition. Also the reduced P-N interface area can reduce a leak current at the non-

conducting condition of the output terminals. Moreover, the SOI structure can assure sufficient flexibility for mounting the LDMOSFET on the supporting plate, either with one of the drain and source being electrically connected to the supporting plate or being electrically isolated, in accordance with particular demands.

One of the source region and the drain region is configured to surround the other within a plane of the silicon layer. This surrounding arrangement enables the source region to confront the drain region over a prolonged line in the plane of the silicon layer, thereby reducing an on-state resistance between the output terminals of the relay. Accordingly, the relay can enjoy an optimum combination of the low output capacitance and the low on-state resistance. Although there exists a factual relation that the smaller the on-state resistance is, the greater the output capacitance becomes, the above structure of reducing the P-N interface area is most effective to minimize the output capacitance when the on-state resistance is required to be reduced to an acceptable extent. Preferably, the source region is configured to surround the drain region.

Further, the present invention envisages to minimize an effect of developing an additional capacitance between the source and the drain or between the gate and the source owing to the presence of the buried oxide layer, particularly when the single supporting plate mounting the pair of LDMOSFETs is utilized to electrically interconnect the sources of LDMOSFETs or when the two separate supporting plates each mounting the LDMOSFET are each utilized to interconnect the drain and the output terminal of the relay. In order to facilitate the recognition of several advantages of the present invention, there are introduced terms, “primary drain-source capacitance” and “secondary drain-source capacitance”. The primary drain-source capacitance is utilized to

denote the capacitance substantially developed through a portion of the silicon layer between drain region and source region, while the secondary drain-source capacitance is for an additional capacitance developed through the buried oxide layer in a vertical path from the source region to the supporting plate kept at the same potential of the drain or from the drain region to the supporting plate at the same potential of the source.

The silicon layer has a peripheral zone located laterally outwardly of the well region and electrically isolated from the drain region by the well region. It is preferred to electrically connect the peripheral zone and the drain commonly to the supporting plate. Thus, the peripheral zone around the well region can be kept at the same potential as the drain region, thereby eliminating an additional path of developing a capacitance through the buried oxide layer between the peripheral zone and the silicon substrate. Otherwise, the additional path would add a capacitance in parallel with the secondary drain-source capacitance inevitably developed between the bottom of the well region and the supporting plate through the buried oxide layer, thereby bringing about unduly large parallel connected capacitance between the source and drain.

In addition, a separator ring of dielectric material may be formed in the peripheral zone to surround closely the well region in such a manner as to electrically isolate the well region from the peripheral zone. Thus, it is possible to prevent an unduly high capacitance from developing between the well region and the peripheral zone, thereby minimizing the overall drain-source capacitance when the drain and the peripheral zone are electrically connected to the supporting plate.

Further, at least one separated land of the second conductive type

may be diffused in the silicon layer outwardly of the well region in a spaced relation therefrom. At least one of the source electrode and the gate electrode extends over the separated land in a spaced relation thereto from the corresponding one of the source and the channel to form a wiring pad for wiring connection to a complementary circuit element. Also with this arrangement of providing the wiring pad over the separated land, it is possible to reduce an additional capacitance resulting from the provision of the pad and correspondingly minimize the overall source-drain or gate-drain capacitance.

Alternatively, at least one separated land of the first conductive type may be diffused within the well region to extend the full depth of the silicon layer in an electrically isolated relation from the source region. At least one of the source electrode and the gate electrode extends over the separator region in a spaced relation thereto from the corresponding one of the source and the channel to form a wiring pad for wiring connection to a complementary circuit element for the purpose of minimizing the in order to minimize the overall source-drain or gate-drain capacitance in the manner as discussed in the above.

When the drain region is configured to surround the well region and the supporting plate is utilized to electrically interconnect the sources of the two LDMOSFETs, it is preferred to connect a peripheral zone outwardly of the drain region electrically to the supporting plate. Thus, the peripheral zone outwardly of the drain region can develop no additional capacitance through the corresponding portion of the buried oxide layer, thereby minimizing the source-drain capacitance. Also in this structure, a dielectric separator ring may be utilized to surround closely the drain region. The separator ring is formed in the silicon layer to isolate the drain region from the peripheral zone of the silicon

layer, in order to give an optimum dielectric strength between the drain and the source, in addition to minimizing the source-drain capacitance.

When the source or drain is electrically connected to the supporting plate, the silicon substrate is preferably formed with a cavity or recess extending in correspondence to the drain region or well region in order to further reduce the drain-source capacitance by the intervention of the cavity or recess between the source or drain region and the supporting plate.

In a further version, there is formed an electrically insulator stud which extends from the buried oxide layer through a center of the drain region to project on the top surface of the silicon layer in such a manner as to expose the drain region in an annular shape around the stud. The associated drain electrode is arranged to extend over the insulator stud with a peripheral zone of the drain electrode being electrically connected to the drain region of the annular shape. The combination of the insulator stud and drain electrode can effectively reduce the drain-source capacitance while assuring sufficient dimensions for the drain electrode.

The silicon substrate may comprise a pair of semiconductor stratums of opposite conductive types which develops a depletion layer at the P-N interface therebetween. The resulting depletion layer gives an additional capacitance which is added in series capative connection with the secondary drain-source capacitance of the buried oxide layer, thereby reducing the overall drain-source capacitance.

The relay of the present invention may further include a dielectric layer on a bottom of the silicon substrate opposite of said buried oxide layer in order to further reduce the secondary drain-source capacitance.

In a further version of the present invention, it is contemplated to integrate the two LDMOSFET in a single device structure. In this

structure, the well region are formed in the single silicon layer over the full depth thereof in such a manner as to form therein a laterally isolated pair of first and second active zones. Diffused in the well region is a pair of first and second source regions which surround respectively the first and second active zones and define first and second channels extending within the well regions from the first and second source regions to confronting boundaries of the first and second active zones, respectively. First and second drain regions are diffused respectively within the first and second active zone so as to be isolated from each other by the well region. First and second drain electrodes are placed respectively on the first and second drain regions in an electrical connecting relationship therewith. At least one gate electrode is electrically connected to first and second gate layers which are placed over the first and second channels respectively through dielectric layers and define first and second gates of the two LDMOSFETs, respectively. A common source electrode is provided to bridge over the first and second source regions and is electrically connected thereto. The silicon substrate carrying the silicon layer through the buried oxide layer is mounted on the supporting frame with the output terminals being electrically connected respectively to the first and second drains. Thus, the two LDMOSFETs can be realized in the single device structure and can be easily assembled into the solid-state relay, while retaining to minimize drain-source capacitance.

In this structure of realizing the two LDMOSFETs commonly in the single silicon layer, the supporting plate may be electrically isolated from the common source as well as from the first and second drains, and the output terminals are formed separately from the supporting plate for electrically connection with the first and second drains.

These and still other objects and advantageous features of the present invention will become more apparent from the following description of the embodiments when taking in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a solid-state relay of the present invention;

FIG. 2 is a schematic view illustrating a typical arrangement of electrical connections of the above relay in accordance with a first embodiment of the present invention;

FIG. 3 is a partial vertical section of an SOI-LDMOSFET utilized in the relay of the first embodiment;

FIG. 4 illustrates a planar arrangement of well, source, drain regions of the SOI-MOSFET of FIG. 3;

FIG. 5 illustrates a planar arrangement of gate, drain, and source electrodes and individual pads thereof for the above SOI-MOSFET;

FIG. 6 is a schematic view illustrating a typical arrangement of electrical connections of the above relay in accordance with a second embodiment of the present invention;

FIG. 7 is a partial vertical section of an SOI-LDMOSFET utilized in the relay of the second embodiment;

FIG. 8 illustrates a planar arrangement of well, source, drain regions of the SOI-MOSFET of FIG. 7;

FIG. 9 illustrates a planar arrangement of gate, drain, and source electrodes and individual pads thereof for the above SOI-MOSFET;

FIG. 10 is a partial vertical section of an SOI-LDMOSFET utilized in

the relay in accordance with a third embodiment of the present invention;

FIG. 11 illustrates a planar arrangement of well, source, drain regions of the SOI-MOSFET of FIG. 10;

FIG. 12 illustrates a planar arrangement of gate, drain, and source electrodes and individual pads thereof for the above SOI-MOSFET;

FIG. 13 is a partial vertical section of an SOI-LDMOSFET utilized in the relay in accordance with a fourth embodiment of the present invention;

FIG. 14 illustrates a planar arrangement of well, source, drain regions of the SOI-MOSFET of FIG. 13;

FIG. 15 illustrates a planar arrangement of gate, drain, and source electrodes and individual pads thereof for the above SOI-MOSFET;

DESCRIPTION OF THE EMBODIMENT

As shown in FIG. 1, a solid-state relay of the present invention comprises a pair of LDMOSFETs (Lateral Double-diffused Metal Oxide Semiconductor Field Effect Transistors) **T** connected in series between output terminals **2** which are adapted to be connected across a load to be operated by the relay. LDMOSFETs (hereinafter sometimes referred to simply as FETs) are driven to turn on and off by a control unit **3** which gives an electrical energy upon receipt of an input signal. The control unit **3** is composed of a light emitting diode **4** connected to give off a light upon conduction between input terminals **1**, a photovoltaic cells **5** which generate a photovoltaic voltage upon receiving an optical signal from the light emitting diode **4**, and a driver **6** connected in circuit to develop an operating voltage from the photovoltaic voltage and apply the

operating voltage to gates of the individual FETs. The control unit **3** is provided in the form of a single chip **8** which is mounted together with chips of FETs on a supporting plate **9** of an electrically conductive material, as shown in FIG. 2.

Sources **S** of the two FETs **T** are connected to each other through the supporting plate **9**, while gates **G** of the two FETs are commonly connected a corresponding electrode of the control unit **3**. Drains **D** of the two FETs are connected respectively to output terminals **2** formed separately from the supporting plate **9**. Alternatively, the two FETs and the chip **8** of the control unit **3** may be mounted respectively on separate supporting plates. The two FETs and the chip of the control unit **3** are encapsulated in a molded relay housing together with the associated supporting plate or plates.

Referring now to FIGS. 3 and 4, there is shown a cross-section of LDMOSFET provided in an SOI (Silicon-On-Insulator) structure which comprises a silicon layer **10**, a buried oxide layer of SiO2 **20** and a silicon substrate **30**. The silicon layer **10** is of a first conductive type, typically N-type in which a well region **11** of the second conductive type, i.e., P-type is diffused to extend around the periphery of the silicon layer **10**. The well region **11** extends the full depth of the silicon layer to have its bottom surface reaching the buried oxide layer **20**. Diffused in the top surface of the well region **11** is a source region **12** of N-type which extends in the form of a closed loop to define the source of FET and to define a loop-shaped channel **13** between the source region **12** and a confronting inner periphery of the well region **11**. A drain region **14** of N-type is diffused centrally in the top surface of the silicon layer **10** within a confine of the well region **11** in a laterally spaced relation therefrom to define the drain of FET. Extending centrally through the

silicon layer **10** and through the drain region **14** is an insulator stud **15** which is formed by LOCOS (Local Oxidation of Silicon) technique to have its top projecting above the top surface of the silicon layer **10** and have its bottom integrating into the buried oxide layer **20**.

The top surface of the silicon layer **10** is covered with a field oxide layer of SiO_2 **40** having a gate layer **41** of doped polysilicon, an aluminum-made gate electrode **43**, an aluminum-made source electrode **42**, and an aluminum-made drain electrode **44**. The gate layer **41** extends over the channel **13** in a spaced relation therefrom to define the gate of FET and is connected to the gate electrode **44**. The source electrode **42** penetrates through the field oxide layer **40** to reach a portion bridging over the source region **12** and the well region **11** on top of the silicon layer **10**, while the drain electrode **44** penetrates through the silicon layer **10** over the insulator stud **15** to contact with an annulus of the drain region around the insulator stud **15**. As shown in FIG. 5, the source electrode **42** is of a closed loop configuration in a horizontal plane and is provided with a square pad **52** for wiring connection to the supporting plate **9**. The drain electrode **44** is formed thereon with a like square pad **54** for wiring connection to the corresponding output terminal **2**. The gate electrode **43** is extends laterally outwardly from the loop-shaped gate layer **41** to have an extension on which a like pad **53** is formed for wiring connection to the corresponding element of the control unit **3**.

Turning back to FIG. 3, the silicon substrate **30** is composed of a N-type upper stratum **31** and a P-type lower stratum **32** placed on the supporting plate **9** through a dielectric layer **35** which may be an oxide, nitride, or non-doped silicon layer integral with the silicon substrate **30** or a separately formed dielectric layer. The upper stratum **31** includes

a cavity **33** which is formed at an interface with the buried oxide layer **20** to extend in an opposed relation to a portion of the silicon layer **10** ranging from the drain region **14** to the inner periphery of the well region **11**.

In the above structure, a primary drain-source capacitance is developed in a lateral path between the drain source region **14** and the well region **11**. However, because of the bottom of the well region **11** contacts directly with the buried oxide layer rather than through a portion of the silicon layer **10** having intrinsically large specific capacitance than the oxide layer **20**, the primary drain-source capacitance developed in the primary vertical path is much reduced.

As a result of the supporting plate **9** is utilized to be electrically connected to the source, there develops a secondary drain-source capacitance in a vertical path from the drain region **14** or drain electrode **44** to the supporting plate **9** through corresponding portions of the buried oxide layer **20**, the silicon substrate **30**, and the dielectric layer **35**. Although the secondary capacitance is smaller than the primary capacitance owing to the intervention of the buried oxide layer **20** of small specific capacitance, the secondary capacitance is connected in parallel with the primary capacitance to increase the parallel sum of the capacitance. Therefore, it is required to reduce the secondary capacitance as much as possible. The secondary capacitance can be reduced by the provisions of the insulator stud **15**, the dielectric layer **35**, the P-N junction in the silicon substrate **30**, and the cavity **33** in the silicon substrate **30**. Firstly, the insulator stud **15** can reduce an effective area of the drain region **14** responsible for developing the secondary capacitance with the supporting plate **9**, while assuring sufficient dimensions for providing the pad **54** on the drain electrode **44**,

thereby reducing the secondary capacitance developed in the vertical path. Secondly, the intervention of the dielectric layer **35** will add a capacitance which is added in series capative connection with the capacitance of the buried oxide layer to thereby lower the secondary capacitance. Thirdly, the P-N junction formed in the silicon substrate **30**, i.e. between the upper and lower stratums **31** and **32** will develop a depletion layer which develops a capacitance to be connected in a series relation with the capacitance of the buried oxide layer **20**, lowering the secondary capacitance. Further, the cavity **33** at the interface between the buried oxide layer **20** and the silicon substrate **30** can adds a capacitance in series capative connection with the capacitance of the buried oxide layer **20** to lower the secondary capacitance. Accordingly, the overall drain-source capacitance can be much reduced to thereby minimize the output capacitance between the output terminals **2** of the relay. It should be noted in this connection that although the provisions of the insulator stud **15**, the dielectric layer **35**, the PN-junction in the silicon substrate **30**, and the cavity **33** in the silicon substrate **30** are preferred to reduce the secondary drain-source capacitance and therefore the overall drain-source capacitance, the overall drain-source capacitance can be reduced sufficiently without any of these features.

FIG. 6 illustrates a solid-state relay in accordance with a second embodiment of the present invention in which each of two MOSFETs **T** is mounted on a separate supporting plate **9A** of electrically conductive material and has its gate connected to a like control unit chip **3A** mounted on a separate frame **7**. Drain of each FET is electrically connected to each supporting plate **9A** formed with an output terminals **2A** as an integral part thereof.

As shown in FIGS. 7 and 8, FET is also of the SOI structure having an N-type silicon layer **10A**, a buried oxide layer **20A**, and a silicon substrate **30A**. A P-type well region **11A** of a closed loop configuration is diffused in the silicon layer **10A** over the full depth thereof so as to leave therearound a peripheral isolated zone **16**. A P-type source region **12A** of the like closed loop configuration is diffused in the top surface of the well region **11A** to define the source of FET as well as to define a channel **13A** between the source region **12A** and a confronting inner periphery of the well region **11A**. An N-type drain region **14A** is diffused centrally in the top surface of the silicon layer **10A** within a confine of the well region **11A** to define the drain of FET. Extending immediately around of the well region **11A** is a dielectric separator ring **17** of silicon oxide formed by the LOCOS method to have its bottom reaching the buried oxide layer **20A**. The separator ring **17** projects above the silicon layer **10A** and merges into a field oxide layer **40A** covering the top surface of the silicon layer **10A**. The field oxide layer **40A** includes a gate layer **41A** of doped polysilicon extending in a closed loop over the channel **13A** in a spaced relation therefrom to define the gate of FET. The gate layer **41A** is electrically connected to a gate electrode **43A**. Drain electrode **44A** and source electrode **42A** are formed to penetrate through the field oxide layer **40A** for electrical connection respectively with the drain region **14A** and a portion bridging the source region **12A** and the well region **11A**. The source electrode **42A** and the gate electrode **43A** extend laterally over the separator ring **17** to define individual pads **52A** and **53A** of square configuration for wiring connection to the associated circuit elements, as shown in FIG. 9. A like square pad **54A** is formed centrally on the drain electrode **44A** for wiring connection to the output terminal.

In this embodiment, the peripheral zone **16** is electrically connected to the supporting plate **9A** together with the drain to be kept at the same electrical potential as the drain. With this arrangement, the buried oxide layer **20A** corresponding to the peripheral zone **16** will not act to cause any capacitance which is added in parallel with the primary drain-source capacitance and also with the secondary capacitance formed in a vertical path from the bottom of the well region **11A** and the supporting plate **9A**. In this sense, the overall drain-source capacitance can be much reduced even with the presence of the peripheral zone **16**. In addition, the separator ring **17** can prolong a horizontal path from the well region **11A** to the peripheral zone **16**, thereby reducing a capacitance therebetween and therefore serving to minimize the overall drain-source capacitance.

Also in this embodiment, the silicon substrate **30A** is composed of an N-type upper stratum **31A** and a P-type lower stratum **32A** placed on the supporting plate **9A** through a dielectric layer **35A**. The upper stratum **31A** includes a cavity **33A** of annular configuration in a horizontal plane which is formed at an interface with the buried oxide layer **20A** to extend horizontally in an opposed relation to a portion of the silicon layer **10A** covering the well region **11A** and the separator ring **17**. The cavity **33A**, the P-N interface between the stratums **31A** and **32A**, as well as the dielectric layer **35A** function to reduce the overall drain-source capacitance in the same manner as explained with reference to the first embodiment.

FIGS. 10 to 12 illustrate another structure of SOI-LDMOSFET in accordance with a third embodiment of the present invention. FET of

illustrated structure is adapted in use for the circuit configuration as shown in FIG. 6, and comprises a N-type silicon layer **10B**, buried oxide layer **20B**, and a silicon substrate **30B**. A P-type well region **11B** of a closed loop configuration is diffused in the silicon layer **10B** over the full depth thereof so as to leave therearound a peripheral isolated zone **16B**. A P-type source region **12B** of the like closed loop is diffused in the top surface of the well region **11B** to define a channel **13B** between the source region **12B** and a confronting inner periphery of the well region **11B**. An N-type drain region **14B** is diffused centrally in the top surface of the silicon layer **10B** within a confine of the well region **11B**. Locally diffused in the peripheral zone **16B** are a pair of P-type land **18** which extend the full depth of the silicon layer **10B** and arranged in a horizontal plate to be diametrically opposed to each other. The top surface of the silicon layer **10B** is covered by a field oxide layer **40A** provided with a gate layer **41B** of doped polysilicon which extends over the channel **13B** in a spaced relation therefrom and is electrically connected to a gate electrode **43B**. Drain electrode **44B** and source electrode **42B** are formed to penetrate through the field oxide layer **40B** for electrical connection respectively with the drain region **14B** and a portion bridging the source region **12B** and the well region **11B**. The source electrode **42B** and the gate electrode **43B** extends laterally over the P-type lands **18** to define thereat individual pads **52B** and **53B** of square configuration for wiring connection to the associated circuit elements, as shown in FIG. 12. A like square pad **54B** is centrally formed on the drain electrode **44B** for wiring connection to the output terminal.

Also in this embodiment, the peripheral zone **16B** is electrically connected to the supporting plate **9B** together with the drain to be kept at

the same electrical potential as the drain for reducing the overall drain-source capacitance for the same reason as explained in the second embodiment. With the provision of the lands **18** below the pads **52B** and **53B** for the source and gate electrodes **42B** and **43B**, each land adds its own capacitance resulting from the P-N junction with the peripheral zone **16B** in series connection with a capacitance of the field oxide layer **40B** caused by the pad, thereby reducing the capacitance developed between each pad to the peripheral zone **16B**. Otherwise, the capacitance of the field oxide layer **40B** would be alone connected in parallel with the inevitable drain-source and drain-gate capacitance to eventually increase the overall drain-source and gate-drain capacitance.

The silicon substrate **30B** is of N-type formed with a recess **34** which is of an annular-shape in a horizontal plane and which extends the full depth of the silicon substrate **30B**. The recess **34** covers a portion of the silicon layer **10B** ranging laterally outwardly m the well region **11B** and to the lands **18B**, thus forming a capative element between the supporting plate **9B** and the well regions **11B** as well as the pads **52B** and **53B**. The resulting capacitances are connected in series with the inevitable drain-source and gate-drain capacitance including those caused by the provision of the pads, thereby reducing the overall drain-source and gate-drain capacitance. A like dielectric layer **35B** is provided on the supporting plate **9B** for the same purpose as discussed in the previous embodiment.

Instead of providing the lands **18** in the silicon layer **10B**, it is equally possible to provide like lands of N-type within the well region **11B** in a laterally isolated relation from the source region **12B** for reducing the drain-source and gate-drain capacitance resulting from the provision of the pads for the source and gate electrodes.

It should be noted that, although the above illustrated embodiment discloses the configuration in which the drain region surrounded by the well region, it is equally possible to provide a configuration in which a like well region is formed centrally in the silicon layer and surrounded by a like drain region. In this modification, a peripheral zone around the drain region is electrically connected to a like supporting plate together with the source region. Also, a like separator ring may be formed around the drain region to electrically isolate the drain region from the peripheral zone.

Referring to FIGS. 13 to 15, there is shown a solid-state relay in accordance with a fourth embodiment of the present invention. The relay comprises a pair of LDMOSFETs integrated into a single device of the SOI structure composed of a N-type silicon layer **100**, a buried oxide layer **200**, and a silicon substrate **300**. The single device is mounted on a supporting plate **9** of an electrically conductive material with a dielectric layer **350** interposed therebetween. A P-type well region **111** is diffused in the silicon layer **100** over the full depth thereof in such a manner as to form therein a laterally isolated pair of first and second active zones **101** and **102** of elliptical configuration. Formed respectively around the first and second active zones **101** and **102** are N-type first and second source regions **121** and **122** which are of closed loop configuration and diffused in the top surface of the well region **111** to define individual sources of FETs. The first and second source regions **121** and **122** also defines first and second channel **131** and **132** of closed loop within the well region between the individual source regions and the inwardly opposed peripheries of the first and second active zones **101** and **102**. First and second N-type drain regions **141**

and **142** are diffused in the top surface of silicon layer **100** respectively within the first and second active zone **101** and **102** in a laterally spaced relation to the well region **111** to define individual drains of FETs. First and second insulator studs **151** and **152** are formed by the LOCOS technique to project above the silicon layer **100** from the buried oxide layer **200** through the centers of the first and second drain regions **141** and **142**, respectively.

The top surface of the silicon layer **100** is covered with a field oxide layer of SiO_2 **400** having a pair of first and second gate layers **411** and **412** of doped polysilicon, a gate electrode **431**, a source electrode **421**, and a drain electrode **441**. The first and second gate layers **411** and **412** extend respectively over the first and second channels **131** and **132** in a spaced relation therefrom to define the individual gates of FET and are commonly connected to the gate electrode **431**. The source electrode **421** penetrates through the field oxide layer **400** to reach a portion on the silicon layer **100** bridging over the first and source regions **121** and **122** through the well region **111** formed therebetween for interconnection of the sources of the two FETs. The first and second drain electrode **441** and **442** penetrate through the silicon layer **100** over the insulator studs **151** and **152** to contact with annuli of the first and second drain regions **141** and **142** around the insulator studs. As shown in FIG. 15, the gate electrode **431** is provided with a pad **531** for wiring connection with the associated circuit element, i.e., the control unit as shown in FIG. 1. The first and second drain electrodes **441** and **442** are provided respectively with pads **541** and **542** for wiring connection to output terminals of the relay. The source electrode **421** is provided with a single pad **521** for wiring connection to the supporting plate **9**. The source is not necessarily connected to the supporting plate **9**.

In the above structure, the well region **111** extends the full depth of the silicon layer **100** to form the two isolated active zone **101** and **102** on the buried oxide layer **200**, enabling the formation of the two FETs in a single SOI structure, in addition to reducing the drain-source capacitance because of the reduced area of the well region **111** laterally confronting the drain region **141**, **142** and also because of the lower specific capacitance of the buried oxide layer **200** than the silicon layer **100**.

Despite that the buried oxide layer **200** has the low specific inductive capacitance, it will give a secondary capacitance particularly when the source is electrically connected to the supporting plate **9**. The secondary capacitance is developed substantially in vertical paths from the drain regions **141** and **142** to the supporting plate **9** through the buried oxide layer **200** and is added in parallel capative connection with the primary drain-source capacitance developed substantially in the lateral path from the drain regions to the well region. In order to nevertheless cancel the secondary capacitance as much as possible, the N-type silicon substrate **300** is formed with a pair of laterally spaced recesses **341** and **342** and is placed on the supporting plate **9** through the dielectric layer **350**.

Each of the recesses **341** and **342** extend the full depth of the silicon substrate **300** and has an elliptical configuration in a horizontal plane so as to cover a portion of the silicon layer **100** bounded by each of the first and second source regions **121**, **122** and including the first and second drain regions **141**, **142**. The recesses **341** and **342** and the dielectric layer **350** give individual capacitances which are added in series capative connection with the drain-source capacitance of the buried oxide layer for reducing the total secondary drain-source capacitance, thereby minimizing the overall drain-source capacitance

and therefore the output capacitance.

It should be noted in this connection that the supporting plate could be electrically isolated from the sources as well as from drain of each FET, while assuring a greatly reduced drain-source capacitance. In such modification, the silicon substrate would not require the recesses or cavity, and even the dielectric layer **350** may be eliminated.

Further, it is within the concept of the present invention to combine the specific features of the individual embodiments in order to reduce the secondary source-drain capacitance developed through the buried oxide layer. Those specific features include the provision of the insulator stud **15** through the drain region **14** (typically shown in FIG. 3), the intervention of the dielectric layer **35** between the supporting plate **9** and the silicon substrate **30** (typically shown in FIG. 3), the provision of cavity **33** or recess **34** (typically shown in FIGS. 3 and 10), and the provision of the stratums **31** and **32** of opposed type as the silicon substrate **30** forming therebetween the P-N junction (typically shown in FIG. 3).

LIST OF REFERENCE NUMERALS

1	input terminal
2	output terminal
3	control unit
4	light emitting diode
5	photovoltaic cell
6	driver
7	frame
8	chip (photodetector)
9	supporting plate
10	silicon layer
11	well region
12	source region
13	channel
14	drain region
15	insulating stud
16	peripheral zone
17	separator ring
18	land
20	buried oxide layer
30	silicon substrate
31	upper stratum
32	lower stratum
33	cavity
34	recess
35	dielectric layer
40	field oxide layer
41	gate layer
42	source electrode
43	gate electrode
44	drain electrode
52	pad for source electrode
53	pad for gate electrode
54	pad for drain electrode
60	dielectric layer
100	silicon layer
101	drift region
102	drift region
111	well region
121	source region
122	source region
131	channel
132	channel
141	drain region
142	drain region
151	insulator stud
152	insulator stud
200	buried oxide layer
300	silicon substrate
341	recess
342	recess
350	dielectric layer
400	field oxide layer
411	gate layer
412	gate layer
421	source electrode
431	gate electrode
432	gate electrode
441	drain electrode
442	drain electrode
521	pad for source electrode
531	pad for gate electrode
541	pad for drain electrode

CLAIMS:

1. A solid-state relay having a pair of output terminals for connection with a load to be controlled, said solid-state relay comprising:

a control means (3) which gives an electrical energy upon receipt of an input signal;

a pair of LDMOSFETs (Lateral Double-diffused Metal Oxide Semiconductor Field Effect Transistors), said LDMOSFETs having individual gates connected commonly to receive said electrical energy to be driven thereby, having individual source connected to each other, and having individual drains connected to said output terminals (2), respectively;

at least one supporting plate (9; 9A; 9B) of electrically conductive material mounting thereon said LDMOSFETs;

each of said LDMOSFET comprising:

a silicon layer (10; 10A; 10B, 100) of a first conductive type having top and bottom surfaces,

a drain region (14; 14A; 14B; 141, 142) of said the first conductive type diffused in the top surface of said silicon layer to define said drain of the LDMOSFET;

a well region (11; 11A; 11B; 111) of a second conductive type diffused in said silicon layer in a laterally spaced relation from said drain region;

a source region (12; 12A; 12B; 121, 122) of the first conductive type diffused within said well region to define a channel extending between said source region and a confronting edge of said well region along the top surface of said silicon layer, said source region defining said source of the LDMOSFET;

a drain electrode (44; 44A; 44B; 441,442) being placed on said drain region and electrically connected thereto;

a gate electrode electrically connected to a gate layer (41; 41A; 41B; 411, 412) of an electrically conductive material which is placed over said channel through a dielectric layer to define said gate; and

a source electrode (42; 42A; 42B; 421) being placed over said source region and electrically connected thereto;

characterized in that each of said LDMOSFET is of an SOI (Silicon-On-Insulator) structure which comprises a silicon substrate (30; 30A; 30B, 300), a buried oxide layer (20; 20A; 20B; 200) formed on said silicon substrate, and said silicon layer (10; 10A; 10B; 100) formed on said buried oxide layer, said silicon substrate being mounted on said supporting plate, and wherein said well region extends the full depth of said silicon layer to have a bottom abutted against said buried oxide layer.

2. The solid-state relay as set forth in claim 1, wherein one of said source region and said drain region is configured to surround the other of said source region and said drain region within a plane of said silicon layer.

3. The solid-state relay as set forth in claim 2, wherein said source region is configured to surround said drain region.

4. The solid-state relay as set forth in claim 3, wherein said silicon

layer is formed with a peripheral zone (16; 16B) located outwardly of said well region and isolated from said drain region by said well region, said peripheral zone and said drain region being electrically connected commonly to said supporting plate.

5. The solid-state relay as set forth in claim 3, wherein a separator ring (17) of a dielectric material surrounds closely said well region, said separator ring being formed in said silicon layer to isolate said well region from a peripheral zone of said silicon layer, said peripheral zone and said drain region being electrically connected commonly to said supporting plate.

6. The solid-state relay as set forth in claim 5, wherein at least one of said source electrode and said gate electrode extends laterally over said upper portion of said separator ring (17) from above said well region.

7. The solid-state relay as set forth in claim 4, wherein at least one separated land (18) of the second conductive type is diffused in said silicon layer laterally outwardly of said well region in a spaced relation from said well region, at least one of said source electrode and said gate electrode extends over said at least one separator land in a spaced relation thereto from the corresponding one of said source and said channel to define thereat a wiring pad (52B; 53B) for connection with complementary circuit element.

8. The solid state relay as set forth in claim 4, wherein a land (18) of the first conductive type is diffused within said well region to extend the full depth of said silicon layer in an electrically isolated relation from said source region, at least one of said source electrode and said gate electrode extends over said separator region in a spaced relation thereto from the corresponding one of said source and said channel to define thereat a wiring pad for connection with complementary circuit element.

9. The solid-state relay as set forth in claim 2, wherein the one of said source region and said drain region surrounding the other of said source region and said drain region is electrically connected to said supporting plate of an electrical conductive material so that said supporting plate has the same electrical potential as the one of said well region and said drain region.

10. The solid-state relay as set forth in claim 2, wherein said drain region is configured to surround said well region.

11. The solid-state relay as set forth in claim 10, wherein said silicon layer is formed with a peripheral zone (16; 16B) located outwardly of said drain region, said peripheral zone and said source region being electrically connected commonly to said supporting plate.

12. The solid-state relay as set forth in claim 10, wherein a dielectric separator ring (17) surrounds closely said drain region, said separator ring being formed in said silicon layer to isolate said drain region from a peripheral zone of said silicon layer, said peripheral zone and said source region being electrically connected commonly to said supporting plate.

13. The solid-state relay as set forth in claim 1, wherein said source region (12) is electrically connected to said supporting plate (9).

14. The solid-state relay as set forth in claim 13, wherein said silicon substrate (30) is formed to have a cavity (33) which extends at the interface with said buried oxide layer and has a width covering said drain region.

15. The solid-state relay as set forth in claim 13, wherein said silicon substrate (30B) is formed to have a recess (34) of which bottom is defined by said buried oxide layer and has a width covering said drain region.

16. The solid-state relay as set forth in claim 7, wherein said supporting plate is formed separately from said output terminal.

17. The solid-state relay as set forth in claim 1, wherein said drain

region (14A; 14B) is electrically connected to said supporting plate (9A; 9B).

18. The solid state relay as set forth in claim 17, wherein said silicon substrate (30A) is formed with a cavity (33A) which extends at the interface with said buried oxide layer (20A) and has a width covering said source.

19. The solid-state relay as set forth in claim 17, wherein said silicon substrate (300) is formed to have a recess (341, 342) of which bottom is defined by said buried oxide layer (200) and has a width covering said source region (121, 122).

20. The solid-state relay as set forth in claim 17, wherein said supporting plate (9A) is formed to have said output terminal (2A) as an integral part thereof.

21. The solid-state relay as set forth in claim 1, wherein an insulator stud (15; 151, 152) extends from said buried oxide layer (20; 200) through a center of said drain region (14; 141, 142) to project on the top surface of said silicon layer so as to expose said drain region in an annular shape around said stud, said drain electrode extending over said insulator stud with a peripheral portion of the drain electrode being electrically connected to said drain region of the annular shape.

22. The solid-state relay as set forth in claim 1, wherein said silicon substrate (30; 30A) comprises a pair of semiconductor stratums (31, 32; 31A, 32A) of opposite conductive type.

23. The solid-state relay as set forth in claim 1, wherein a dielectric layer (35; 35A; 35B; 350) is formed on a bottom of the silicon substrate opposite of said buried oxide layer.

24. The solid-state relay as set forth in claim 1, wherein said well region (111) is formed in said silicon layer over the full depth thereof in such a manner as to form therein a laterally isolated pair of first and second active zones (101,102) around which a pair of first and second source regions (121,122) are formed respectively in said well region, and wherein a pair of first and second drain regions are formed respectively in said first and second active zones to realize both of said LDMOSFETs in a single device structure,

said first and second source regions (121,122) being diffused respectively within said well region (111) so as to be laterally spaced from each other and defining first and second channels (131, 132) each extending between each of said first and second source regions to a confronting edge of each corresponding one of said first and second active zones along the top surface of said silicon layer, said first and second source regions defining first and second sources of the two LDMOSFETs, respectively;

said first and second drain regions (141, 142) being diffused respectively within said first and second active zone so as to be isolated from each other by said well region and to define the drains of the two LDMOSFETs, respectively;

first and second drain electrodes (441, 442) placed respectively on said first and second drain regions in an electrical connecting relationship therewith;

at least one gate electrode (431) being electrically connected to first and second gate layers (411, 412) which are placed over said first and second channels respectively through dielectric layers and define first and second gates of said two LDMOSFETs, respectively;

a common source electrode (421) bridging over said first and second source regions and being electrically connected thereto;

said first drain (141) being cooperative with said first gate (411) and said first source (121) to make the one of said LDMOSFETs, while said second drain (142) is cooperative with said second gate (412) and said second source (122) to make the other LDMOSFET, and

said silicon substrate which carries said silicon layer through said buried oxide layer being mounted on said supporting frame with said output terminals being electrically connected respectively to said first and second drains.

25. The solid-state relay as set forth in claim 24, wherein said silicon substrate is electrically isolated from said first and second sources and said first and second drains, said output terminals being formed separately from said supporting plate.

Fig. 1

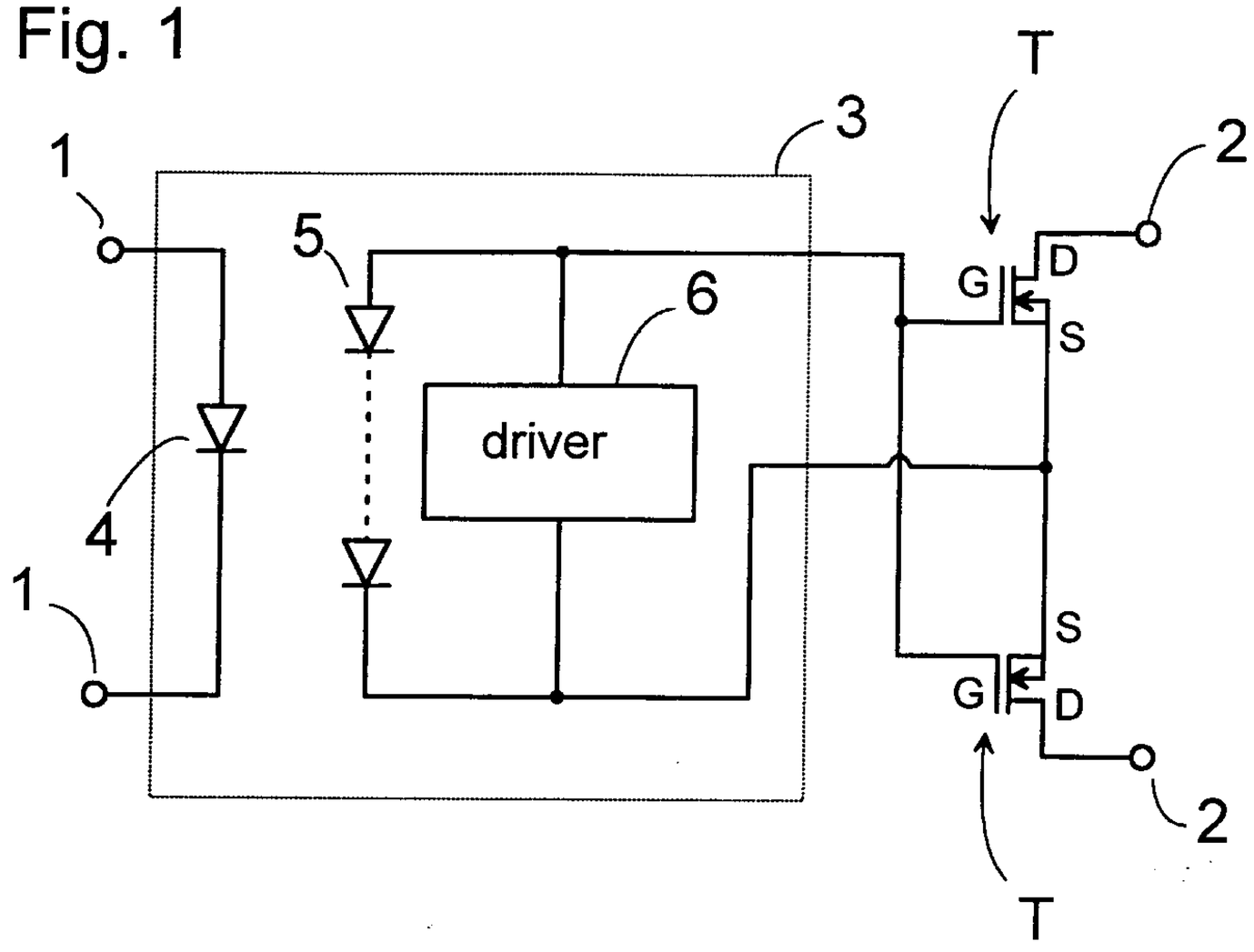

Fig. 2

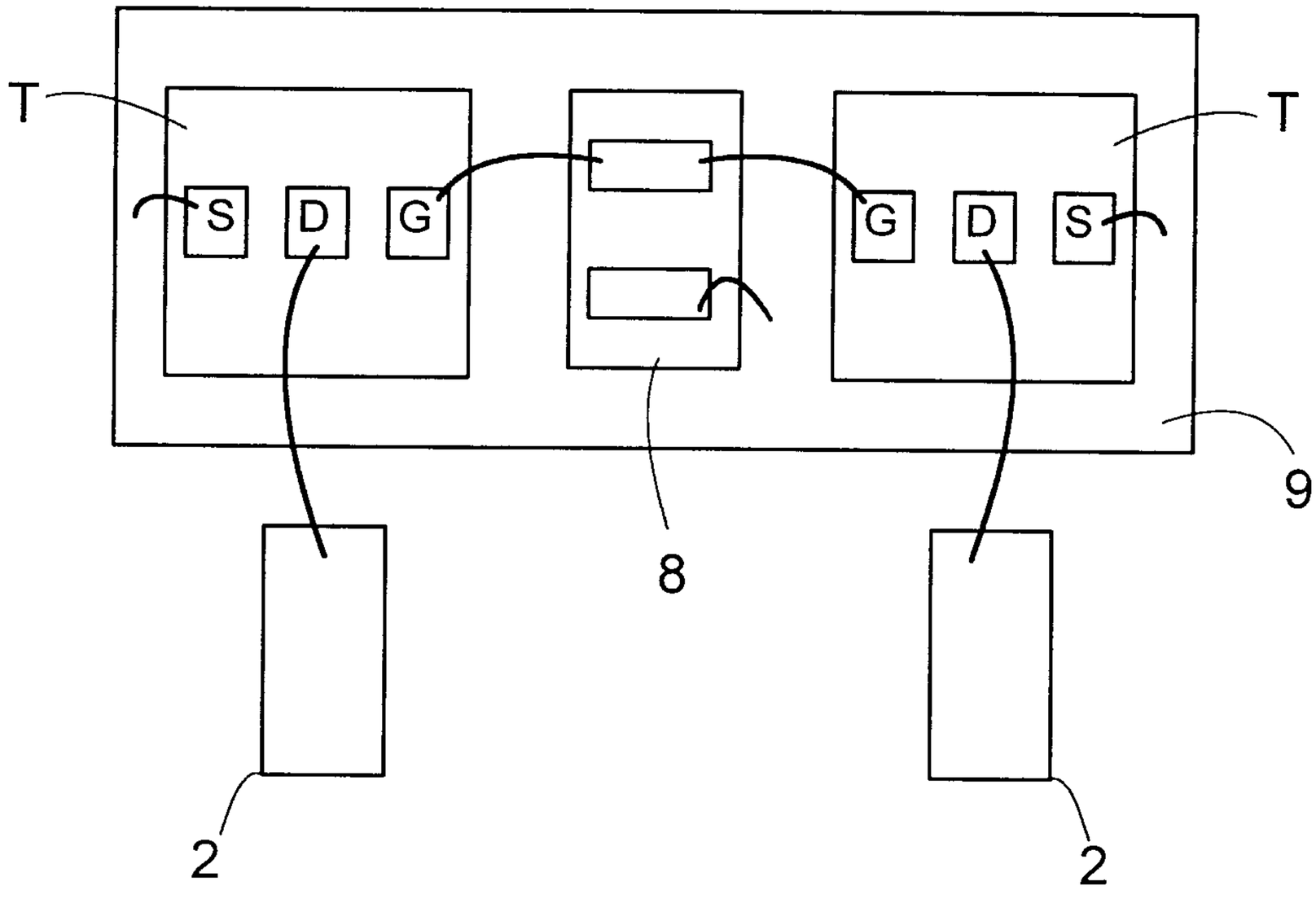

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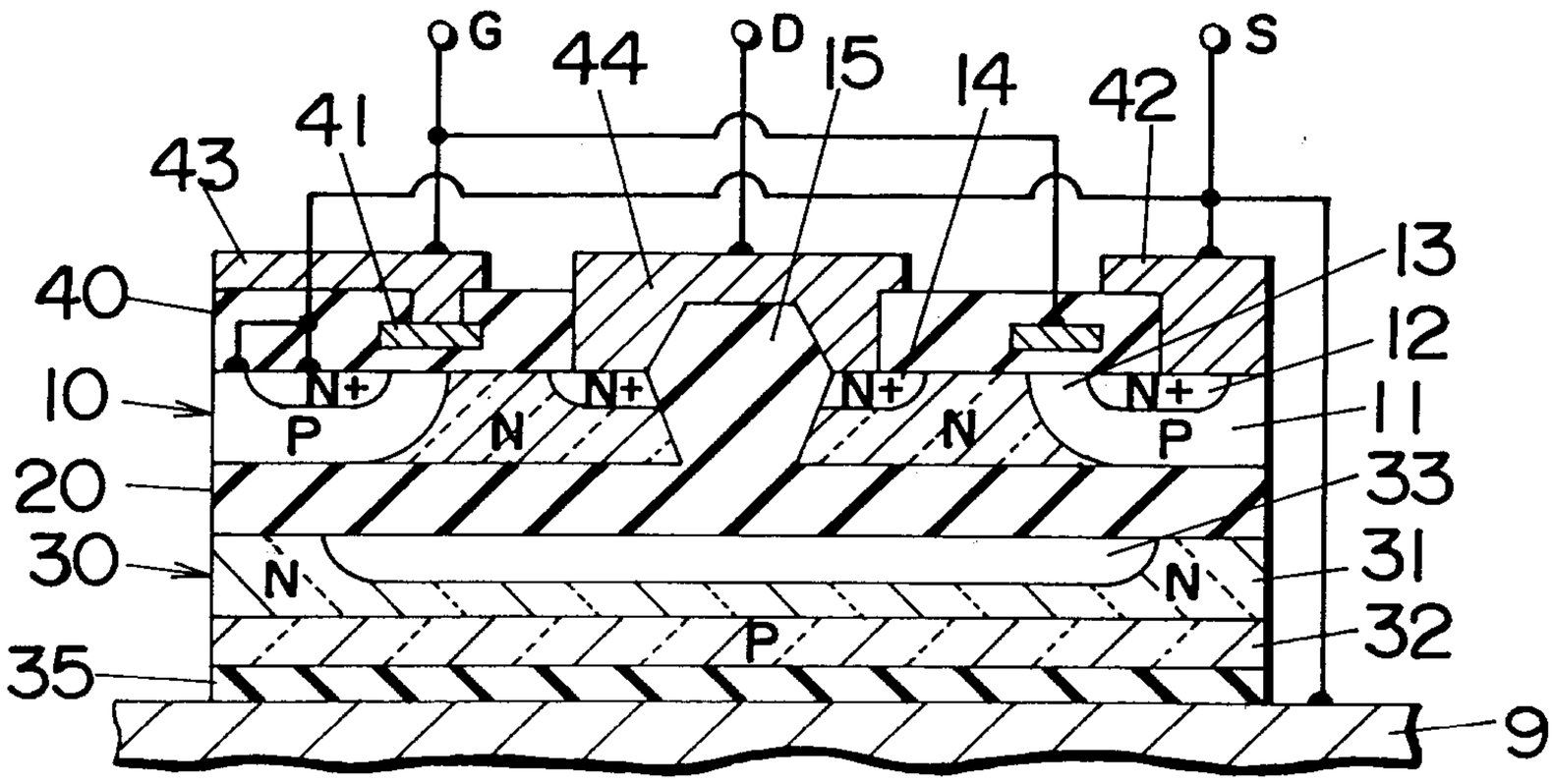
Fig.3


G
44
D
15
14
42
S
41
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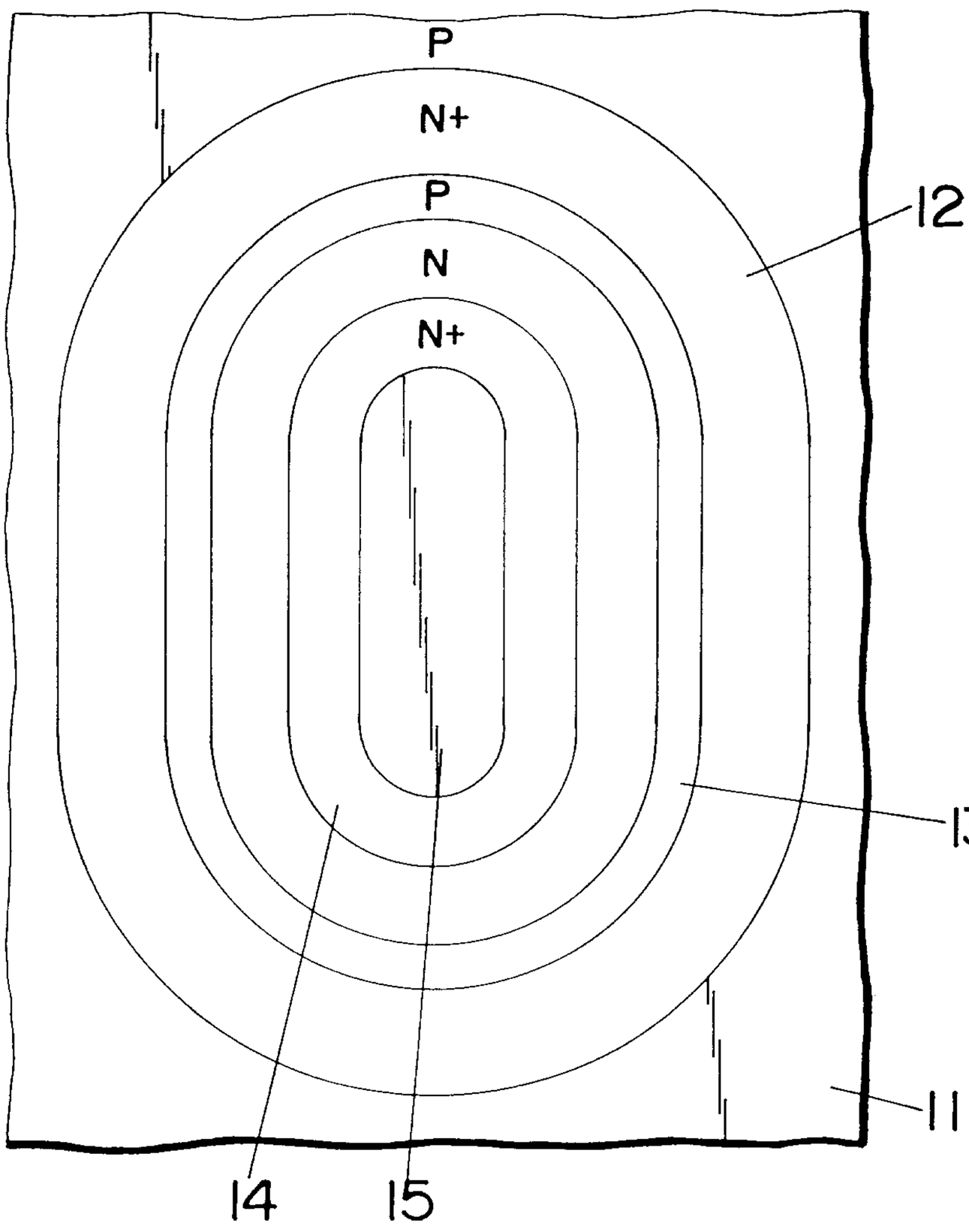
13
12
11
33
31
32
9
40
10
20
30
35
N+
P
N

Fig.4


P
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N
N+
12
13
11
14
15

Fig.5

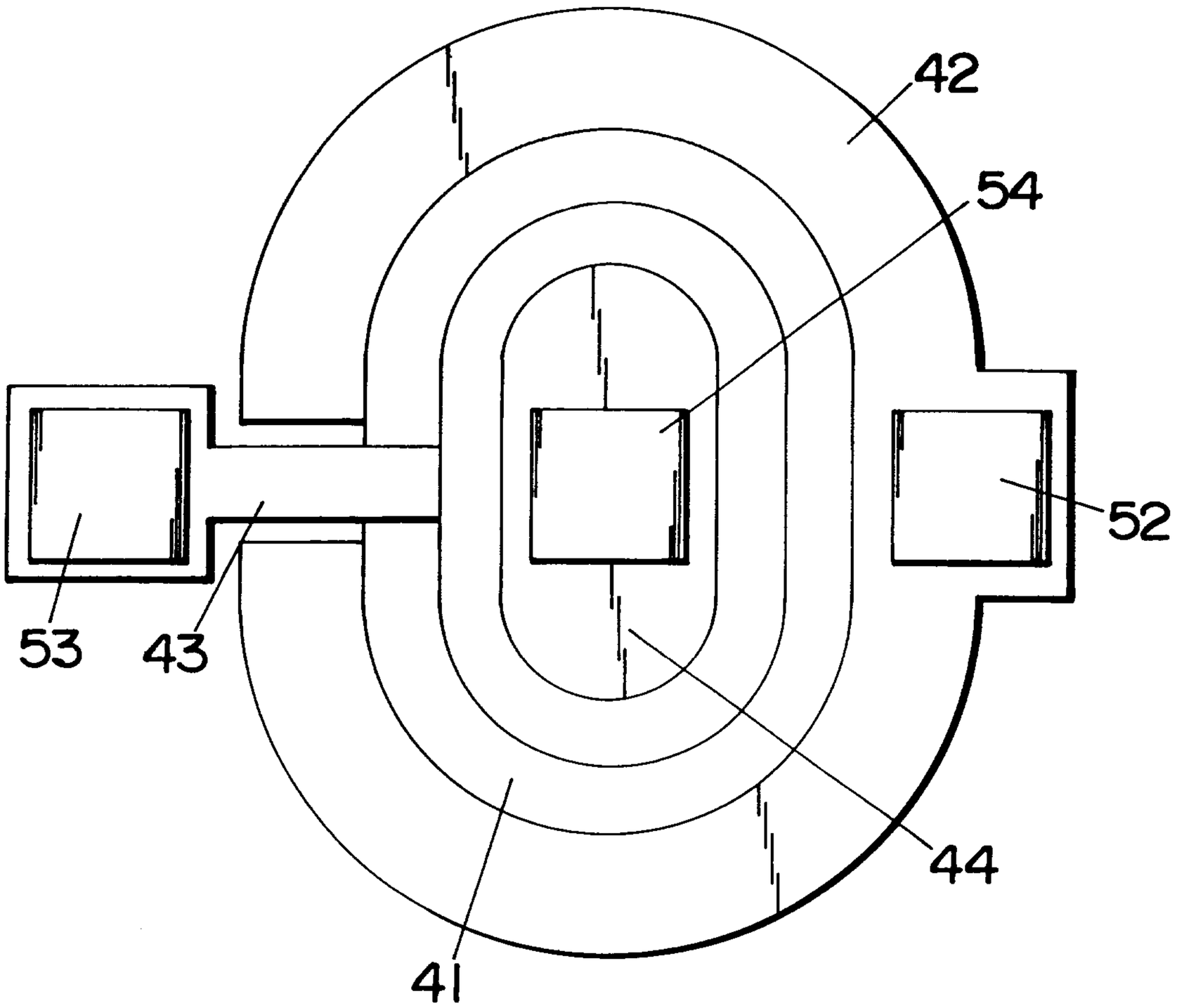

Fig. 6

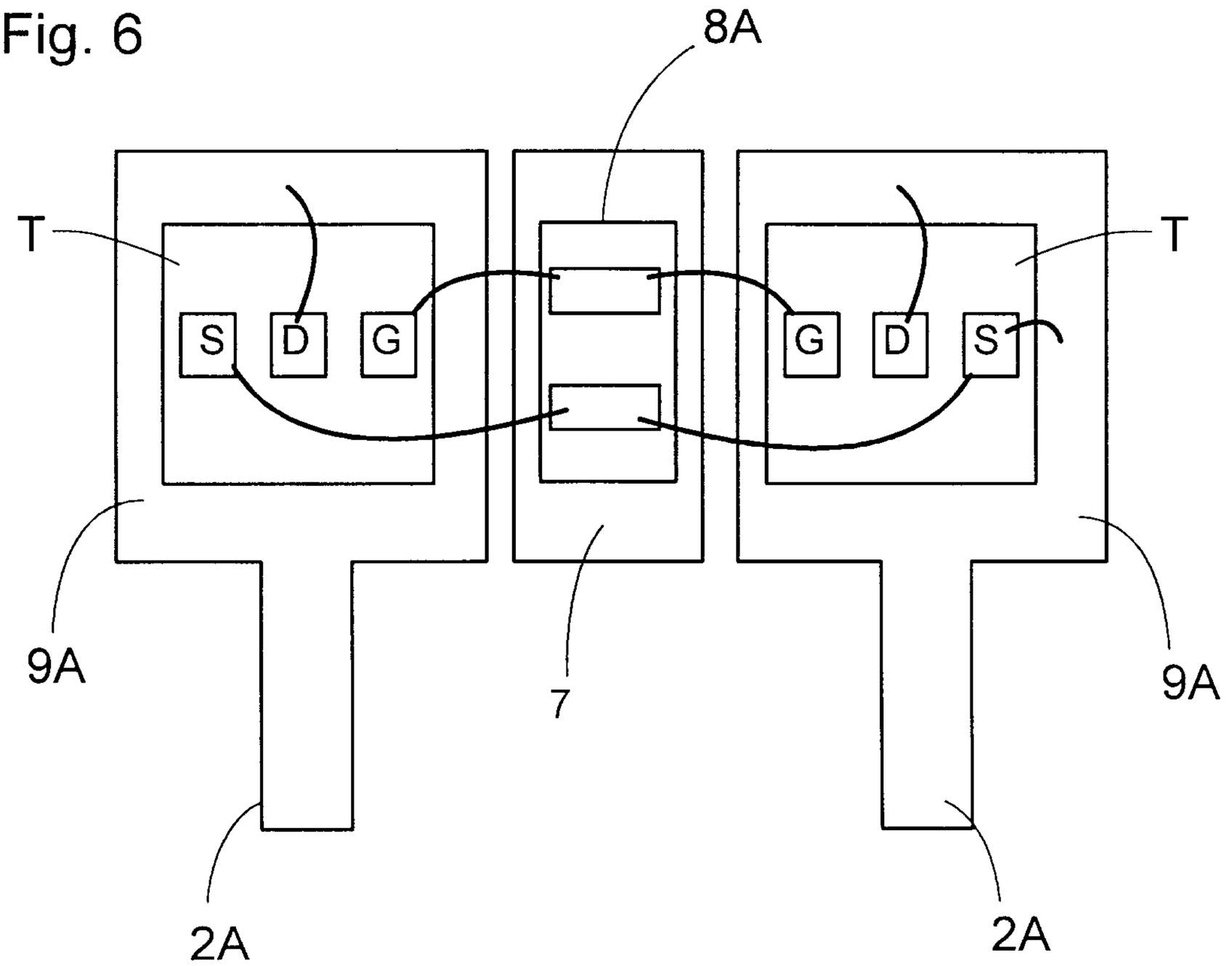

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Fig.7

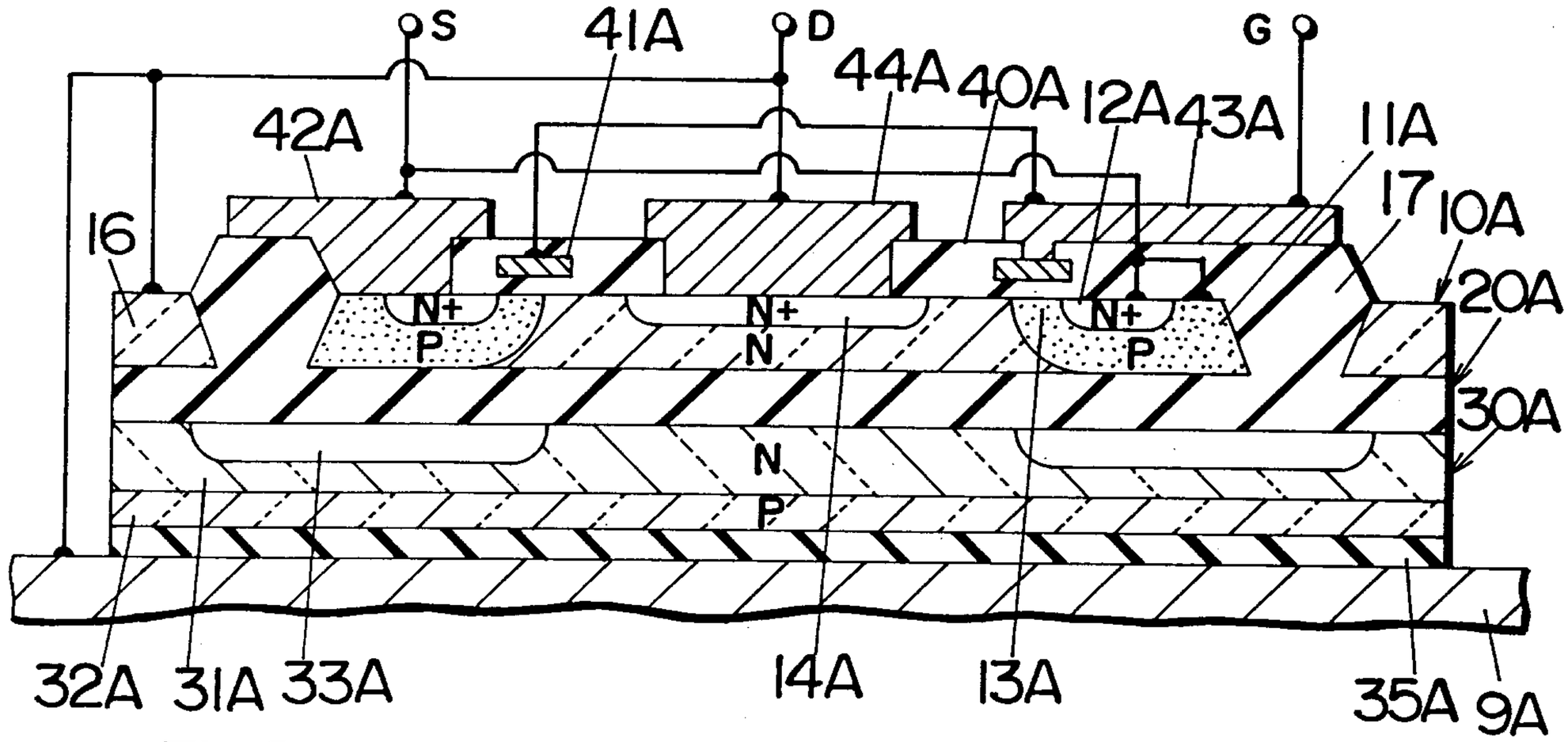

Fig.8

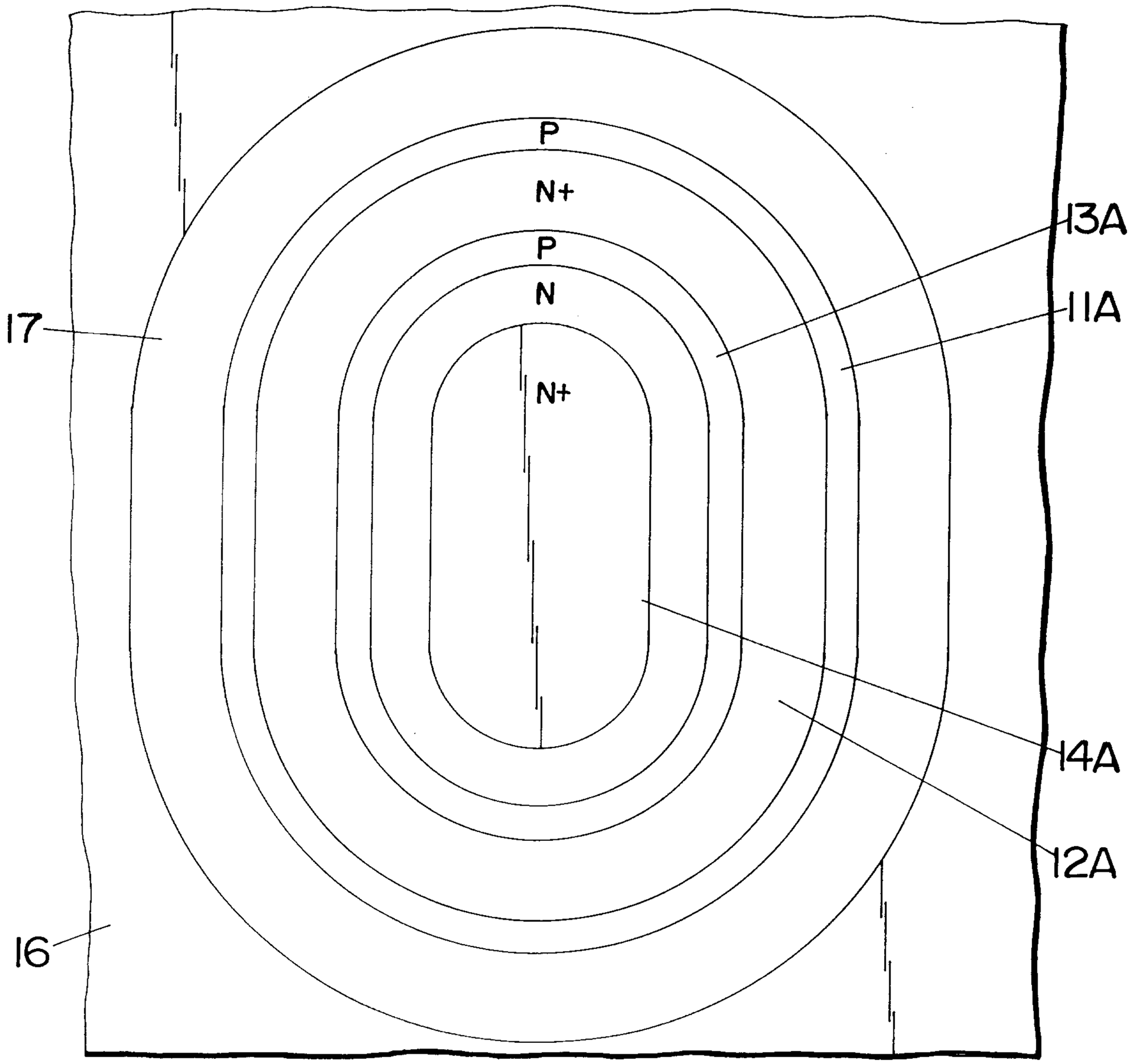

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Fig.9

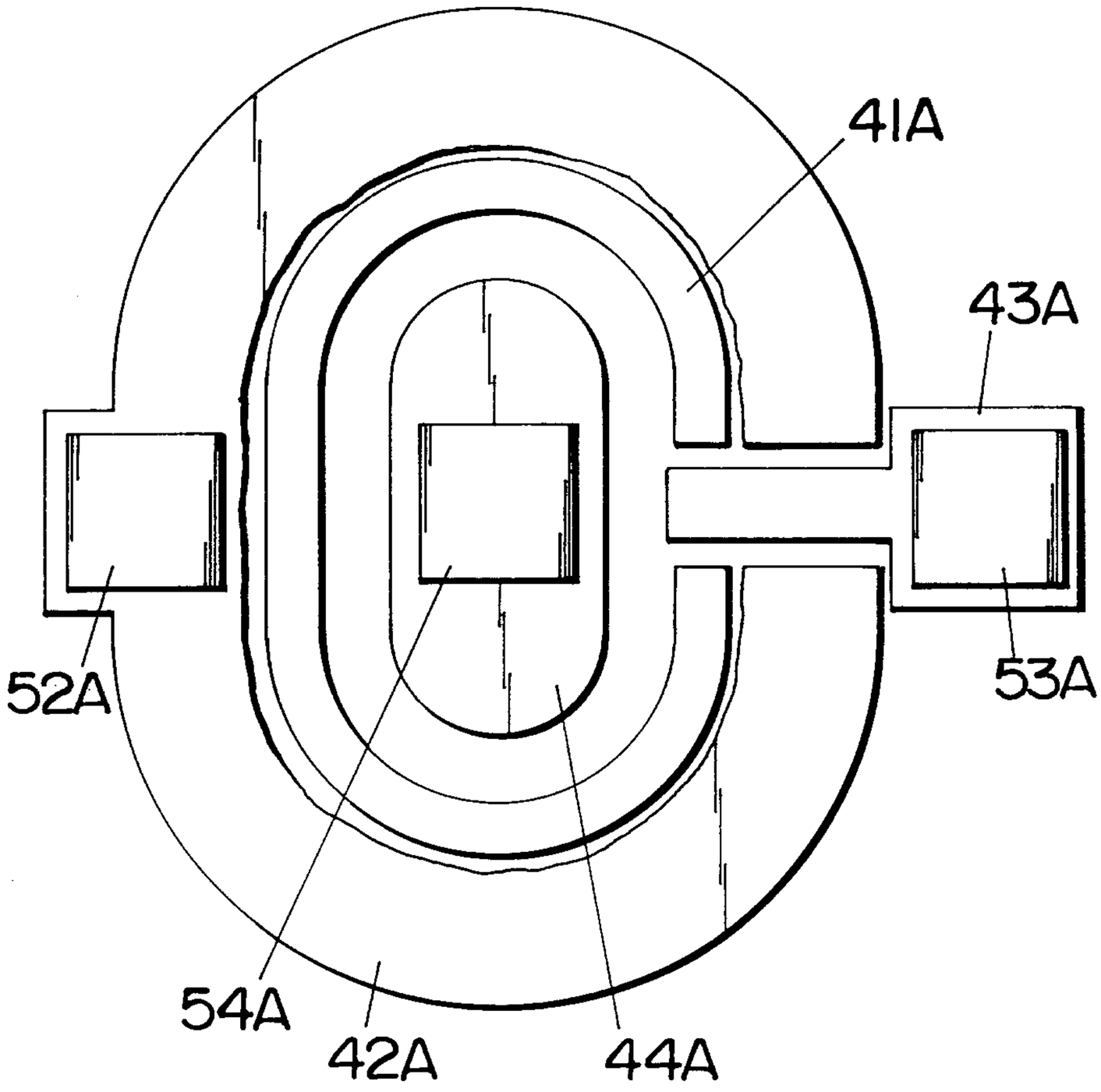

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Fig.10

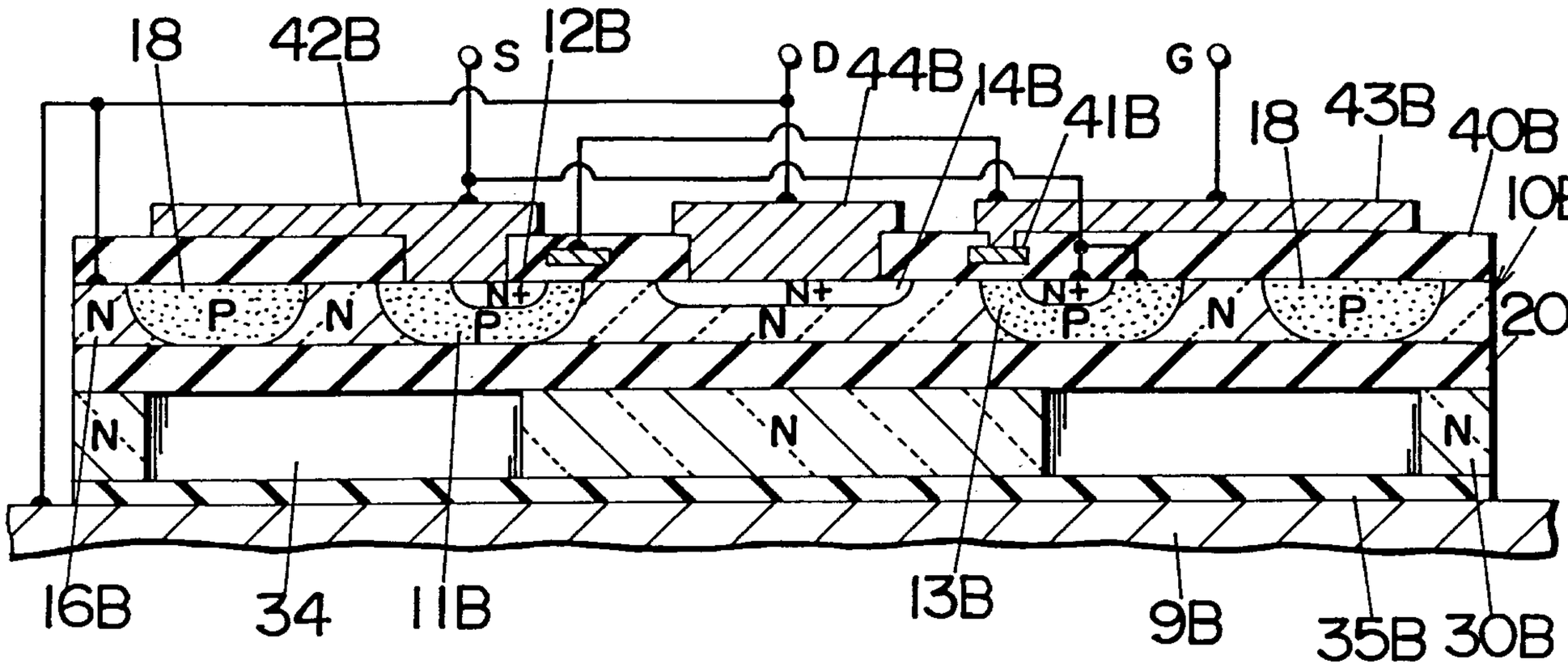
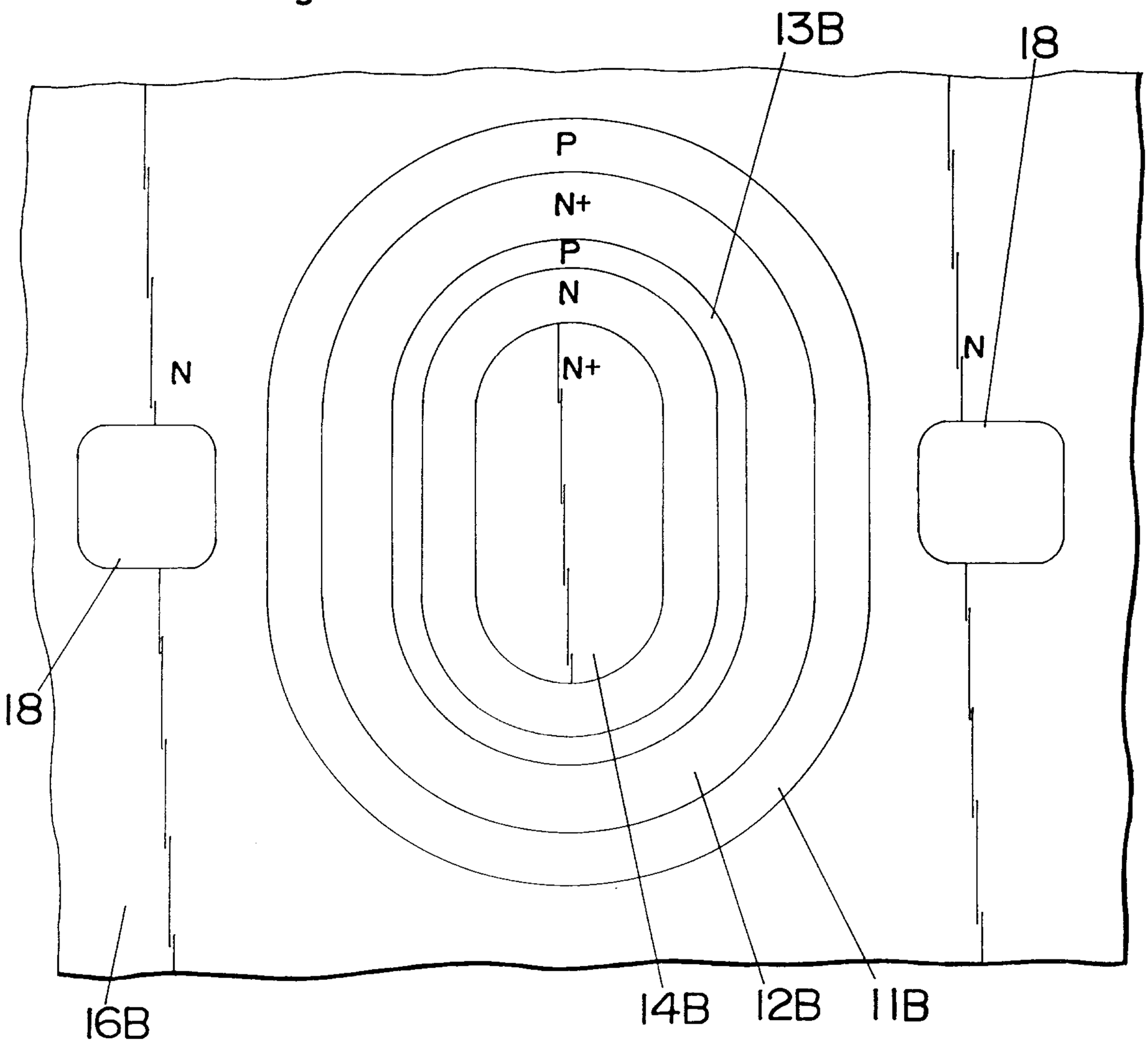

18
42B
S
12B
D
44B
14B
41B
G
18
43B
40B
10B
20B
N
P
N
N+
N+
N+
P
N
P
N
N
N
N
16B
34
11B
13B
9B
35B
30B

Fig.11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11B

Fig.12

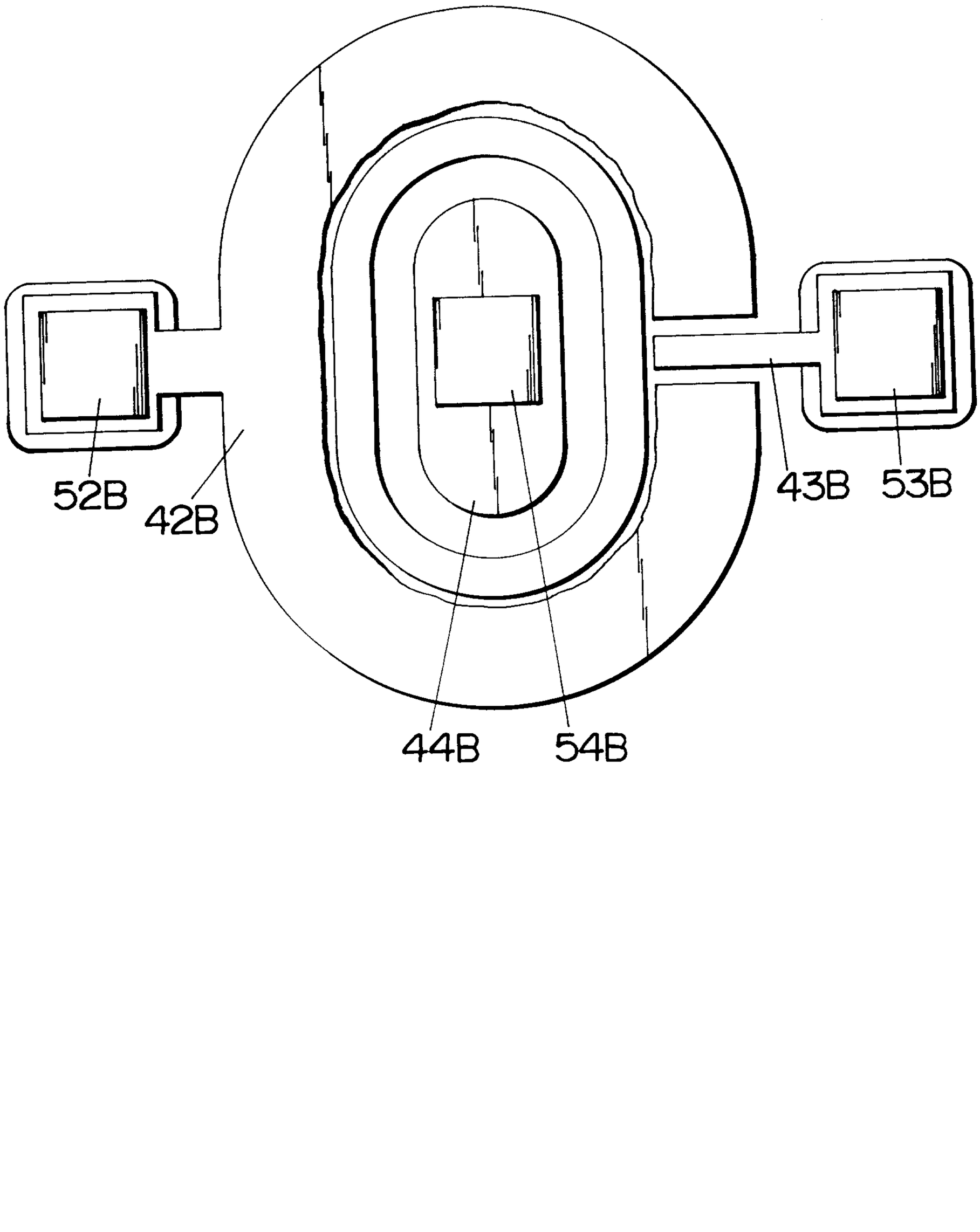

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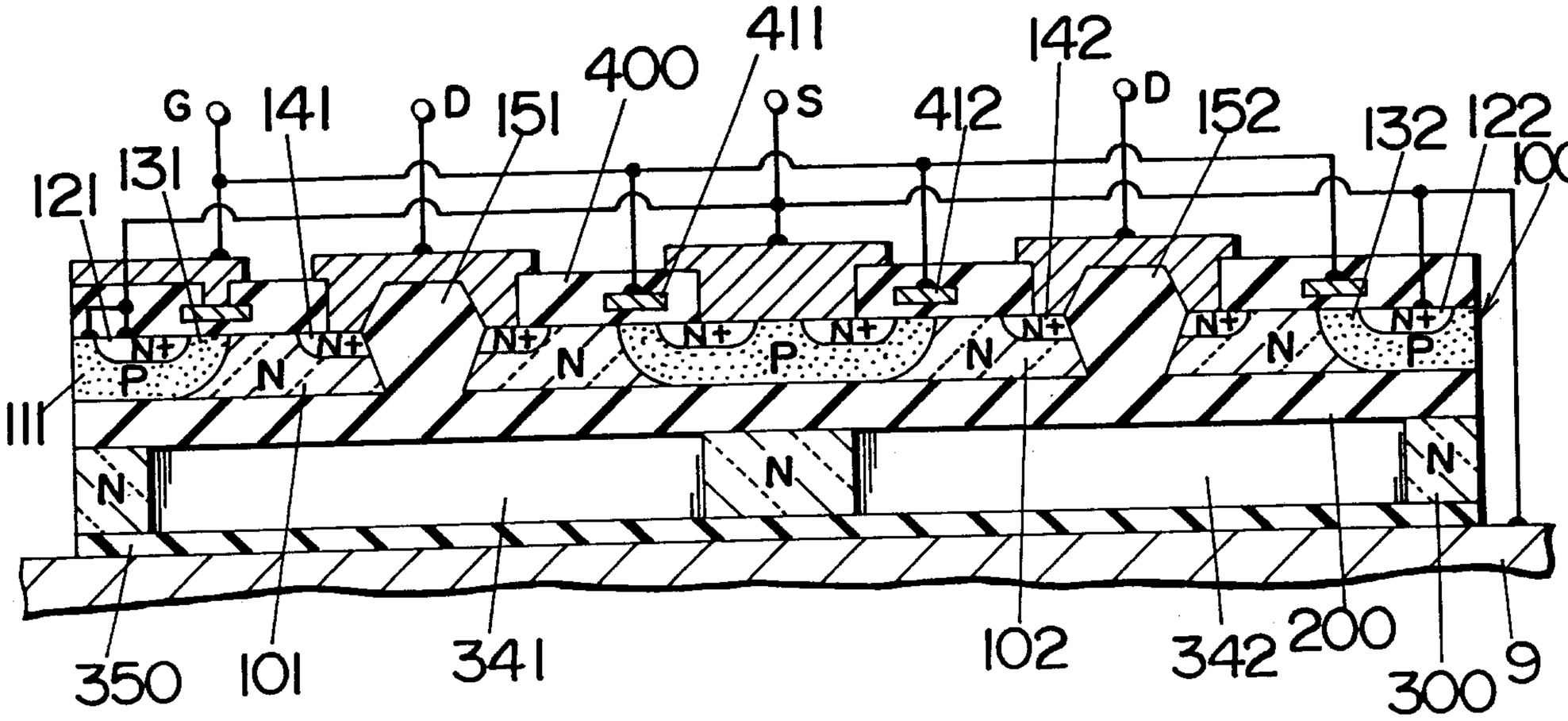
Fig.13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141
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412
D
152
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122
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131
111
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N+
N
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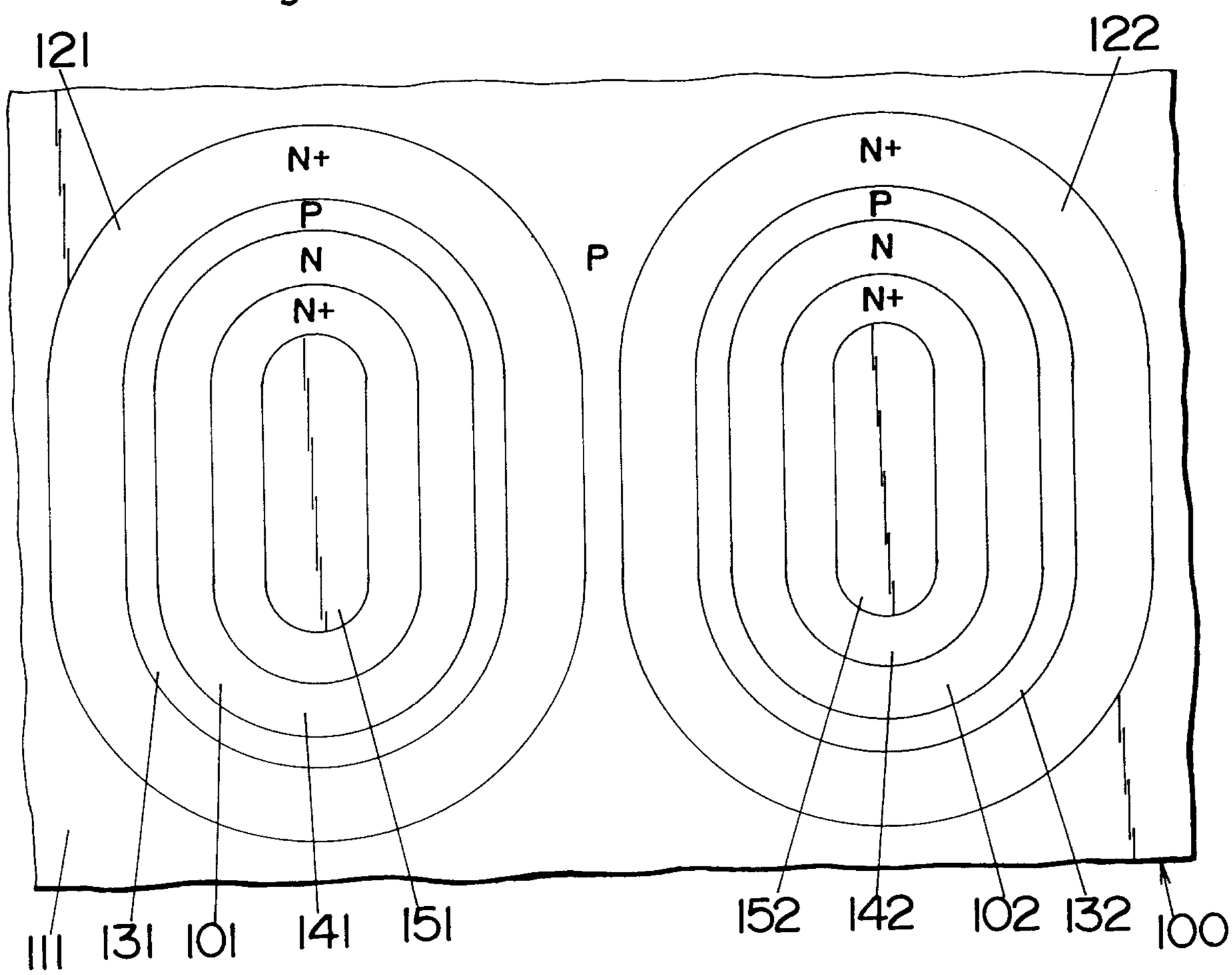
200
300
9

Fig.14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152
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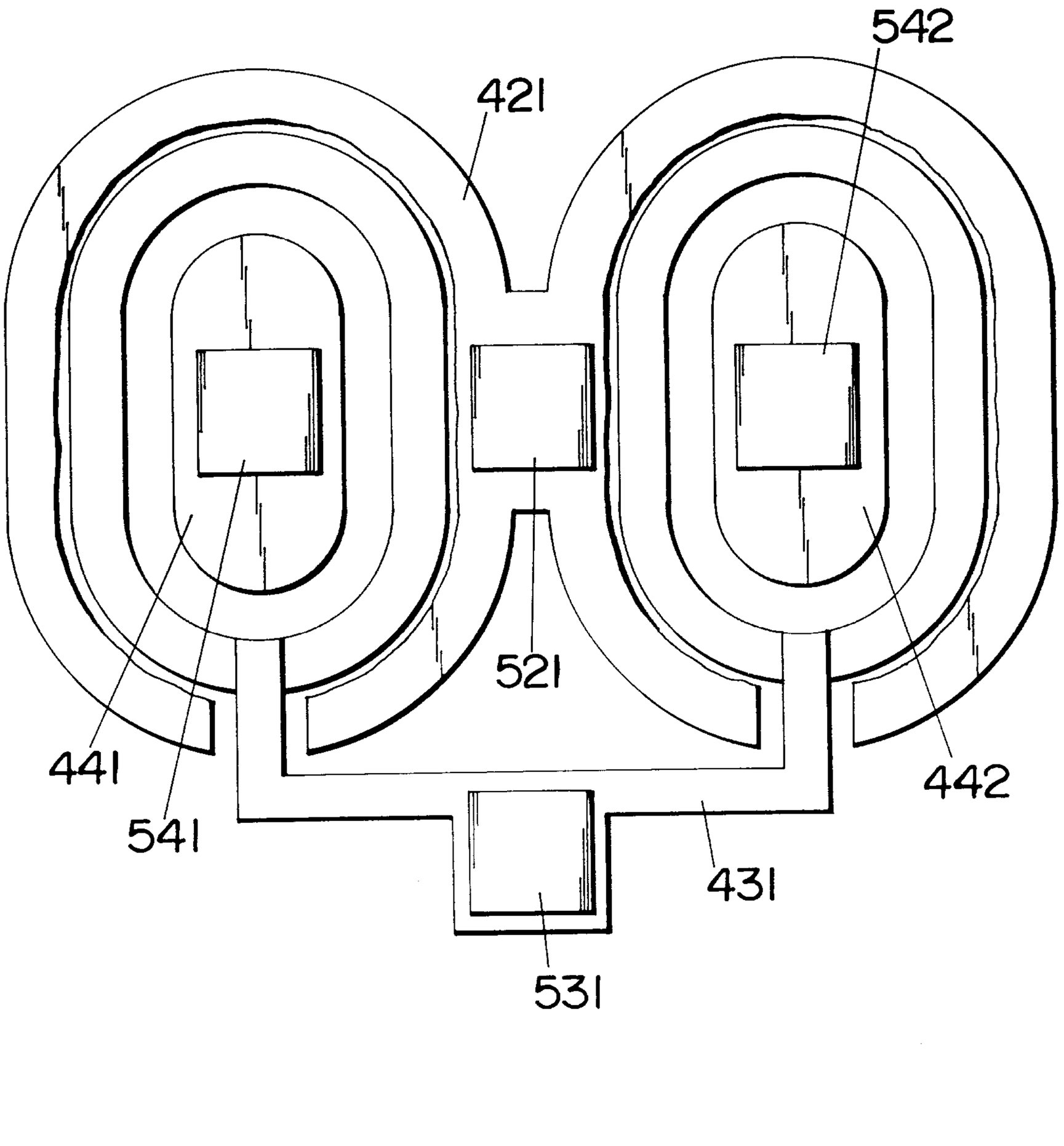
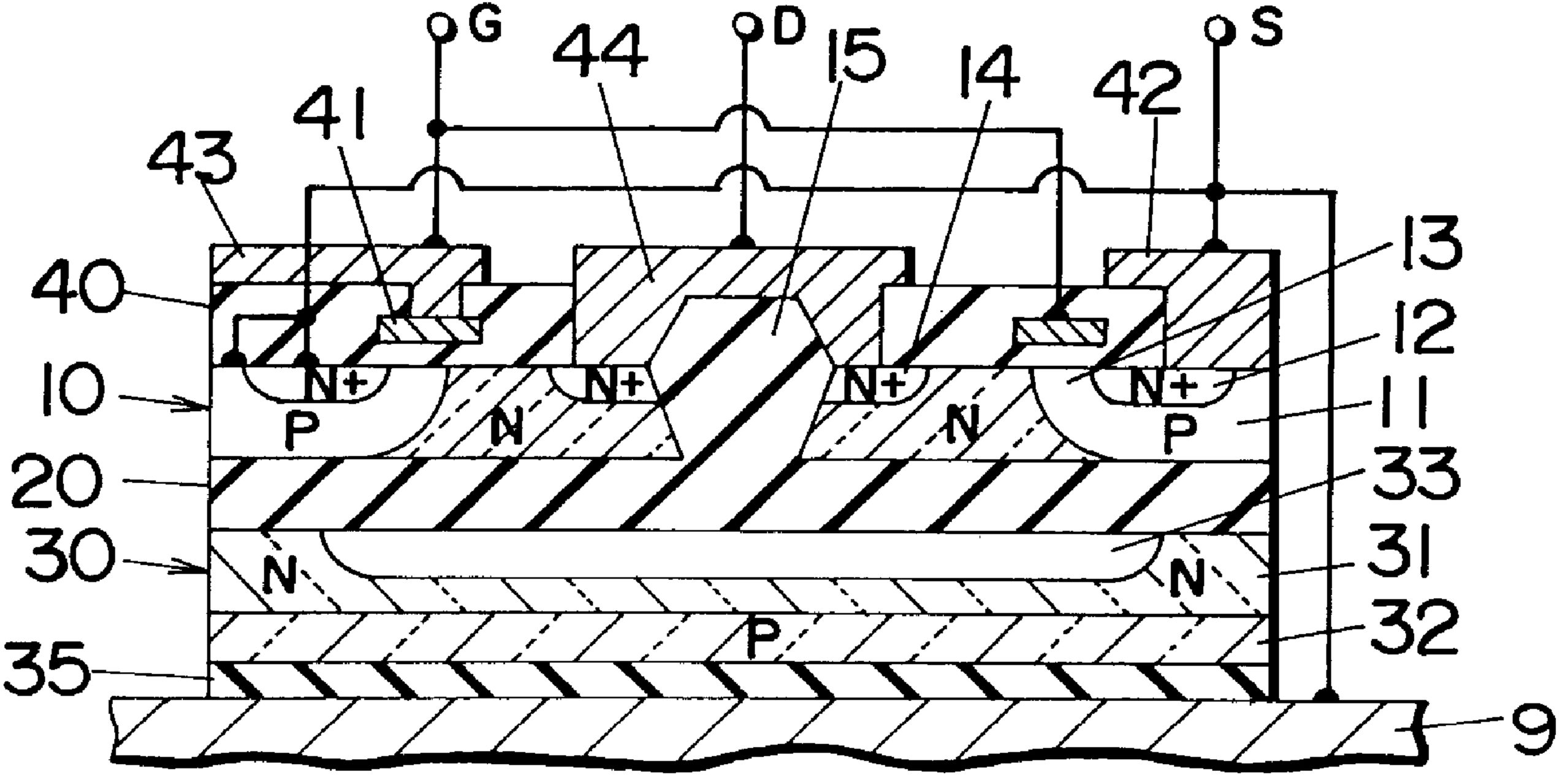
102
132
100

Fig.15




G
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33
31
32
9
N+
N+
N+
N+
P
N
N
P
N
N
P