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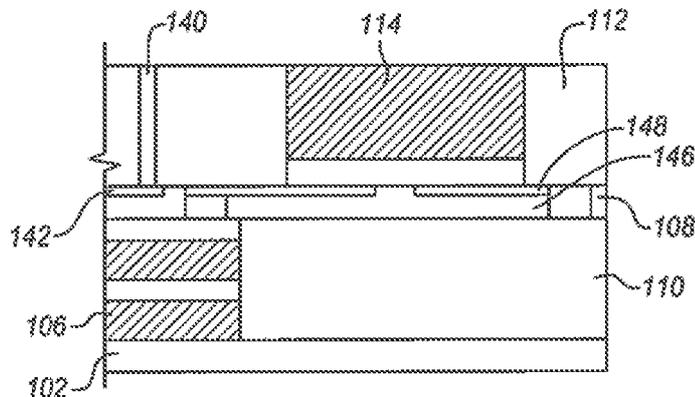


FIG. 1B

(57) **Abstract:** A flexible packaging architecture is described that is suitable for curved package shapes. In one example a package has a first die, a first mold compound layer over the first die, a wiring layer over the first mold compound layer, a second die over the wiring layer and electrically coupled to the wiring layer, and a second mold compound layer over the second die.

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FLEXIBLE PACKAGING ARCHITECTURE

FIELD

The present disclosure relates to the field of semiconductor chip packaging and, in particular, to packaging that is flexible for curved package shapes.

BACKGROUND

Semiconductor and micromechanical dies or chips are frequently packaged for protection against an external environment. The package provides physical protection, stability, external connections, and in some cases, cooling to the die inside the packages. Typically the chip or die is attached to a substrate and then a cover that attaches to the substrate is placed over the die. Alternatively, the die is attached to a cover and then a package substrate is formed on the die.

There is a trend to add more functions to each die and to put more than one die in a single package. This causes the packages to be larger and also increases specialization for packages. While a very high volume product, such as a cellular telephone may benefit from highly specialized purpose built components, a low volume product does not. For lower volume and more specialized products, it may be less expensive to select from multiple existing smaller dies. This allows more flexibility in the functions provided for the product and allows the product to use smaller packaged dies.

Current packaging technologies use rigid pre-impregnated fiberglass or silicon to carry different dies and to connect the dies to each other. This provides a stable platform to hold the dies and for the wiring layers used by the dies. However, a rigid substrate requires a wide, flat, and rigid location to be mounted in a device. As the Internet of Things, further automation, and connectivity expand, microelectronics are desired for a wider variety of different things. These microelectronic applications may include clothing, writing accessories, medical devices, and a wide range of small pocketable and wearable things. Many such things do not provide a wide, flat, rigid location for a device package.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1A is a cross-sectional side view diagram of a flexible package according to an embodiment.

Figure 1B is an enlarged view of a portion of Figure 1A according to an embodiment.

Figures 2A to 2G are a sequence of side view diagrams of stages of forming the flexible package of Figure 1A according to an embodiment

Figure 2H is a top view diagram of the flexible package of Figure 2G according to an embodiment

5 Figure 2I is a top view of the flexible package of Figure 2G after rolling according to an embodiment

Figure 2J is a top view partially cut away of the flexible package of Figure 2G after curving according to an embodiment

10 Figure 3 is a cross-sectional side view diagram of an alternative flexible package according to an embodiment

Figure 4 is top view diagram of the flexible package of Figure 3 according to an embodiment

15 Figures 5A to 5F are cross-sectional side view diagrams of stages of an example process flow of performing photolithography on mold compound to produce wire routing shown for the package of Figure 4 according to an embodiment

Figure 6 is a cross-sectional side view diagram of an alternative flexible package according to an embodiment

Figure 7 is top view diagram of the flexible package of Figure 6 according to an embodiment

20 Figures 8A to 8E are a sequence of side view diagrams of stages of forming the flexible package of Figure 6 according to an embodiment

Figure 9 is a block diagram of a computing device incorporating a package with an integral EMI shield according to an embodiment

DETAILED DESCRIPTION

25 A method to assemble low-profile and highly integrated systems for wearable device applications is described. Multiple layers of flexible thin-film substrate with embedded silicon devices interconnect through one or more flexible interposers. The silicon devices may include central processing units, memory, sensors and power management controllers, among others. The low-profile flexible package has one or more thin-film thermal distribution layers at the top
30 or bottom of the packaging system.

This provides highly-integrated and low-profile wearable devices using embedded-die thin films and flexible interposers. The thermal conditions for the silicon devices are improved using the thin-film thermal distribution layers. In addition, highly heterogeneous devices may be integrated. The device and the input/output functionality may be segmented using different

silicon devices and by repartitioning functional IP-blocks. The overall system is flexible to bend into various locations and may be provided to market in a shorter time compared to highly complex system-on-chip (SOC) packages that have a significantly larger silicon footprint

When the package is bent to fit into an unconventional location, the limitations on cooling may limit the power and performance of a system such as a SoC processor. By using a molded region of a stacked die package assembly as both a package level integrated heat spreader and also an additional ground plane to provide improved signal return paths and noise shielding of the entire package assembly, the heat can more easily be dissipated from the silicon devices. For higher performance an additional heat sink may be coupled to the package level integrated heat spreader.

Figure 1A is a cross-sectional side view diagram of a package 101 for silicon dies that is able to accommodate a variety of different form factors. The package has two layers LI, L2 to show how multiple dies may be combined into multiple layers. However, in some embodiments, one only layer LI is required. The base 102 of the package is a thermal distribution layer formed of a thermally conductive material such as silver or copper plating. A flexible interposer 108 is positioned between the two layers LI, L2.

The two layers are each formed of a flexible substrate 110, 112. Silicon dies are embedded into the substrate which may be formed of a variety of different materials such as a poly resin mold compound. The first layer LI is shown as having a first die 104 attached to the flexible interposer 108 and a die stack 106 coupled to the interposer. The dies may be attached using a surface mount, ball grid, thermal compression bonding, surface activated bonding, or any other attachment approach. In the die stack the lower die is attached to the upper die using pads on the lower die and through-silicon vias on the upper stack. An interposer or any other desired technique may alternatively be used to couple the two dies.

In the second layer L2, two additional dies 114, 116 are also embedded into the flexible substrate in the same way as the dies in the first layer. This allows all of die dies to be coupled to any other dies or any desired external device. In this example all of the wiring connections are through the flexible interposer that runs between the two layers. The dies are embedded in the encapsulant layer 110, 112 so that they are held securely in place and in connection with the interposer. Encapsulant layers serve as the package substrate in this example. The interposer and the encapsulant are flexible so that the package can be shaped into any desired form. The thermal distribution layer 102 is applied to one or both of the encapsulant layers to dissipate heat from the dies to the external ambient. As shown it is attached to the lower layer LI.

Figure 1B shows a portion of the package of Figure 1A in more detail. As shown, the flexible interposer 108 may have metal routing layers 142. The metal routing layers may be in one or more layers of the interposer. A dielectric material 146 may be used between the metal layers. The metal layers may include pads 148 to attach to contact or lands (not shown) of the dies 114 or die stacks 106, and pads to connect to vias 140. The via may be bored, etched, or drilled through the encapsulant layer to form connections for an external system or component. The via may also be used to connect to the heat spreader to conduct heat from the interposer and from a die connected to the interposer to the heat spreader. The via may also have a contact that makes a connection to another part of the package when the package is folded or rolled into its final configuration as described in more detail below.

Figures 2A to 2H show a simplified assembly process flow for a flexible or roilable system-in-package (SiP) 101 for wearable applications. Figure 2A is a cross-sectional side view diagram of a temporary carrier 103. One or more silicon devices 114, 116, such as CPU, PCH, sensors, wireless chip and DRAM memory are attached to the carrier by adhesive, solder, or in any other way. The temporary carrier 103 may be metal, silicon, or any other suitably rigid material. The silicon devices may also include embedded dies 106 in a stacked configuration. The stacked dies may have vertical through silicon via interconnections to each other. Any of the silicon devices may have contact on top or bottom surfaces to connect with other devices in the package or with external devices.

In Figure 2B, the dies are embedded in a substrate 112. The thin-film flexible substrate is a flexible encapsulant that protects the dies and electrically isolates the dies and any other layers from each other. The encapsulant may be made of any of a variety of different materials, including polyester (Mylar), polyimide (Kapton), aramid, fiber-glass epoxy and silicone composites. Alternative materials include poly siloxanes, epoxy resins, acrylates e.g. poly methyl methacrylate, both UV curable and Q_2H_2O initiated, polyurethanes, benzocyclobutene (BCB), polyimide, polyamide, high-density polyethylene (HDPE), bismaleimide-triazine (BT) resin, liquid crystal polymer (LCP), aramide, and polydimethylsiloxane (PDMS). The flexible encapsulant may be semi-cured during this process step depending on the material selection,

in Figure 2C, vertical channels 138 are formed through the encapsulant to the temporary carrier 103. The vertical channels may be drilled mechanically or optically by a laser or formed in any other way. The vertical channels may be in any desired pattern or structure depending on the particular implementation. In addition additional channels may be drilled to improve the flexibility of the package. Kerfs may be drilled or cut through the encapsulant to allow the

encapsulant to be compressed into the kerf when folded or rolled. The kerfs may be straight sided or angled so that the kerf is wider at its opening.

In Figure 2D, die channels are filled with a conductor, such as copper, to create conductive vias through the encapsulant. This may be done using any of a variety of different filling and deposition processes, including chemical and plasma vapor deposition. The vias may be filled or plated depending on the desired electrical characteristics. In Figure 2E, electrical contact points ISO are applied to the top of each via and the carrier is removed. The carrier may be removed by releasing the adhesive, etching, or in other ways.

Figure 2F is an exploded side view diagram of multiple layers L1, L2 of the package. The thin-film flexible substrate is prepared as one or more, in this case two, thin layers 110, 112 with silicon devices 104, 106, 114, 116 embedded in the substrate.

Figure 2F also shows the interposer 108 between the two layers 110, 112. Electrical interconnections between the silicon devices in the thin-film flexible substrate layers (L1/L2) may be made using the metal routing layers of the flexible interposer layer. The flexible interposer layer has embedded redistribution metal layers 142 (e-RDL) that provide the electrical path between the silicon devices. The thin-film flexible substrate and interposer may be formed of elastomer-based material compounds. While two layers are shown more or fewer may be used by adding additional layers of substrate with interposer between each layer. This allows for more layers of thin-film flexible substrate layers.

The flexible or reliable package 100 also includes one or more thin-film thermal distribution layers or heat spreaders 102 at the package base or top layer. The thin-film thermal distribution layer may be formed of silver or copper-based composites or nano-composites to provide efficient heat distribution across the device. The thin-film thermal distribution layer may also or alternatively be attached to the package top layer in another embodiment. In another embodiment, the thermal distribution layer for example a silver or copper plate, may be formed directly on the back-surface of the base package layer 110 through an electroplating, sputtering, or deposition process.

As mentioned above, to improve the flexibility of the package, kerfs (not shown) may be cut into one or both of the encapsulant or flexible substrate portions of the package. The kerfs are cut into the encapsulant on the inside of the rolled portion, in this example the bottom of the die. This may be done before the optional heat spreader is applied to this surface and before the flexible interposer is placed between the two substrates. The kerfs may be cut as v-shaped channels or grooves in a lateral direction or in other words parallel to the axis about which the package is bent or rolled.

In Figure 2G, the components are joined together. This is a simplified diagram to indicate the relative positions of the components after being joined together and is essentially the same as Figure 1A. The substrate layers with the embedded dies are joined to the interposer and coupled to the redistribution layers in the interposer. In one example, the interposer and redistribution layers are formed over one of the substrate layers such as the base layer 110. The second substrate layer may then be attached over the base layer. The thin-film substrate, interposer and thermal distribution layers may be aligned and integrated through any of a variety of different bonding processes, including for example surface activated bonding (SAB) or thermal compression bonding (TGB). The thermal distribution layer may optionally be then added to one or the other outer surfaces by plating, for example.

Figure 2H is a top plan view of the assembled package of Figure 2G. As shown in Figure 2G and 2I, the silicon devices alternate in position between the two substrates. This provides a higher degree of device flexibility and a greater bending-angle. The silicon devices are positioned in an alternating configuration so that a die is not directly over another die and so that there is a space between each die within the same substrate.

Figure 2H shows the two dies 104, 106 of the lower substrate 110 and the two dies 114, 116 of the upper substrate 112. The dies are connected with a simplified pattern of connection lines 118 to connect the silicon devices to each other and also to any external devices. In the illustrated example, there are two groups of external connectors 120, 122, one at each end of the package. This allows for more convenient connections in some applications. Power may be supplied at one end and data at the other for example. The two different connection areas may be divided in any suitable way to fit any desired form factor. The surface pads 150 which connect to the tops of vias 140 are also shown. The surface contact pads are particularly useful for external connections with a curved, folded, or bent package configuration.

In Figure 2I, the package 101 has been rolled into a cylindrical shape so that the base layer 110 and the thin film heat spreader 102 are on the outside of the cylindrical package. The low-profile flexible package is first shaped by a suitable process, such as rolling. Then the shaped package may then be cured to retain the desired form. The curing process may be used, for example, to harden the substrate material so that it holds its shape.

Figure 2J is a cross-sectional diagram of an alternate curved package shape that may be formed instead of the rolled shape of Figure 2I. Figure 2J shows the two encapsulant layers 110, 112 which are formed into a curved or wavy shape. The curvature package is allowed to bend in part using kerfs 152 sliced through one or both of the encapsulant layers. The kerfs reduce the compression of the encapsulant when the encapsulant is bent. The silicon devices 116, 106, 114

are not required to bend. The alternating position allows the encapsulant to bend around the devices. The contact pads 150 allow for external connections.

A flexible and a rollable package have a variety of different applications. The cylindrical configuration allows the SiP to be used in a variety of different wearable applications such as a smart-pen with various communication, authentication, or security capabilities. Such a package may also be used in other wearable applications such as fabric, glasses, shoes, wallets and wristbands. The package may instead be bent into other curved shapes that are not cylindrical. The package may be curved in more than one direction so that it is able to fit into other curved shapes.

Figure 3 is a cross-sectional side view diagram of an alternate configuration for a flexible package. The package has a package substrate 302. Silicon devices are connected to the substrate with a ball grid, land grid, or other attachment technology. The dies are then embedded in a layer of encapsulant 304 that covers the dies and the substrate. The encapsulant may be the same materials as mentioned above, or a mold compound may be used in this example as well as that of Figures 1A and 1B. Metal pads and routes 324 are then formed over the first layer of mold compound. Additional silicon devices are connected to the metal pads in a manner similar to how the devices were coupled to the substrate. A second layer of mold compound 306 is formed over the devices and the first mold compound to seal the package and hold the devices in place.

As in the example of Figure 21, kerfs may be cut into the top of the upper mold compound 306. Additional kerfs may be cut into the top of the lower mold compound 304 before the wiring layers 324 are added.

Figure 4 shows the same package as a top view in which the top layer of mold compound 306 is transparent. In this view each of the silicon devices may be seen. The metal pads and routing layers on the mold are shown in top view to show how silicon devices may be connected using pads for solder ball or wire bond connections.

The electrical paths in the package mold compound provide an additional avenue for establishing direct electrical connections between modules or dies in a multi-chip (or multi-chip stacked die) package assembly. This may be used instead of a specific interposer layer. As shown in Figure 3, the mold compound is used as the substrate for the routing layers and pads.

As described, the bottom dies are first attached to the package substrate. The remaining structure is then overmolded. Photolithography may then be used on the mold compound to form metal pads and metal routes. These metal pads and metal routes on the mold compound function to electrically connect dies of the multi-chip package. In addition to the metal routes,

the active side or back side of a die may be electrically connected using through-silicon vias. The metal pads may be connected using solder balls or wire bonding 322, or in any other desired way.

5 The substrate may be a conventional mini FCB (core or coreless) with overlaying layers of dielectric and metal routing stacked up and a solder-resist layer on the top and bottom surfaces. The substrate may be a conventional package substrate adapted for flexibility. The substrate may also be a flexible PCB with metal routings or redistribution metal layers (e.g. wire meshes or metal traces) encapsulated within an elastomer compound. As mentioned above, the mold compound may be any polymer / poly-resin mold compound or an elastomer compound,
10 among others.

Figure 3 shows a multi-chip package assembly with multiple dies attached to the package substrate 302 as a cross-sectional side view. The dies provide enough components to form a powerful connected computing system. The silicon devices include a processor 310, chipset or co-processor 318, memory 314, radio 320, MEMs/sensors 316, power controller 312, and any
15 other desired components. The metal pads and metal routes are laid on the mold compound and function as electrical interconnects between the various modules or silicon devices on the multi-chip package.

The metal routing layer increases the total number of electrical paths for inter-module communications and may be used in stacked or single layer packages. The increase in electrical
20 paths facilitates higher density module integration in a multi-chip package assembly for wearable devices. Fewer electrical paths may limit the number of modules that can be effectively integrated into a single multi-chip package assembly. The connections formed on the mold compound may be shorter and more direct. The modules may be directly connected to each other by metal routes on the mold compound without having to go through an intermediate die or
25 a package substrate. This improves communication speed and efficiency between the modules of the package.

In addition, the thickness and the number of metal layers of a package substrate may be reduced by moving some metal routings from the package substrate 302 to the package mold 304. This reduces the amount of substrate required which reduces the cost of the multi-chip
30 package assembly.

Figures 5A to 5F are cross-sectional side view diagrams to show an example process flow of performing photolithography on mold compound to produce the wire routing shown, for example, in Figure 4. In Figure 5A a passivation layer is coated over the mold compound. The embedded dies and package substrate are not shown for simplicity. The passivation layer may be

made from silicon dioxide (SiO₂) and other dielectric or insulation materials. In Figure 5B a photoresist layer is applied over the passivation layer, exposed and developed to produce the desired pattern. In Figure 5C, the passivation layer is patterned based on the patterned photoresist by removing the exposed passivation layer. In Figure 5D, the photoresist layer is removed leaving the patterned passivation layer.

In Figure 5E a copper layer or other conductive material layer is coated over the passivation layer. The metal routing is then finished by backgrinding the copper down to the level of the passivation layer. This leaves a pattern of copper with dielectric between the copper. The copper may be formed into pads, lines and any other desired shape based on what is possible for the photoresist. The metal routing layers may be formed in any other desired way. This process flow is provided only as an example. The same techniques may be used to form the redistribution layer on the interposer of Figure 1. In addition more layers may be applied over the pattern of Figure 5E to produce more complex wiring layers and multiple levels of patterns.

Figure 6 is a cross-sectional diagram of another flexible package or a part of a package. The package has a substrate 602 with a ground plane 604. The package may have many more layers for interconnecting silicon devices or it may just provide ground or power or both. One or more silicon devices 606, 607 are connected to the substrates using a ball or land grid array. A first layer of mold compound 608 is then formed over these dies.

The package as shown includes a stacked die assembly with a top die 610 coupled to respective bottom die 606. There may be more than one stack, depending on the particular implementation. The dies are stacked with connections from a solder ball of the top die to a through-silicon via of the bottom die. However, any other die connection may be used including those shown in Figures 1 and 3.

The package assembly is molded with a bottom layer mold compound 608 that spreads across a wide surface area of the package substrate 602 compared to the surface area of the bottom dies 606. The z-height of the bottom layer mold compound is slightly higher than the Z-height of the bottom dies so that the mold compound completely covers the bottom dies.

In the example of Figure 6, the bottom layer molded region of the package may be used as an integrated heat spreader. Special insulation materials with good heat transfer characteristics may be used as the package bottom layer mold compound. An additional heat conductive layer 616, for example a metal such as copper or aluminum, may be laid, plated, sputtered, or deposited on top of the bottom layer molded region of the package assembly to further spread heat across the entire surface area of the bottom layer molded region through a heat conduction process. Heat from a bottom die may be conducted onto the bottom layer mold

compound and spread across the entire surface area of the molded region's metal layer surface to be dissipated through a natural heat dissipation process.

A second thin layer of high heat conduction molding compound 612 may be formed over the top of the bottom layer molded region 608 to protect the metal layers 616 and still provide good heat dissipation for the entire package assembly. The metal layers 616 include heat spreader layers and connection interfaces or redistribution layers between dies, such as between the dies 606, 610 on the left side of the diagram and the die 607 on the right side of the diagram.

In one embodiment, the metal layer 616 on the package bottom layer molded region is electrically connected to the package substrate ground plane 604 using wirebond or laser drilled vias 614 through the bottom layer mold compound 608. This connection provides additional heat dissipation channels within the package through the heat spreader layer 616. The connection also provides additional signal return paths (for improved electrical performance) and shielding from electromagnetic interference from other communication silicon devices within the SiP.

Figure 7 is a top plan view of the package in which the upper layer molded region is transparent. The two silicon devices are shown as near each other. Both are surrounded by the heat spreader layer 616. The through-mold vias 614 may be plated to improve conduction. There may be more than the three vias as shown. Vias may also be added between the two dies.

The mold compound 608, 612 in both layers is a thermal conductor with high heat transfer characteristics and may also be an electrical insulator. This allows the devices 606, 610 to cool through the mold compound. The package may be finished with an additional thermal heat spreader layer (not shown), such as a metal (e.g. copper) layer. The metal may be laid on top of the mold compound 612 which functions as an on-mold heat spreader. The metal layer may be electrically connected to the package substrate ground pins to provide additional signal return paths and electromagnetic interference shielding layer.

The added heat spreader layer 616 increases the natural heat dissipation capabilities of a multi-chip stacked die package assembly. This allows a multi-chip stacked die package assembly to house higher TDP silicon modules for wearable devices. The added heat spreader layer also increases the effectiveness of the noise shielding of a multi-chip stacked die package assembly. The ground reference plane requirements for a package substrate (or PCB) can be effectively reduced. This allows the substrate thickness and the number of layers to also be reduced reducing the overall cost of the package.

Figures 8A to 8E are cross-sectional side view diagrams of a simplified fabrication process flow for the package of Figures 8 and 9. In Figure 8A, the dies 806, 808 are attached to the package substrate 802. The substrate has already been formed and includes a ground plane

804 and connection pads for the dies. The dies may be attached using any of the techniques mentioned above, depending on the intended application and the nature of the dies. Two of the dies 808 are stacked. More or fewer die stacks may be used, depending on the overall system design.

5 In Figure 8B, a lower mold compound layer 810 is formed over the substrate and the dies. The mold compound in the illustrated example covers most of the substrate and covers the lower levels of the dies. In Figure 8C a copper layer or any other suitable heat conductive layer 812 is formed over the mold compound 810. This is the integrated heat spreader described above. Optionally, a portion of the heat spreader layer may be used for routing layers and metal
10 pads.

In Figure 8D, through-mold vias are formed through the heat spreader layer and the mold. The vias extend all the way down to the ground plane 804 of the substrate 802. The vias are then filled or plated to ensure that they are electrically conductive and connect the heat spreader layer to the ground plane. In Figure 8E a second layer of mold compound 816 is added over the dies
15 and the heat spreader layer. This layer covers the entire substrate and can act as a protective layer over all the rest of the structure.

After the structure of Figure 8E is obtained, the entire SiP may be shaped to any suitable configuration to fit a desired form factor. The SiP may be rolled as in Figure 21, bent, curved, or folded as desired.

20 The RDL layers described herein may have a first dielectric layer closest to the chip, a conductor layer with metal pathways, and a solder stop layer. The chip is connected to the metal pathways by vias through the first dielectric layer. The metal pathways may be formed of any of a variety of different metals including copper, aluminum, titanium, tungsten, nickel, palladium, gold, or of metal alloys including one or more of copper, aluminum, titanium, tungsten, nickel,
25 palladium, and gold. The RDL may be in the form of a package substrate, a BBUL (Bumpless Build-Up Layer), or alternating patterns of dielectric and conductive layers formed over the die. The particular choice of RDL may be adapted to suit any of a variety of different package types.

The mold or molding compound described herein may be formed of any of a variety of different materials, depending on the nature of the package and its intended use. Suitable mold
30 compounds may include, or may consist of, a plastic material, such as a thermosetting polymer or an epoxy resin or a filled epoxy resin such as a thermosetting mold compound. Alternatively, an underfill or other material may be used to protect the die.

The metal layer described herein for heat spreading, additional routing paths, and noise shielding may be copper, aluminum, gold, or any other electrically conductive material including

non-metals. It may be applied by sputtering, by deposition, or in a variety of other ways. The metal layer may physically contact and electrically connects with the ground layer of the RDL.

The packages described herein may be further finished with additional coatings or covers. The package may be covered with another layer of mold compound or it may be covered with a
5 molded polymer cover or both, depending on the particular type of package, in addition, additional dies, RDLs, passive components, or other elements may be added to the package to form a system in a package, or multi-chip packages of different types. The metal layers may be covered with polymer or dielectric resins for protection and the vias may be filled to provide protection and physical stability to the package. Alternatively, the vias may be filled with metal
10 instead of coated with metal.

Figure 9 illustrates a computing device 100 in accordance with one implementation of the invention. The computing device 100 houses a system board 2. The board 2 may include a number of components, including but not limited to a processor 4 and at least one communication package 6. The communication package is coupled to one or more antennas 16.
15 The processor 4 is physically and electrically coupled to the board 2. At least one of either the RF or digital die packages shielded using a pattern of metal lined vias in the package and the metal layer and electrically coupled to the board 2 through the package. In some implementations of the invention, any one or more of the components, controllers, hubs, or interfaces are formed on dies using metal coated through mold vias as described above.

Depending on its applications, computing device 100 may include other components that may or may not be physically and electrically coupled to the board 2. These other components include, but are not limited to, volatile memory (e.g., DRAM) 8, non-volatile memory (e.g., ROM) 9, flash memory (not shown), a graphics processor 12, a digital signal processor (not shown), a crypto processor (not shown), a chipset 14, an antenna 16, a display 18 such as a
25 touchscreen display, a touchscreen controller 20, a battery 22, an audio codec (not shown), a video codec (not shown), a power amplifier 24, a global positioning system (GPS) device 26, a compass 28, an accelerometer (not shown), a gyroscope (not shown), a speaker 30, a camera 32, and a mass storage device (such as hard disk drive) 10, compact disk (CD) (not shown), digital versatile disk (DVD) (not shown), and so forth). These components may be connected to the
30 system board 2, mounted to the system board, or combined with any of the other components.

The communication package 6 enables wireless and/or wired communications for the transfer of data to and from the computing device 100. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic

radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication package 6 may implement any of a number of wireless or wired standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, 5 long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, Ethernet derivatives thereof, as well as any other wireless and wired protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 100 may include a plurality of communication packages 6. For instance, a first communication package 6 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a 10 second communication package 6 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The entire system 100 or any part of the system may be constructed as a bendable, flexible, or rollable package. One portion of the system may be provided on a rigid board while another portion of the system is provided on a flexible or shaped board.

15 In various implementations, the computing device 100 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 100 may be any other electronic device, such as a pen, a 20 wallet, a watch, or an appliance that processes data.

Embodiments may be implemented as a part of one or more memory chips, controllers, CPUs (Central Processing Unit), microchips or integrated circuits interconnected using a motherboard, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA).

25 References to "one embodiment", "an embodiment", "example embodiment", "various embodiments", etc., indicate that the embodiment(s) of the invention so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Further, some embodiments may have some, all, or none of the features described for other embodiments.

30 In the following description and claims, the term "coupled" along with its derivatives, may be used. "Coupled" is used to indicate that two or more elements co-operate or interact with each other, but they may or may not have intervening physical or electrical components between them.

As used in the claims, unless otherwise specified, the use of the ordinal adjectives "first", "second", "third", etc., to describe a common element, merely indicate that different instances of like elements are being referred to, and are not intended to imply that the elements so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

5 The drawings and the forgoing description give examples of embodiments. Those skilled in the art will appreciate that one or more of the described elements may well be combined into a single functional element. Alternatively, certain elements may be split into multiple functional elements. Elements from one embodiment may be added to another embodiment. For example, orders of processes described herein may be changed and are not limited to the manner described
10 herein. Moreover, the actions of any flow diagram need not be implemented in the order shown; nor do all of the acts necessarily need to be performed. Also, those acts that are not dependent on other acts may be performed in parallel with the other acts. The scope of embodiments is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are
15 possible. The scope of embodiments is at least as broad as given by the following claims.

The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications. Some embodiments pertain to a method that includes embedding a plurality of silicon dies in a flexible substrate, forming a flexible
20 interposer layer over the embedded dies, forming a thin film thermal distribution layer over the substrate opposite the flexible interposer layer, shaping the substrate with the dies and the interposer, and curing the shaped substrate.

Further embodiments include stacking another die over one of the plurality of silicon dies, or forming a through-silicon via in one of the plurality of dies and electrically connecting
25 the via to the stacked die.

In further embodiments, the flexible interposer comprises an embedded redistribution metal layer to provide an electrical path to the flexible substrate. The flexible interposer comprises an elastomer to carry the metal layer. Forming the flexible interposer comprises forming a plurality of alternating metal and dielectric layers. The thin film thermal distribution
30 layer comprises a copper-based composite.

Further embodiments include bonding the plurality of silicon dies to the flexible interposer.

In further embodiments bonding comprises surface-activated bonding or thermal compression bonding. Shaping comprises rolling.

Some embodiments pertain to a package that includes a plurality of silicon dies embedded in a flexible substrate, a flexible interposer layer over the embedded dies, a thin film thermal distribution layer over the substrate opposite the flexible interposer layer, the flexible substrate being shaped with the dies and the interposer to a curved shape and cured so that the flexible substrate holds its shape.

In further embodiments at least one die of the plurality of silicon dies is stacked over another die.

Further embodiments include a through-silicon via to connect the slacked die to another die.

In further embodiments the flexible interposer comprises an embedded redistribution metal layer to provide an electrical path to the flexible substrate. The flexible interposer comprises an elastomer to carry the metal layer. The flexible interposer comprises a plurality of alternating metal and dielectric layers. The thin film thermal distribution layer comprises a copper-based composite. The plurality of silicon dies are electrically coupled and bonded to the flexible interposer. The bond is by surface-activated bonding or thermal compression bonding.

Further embodiments include a second plurality of silicon dies embedded in a second flexible substrate, the second substrate being in electrical contact with the flexible interposer opposite the first silicon substrate. Further embodiments include a thin film thermal distribution layer over the second substrate opposite the flexible interposer.

Some embodiments pertain to an electronic computing system that has a power supply, a display and a semiconductor computing device package having a plurality of silicon dies embedded in a flexible substrate, a flexible interposer layer over the embedded dies, and a thin film thermal distribution layer over the substrate opposite the flexible interposer layer, the flexible substrate being shaped with the dies and the interposer to a curved shape and cured so that the flexible substrate holds its shape.

Some embodiments pertain to a method that includes attaching a plurality of dies to a substrate, overmolding the attached dies, forming metal pads and routing on the mold compound, and connecting at least one die of the plurality of dies to the formed metal pads and routing.

Further embodiments include forming the metal pads and routing comprising using photolithography.

In further embodiments forming the metal pads and routing comprises applying metal over a patterned passivation layer and backgrinding the metal layer. Connecting comprises connecting using a wirebond between a pad on the respective die and a formed metal pad on the mold compound. Connecting comprises connecting a through-silicon via in the respective at

least one die to a formed metal pad. Attaching an additional die over formed metal pads on the molding compound

Some embodiments pertain to a package that includes a first die, a first mold compound layer over the first die, a wiring layer over the first mold compound layer, a second die over the wiring layer and electrically coupled to the wiring layer, and a second mold compound layer over the second die.

In further embodiments, the first die is electrically coupled to the wiring layer. The first die is electrically coupled to the wiring layer through a through silicon via in the first die that extends from a top surface of the first die to circuits within the first die. The second die is electrically coupled to the wiring layer through wiring pads formed on the bottom of the second die.

Further embodiments include a flexible substrate below the first die.

In further embodiments the flexible substrate is thermally conducting and thermally coupled to the first die.

Further embodiments include a through-mold via to couple the wiring layer to the flexible substrate

In further embodiments the flexible substrate comprises a redistribution layer and is electrically coupled to the first die. The redistribution layer is coupled to the first die by wirebonds. The second die is not over the first die and the second die is laterally displaced from the first die.

Further embodiments include an electrical contact area over the first mold compound coupled to the wiring layer to connect the second die to an external device.

Further embodiments include a flexible interposer over the first mold compound layer and wherein the wiring layer is formed over the flexible interposer.

Further embodiments include a third die over the wiring layer and wherein the second die and the third die are coupled by the wiring layer.

In further embodiments, the wiring layer comprises metal pad to electrically connect to the second die.

Some embodiments pertain to an electronic computing system that includes a power supply, a display, and a semiconductor computing device package having a first die, a first mold compound layer over the first die, a wiring layer over the first mold compound layer, a second die over the wiring layer and electrically coupled to the wiring layer, and a second mold compound layer over the second die.

Some embodiments pertain to a method that includes attaching a plurality of dies to a substrate, overmolding the attached dies and the substrate with a thermally conductive mold compound, and depositing a thermally conductive layer as a heat spreader over the mold compound.

5 In further embodiments, the mold compound is filled with thermally conductive materials to conduct heat from the dies to the heat spreader. The heat spreader is formed of a thermally conductive material, such as copper or aluminum.

Further embodiments include forming a thermally conductive via through the mold compound before depositing to connect the heat spreader to the substrate.

10 In further embodiments, the substrate comprises a ground plane and the via is coupled to the ground plane of the substrate.

Some embodiments pertain to a package that includes a substrate, a die on the substrate and connected to the substrate, a thermally conductive mold compound over the die and the substrate, and a heat spreader over the mold compound.

15 In further embodiments, the mold compound is filled with thermally conductive materials. The heat spreader is formed of a thermally conductive material, such as copper or aluminum.

Further embodiments include a thermally conductive via through the mold to connect the heat spreader to the substrate.

20 In further embodiments, the substrate comprises a ground plane and the heat spreader is coupled to the ground plane of the substrate.

Further embodiments include a plurality of heat fins thermally coupled to the heat spreader.

25 In further embodiments, the mold compound comprises a plurality of kerfs to allow the package to bend.

Some embodiments pertain to an electronic computing system that includes a power supply, a display, and a semiconductor computing device package having a substrate, a die on the substrate and connected to the substrate, a thermally conductive mold compound over the die and the substrate, and a heat spreader over the mold compound.

30

CLAIMS

1. A method comprising:
embedding a plurality of silicon dies in a flexible substrate;
forming a flexible interposer layer over the embedded dies;
5 forming a thin film thermal distribution layer over the substrate opposite the flexible interposer layer;
shaping the substrate with the dies and the interposer, and
curing the shaped substrate.
2. The method of Claim 1, further comprising stacking another die over one of the
10 plurality of silicon dies.
3. The method of Claim 1, further comprising forming a through-silicon via in one of the plurality of dies and electrically connecting the via to the stacked die.
4. The method of Claim 1, wherein the flexible interposer comprises an embedded redistribution metal layer to provide an electrical path to the flexible substrate.
- 15 5. The method of Claim 1, wherein the flexible interposer comprises an elastomer to carry the metal layer.
6. The method of Claim 1, wherein forming the flexible interposer comprises forming a plurality of alternating metal and dielectric layers.
7. The method of Claim I, wherein the thin film thermal distribution layer comprises
20 a copper-based composite.
8. The method of Claim 1, further comprising bonding the plurality of silicon dies to the flexible interposer.
9. The method of Claim 1, wherein bonding comprises surface-activated bonding or thermal compression bonding.
- 25 10. The method of Claim 1, wherein shaping comprises rolling, casting, bending or folding.
11. A package comprising:
a plurality of silicon dies embedded in a flexible substrate;
a flexible interposer layer over the embedded dies;
30 a thin film thermal distribution layer over the substrate opposite the flexible interposer layer,
the flexible substrate being shaped with the dies and the interposer to a curved shape and cured so that the flexible substrate holds its shape.

12. The package of Claim 11, wherein at least one die of the plurality of silicon dies is stacked over another die.

13. The package of Claim 11, further comprising a through-silicon via to connect the stacked die to another die.

5 14. The package of Claim 11, wherein the flexible interposer comprises an embedded redistribution metal layer to provide an electrical path to the flexible substrate.

15. The package of Claim 11, wherein the flexible interposer comprises an elastomer to carry the metal layer.

10 16. The package of Claim 11, wherein the flexible interposer comprises a plurality of alternating metal and dielectric layers.

17. The package of Claim 11, wherein the thin film thermal distribution layer comprises a copper-based composite.

18. The package of Claim 11, wherein the plurality of silicon dies are electrically coupled and bonded to the flexible interposer.

15 19. The package of Claim 11, wherein the bond is by surface-activated bonding or thermal compression bonding.

20 20. The package of Claim 11, further comprising a second plurality of silicon dies embedded in a second flexible substrate, the second flexible substrate being in electrical contact with the flexible interposer opposite the first flexible substrate.

21. The package of Claim 11, further comprising a thin film thermal distribution layer over the second substrate opposite the flexible interposer.

22. An electronic computing system comprising:

a power supply;

a display; and

25 a semiconductor computing device package having a plurality of silicon dies embedded in a flexible substrate, a flexible interposer layer over the embedded dies, and a thin film thermal distribution layer over the substrate opposite the flexible interposer layer, the flexible substrate being shaped with the dies and the interposer to a curved shape and cured so that the flexible substrate holds its shape.

30 23. A method comprising:

attaching a plurality of dies to a substrate;

overmolding the attached dies;

forming metal pads and routing on the mold compound; and

connecting at least one die of the plurality of dies to the formed metal pads and routing.

24. The method of Claim 23, wherein forming the metal pads and routing comprising using photolithography.

25. The method of Claim 23, wherein forming the metal pads and routing comprises applying metal over a patterned passivation layer and backgrinding the metal layer.

5 25. The method of Claim 23, wherein connecting comprises connecting using a wirebond between a pad on the respective die and a formed metal pad on the mold compound.

27. The method of Claim 23, wherein connecting comprises connecting a through silicon via in the respective at least one die to a formed metal pad.

10 28. The method of Claim 23, attaching an additional die over formed metal pads on the molding compound.

29. A package comprising:

a first die;

a first mold compound layer over the first die;

a wiring layer over the first mold compound layer;

15 a second die over the wiring layer and electrically coupled to the wiring layer; and

a second mold compound layer over the second die.

30. The package of Claim 29, wherein the first die is electrically coupled to the wiring layer.

20 31. The package of Claim 29, wherein the first die is electrically coupled to the wiring layer through a through silicon via in the first die that extends from a top surface of the first die to circuits within the first die.

32. The package of Claim 29, wherein the second die is electrically coupled to the wiring layer through wiring pads formed on the bottom of the second die.

25 33. The package of Claim 29, further comprising a flexible substrate below the first die.

34. The package of Claim 29, wherein the flexible substrate is thermally conducting and thermally coupled to the first die.

35. The package of Claim 34, further comprising a through-mold via to couple the wiring layer to the flexible substrate

30 36. The package of Claim 29, wherein the flexible substrate comprises a redistribution layer and is electrically coupled to the first die.

37. The package of Claim 36, wherein the redistribution layer is coupled to the first die by wirebonds.

38. The package of Claim 29, wherein the second die is not over the first die and the second die is laterally displaced from the first die,

39. The package of Claim 29, further comprising an electrical contact area over the first mold compound coupled to the wiring layer to connect the second die to an external device.

5 40. The package of Claim 29, further comprising a flexible interposer over the first mold compound layer and wherein the wiring layer is formed over the flexible interposer.

41. The package of Claim 29, further comprising a third die over the wiring layer and wherein the second die and the third die are coupled by the wiring layer.

10 42. The package of Claim 29, wherein the wiring layer comprises a metal pad to electrically connect to the second die.

43. An electronic computing system comprising:
a power supply;

a display; and

15 a semiconductor computing device package having a first die, a first mold compound layer over the first die, a wiring layer over the first mold compound layer, a second die over the wiring layer and electrically coupled to the wiring layer, and a second mold compound layer over the second die.

44. A method comprising:

attaching a plurality of dies to a substrate;

20 overmolding the attached dies and the substrate with a thermally conductive mold compound; and

depositing a thermally conductive layer as a heat spreader over the mold compound.

45. The method of Claim 44, wherein the mold compound is filled with thermally conductive materials to conduct heat from the dies to the heat spreader.

25 46. The method of Claim 44, wherein the heat spreader is formed of a thermally conductive material, such as copper or aluminum.

47. The method of Claim 44, further comprising forming a thermally conductive via through the mold compound before depositing to connect the heat spreader to the substrate.

30 48. The method of Claim 47, wherein the substrate comprises a ground plane and wherein the via is coupled to the ground plane of the substrate.

49. A package comprising:

a substrate;

a die on the substrate and connected to the substrate;

a thermally conductive mold compound over the die and the substrate; and

a heat spreader over the mold compound.

50. The package of Claim 49, wherein the mold compound is filled with thermally conductive materials.

5 51. The package of Claim 49, wherein the heat spreader is formed of a thermally conductive material, such as copper or aluminum.

52. The package of Claim 49, further comprising a thermally conductive via through the mold to connect the heat spreader to the substrate.

53. The package of Claim 52, wherein the substrate comprises a ground plane and the heat spreader is coupled to the ground plane of the substrate.

10 54. The package of Claim 49, further comprising a plurality of heat fins thermally coupled to the heat spreader.

55. The package of Claim 49, wherein the mold compound comprises a plurality of kerfs to allow the package to bend.

15 56. An electronic computing system comprising:
a power supply;
a display; and

a semiconductor computing device package having a substrate, a die on the substrate and connected to the substrate, a thermally conductive mold compound over the die and the substrate, and a heat spreader over the mold compound.

20 second die.

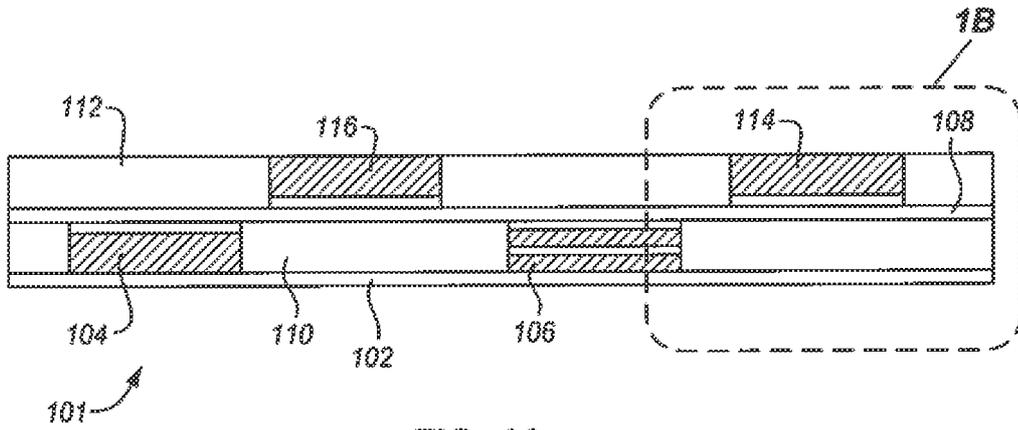


FIG. 1A

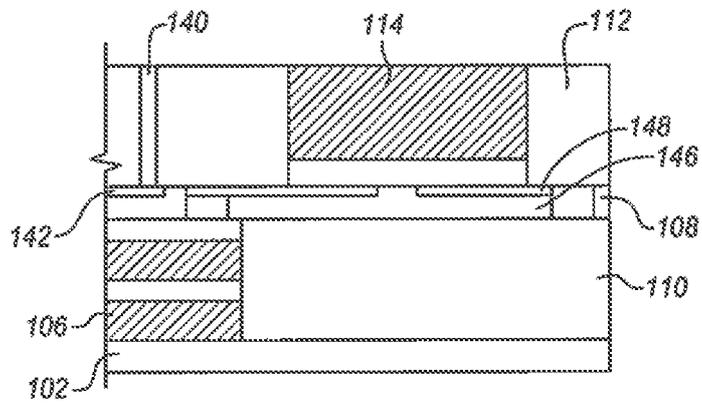


FIG. 1B

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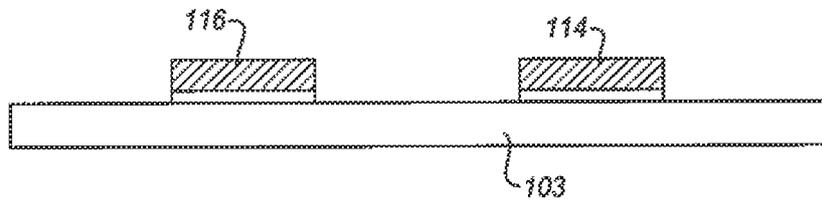


FIG. 2A

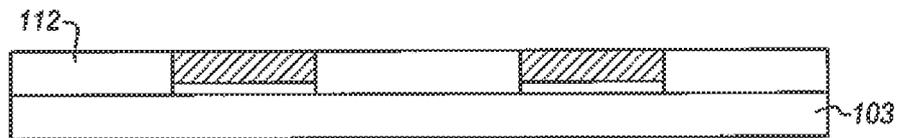


FIG. 2B

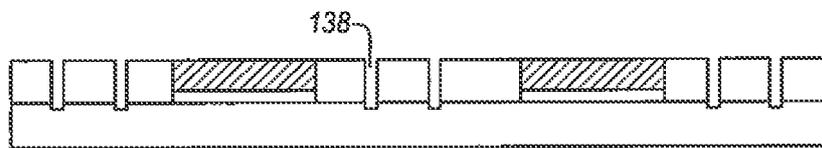


FIG. 2C

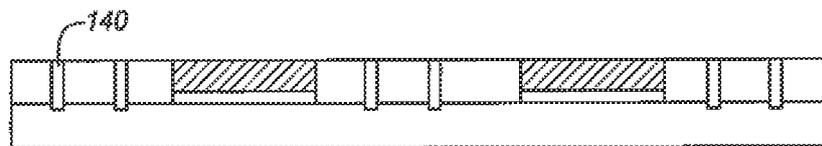


FIG. 2D



FIG. 2E

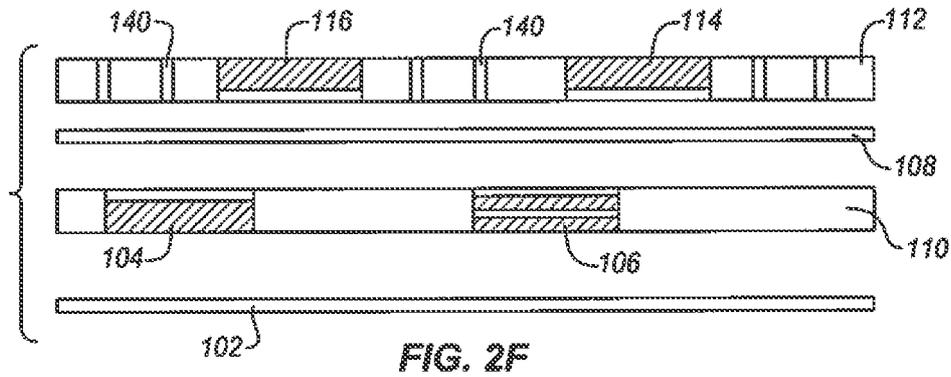


FIG. 2F

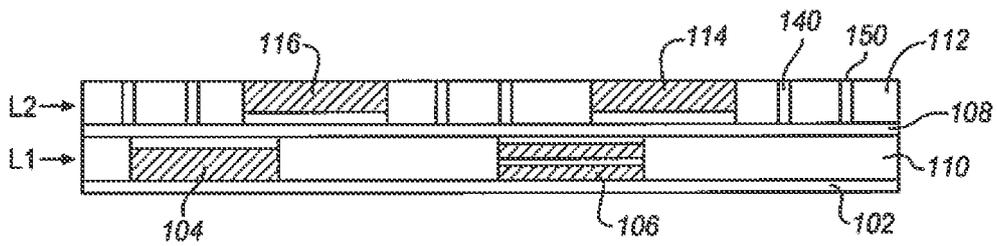


FIG. 2G

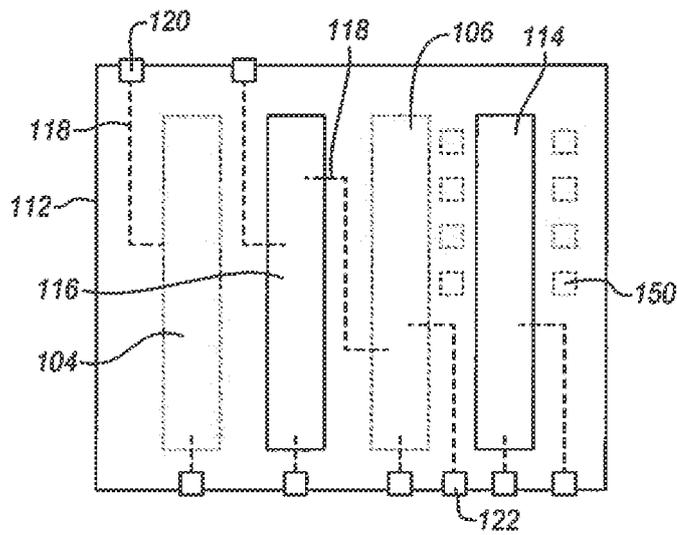


FIG. 2H

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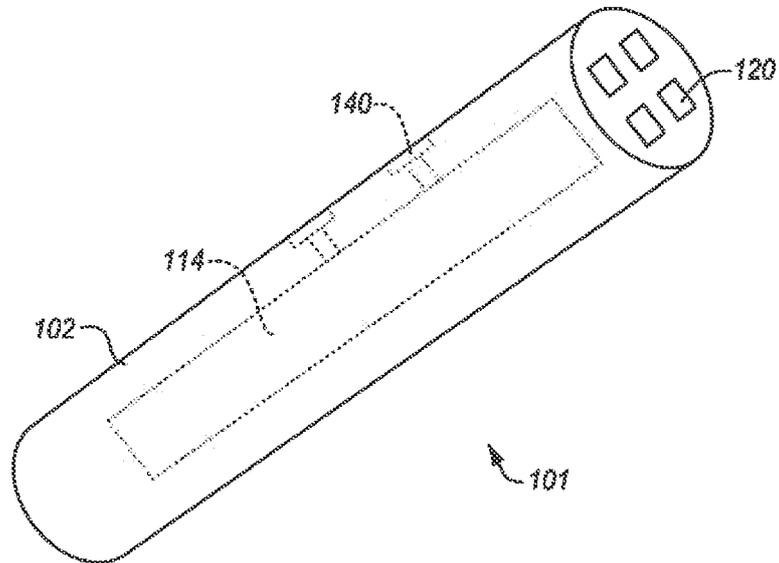


FIG. 2I

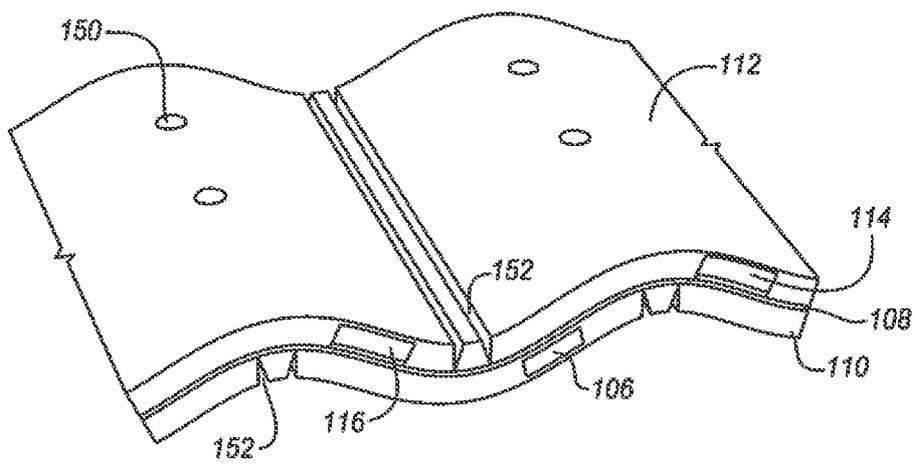


FIG. 2J

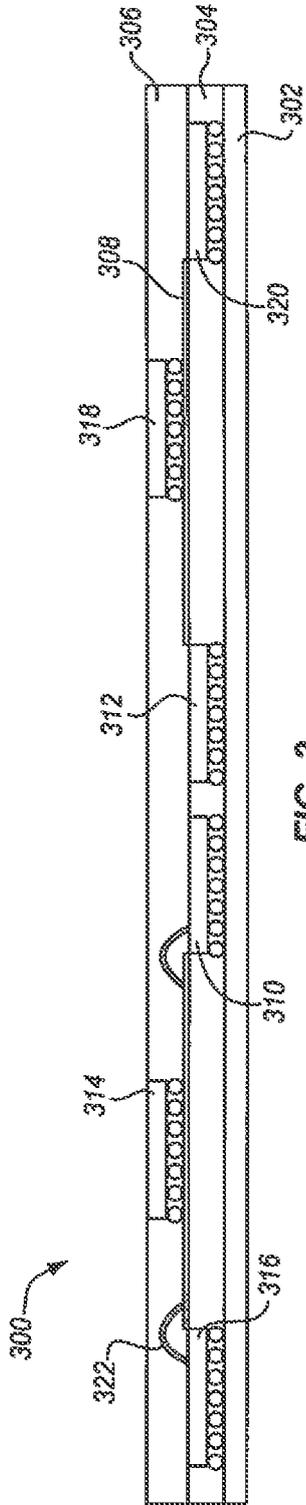


FIG. 3

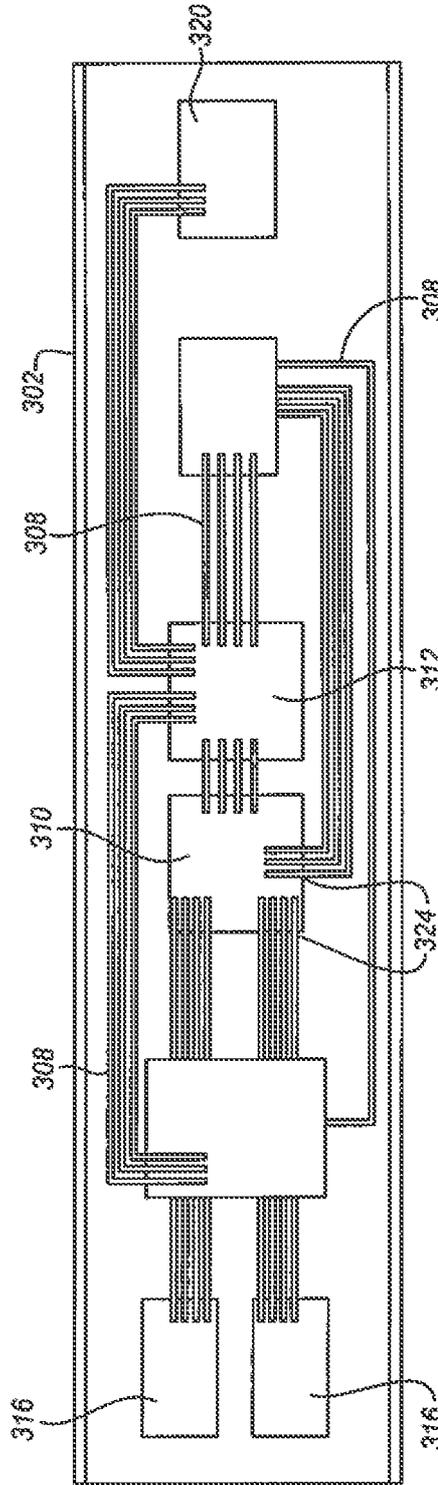


FIG. 4

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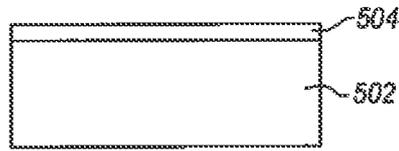


FIG. 5A

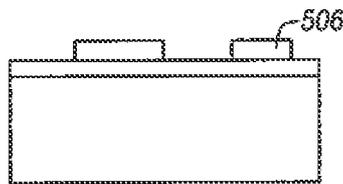


FIG. 5B

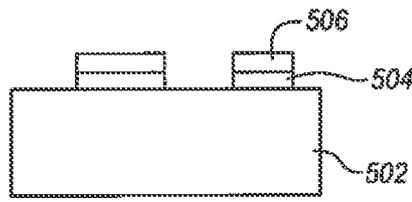


FIG. 5C

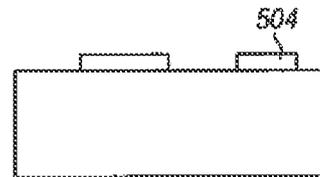


FIG. 5D

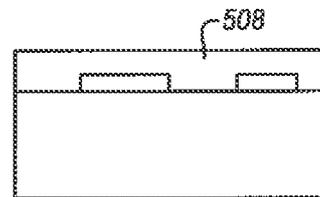


FIG. 5E

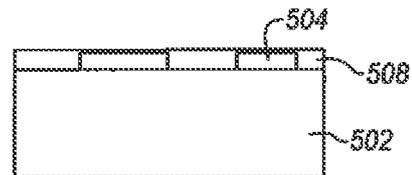


FIG. 5F

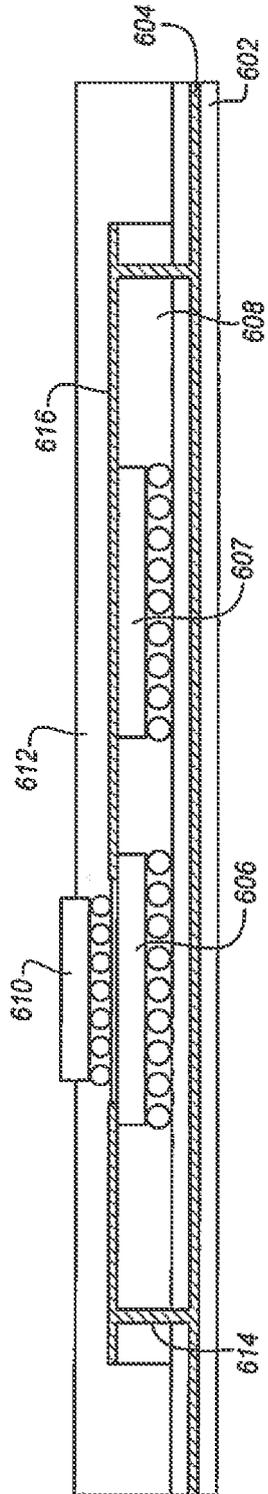


FIG. 6

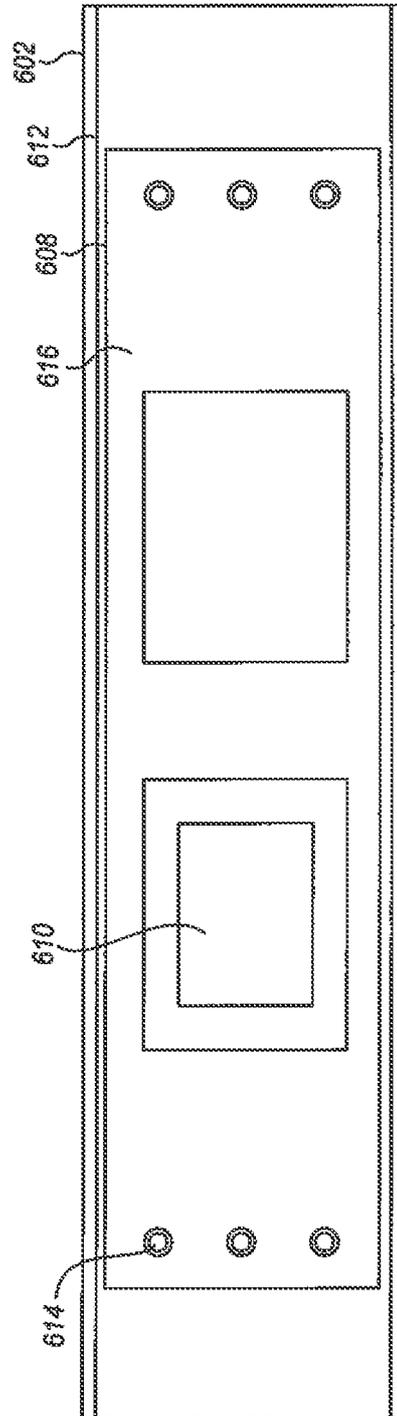


FIG. 7

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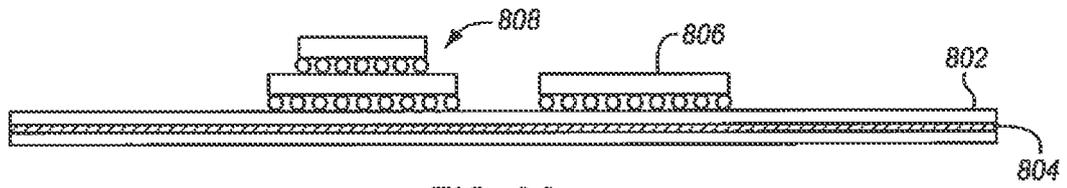


FIG. 8A

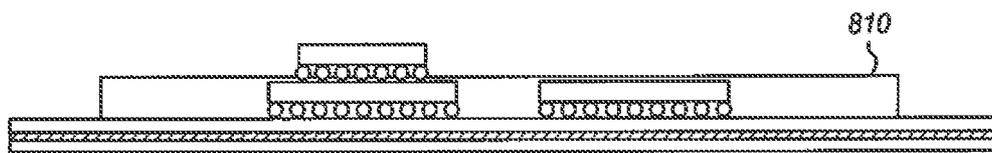


FIG. 8B

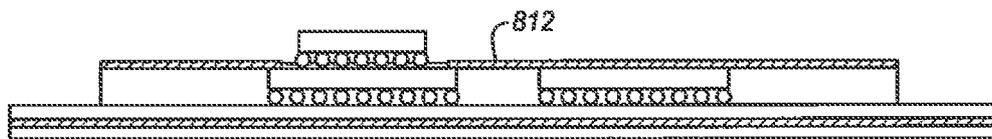


FIG. 8C

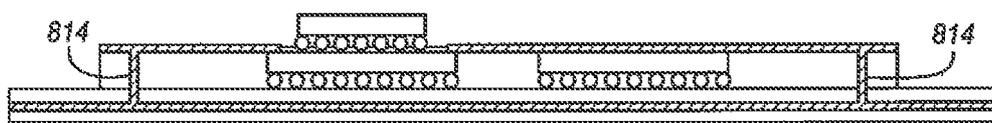


FIG. 8D

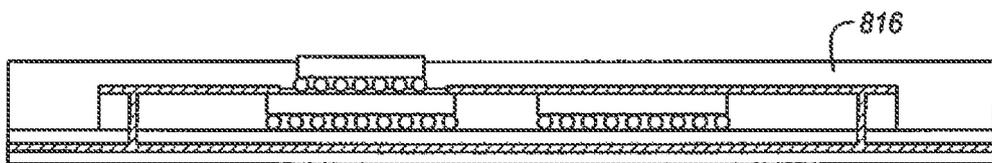
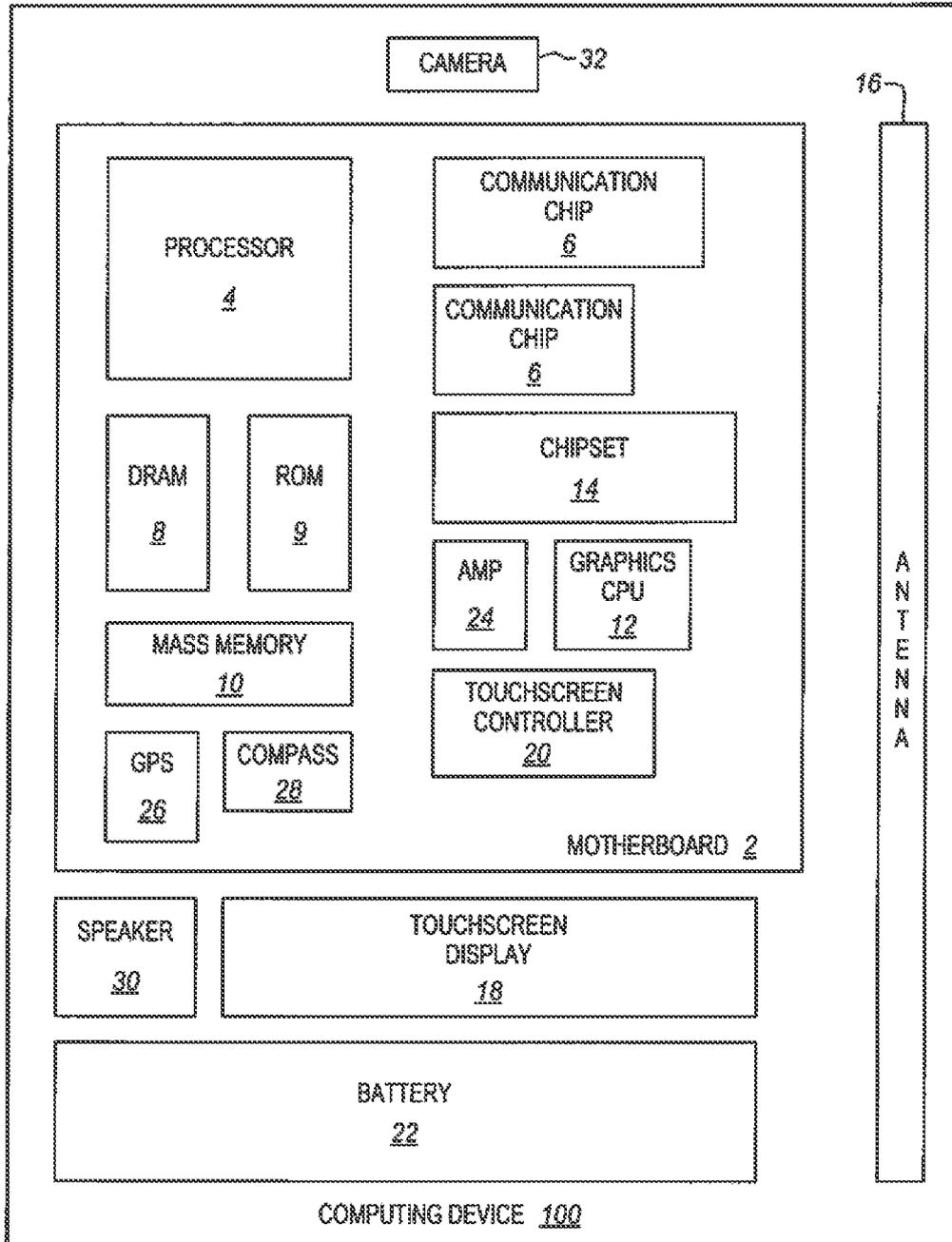


FIG. 8E

FIG. 9



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/057648

A. CLASSIFICATION OF SUBJECT MATTER

HOIL 23/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 23/12; H05K 3/30; A61F 9/08; H05K 7/20; H01L 23/34; G02F 1/133; G02F 1/1333; H01L 25/00; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: package, embedded chip, flexible substrate, shape, curve

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category'	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0185935 AI (CHARLES W. EICHELBEGER et al.) 25 July 2013 See abstract , paragraphs [0004] , [0035H0071] , [0130] and figures 2-4N .	23-32, 39,41-43
Y		33-37 ,44-46 ,49-51 ,54,56
A		1-22 ,38,40, 47-48 ,52-53 ,55
Y	US 2013-0207249 AI (AL VINDASIUS et al.) 15 August 2013 See abstract , paragraphs [0027]-[0047] and figure 6 .	33-37
Y	US 2007-0065984 AI (DANIEL K. LAU et al.) 22 March 2007 See abstract , paragraph [0041] and figure 1 .	44-46 ,49-51 ,54,56
A	US 2013-0100392 AI (YASUMORI FUKUSHIMA) 25 April 2013 See abstract , paragraphs [0009]-[0011] , claim 1 and figures 1-2 .	1-56
A	US 2012-0283799 AI (LONG-SHENG FAN) 08 November 2012 See abstract , paragraphs [0005]-[0015] and figures 1A-2A. ** Thi s Int ernat ional Search Report has been est ablished on the assumpt ion that claims 34, 36 refer to claim 33 .	1-56

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 June 2015 (26.06.2015)

Date of mailing of the international search report

26 June 2015 (26.06.2015)

Name and mailing address of the ISA/KR

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Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/057648

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