(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 November 2017 (23.11.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/199130 A1

(51) International Patent Classification:
H01L 29/786 (2006.01) *C23C 14/08* (2006.01)

(21) International Application Number:
PCT/IB2017/052714

(22) International Filing Date:
10 May 2017 (10.05.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2016-100939 19 May 2016 (19.05.2016) JP

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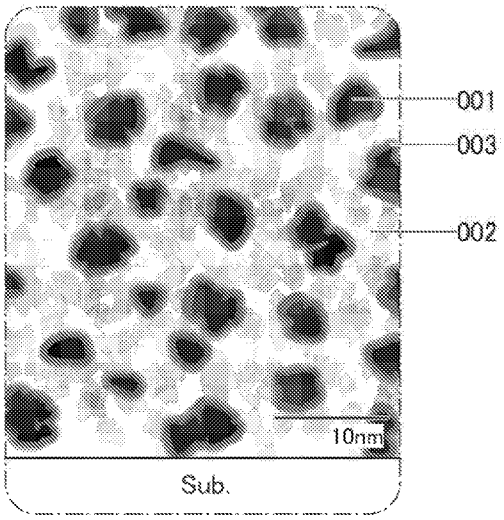
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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: COMPOSITE OXIDE SEMICONDUCTOR AND TRANSISTOR

FIG. 1



(57) Abstract: A novel material is provided. A composite oxide semiconductor includes a first region and a second region. The first region contains indium. The second region contains an element *M* (the element *M* is one or more of Ga, Al, Hf, Y, and Sn). The first region and the second region are arranged in a mosaic pattern. The composite oxide semiconductor further includes a third region. The element M is gallium. The first region contains indium oxide or indium zinc oxide. The second region contains gallium oxide or gallium zinc oxide. The third region contains zinc oxide.

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Published:
— *with international search report (Art. 21(3))*

DESCRIPTION

COMPOSITE OXIDE SEMICONDUCTOR AND TRANSISTOR

TECHNICAL FIELD

[0001]

The present invention relates to an object, a method, or a manufacturing method. The present invention relates to a process, a machine, manufacture, or a composition of matter. One embodiment of the present invention particularly relates to an oxide semiconductor or a manufacturing method of the oxide semiconductor. One embodiment of the present invention relates to a semiconductor device, a display device, a liquid crystal display device, a light-emitting device, a power storage device, a memory device, a method for driving them, or a method for manufacturing them.

[0002]

In this specification and the like, a semiconductor device generally means a device that can function by utilizing semiconductor characteristics. A semiconductor element such as a transistor, a semiconductor circuit, an arithmetic device, and a memory device are each an embodiment of a semiconductor device. An imaging device, a display device, a liquid crystal display device, a light-emitting device, an electro-optical device, a power generation device (including a thin film solar cell, an organic thin film solar cell, and the like), and an electronic appliance may each include a semiconductor device.

BACKGROUND ART

[0003]

Non-Patent Document 1 discloses a solid solution range in the In_2O_3-Ga_2ZnO_4-ZnO system.

[0004]

Furthermore, a technique in which a transistor is fabricated using an In-Ga-Zn-based oxide semiconductor is disclosed (for example, see Patent Document 1).

[0005]

Non-Patent Document 2 discusses a structure where an oxide semiconductor consisting of a dual-layer stack of indium zinc oxide and IGZO is used as an active layer of a transistor.

[Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2007-96055

[Non-Patent Documents]

[0007]

[Non-Patent Document 1] M. Nakamura, N. Kimizuka, and T. Mohri, "The Phase Relations in the In_2O_3-Ga_2ZnO_4-ZnO System at 1350 °C", *J. Solid State Chem.*, 1991, Vol. 93, pp. 298–315.

[Non-Patent Document 2] John F. Wager, "Oxide TFTs: A Progress Report", Information Display 1/16, SID 2016, Jan/Feb 2016, Vol. 32, No. 1, pp. 16–21.

DISCLOSURE OF INVENTION

[0008]

In Non-Patent Document 2, a channel-protective bottom-gate transistor achieves high field-effect mobility (μ = 62 $cm^2V^{-1}s^{-1}$). An active layer of the transistor is a dual-layer stack of indium zinc oxide and IGZO, and the thickness of the indium zinc oxide where a channel is formed is 10 nm. However, the S value (the subthreshold swing (SS)), which is one of transistor characteristics, is as large as 0.41 V/decade. Moreover, the threshold voltage (V_{th}), which is also one of transistor characteristics, is –2.9 V, which means that the transistor has a normally-on characteristic.

[0009]

In view of the above problem, an object of one embodiment of the present invention is to provide a novel oxide semiconductor. Another object is to give favorable electrical characteristics to a semiconductor device. Another object of the present invention is to provide a highly reliable semiconductor device. Another object is to provide a semiconductor device with a novel structure. Another object is to provide a display device with a novel structure.

[0010]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0011]

One embodiment of the present invention is a composite oxide semiconductor including a first region and a second region. The first region contains indium. The second region contains an element *M* (the element *M* is one or more of Ga, Al, Hf, Y, and Sn). The first region and the second region are arranged in a mosaic pattern.

[0012]

The composite oxide semiconductor having the above composition further includes a

third region. The element *M* is gallium. The first region contains indium oxide or indium zinc oxide. The second region contains gallium oxide or gallium zinc oxide. The third region contains zinc oxide.

[0013]

In the above composition, the first region, the second region, or the third region has a blurred periphery and a cloud-like composition.

[0014]

In the composite oxide semiconductor having the above composition, a diameter of the second region is greater than or equal to 0.5 nm and less than or equal to 10 nm, or a neighborhood thereof.

[0015]

In the composite oxide semiconductor having the above composition, a diameter of the second region is greater than or equal to 1 nm and less than or equal to 2 nm, or a neighborhood thereof.

[0016]

In the composite oxide semiconductor having the above composition, an atomic ratio of the indium to the gallium and the zinc is 4:2:3 or a neighborhood thereof.

[0017]

In the composite oxide semiconductor having the above composition, an atomic ratio of the indium to the gallium and the zinc is 5:1:6 or a neighborhood thereof.

[0018]

In the composite oxide semiconductor having the above composition, an atomic ratio of the indium to the gallium and the zinc is 1:1:1 or a neighborhood thereof.

[0019]

Another embodiment of the present invention is a transistor including the composite oxide semiconductor having the above composition.

[0020]

According to one embodiment of the present invention, a novel oxide semiconductor can be provided. According to one embodiment of the present invention, a semiconductor device can be provided with favorable electrical characteristics. A highly reliable semiconductor device can be provided. A semiconductor device with a novel structure can be provided. A display device with a novel structure can be provided.

[0021]

Note that the description of these effects does not preclude the existence of other effects. One embodiment of the present invention does not necessarily achieve all the effects listed above.

Other effects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

BRIEF DESCRIPTION OF DRAWINGS

[0022]

In the accompanying drawings:

FIG. 1 is a conceptual diagram of a composition of an oxide semiconductor;

FIG. 2 is a conceptual diagram of a composition of an oxide semiconductor;

FIGS. 3A to 3C are a top view and cross-sectional views illustrating a semiconductor device;

FIGS. 4A to 4C are a top view and cross-sectional views illustrating a semiconductor device;

FIGS. 5A and 5B are cross-sectional views illustrating a semiconductor device;

FIGS. 6A to 6D are cross-sectional views illustrating a method for manufacturing a semiconductor device;

FIGS. 7A to 7C are cross-sectional views illustrating a method for manufacturing a semiconductor device;

FIGS. 8A to 8C are cross-sectional views illustrating a method for manufacturing a semiconductor device;

FIGS. 9A to 9C are a top view and cross-sectional views illustrating a semiconductor device;

FIGS. 10A to 10C are a top view and cross-sectional views illustrating a semiconductor device;

FIGS. 11A to 11C are a top view and cross-sectional views illustrating a semiconductor device;

FIGS. 12A to 12C are a top view and cross-sectional views illustrating a semiconductor device;

FIGS. 13A to 13C each illustrate an atomic ratio range of an oxide semiconductor of the present invention;

FIG. 14 shows measurement results of XRD spectra of samples of Example;

FIGS. 15A to 15F show cross-sectional TEM images and electron diffraction patterns of samples of Example;

FIGS. 16A to 16L show a plan-view TEM image, a cross-sectional TEM image, and electron diffraction patterns of a sample of Example;

FIG. 17 shows plan-view TEM images of samples of Example and images obtained

through analysis thereof;

FIGS. 18A to 18D illustrate a method for deriving a rotation angle of a hexagon;

FIGS. 19A to 19E illustrate a method for forming a Voronoi diagram;

FIG. 20 shows the number and proportions of shapes of Voronoi regions of Example;

FIGS. 21A to 21H show a plan-view TEM image, a cross-sectional TEM image, and EDX mapping images of a sample of Example;

FIGS. 22A to 22C show EDX mapping images of a sample of Example;

FIG. 23 shows I_d-V_g curves of samples of Example;

FIG. 24 shows I_d-V_g characteristics of samples of Example after +GBT stress tests;

FIGS. 25A to 25F show cross-sectional TEM images and electron diffraction patterns of samples of Example;

FIGS. 26A to 26F show plan-view TEM images of samples of Example and images obtained through analysis thereof;

FIGS. 27A to 27C show the number and proportions of shapes of Voronoi regions of Example;

FIGS. 28A to 28H show a plan-view TEM image, a cross-sectional TEM image, and EDX mapping images of a sample of Example;

FIGS. 29A to 29C show EDX mapping images of a sample of Example; and

FIG. 30 shows I_d-V_g curves of samples of Example.

BEST MODE FOR CARRYING OUT THE INVENTION

[0023]

Hereinafter, embodiments will be described with reference to drawings. However, the embodiments can be implemented with various modes. It will be readily appreciated by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Thus, the present invention should not be interpreted as being limited to the following description of the embodiments.

[0024]

In the drawings, the size, the layer thickness, or the region is exaggerated for clarity in some cases. Therefore, the size, the layer thickness, or the region is not limited to the illustrated scale. Note that the drawings are schematic views showing ideal examples, and embodiments of the present invention are not limited to shapes or values shown in the drawings.

[0025]

Note that in this specification, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not limit the components

numerically.

[0026]

In this specification, terms for describing arrangement, such as "over", "above", "under", and "below", are used for convenience in describing a positional relation between components with reference to drawings. Furthermore, the positional relation between components is changed as appropriate in accordance with a direction in which each component is described. Thus, there is no limitation on terms used in this specification, and description can be made appropriately depending on the situation.

[0027]

In this specification and the like, a transistor is an element having at least three terminals of a gate, a drain, and a source. The transistor has a channel region between a drain (a drain terminal, a drain region, or a drain electrode) and a source (a source terminal, a source region, or a source electrode), and current can flow between the source and the drain through the channel region. Note that in this specification and the like, a channel region refers to a region through which current mainly flows.

[0028]

Furthermore, functions of a source and a drain might be switched when transistors having different polarities are employed or a direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be switched in this specification and the like.

[0029]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an "object having any electric function". There is no particular limitation on the "object having any electric function" as long as electric signals can be transmitted and received between components that are connected through the object. Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0030]

In this specification and the like, a "silicon oxynitride film" refers to a film that includes oxygen at a higher proportion than nitrogen, and a "silicon nitride oxide film" refers to a film that includes nitrogen at a higher proportion than oxygen.

[0031]

In the description of modes of the present invention in this specification and the like with reference to the drawings, the same components in different drawings are commonly

denoted by the same reference numeral in some cases.

[0032]

In this specification and the like, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly also includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. In addition, the term "substantially parallel" indicates that the angle formed between two straight lines is greater than or equal to −30° and less than or equal to 30°. In addition, the term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly also includes the case where the angle is greater than or equal to 85° and less than or equal to 95°. In addition, the term "substantially perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 60° and less than or equal to 120°.

[0033]

In this specification and the like, the terms "film" and "layer" can be interchanged with each other depending on the case. For example, the term "conductive layer" can be changed into the term "conductive film" in some cases. Also, the term "insulating film" can be changed into the term "insulating layer" in some cases.

[0034]

Note that a "semiconductor" includes characteristics of an "insulator" in some cases when the conductivity is sufficiently low, for example. Furthermore, a "semiconductor" and an "insulator" cannot be strictly distinguished from each other in some cases because a border between the "semiconductor" and the "insulator" is not clear. Accordingly, a "semiconductor" in this specification can be called an "insulator" in some cases. Similarly, an "insulator" in this specification can be called a "semiconductor" in some cases.

[0035]

Note that in this specification and the like, "In:Ga:Zn = 4:2:3 or a neighborhood of In:Ga:Zn = 4:2:3" refers to an atomic ratio where, when In is 4 with respect to the total number of atoms, Ga is greater than or equal to 1 and less than or equal to 3 ($1 \leq Ga \leq 3$) and Zn is greater than or equal to 2 and less than or equal to 4 ($2 \leq Zn \leq 4$). "In:Ga:Zn = 5:1:6 or a neighborhood of In:Ga:Zn = 5:1:6" refers to an atomic ratio where, when In is 5 with respect to the total number of atoms, Ga is greater than 0.1 and less than or equal to 2 ($0.1 < Ga \leq 2$) and Zn is greater than or equal to 5 and less than or equal to 7 ($5 \leq Zn \leq 7$). "In:Ga:Zn = 1:1:1 or a neighborhood of In:Ga:Zn = 1:1:1" refers to an atomic ratio where, when In is 1 with respect to the total number of atoms, Ga is greater than 0.1 and less than or equal to 2 ($0.1 < Ga \leq 2$) and

Zn is greater than 0.1 and less than or equal to 2 ($0.1 < Zn \leq 2$).

[0036]

(Embodiment 1)

In this embodiment, an oxide semiconductor material of one embodiment of the present invention will be described.

[0037]

Note that an oxide semiconductor material preferably contains at least indium. In particular, indium and zinc are preferably contained. In addition, gallium, aluminum, yttrium, tin, or the like is preferably contained. Furthermore, one or more elements selected from boron, silicon, titanium, iron, nickel, germanium, zirconium, molybdenum, lanthanum, cerium, neodymium, hafnium, tantalum, tungsten, magnesium, and the like may be contained.

[0038]

Here, the case where an oxide semiconductor material contains indium, an element *M*, and zinc is considered. The element *M* is gallium, aluminum, yttrium, tin, or the like. Other elements that can be used as the element *M* include boron, silicon, titanium, iron, nickel, germanium, zirconium, molybdenum, lanthanum, cerium, neodymium, hafnium, tantalum, tungsten, and magnesium. Note that two or more of the above elements may be used in combination as the element *M*. Note that the terms of the atomic ratio of indium to the element *M* and zinc in the oxide semiconductor are denoted by [In], [*M*], and [Zn], respectively.

[0039]

<Composition of oxide semiconductor material>

FIG. 1 and FIG. 2 are conceptual diagrams of oxide semiconductor materials of the present invention. In this specification, an oxide semiconductor of one embodiment of the present invention is defined as a cloud-aligned composite oxide semiconductor (CAC-OS).

[0040]

As illustrated in FIG. 1, the CAC has, for example, a composition in which elements included in the oxide semiconductor material are unevenly distributed, and regions 001, regions 002, and regions 003 mainly including the respective elements are formed. The regions 001, 002, and 003 are mixed to form a mosaic pattern. In other words, in the composition of the CAC-OS, materials including unevenly distributed elements each have a size of greater than or equal to 0.5 nm and less than or equal to 10 nm, preferably greater than or equal to 1 nm and less than or equal to 2 nm, or a similar size. Note that in the following description of an oxide semiconductor, a state in which one or more metal elements are unevenly distributed and regions including the metal element(s) are mixed is referred to as a mosaic pattern or a patch-like pattern. The region has a size of greater than or equal to 0.5 nm and less than or equal to 10 nm,

preferably greater than or equal to 1 nm and less than or equal to 2 nm, or a similar size.

[0041]

For example, an In-*M*-Zn oxide with the CAC composition has a composition in which materials are separated into indium oxide (InO_{X1}, where $X1$ is a real number greater than 0) or indium zinc oxide ($In_{X2}Zn_{Y2}O_{Z2}$, where $X2$, $Y2$, and $Z2$ are real numbers greater than 0), and an oxide of the element *M* (MO_{X3}, where $X3$ is a real number greater than 0) or an *M*-Zn oxide ($M_{X4}Zn_{Y4}O_{Z4}$, where $X4$, $Y4$, and $Z4$ are real numbers greater than 0), and a mosaic pattern is formed. InO_{X1} or $In_{X2}Zn_{Y2}O_{Z2}$ forming the mosaic pattern is uniformly distributed in the film. This composition is also referred to as a cloud-like composition.

[0042]

Here, suppose that the concept of FIG. 1 is applied to an In-*M*-Zn oxide with the CAC composition. In this case, it can be said that the region 001 is a region including MO_{X3} as a main component, the region 002 is a region including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component, and the region 003 is a region including at least Zn. Surrounding portions of the region including MO_{X3} as a main component, the region including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component, and the region including at least Zn are unclear (blurred), so that boundaries are not clearly observed in some cases.

[0043]

That is, the In-*M*-Zn oxide with the CAC composition is a composite oxide semiconductor with a composition in which a region including MO_{X3} as a main component and a region including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are mixed. Thus, the oxide semiconductor material is referred to as a composite oxide semiconductor in some cases. Note that in this specification, for example, when the atomic ratio of In to the element *M* in the region 002 is greater than the atomic ratio of In to the element *M* in the region 001, the region 002 has higher In concentration than the region 001.

[0044]

Note that in the CAC composition, a stacked-layer structure including two or more films with different atomic ratios is not included. For example, a two-layer structure of a film including In as a main component and a film including Ga as a main component is not included.

[0045]

Specifically, of In-Ga-Zn oxide (hereinafter also referred to as IGZO), CAC-IGZO is described. The CAC-IGZO is an oxide material in which materials are separated into InO_{X1} or $In_{X2}Zn_{Y2}O_{Z2}$, and gallium oxide (GaO_{X5}, where $X5$ is a real number greater than 0) or gallium zinc oxide ($Ga_{X6}Zn_{Y6}O_{Z6}$, where $X6$, $Y6$, and $Z6$ are real numbers greater than 0), for example, and a mosaic pattern is formed. InO_{X1} or $In_{X2}Zn_{Y2}O_{Z2}$ forming the mosaic pattern is a cloud-like

oxide material.

[0046]

That is, the CAC-IGZO is a composite oxide semiconductor with a composition in which a region including GaO_{X5} as a main component and a region including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are mixed. Surrounding portions of the region including GaO_{X5} as a main component and the region including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are unclear (blurred), so that boundaries are not clearly observed in some cases.

[0047]

Note that the sizes of the regions 001 to 003 can be obtained by EDX mapping. For example, the diameter of the region 001 is greater than or equal to 0.5 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 2 nm in the EDX mapping image of a cross-sectional photograph in some cases. The density of an element which is a main component is gradually lowered from the central portion of the region toward the surrounding portion. For example, when the number (abundance) of atoms of an element countable in an EDX mapping image gradually changes from the central portion toward the surrounding portion, the surrounding portion of the region is unclear (blurred) in the EDX mapping of the cross-sectional photograph. For example, from the central portion toward the surrounding portion in the region including GaO_{X5} as a main component, the number of Ga atoms gradually reduces and the number of Zn atoms gradually increases, so that the region including $Ga_{X6}Zn_{Y6}O_{Z6}$ as a main component gradually appears. Accordingly, the surrounding portion of the region including GaO_{X5} as a main component is unclear (blurred) in the EDX mapping image.

[0048]

Here, a compound including In, Ga, Zn, and O is also known as IGZO. Typical examples of IGZO include a crystalline compound represented by $InGaO_3(ZnO)_{m1}$ ($m1$ is a natural number) and a crystalline compound represented by $In_{(1+x0)}Ga_{(1-x0)}O_3(ZnO)_{m0}$ ($-1 \leq x0 \leq 1$; $m0$ is a given number).

[0049]

The above crystalline compounds have a single crystal structure, a polycrystalline structure, or a c-axis-aligned crystalline (CAAC) structure. Note that the CAAC structure is a layered crystal structure in which a plurality of IGZO nanocrystals have c-axis alignment and are connected in the a–b plane direction without alignment.

[0050]

In contrast, the crystal structure is a secondary element for the CAC-IGZO. In this specification, CAC-IGZO can be defined as an oxide material containing In, Ga, Zn, and O in

the state where a plurality of regions including Ga as a main component and a plurality of regions including In as a main component are each dispersed randomly in a mosaic pattern.

[0051]

For example, in the conceptual diagram of FIG. 1, the region 001 and the region 002 correspond to a region including Ga as a main component and a region including In as a main component, respectively. In addition, the region 003 corresponds to a region including Zn. Note that the region including Ga as a main component and the region including In as a main component may each be referred to as a nanoparticle. The diameter of the nanoparticle is greater than or equal to 0.5 nm and less than or equal to 10 nm, typically greater than or equal to 1 nm and less than or equal to 2 nm. Surrounding portions of the nanoparticles are unclear (blurred), so that a boundary is not clearly observed in some cases.

[0052]

In addition, FIG. 2 is a modification example of the conceptual diagram of FIG. 1. As shown in FIG. 2, the shapes and densities of the regions 001, 002, and 003 may change depending on formation conditions of the CAC-OS.

[0053]

The crystallinity of the CAC-IGZO can be analyzed by electron diffraction. For example, a ring-like region with high luminance is observed in an electron diffraction pattern image. Furthermore, a plurality of spots are observed in the ring-like region in some cases.

[0054]

As described above, CAC-IGZO has a structure different from that of an IGZO compound in which metal elements are evenly distributed, and has characteristics different from those of the IGZO compound. That is, in CAC-IGZO, regions including GaO_{X5} or the like as a main component and regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are separated to form a mosaic pattern. Accordingly, when CAC-IGZO is used for a semiconductor element, the property derived from GaO_{X5} or the like and the property derived from $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} complement each other, whereby high on-state current (I_{on}), high field-effect mobility (μ), and low off-state current (I_{off}) can be achieved.

[0055]

Note that the conduction mechanism of a semiconductor element including CAC-IGZO that achieves high on-state current (I_{on}), high field-effect mobility (μ),and low off-state current (I_{off}) can be presumed by a random-resistance-network model in percolation theory.

[0056]

A semiconductor element including CAC-IGZO has high reliability. Thus, CAC-IGZO is suitably used in a variety of semiconductor devices typified by a display.

[0057]

<Transistor including oxide semiconductor material>

Next, the case where the oxide material is used for an oxide semiconductor in a transistor is described.

[0058]

With the use of the oxide material in a transistor, the transistor can have high field-effect mobility and high switching characteristics. In addition, the transistor can have high reliability.

[0059]

A semiconductor with a low carrier density is preferably used in a transistor. For example, an oxide semiconductor whose carrier density is lower than 8×10^{11} /cm^3, preferably lower than 1×10^{11} /cm^3, further preferably lower than 1×10^{10} /cm^3, and greater than or equal to 1×10^{-9} /cm^3 is used.

[0060]

A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier generation sources, and thus can have a low carrier density. A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has a low density of defect states and accordingly has a low density of trap states in some cases.

[0061]

Charges trapped by the trap states in the oxide semiconductor take a long time to be released and may behave like fixed charges. Thus, the transistor whose channel region is formed in the oxide semiconductor having a high density of trap states has unstable electrical characteristics in some cases.

[0062]

To obtain stable electrical characteristics of the transistor, it is effective to reduce the concentration of impurities in the oxide semiconductor. In addition, to reduce the concentration of impurities in the oxide semiconductor, the concentration of impurities in a film that is adjacent to the oxide semiconductor is preferably reduced. Examples of impurities include hydrogen, nitrogen, alkali metal, alkaline earth metal, iron, nickel, and silicon.

[0063]

Here, the influence of impurities in the oxide semiconductor will be described.

[0064]

When silicon or carbon that is one of Group 14 elements is contained in the oxide semiconductor, defect states are formed. Thus, the concentration of silicon or carbon in the oxide semiconductor and around an interface with the oxide semiconductor (measured by

secondary ion mass spectrometry (SIMS)) is set lower than or equal to 2×10^{18} atoms/cm^3, and preferably lower than or equal to 2×10^{17} atoms/cm^3.

[0065]

When the oxide semiconductor contains alkali metal or alkaline earth metal, defect states are formed and carriers are generated, in some cases. Thus, a transistor including an oxide semiconductor which contains alkali metal or alkaline earth metal is likely to be normally-on. Therefore, it is preferable to reduce the concentration of alkali metal or alkaline earth metal in the oxide semiconductor. Specifically, the concentration of alkali metal or alkaline earth metal in the oxide semiconductor, which is measured by SIMS, is lower than or equal to 1×10^{18} atoms/cm^3, preferably lower than or equal to 2×10^{16} atoms/cm^3.

[0066]

When the oxide semiconductor contains nitrogen, the oxide semiconductor easily becomes n-type by generation of electrons serving as carriers and an increase of carrier density. Thus, a transistor including an oxide semiconductor which contains nitrogen is likely to be normally-on. For this reason, nitrogen in the oxide semiconductor is preferably reduced as much as possible; the nitrogen concentration measured by SIMS is set, for example, lower than 5×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, further preferably lower than or equal to 1×10^{18} atoms/cm^3, and still further preferably lower than or equal to 5×10^{17} atoms/cm^3.

[0067]

Hydrogen contained in an oxide semiconductor reacts with oxygen bonded to a metal atom to be water, and thus causes an oxygen vacancy (V_O), in some cases. Due to entry of hydrogen into the oxygen vacancy (V_O), an electron serving as a carrier is generated in some cases. Furthermore, in some cases, bonding of part of hydrogen to oxygen bonded to a metal atom causes generation of an electron serving as a carrier. Thus, a transistor including an oxide semiconductor that contains hydrogen is likely to be normally-on. Accordingly, it is preferable that hydrogen in the oxide semiconductor be reduced as much as possible. Specifically, the hydrogen concentration measured by SIMS is set lower than 1×10^{20} atoms/cm^3, preferably lower than 1×10^{19} atoms/cm^3, further preferably lower than 5×10^{18} atoms/cm^3, and still further preferably lower than 1×10^{18} atoms/cm^3.

[0068]

Note that oxygen vacancies (V_O) in the oxide semiconductor can be reduced by introduction of oxygen into the oxide semiconductor. That is, the oxygen vacancies (V_O) in the oxide semiconductor disappear when the oxygen vacancies (V_O) are filled with oxygen. Accordingly, diffusion of oxygen in the oxide semiconductor can reduce the oxygen vacancies

(V_O) in a transistor and improve the reliability of the transistor.

[0069]

As a method for introducing oxygen into the oxide semiconductor, for example, an oxide in which oxygen content is higher than that in the stoichiometric composition is provided in contact with the oxide semiconductor. That is, in the oxide, a region including oxygen in excess of that in the stoichiometric composition (hereinafter also referred to as an excess-oxygen region) is preferably formed. In particular, in the case of using an oxide semiconductor in a transistor, an oxide including an excess-oxygen region is provided in a base film, an interlayer film, or the like in the vicinity of the transistor, whereby oxygen vacancies in the transistor are reduced, and the reliability can be improved.

[0070]

When an oxide semiconductor with sufficiently reduced impurity concentration is used for a channel formation region in a transistor, the transistor can have stable electrical characteristics.

[0071]

<Method for forming oxide semiconductor material>

An example of a method for forming the oxide semiconductor material is described below.

[0072]

The oxide semiconductor is preferably deposited at a temperature higher than or equal to room temperature and lower than 140 °C. Note that room temperature includes not only the case where temperature control is not performed but also the case where temperature control is performed, e.g., the case where a substrate is cooled.

[0073]

As a sputtering gas, a rare gas (typically argon), oxygen, or a mixed gas of a rare gas and oxygen is used as appropriate. When the mixed gas is used, the proportion of the oxygen gas in the whole deposition gas is higher than or equal to 5 % and lower than or equal to 30 %, preferably higher than or equal to 7 % and lower than or equal to 20 %.

[0074]

When the sputtering gas contains oxygen, oxygen can be added to a film under the oxide semiconductor and an excess-oxygen region can be provided at the same time as the deposition of the oxide semiconductor. In addition, increasing the purity of a sputtering gas is necessary. For example, when a gas which is highly purified to have a dew point of −40 °C or lower, preferably −80 °C or lower, further preferably −100 °C or lower, still further preferably −120 °C or lower, is used as a sputtering gas, i.e., the oxygen gas or the argon gas, entry of

moisture or the like into the oxide semiconductor can be minimized.

[0075]

In the case where the oxide semiconductor is deposited by a sputtering method, a chamber in a sputtering apparatus is preferably evacuated to be a high vacuum state (to the degree of about 5×10^{-7} Pa to 1×10^{-4} Pa) with an adsorption vacuum evacuation pump such as a cryopump in order to remove water or the like, which serves as an impurity for the oxide semiconductor, as much as possible. Alternatively, a turbo molecular pump and a cold trap are preferably combined so as to prevent a backflow of a gas, especially a gas containing carbon or hydrogen from an exhaust system to the inside of the chamber.

[0076]

As a target, an In-Ga-Zn metal oxide target can be used. For example, a metal oxide target where an atomic ratio [In]:[Ga]:[Zn] is 4:2:4.1, 5:1:7, or a neighborhood thereof is preferably used.

[0077]

In the sputtering apparatus, the target may be rotated or moved. For example, a magnet unit is oscillated vertically and/or horizontally during the deposition, whereby the composite oxide semiconductor of the present invention can be formed. For example, the target may be rotated or moved with a beat (also referred to as rhythm, pulse, frequency, period, cycle, or the like) of greater than or equal to 0.1 Hz and less than or equal to 1 kHz. Alternatively, the magnet unit may be oscillated with a beat of greater than or equal to 0.1 Hz and less than or equal to 1 kHz.

[0078]

The oxide semiconductor of the present invention can be formed, for example, in the following manner: a mixed gas of oxygen and a rare gas in which the proportion of oxygen is approximately 10 % is used; the substrate temperature is 130 °C; and an In-Ga-Zn metal oxide target where an atomic ratio [In]:[Ga]:[Zn] is 4:2:4.1 is oscillated during the deposition.

[0079]

The structure described in this embodiment can be used in appropriate combination with any of the structures described in the other embodiments or examples.

[0080]

(Embodiment 2)

In this embodiment, semiconductor devices each including the oxide material of embodiments of the present invention, and manufacturing methods thereof will be described with reference to FIGS. 3A to 3C, FIGS. 4A to 4C, FIGS. 5A and 5B, FIGS. 6A to 6D, FIGS. 7A to 7C, FIGS. 8A to 8C, FIGS. 9A to 9C, FIGS. 10A to 10C, FIGS. 11A to 11C, and FIGS. 12A to

12C.

[0081]

<Structure example 1 of transistor>

FIG. 3A is a top view of a transistor 100 that is a semiconductor device including the oxide material of one embodiment of the present invention. FIG. 3B is a cross-sectional view taken along dashed-dotted line X1–X2 in FIG. 3A. FIG. 3C is a cross-sectional view taken along dashed-dotted line Y1–Y2 in FIG. 3A. Note that in FIG. 3A, some components of the transistor 100 (e.g., an insulating film functioning as a gate insulating film) are not illustrated to avoid complexity. The direction of the dashed-dotted line X1–X2 may be called a channel length direction, and the direction of the dashed-dotted line Y1–Y2 may be called a channel width direction. As in FIG. 3A, some components are not illustrated in some cases in top views of transistors described below.

[0082]

The transistor 100 illustrated in FIGS. 3A to 3C is what is called a top-gate transistor.

[0083]

The transistor 100 includes an insulating film 104 over a substrate 102, an oxide semiconductor film 108 over the insulating film 104, an insulating film 110 over the oxide semiconductor film 108, a conductive film 112 over the insulating film 110, and an insulating film 116 over the insulating film 104, the oxide semiconductor film 108, and the conductive film 112.

[0084]

In a region which overlaps with the conductive film 112, the oxide semiconductor film 108 is provided over the insulating film 104. For example, the oxide semiconductor film 108 preferably contains In, *M* (*M* is Al, Ga, Y, or Sn), and Zn.

[0085]

The oxide semiconductor film 108 includes regions 108n which do not overlap with the conductive film 112 and are in contact with the insulating film 116. The regions 108n are n-type regions in the oxide semiconductor film 108 described above. The regions 108n are in contact with the insulating film 116, and the insulating film 116 contains nitrogen or hydrogen. Nitrogen or hydrogen in the insulating film 116 is added to the regions 108n to increase the carrier density, thereby making the regions 108n n-type.

[0086]

The oxide semiconductor film 108 preferably includes a region in which the atomic proportion of In is larger than the atomic proportion of *M*. For example, the atomic ratio of In to *M* and Zn in the oxide semiconductor film 108 is preferably In:*M*:Zn = 4:2:3 or in the

neighborhood thereof.

[0087]

Note that the composition of the oxide semiconductor film 108 is not limited to the above. For example, the atomic ratio of In to *M* and Zn in the oxide semiconductor film 108 is preferably In:*M*:Zn = 5:1:6 or in the neighborhood thereof. The term "neighborhood" includes the following: when In is 5, *M* is greater than or equal to 0.5 and less than or equal to 1.5, and Zn is greater than or equal to 5 and less than or equal to 7.

[0088]

When the oxide semiconductor film 108 has a region in which the atomic proportion of In is larger than the atomic proportion of *M*, the transistor 100 can have high field-effect mobility. Specifically, the field-effect mobility of the transistor 100 can exceed 10 cm^2/Vs, preferably exceed 30 cm^2/Vs.

[0089]

For example, the use of the transistor with high field-effect mobility in a gate driver that generates a gate signal allows the display device to have a narrow frame. The use of the transistor with high field-effect mobility in a source driver (particularly in a demultiplexer connected to an output terminal of a shift register included in a source driver) that is included in a display device and supplies a signal from a signal line can reduce the number of wirings connected to the display device.

[0090]

Even when the oxide semiconductor film 108 includes a region in which the atomic proportion of In is higher than the atomic proportion of *M*, the field-effect mobility might be low if the oxide semiconductor film 108 has high crystallinity.

[0091]

Note that the crystallinity of the oxide semiconductor film 108 can be determined by analysis by X-ray diffraction (XRD) or with a transmission electron microscope (TEM), for example.

[0092]

First, oxygen vacancies that might be formed in the oxide semiconductor film 108 will be described.

[0093]

Oxygen vacancies formed in the oxide semiconductor film 108 adversely affect the transistor characteristics and therefore cause a problem. For example, hydrogen is trapped in oxygen vacancies formed in the oxide semiconductor film 108 to serve as a carrier supply source. The carrier supply source generated in the oxide semiconductor film 108 causes a change in the

electrical characteristics, typically, shift in the threshold voltage, of the transistor 100 including the oxide semiconductor film 108. Therefore, it is preferable that the amount of oxygen vacancies in the oxide semiconductor film 108 be as small as possible.

[0094]

In one embodiment of the present invention, the insulating film in the vicinity of the oxide semiconductor film 108 contains excess oxygen. Specifically, one or both of the insulating film 110 which is formed over the oxide semiconductor film 108 and the insulating film 104 which is formed below the oxide semiconductor film 108 contain excess oxygen. Oxygen or excess oxygen is transferred from the insulating film 104 and/or the insulating film 110 to the oxide semiconductor film 108, whereby oxygen vacancies in the oxide semiconductor film can be reduced.

[0095]

Impurities such as hydrogen and moisture entering the oxide semiconductor film 108 adversely affect the transistor characteristics and therefore cause a problem. Thus, it is preferable that the amount of impurities such as hydrogen and moisture in the oxide semiconductor film 108 be as small as possible.

[0096]

Note that it is preferable to use, as the oxide semiconductor film 108, an oxide semiconductor film in which the impurity concentration is low and the density of defect states is low, in which case the transistor can have more excellent electrical characteristics. Here, the state in which the impurity concentration is low and the density of defect states is low (the amount of oxygen vacancies is small) is referred to as "highly purified intrinsic" or "substantially highly purified intrinsic". A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier generation sources, and thus can have a low carrier density. Thus, a transistor in which a channel region is formed in the oxide semiconductor film rarely has a negative threshold voltage (is rarely normally on). A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has a low density of defect states and accordingly has a low density of trap states in some cases. Furthermore, the highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has an extremely low off-state current; even when an element has a channel width of 1×10^6 μm and a channel length of 10 μm, the off-state current can be less than or equal to the measurement limit of a semiconductor parameter analyzer, that is, less than or equal to 1×10^{-13} A, at a voltage (drain voltage) between a source electrode and a drain electrode of from 1 V to 10 V.

[0097]

As illustrated in FIGS. 3A to 3C, the transistor 100 may further include an insulating

film 118 over the insulating film 116, a conductive film 120a electrically connected to the region 108n through an opening 141a formed in the insulating films 116 and 118; and a conductive film 120b electrically connected to the region 108n through an opening 141b formed in the insulating films 116 and 118.

[0098]

Note that in this specification and the like, the insulating film 104 may be referred to as a first insulating film, the insulating film 110 may be referred to as a second insulating film, the insulating film 116 may be referred to as a third insulating film, and the insulating film 118 may be referred to as a fourth insulating film. The conductive films 112, 120a, and 120b function as a gate electrode, a source electrode, and a drain electrode, respectively.

[0099]

The insulating film 110 functions as a gate insulating film. The insulating film 110 includes an excess-oxygen region. Since the insulating film 110 includes the excess-oxygen region, excess oxygen can be supplied to the oxide semiconductor film 108. As a result, oxygen vacancies that might be formed in the oxide semiconductor film 108 can be filled with excess oxygen, and the semiconductor device can have high reliability.

[0100]

To supply excess oxygen to the oxide semiconductor film 108, excess oxygen may be supplied to the insulating film 104 that is formed below the oxide semiconductor film 108. In that case, excess oxygen contained in the insulating film 104 might also be supplied to the regions 108n, which is not desirable because the resistance of the regions 108n might be increased. In contrast, in the structure in which the insulating film 110 formed over the oxide semiconductor film 108 contains excess oxygen, excess oxygen can be selectively supplied only to a region overlapping with the conductive film 112.

[0101]

<Components of semiconductor device>

Next, components of the semiconductor device in this embodiment will be described in detail.

[0102]

[Substrate]

There is no particular limitation on a material and the like of the substrate 102 as long as the material has heat resistance high enough to withstand at least heat treatment to be performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like may be used as the substrate 102. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon or silicon carbide,

a compound semiconductor substrate of silicon germanium, an SOI substrate, or the like can be used, or any of these substrates provided with a semiconductor element may be used as the substrate 102. In the case where a glass substrate is used as the substrate 102, a glass substrate having any of the following sizes can be used: the 6th generation (1500 mm × 1850 mm), the 7th generation (1870 mm × 2200 mm), the 8th generation (2200 mm × 2400 mm), the 9th generation (2400 mm × 2800 mm), and the 10th generation (2950 mm × 3400 mm). Thus, a large-sized display device can be fabricated.

[0103]

Alternatively, a flexible substrate may be used as the substrate 102, and the transistor 100 may be provided directly on the flexible substrate. Alternatively, a separation layer may be provided between the substrate 102 and the transistor 100. The separation layer can be used when part or the whole of a semiconductor device formed over the separation layer is separated from the substrate 102 and transferred onto another substrate. In such a case, the transistor 100 can be transferred to a substrate having low heat resistance or a flexible substrate as well.

[0104]

[First insulating film]

The insulating film 104 can be formed by a sputtering method, a CVD method, an evaporation method, a pulsed laser deposition (PLD) method, a printing method, a coating method, or the like as appropriate. For example, the insulating film 104 can be formed to have a single-layer structure or stacked-layer structure including an oxide insulating film and/or a nitride insulating film. To improve the properties of the interface with the oxide semiconductor film 108, at least a region of the insulating film 104 which is in contact with the oxide semiconductor film 108 is preferably formed using an oxide insulating film. When the insulating film 104 is formed using an oxide insulating film from which oxygen is released by heating, oxygen contained in the insulating film 104 can be moved to the oxide semiconductor film 108 by heat treatment.

[0105]

The thickness of the insulating film 104 can be greater than or equal to 50 nm, greater than or equal to 100 nm and less than or equal to 3000 nm, or greater than or equal to 200 nm and less than or equal to 1000 nm. By increasing the thickness of the insulating film 104, the amount of oxygen released from the insulating film 104 can be increased. In addition, interface states at the interface between the insulating film 104 and the oxide semiconductor film 108 and oxygen vacancies included in the oxide semiconductor film 108 can be reduced.

[0106]

For example, the insulating film 104 can be formed to have a single-layer structure or

stacked-layer structure including silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, aluminum oxide, hafnium oxide, gallium oxide, a Ga-Zn oxide, or the like. In this embodiment, the insulating film 104 has a stacked-layer structure including a silicon nitride film and a silicon oxynitride film. With the insulating film 104 having such a stack-layer structure including a silicon nitride film as a lower layer and a silicon oxynitride film as an upper layer, oxygen can be efficiently introduced into the oxide semiconductor film 108.

[0107]

[Conductive film]

The conductive film 112 functioning as a gate electrode and the conductive films 120a and 120b functioning as a source electrode and a drain electrode can each be formed using a metal element selected from chromium (Cr), copper (Cu), aluminum (Al), gold (Au), silver (Ag), zinc (Zn), molybdenum (Mo), tantalum (Ta), titanium (Ti), tungsten (W), manganese (Mn), nickel (Ni), iron (Fe), and cobalt (Co); an alloy including any of these metal elements as its component; an alloy including a combination of any of these metal elements; or the like.

[0108]

Furthermore, the conductive films 112, 120a, and 120b can be formed using an oxide conductor or an oxide semiconductor, such as an oxide including indium and tin (In-Sn oxide), an oxide including indium and tungsten (In-W oxide), an oxide including indium, tungsten, and zinc (In-W-Zn oxide), an oxide including indium and titanium (In-Ti oxide), an oxide including indium, titanium, and tin (In-Ti-Sn oxide), an oxide including indium and zinc (In-Zn oxide), an oxide including indium, tin, and silicon (In-Sn-Si oxide), or an oxide including indium, gallium, and zinc (In-Ga-Zn oxide).

[0109]

Here, an oxide conductor is described. In this specification and the like, an oxide conductor may be referred to as OC. For example, oxygen vacancies are formed in an oxide semiconductor, and then hydrogen is added to the oxygen vacancies, so that a donor level is formed in the vicinity of the conduction band. This increases the conductivity of the oxide semiconductor; accordingly, the oxide semiconductor becomes a conductor. The oxide semiconductor having become a conductor can be referred to as an oxide conductor. oxide semiconductors generally transmit visible light because of their large energy gap. Since an oxide conductor is an oxide semiconductor having a donor level in the vicinity of the conduction band, the influence of absorption due to the donor level is small in an oxide conductor, and an oxide conductor has a visible light transmitting property comparable to that of an oxide semiconductor.

[0110]

It is particularly preferred to use the oxide conductor described above for the conductive film 112, in which case excess oxygen can be added to the insulating film 110.

[0111]

A Cu-X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) may be used as the conductive films 112, 120a, and 120b. The use of a Cu-X alloy film results in lower fabrication costs because the film can be processed by wet etching.

[0112]

Among the above-mentioned metal elements, any one or more elements selected from titanium, tungsten, tantalum, and molybdenum are preferably included in the conductive films 112, 120a, and 120b. A tantalum nitride film is particularly preferable as each of the conductive films 112, 120a, and 120b. A tantalum nitride film has conductivity and a high barrier property against copper or hydrogen. Because a tantalum nitride film releases little hydrogen from itself, it can be favorably used as the conductive film in contact with the oxide semiconductor film 108 or the conductive film in the vicinity of the oxide semiconductor film 108.

[0113]

The conductive films 112, 120a, and 120b can be formed by electroless plating. As a material that can be deposited by electroless plating, for example, one or more elements selected from Cu, Ni, Al, Au, Sn, Co, Ag, and Pd can be used. It is further favorable to use Cu or Ag because the resistance of the conductive film can be reduced.

[0114]

[Second insulating film]

As the insulating film 110 functioning as a gate insulating film of the transistor 100, an insulating layer including at least one of the following films formed by a plasma enhanced chemical vapor deposition (PECVD) method, a sputtering method, or the like can be used: a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film, an yttrium oxide film, a zirconium oxide film, a gallium oxide film, a tantalum oxide film, a magnesium oxide film, a lanthanum oxide film, a cerium oxide film, and a neodymium oxide film. Note that the insulating film 110 may have a two-layer structure or a stacked-layer structure including three or more layers.

[0115]

The insulating film 110 that is in contact with the oxide semiconductor film 108 functioning as a channel region of the transistor 100 is preferably an oxide insulating film and preferably includes a region including oxygen in excess of the stoichiometric composition (excess-oxygen region). In other words, the insulating film 110 is an insulating film capable of

releasing oxygen. In order to provide the excess-oxygen region in the insulating film 110, the insulating film 110 is formed in an oxygen atmosphere, or the deposited insulating film 110 is subjected to heat treatment in an oxygen atmosphere, for example.

[0116]

In the case of using a stacked-layer structure containing hafnium oxide for the insulating film 110, the following effects are attained. Hafnium oxide has higher dielectric constant than silicon oxide and silicon oxynitride. Therefore, by using hafnium oxide, the thickness of the insulating film 110 can be made large as compared with the case of using silicon oxide; thus, leakage current due to tunnel current can be low. That is, it is possible to provide a transistor with a low off-state current. Moreover, hafnium oxide having a crystal structure has a higher dielectric constant than hafnium oxide having an amorphous structure. Therefore, it is preferable to use hafnium oxide having a crystal structure, in order to obtain a transistor with a low off-state current. Examples of the crystal structure include a monoclinic crystal structure and a cubic crystal structure. Note that one embodiment of the present invention is not limited to the above examples.

[0117]

It is preferable that the insulating film 110 have few defects and typically have as few signals observed by electron spin resonance (ESR) spectroscopy as possible. Examples of the signals include a signal due to an E′ center observed at a *g*-factor of 2.001. Note that the E′ center is due to the dangling bond of silicon. As the insulating film 110, a silicon oxide film or a silicon oxynitride film whose spin density of a signal due to the E′ center is lower than or equal to 3×10^{17} spins/cm^3 and preferably lower than or equal to 5×10^{16} spins/cm^3 may be used.

[0118]

In addition to the above-described signal, a signal due to nitrogen dioxide (NO_2) might be observed in the insulating film 110. The signal is divided into three signals according to the N nuclear spin; a first signal, a second signal, and a third signal. The first signal is observed at a *g*-factor of greater than or equal to 2.037 and less than or equal to 2.039. The second signal is observed at a *g*-factor of greater than or equal to 2.001 and less than or equal to 2.003. The third signal is observed at a *g*-factor of greater than or equal to 1.964 and less than or equal to 1.966.

[0119]

It is suitable to use an insulating film whose spin density of a signal due to nitrogen dioxide (NO_2) is higher than or equal to 1×10^{17} spins/cm^3 and lower than 1×10^{18} spins/cm^3 as the insulating film 110, for example.

[0120]

Note that a nitrogen oxide (NO_x) such as nitrogen dioxide (NO_2) forms a state in the insulating film 110. The state is positioned in the energy gap of the oxide semiconductor film 108. Thus, when nitrogen oxide (NO_x) is diffused to the interface between the insulating film 110 and the oxide semiconductor film 108, an electron might be trapped by the state on the insulating film 110 side. As a result, the trapped electron remains in the vicinity of the interface between the insulating film 110 and the oxide semiconductor film 108, leading to a positive shift of the threshold voltage of the transistor. Accordingly, the use of a film with a low nitrogen oxide content as the insulating film 110 can reduce a shift of the threshold voltage of the transistor.

[0121]

As an insulating film that releases a small amount of nitrogen oxide (NO_x), for example, a silicon oxynitride film can be used. The silicon oxynitride film releases more ammonia than nitrogen oxide (NO_x) in thermal desorption spectroscopy (TDS) analysis; the typical released amount of ammonia is greater than or equal to 1×10^{18} molecules/cm^3 and less than or equal to 5×10^{19} molecules/cm^3. Note that the released amount of ammonia is the total amount of ammonia released by heat treatment in a range of 50 °C to 650 °C or 50 °C to 550 °C in TDS analysis.

[0122]

Since nitrogen oxide (NO_x) reacts with ammonia and oxygen in heat treatment, the use of an insulating film that releases a large amount of ammonia reduces nitrogen oxide (NO_x).

[0123]

Note that in the case where the insulating film 110 is analyzed by SIMS, the nitrogen concentration in the film is preferably lower than or equal to 6×10^{20} atoms/cm^3.

[0124]

[Oxide semiconductor film]

As the oxide semiconductor film 108, the material described above can be used.

[0125]

<Atomic ratio>

Preferred ranges of the atomic ratio of indium, the element *M*, and zinc contained in the oxide semiconductor according to the present invention are described with reference to FIGS. 13A to 13C. Note that the proportion of oxygen atoms is not illustrated in FIGS. 13A to 13C. The terms of the atomic ratio of indium, the element *M*, and zinc contained in the oxide semiconductor are denoted by [In], [*M*], and [Zn], respectively.

[0126]

In FIGS. 13A to 13C, dashed lines indicate a line where the atomic ratio [In]:[*M*]:[Zn] is

$(1+\alpha):(1-\alpha):1$ where α is a real number greater than or equal to −1 and less than or equal to 1, a line where the atomic ratio [In]:[*M*]:[Zn] is $(1+\alpha):(1-\alpha):2$, a line where the atomic ratio [In]:[*M*]:[Zn] is $(1+\alpha):(1-\alpha):3$, a line where the atomic ratio [In]:[*M*]:[Zn] is $(1+\alpha):(1-\alpha):4$, and a line where the atomic ratio [In]:[*M*]:[Zn] is $(1+\alpha):(1-\alpha):5$.

[0127]

Dashed-dotted lines indicate a line where the atomic ratio [In]:[*M*]:[Zn] is $5:1:\beta$ where β is a real number greater than or equal to 0, a line where the atomic ratio [In]:[*M*]:[Zn] is $2:1:\beta$, a line representing the atomic ratio [In]:[*M*]:[Zn] is $1:1:\beta$, a line where the atomic ratio [In]:[*M*]:[Zn] is $1:2:\beta$, a line where the atomic ratio [In]:[*M*]:[Zn] is $1:3:\beta$, and a line where the atomic ratio [In]:[*M*]:[Zn] is $1:4:\beta$.

[0128]

An oxide semiconductor where the atomic ratio [In]:[*M*]:[Zn] is 0:2:1 or in the neighborhood thereof in FIGS. 13A to 13C tends to have a spinel crystal structure.

[0129]

A plurality of phases (e.g., two phases or three phases) exist in the oxide semiconductor in some cases. For example, with an atomic ratio [In]:[*M*]:[Zn] that is close to 0:2:1, two phases of a spinel crystal structure and a layered crystal structure are likely to exist. In addition, with an atomic ratio [In]:[*M*]:[Zn] that is close to 1:0:0, two phases of a bixbyite crystal structure and a layered crystal structure are likely to exist. In the case where a plurality of phases exist in the oxide semiconductor, a grain boundary might be formed between different crystal structures.

[0130]

A region A in FIG. 13A shows an example of the preferred ranges of the atomic ratio of indium to the element *M* and zinc contained in an oxide semiconductor.

[0131]

In addition, the oxide semiconductor containing indium in a higher proportion can have high carrier mobility (electron mobility). Thus, an oxide semiconductor having a high content of indium has higher carrier mobility than an oxide semiconductor having a low content of indium.

[0132]

In contrast, when the indium content and the zinc content in an oxide semiconductor become lower, carrier mobility becomes lower. Thus, with an atomic ratio [In]:[*M*]:[Zn] that is 0:1:0 and the neighborhood thereof (e.g., a region C in FIG. 13C), insulation performance becomes better.

[0133]

Accordingly, the oxide semiconductor of one embodiment of the present invention preferably has an atomic ratio represented by the region A in FIG. 13A. With the atomic ratio, high carrier mobility is obtained.

[0134]

An oxide semiconductor having an atomic ratio in the region A, particularly in a region B in FIG. 13B, has high carrier mobility and high reliability and is excellent.

[0135]

Note that the region B includes an atomic ratio [In]:[*M*]:[Zn] that is 4:2:3 to 4:2:4.1 and the vicinity thereof. The vicinity includes an atomic ratio [In]:[*M*]:[Zn] that is 5:3:4. Note that the region B includes an atomic ratio [In]:[*M*]:[Zn] that is 5:1:6 and the vicinity thereof and an atomic ratio [In]:[*M*]:[Zn] that is 5:1:7 and the vicinity thereof.

[0136]

Note that the property of an oxide semiconductor is not uniquely determined by an atomic ratio. Even with the same atomic ratio, the property of an oxide semiconductor might be different depending on a formation condition. For example, in the case where the oxide semiconductor is deposited with a sputtering apparatus, a film having an atomic ratio deviated from the atomic ratio of a target is formed. In particular, [Zn] in the film might be smaller than [Zn] in the target depending on the substrate temperature in deposition. Thus, the illustrated regions each represent an atomic ratio with which an oxide semiconductor tends to have specific characteristics, and boundaries of the regions A to C are not clear.

[0137]

In the case where the oxide semiconductor film 108 is formed of In-*M*-Zn oxide, it is preferable to use a target including polycrystalline In-*M*-Zn oxide as the sputtering target. Note that the atomic ratio of metal elements in the formed oxide semiconductor film 108 varies from the above atomic ratios of metal elements of the sputtering targets in a range of ±40 %. For example, when a sputtering target used for the oxide semiconductor film 108 has an atomic ratio In:Ga:Zn that is 4:2:4.1, the atomic ratio of the oxide semiconductor film 108 may be 4:2:3 or in the neighborhood thereof. When a sputtering target used for the oxide semiconductor film 108 has an atomic ratio In:Ga:Zn that is 5:1:7, the atomic ratio of the oxide semiconductor film 108 may be 5:1:6 or in the neighborhood thereof.

[0138]

The energy gap of the oxide semiconductor film 108 is 2 eV or more, preferably 2.5 eV or more. With the use of an oxide semiconductor having such a wide energy gap, the off-state current of the transistor 100 can be reduced.

[0139]

Furthermore, the oxide semiconductor film 108 may have a non-single-crystal structure. Examples of the non-single-crystal structure include a c-axis-aligned crystalline oxide semiconductor (CAAC-OS) which will be described later, a polycrystalline structure, a microcrystalline structure, and an amorphous structure. Among the non-single-crystal structures, an amorphous structure has the highest density of defect states.

[0140]

[Third insulating film]

The insulating film 116 contains nitrogen or hydrogen. A nitride insulating film can be used as the insulating film 116, for example. The nitride insulating film can be formed using silicon nitride, silicon nitride oxide, silicon oxynitride, or the like. The hydrogen concentration in the insulating film 116 is preferably higher than or equal to 1×10^{22} atoms/cm^3. The insulating film 116 is in contact with the region 108n of the oxide semiconductor film 108. Thus, the concentration of an impurity (nitrogen or hydrogen) in the region 108n in contact with the insulating film 116 is increased, leading to an increase in the carrier density of the region 108n.

[0141]

[Fourth insulating film]

As the insulating film 118, an oxide insulating film can be used. Alternatively, a layered film of an oxide insulating film and a nitride insulating film can be used as the insulating film 118. The insulating film 118 can be formed using, for example, silicon oxide, silicon oxynitride, silicon nitride oxide, aluminum oxide, hafnium oxide, gallium oxide, or Ga-Zn oxide.

[0142]

Furthermore, the insulating film 118 preferably functions as a barrier film against hydrogen, water, and the like from the outside.

[0143]

The thickness of the insulating film 118 can be greater than or equal to 30 nm and less than or equal to 500 nm, or greater than or equal to 100 nm and less than or equal to 400 nm.

[0144]

<Structure example 2 of transistor>

Next, a structure of a transistor different from that in FIGS. 3A to 3C will be described with reference to FIGS. 4A to 4C.

[0145]

FIG. 4A is a top view of the transistor 150. FIG. 4B is a cross-sectional view taken along dashed-dotted line X1–X2 in FIG. 4A. FIG. 4C is a cross-sectional view taken along dashed-dotted line Y1–Y2 in FIG. 4A.

[0146]

The transistor 150 illustrated in FIGS. 4A to 4C includes the conductive film 106 over the substrate 102; the insulating film 104 over the conductive film 106; the oxide semiconductor film 108 over the insulating film 104; the insulating film 110 over the oxide semiconductor film 108; the conductive film 112 over the insulating film 110; and the insulating film 116 over the insulating film 104, the oxide semiconductor film 108, and the conductive film 112.

[0147]

Note that the oxide semiconductor film 108 has a structure similar that in the transistor 100 shown in FIGS. 3A to 3C. The transistor 150 shown in FIGS. 4A to 4C includes the conductive film 106 and an opening 143 in addition to the components of the transistor 100 described above.

[0148]

The opening 143 is provided in the insulating films 104 and 110. The conductive film 106 is electrically connected to the conductive film 112 through the opening 143. Thus, the same potential is applied to the conductive film 106 and the conductive film 112. Note that different potentials may be applied to the conductive film 106 and the conductive film 112 without providing the opening 143. Alternatively, the conductive film 106 may be used as a light-blocking film without providing the opening 143. When the conductive film 106 is formed using a light-blocking material, for example, light from the bottom that irradiates a second region can be reduced.

[0149]

In the case of the structure of the transistor 150, the conductive film 106 functions as a first gate electrode (also referred to as a bottom-gate electrode), the conductive film 112 functions as a second gate electrode (also referred to as a top-gate electrode), the insulating film 104 functions as a first gate insulating film, and the insulating film 110 functions as a second gate insulating film.

[0150]

The conductive film 106 can be formed using a material similar to the above-described materials of the conductive films 112, 120a, and 120b. It is particularly suitable to use a material containing copper as the conductive film 106 because the resistance can be reduced. It is favorable that, for example, each of the conductive films 106, 120a, and 120b has a stacked-layer structure in which a copper film is over a titanium nitride film, a tantalum nitride film, or a tungsten film. In that case, by using the transistor 150 as a pixel transistor and/or a driving transistor of a display device, parasitic capacitance generated between the conductive films 106 and 120a and between the conductive films 106 and 120b can be reduced. Thus, the

conductive films 106, 120a, and 120b can be used not only as the first gate electrode, the source electrode, and the drain electrode of the transistor 150, but also as power supply wirings, signal supply wirings, connection wirings, or the like of the display device.

[0151]

In this manner, unlike the transistor 100 described above, the transistor 150 in FIGS. 4A to 4C has a structure in which a conductive film functioning as a gate electrode is provided over and under the oxide semiconductor film 108. As in the transistor 150, a semiconductor device of one embodiment of the present invention may have a plurality of gate electrodes.

[0152]

As illustrated in FIGS. 4B and 4C, the oxide semiconductor film 108 faces the conductive film 106 functioning as a first gate electrode and the conductive film 112 functioning as a second gate electrode and is positioned between the two conductive films functioning as the gate electrodes.

[0153]

Furthermore, the length of the conductive film 112 in the channel width direction is larger than the length of the oxide semiconductor film 108 in the channel width direction. In the channel width direction, the whole oxide semiconductor film 108 is covered with the conductive film 112 with the insulating film 110 placed therebetween. Since the conductive film 112 is connected to the conductive film 106 through the opening 143 provided in the insulating films 104 and 110, a side surface of the oxide semiconductor film 108 in the channel width direction faces the conductive film 112 with the insulating film 110 placed therebetween.

[0154]

In other words, the conductive film 106 and the conductive film 112 are connected through the opening 143 provided in the insulating films 104 and 110, and each include a region positioned outside an edge portion of the oxide semiconductor film 108.

[0155]

Such a structure enables the oxide semiconductor film 108 included in the transistor 150 to be electrically surrounded by electric fields of the conductive film 106 functioning as a first gate electrode and the conductive film 112 functioning as a second gate electrode. A device structure of a transistor, like that of the transistor 150, in which electric fields of the first gate electrode and the second gate electrode electrically surround the oxide semiconductor film 108 in which a channel region is formed can be referred to as a surrounded channel (S-channel) structure.

[0156]

Since the transistor 150 has the S-channel structure, an electric field for inducing a

channel can be effectively applied to the oxide semiconductor film 108 by the conductive film 106 or the conductive film 112; thus, the current drive capability of the transistor 150 can be improved and high on-state current characteristics can be obtained. As a result of the high on-state current, it is possible to reduce the size of the transistor 150. Furthermore, since the transistor 150 has a structure in which the oxide semiconductor film 108 is surrounded by the conductive film 106 and the conductive film 112, the mechanical strength of the transistor 150 can be increased.

[0157]

When seen in the channel width direction of the transistor 150, an opening different from the opening 143 may be formed on the side of the oxide semiconductor film 108 on which the opening 143 is not formed.

[0158]

When a transistor has a pair of gate electrodes between which a semiconductor film is positioned as in the transistor 150, one of the gate electrodes may be supplied with a signal A, and the other gate electrode may be supplied with a fixed potential V_b. Alternatively, one of the gate electrodes may be supplied with the signal A, and the other gate electrode may be supplied with a signal B. Alternatively, one of the gate electrodes may be supplied with a fixed potential V_a, and the other gate electrode may be supplied with the fixed potential V_b.

[0159]

The signal A is, for example, a signal for controlling the on/off state. The signal A may be a digital signal with two kinds of potentials, a potential V1 and a potential V2 (V1 > V2). For example, the potential V1 can be a high power supply potential, and the potential V2 can be a low power supply potential. The signal A may be an analog signal.

[0160]

The fixed potential V_b is, for example, a potential for controlling a threshold voltage V_{thA} of the transistor. The fixed potential V_b may be the potential V1 or the potential V2. In that case, a potential generator circuit for generating the fixed potential V_b is not necessary, which is preferable. The fixed potential V_b may be different from the potential V1 or the potential V2. When the fixed potential V_b is low, the threshold voltage V_{thA} can be high in some cases. As a result, the drain current flowing when the gate–source voltage V_{gs} is 0 V can be reduced, and leakage current in a circuit including the transistor can be reduced in some cases. The fixed potential V_b may be, for example, lower than the low power supply potential. Meanwhile, a high fixed potential V_b can lower the threshold voltage V_{thA} in some cases. As a result, the drain current flowing when the gate–source voltage V_{gs} is a high power supply potential and the operating speed of the circuit including the transistor can be increased in some

cases. The fixed potential V_b may be, for example, higher than the low power supply potential.

[0161]

The signal B is, for example, a signal for controlling the on/off state. The signal B may be a digital signal with two kinds of potentials, a potential V3 and a potential V4 (V3 > V4). For example, the potential V3 can be a high power supply potential, and the potential V4 can be a low power supply potential. The signal B may be an analog signal.

[0162]

When both the signal A and the signal B are digital signals, the signal B may have the same digital value as the signal A. In this case, it may be possible to increase the on-state current of the transistor and the operating speed of the circuit including the transistor. Here, the potential V1 and the potential V2 of the signal A may be different from the potential V3 and the potential V4 of the signal B. For example, if a gate insulating film for the gate to which the signal B is input is thicker than a gate insulating film for the gate to which the signal A is input, the potential amplitude of the signal B (V3 – V4) may be larger than the potential amplitude of the signal A (V1 – V2). In this manner, the influence of the signal A and that of the signal B on the on/off state of the transistor can be substantially the same in some cases.

[0163]

When both the signal A and the signal B are digital signals, the signal B may have a digital value different from that of the signal A. In this case, the signal A and the signal B can separately control the transistor, and thus, higher performance can be achieved. The transistor which is, for example, an n-channel transistor can function by itself as a NAND circuit, a NOR circuit, or the like in the following case: the transistor is turned on only when the signal A has the potential V1 and the signal B has the potential V3, or the transistor is turned off only when the signal A has the potential V2 and the signal B has the potential V4. The signal B may be a signal for controlling the threshold voltage V_{thA}. For example, the potential of the signal B in a period in which the circuit including the transistor operates may be different from the potential of the signal B in a period in which the circuit does not operate. The potential of the signal B may vary depending on the operation mode of the circuit. In this case, the potential of the signal B is not changed as frequently as the potential of the signal A in some cases.

[0164]

When both the signal A and the signal B are analog signals, the signal B may be an analog signal having the same potential as the signal A, an analog signal whose potential is a constant times the potential of the signal A, an analog signal whose potential is higher or lower than the potential of the signal A by a constant, or the like. In this case, it may be possible to increase the on-state current of the transistor and the operating speed of the circuit including the

transistor. The signal B may be an analog signal different from the signal A. In this case, the signal A and the signal B can separately control the transistor, and thus, higher performance can be achieved.

[0165]

The signal A may be a digital signal, and the signal B may be an analog signal. Alternatively, the signal A may be an analog signal, and the signal B may be a digital signal.

[0166]

When both of the gate electrodes of the transistor are supplied with the fixed potentials, the transistor can function as an element equivalent to a resistor in some cases. For example, in the case where the transistor is an n-channel transistor, the effective resistance of the transistor can be sometimes low (high) when the fixed potential V_a or the fixed potential V_b is high (low). When both the fixed potential V_a and the fixed potential V_b are high (low), the effective resistance can be lower (higher) than that of a transistor with only one gate in some cases.

[0167]

The other components of the transistor 150 are similar to those of the transistor 100 described above and have similar effects.

[0168]

An insulating film may further be formed over the transistor 150. The transistor 150 illustrated in FIGS. 4A to 4C includes an insulating film 122 over the conductive films 120a and 120b and the insulating film 118.

[0169]

The insulating film 122 has a function of covering unevenness and the like caused by the transistor or the like. The insulating film 122 has an insulating property and is formed using an inorganic material or an organic material. Examples of the inorganic material include a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, and an aluminum nitride film. Examples of the organic material include photosensitive resin materials such as an acrylic resin and a polyimide resin.

[0170]

<Structure example 3 of transistor>

Next, a structure of a transistor different from that of the transistor 150 in FIGS. 4A to 4C will be described with reference to FIGS. 5A and 5B.

[0171]

FIGS. 5A and 5B are cross-sectional views of a transistor 160. The top view of the transistor 160 is not illustrated because it is similar to that of the transistor 150 in FIG. 4A.

[0172]

The transistor 160 illustrated in FIGS. 5A and 5B is different from the transistor 150 in the stacked-layer structure of the conductive film 112, the shape of the conductive film 112, and the shape of the insulating film 110.

[0173]

The conductive film 112 in the transistor 160 includes a conductive film 112_1 over the insulating film 110 and a conductive film 112_2 over the conductive film 112_1. For example, an oxide conductive film is used as the conductive film 112_1, so that excess oxygen can be added to the insulating film 110. The oxide conductive film can be formed by a sputtering method in an atmosphere containing an oxygen gas. As the oxide conductive film, an oxide including indium and tin, an oxide including tungsten and indium, an oxide including tungsten, indium, and zinc, an oxide including titanium and indium, an oxide including titanium, indium, and tin, an oxide including indium and zinc, an oxide including silicon, indium, and tin, an oxide including indium, gallium, and zinc, or the like can be used, for example.

[0174]

As illustrated in FIG. 5B, the conductive film 112_2 is connected to the conductive film 106 through the opening 143. By forming the opening 143 after a conductive film to be the conductive film 112_1 is formed, the shape illustrated in FIG. 5B can be obtained. In the case where an oxide conductive film is used as the conductive film 112_1, the structure in which the conductive film 112_2 is connected to the conductive film 106 can decrease the contact resistance between the conductive film 112 and the conductive film 106.

[0175]

The conductive film 112 and the insulating film 110 in the transistor 160 have a tapered shape. More specifically, the lower edge portion of the conductive film 112 is positioned outside the upper edge portion of the conductive film 112. The lower edge portion of the insulating film 110 is positioned outside the upper edge portion of the insulating film 110. In addition, the lower edge portion of the conductive film 112 is formed in substantially the same position as that of the upper edge portion of the insulating film 110.

[0176]

As compared with the transistor 160 in which the conductive film 112 and the insulating film 110 have a rectangular shape, the transistor 160 in which the conductive film 112 and the insulating film 110 have a tapered shape is favorable because of better coverage with the insulating film 116.

[0177]

The other components of the transistor 160 are similar to those of the transistor 150 described above and have similar effects.

[0178]

<Method for manufacturing semiconductor device>

Next, a method for manufacturing the transistor 150 illustrated in FIGS. 4A to 4C will be described with reference to FIGS. 6A to 6D, FIGS. 7A to 7C, and FIGS. 8A to 8C. Note that FIGS. 6A to 6D, FIGS. 7A to 7C, and FIGS. 8A to 8C are cross-sectional views in the channel length direction and the channel width direction illustrating the method for manufacturing the transistor 150.

[0179]

First, the conductive film 106 is formed over the substrate 102. Next, the insulating film 104 is formed over the substrate 102 and the conductive film 106, and an oxide semiconductor film is formed over the insulating film 104. Then, the oxide semiconductor film is processed into an island shape, whereby an oxide semiconductor film 108a is formed (see FIG. 6A).

[0180]

The conductive film 106 can be formed using a material selected from the above-mentioned materials. In this embodiment, for the conductive film 106, a stack including a 50-nm-thick tungsten film and a 400-nm-thick copper film is formed with a sputtering apparatus.

[0181]

To process a conductive film to be the conductive film 106, a wet etching method and/or a dry etching method can be used. In this embodiment, in the processing of the conductive film into the conductive film 106, the copper film is etched by a wet etching method, and then the tungsten film is etched by a dry etching method.

[0182]

The insulating film 104 can be formed by a sputtering method, a CVD method, an evaporation method, a pulsed laser deposition (PLD) method, a printing method, a coating method, or the like as appropriate. In this embodiment, as the insulating film 104, a 400-nm-thick silicon nitride film and a 50-nm-thick silicon oxynitride film are formed with a PECVD apparatus.

[0183]

After the insulating film 104 is formed, oxygen may be added to the insulating film 104. As oxygen added to the insulating film 104, an oxygen radical, an oxygen atom, an oxygen atomic ion, an oxygen molecular ion, or the like may be used. Oxygen can be added by an ion doping method, an ion implantation method, a plasma treatment method, or the like. Alternatively, a film that suppresses oxygen release may be formed over the insulating film 104,

and then oxygen may be added to the insulating film 104 through the film.

[0184]

The film that suppresses oxygen release can be formed using a conductive film or a semiconductor film containing one or more of indium, zinc, gallium, tin, aluminum, chromium, tantalum, titanium, molybdenum, nickel, iron, cobalt, and tungsten.

[0185]

In the case where oxygen is added by plasma treatment in which oxygen is excited by a microwave to generate high-density oxygen plasma, the amount of oxygen added to the insulating film 104 can be increased.

[0186]

In forming the oxide semiconductor film 108a, an inert gas (such as a helium gas, an argon gas, or a xenon gas) may be mixed into the oxygen gas. Note that the proportion of the oxygen gas in the whole deposition gas (hereinafter also referred to as an oxygen flow rate ratio) in forming the oxide semiconductor film 108a is higher than or equal to 5 % and lower than or equal to 30 %, preferably higher than or equal to 7 % and lower than or equal to 20 %.

[0187]

The oxide semiconductor film 108a is formed at a substrate temperature higher than or equal to room temperature and lower than or equal to 180 °C, preferably higher than or equal to room temperature and lower than or equal to 140 °C. The substrate temperature when the oxide semiconductor film 108a is formed is preferably, for example, higher than or equal to room temperature and lower than 140 °C because the productivity is increased.

[0188]

The thickness of the oxide semiconductor film 108a is greater than or equal to 3 nm and less than or equal to 200 nm, preferably greater than or equal to 3 nm and less than or equal to 100 nm, further preferably greater than or equal to 3 nm and less than or equal to 60 nm.

[0189]

In the case where a large-sized glass substrate (e.g., the 6th generation to the 10th generation) is used as the substrate 102 and the oxide semiconductor film 108a is formed at a substrate temperature higher than or equal to 200 °C and lower than or equal to 300 °C, the substrate 102 might be changed in shape (distorted or warped). Therefore, in the case where a large-sized glass substrate is used, the change in the shape of the glass substrate can be suppressed by forming the oxide semiconductor film 108a at a substrate temperature higher than or equal to room temperature and lower than 200 °C.

[0190]

In addition, increasing the purity of the sputtering gas is necessary. For example, when

a gas which is highly purified to have a dew point of −40 °C or lower, preferably −80 °C or lower, further preferably −100 °C or lower, still further preferably −120 °C or lower, is used as the sputtering gas, i.e., the oxygen gas or the argon gas, entry of moisture or the like into the oxide semiconductor film can be minimized.

[0191]

In the case where the oxide semiconductor film is deposited by a sputtering method, a chamber in a sputtering apparatus is preferably evacuated to be a high vacuum state (to the degree of about 5×10^{-7} Pa to 1×10^{-4} Pa) with an adsorption vacuum evacuation pump such as a cryopump in order to remove water or the like, which serves as an impurity for the oxide semiconductor film, as much as possible. In particular, the partial pressure of gas molecules corresponding to H_2O (gas molecules corresponding to $m/z = 18$) in the chamber in the standby mode of the sputtering apparatus is preferably lower than or equal to 1×10^{-4} Pa, further preferably lower than or equal to 5×10^{-5} Pa.

[0192]

In this embodiment, the oxide semiconductor film 108a is formed in the following conditions.

[0193]

The oxide semiconductor film 108a is formed by a sputtering method using an In-Ga-Zn metal oxide target. The substrate temperature and the oxygen flow rate at the time of formation of the oxide semiconductor film 108a can be set as appropriate. An oxide material is formed under the following conditions: the pressure in a chamber is 0.6 Pa; and an AC power of 2500 W is supplied to the metal oxide target provided in the sputtering apparatus.

[0194]

To process the formed oxide material into the oxide semiconductor film 108a, a wet etching method and/or a dry etching method can be used.

[0195]

After the oxide semiconductor film 108a is formed, the oxide semiconductor film 108a may be dehydrated or dehydrogenated by heat treatment. The temperature of the heat treatment is typically higher than or equal to 150 °C and lower than the strain point of the substrate, higher than or equal to 250 °C and lower than or equal to 450 °C, or higher than or equal to 300 °C and lower than or equal to 450 °C.

[0196]

The heat treatment can be performed in an inert gas atmosphere containing nitrogen or a rare gas such as helium, neon, argon, xenon, or krypton. Alternatively, the heat treatment may

be performed in an inert gas atmosphere first, and then in an oxygen atmosphere. It is preferable that the above inert gas atmosphere and the above oxygen atmosphere not contain hydrogen, water, or the like. The treatment time may be longer than or equal to 3 minutes and shorter than or equal to 24 hours.

[0197]

An electric furnace, an RTA apparatus, or the like can be used for the heat treatment. With the use of an RTA apparatus, the heat treatment can be performed at a temperature higher than or equal to the strain point of the substrate if the heating time is short. Therefore, the heat treatment time can be shortened.

[0198]

By depositing the oxide semiconductor film while it is heated or by performing heat treatment after the deposition of the oxide semiconductor film, the hydrogen concentration in the oxide semiconductor film, which is measured by SIMS, can be 5×10^{19} atoms/cm^3 or lower, 1×10^{19} atoms/cm^3 or lower, 5×10^{18} atoms/cm^3 or lower, 1×10^{18} atoms/cm^3 or lower, 5×10^{17} atoms/cm^3 or lower, or 1×10^{16} atoms/cm^3 or lower.

[0199]

Next, an insulating film 110_0 is formed over the insulating film 104 and the oxide semiconductor film 108a (see FIG. 6B).

[0200]

For the insulating film 110_0, a silicon oxide film or a silicon oxynitride film can be formed with a plasma-enhanced chemical vapor deposition apparatus (also referred to as a PECVD apparatus or simply a plasma CVD apparatus). In this case, a deposition gas containing silicon and an oxidizing gas are preferably used as a source gas. Typical examples of the deposition gas containing silicon include silane, disilane, trisilane, and silane fluoride. Examples of the oxidizing gas include oxygen, ozone, dinitrogen monoxide, and nitrogen dioxide.

[0201]

A silicon oxynitride film having few defects can be formed as the insulating film 110_0 with the PECVD apparatus under the conditions that the flow rate of the oxidizing gas is more than 20 times and less than 100 times, or more than or equal to 40 times and less than or equal to 80 times the flow rate of the deposition gas and that the pressure in a treatment chamber is lower than 100 Pa or lower than or equal to 50 Pa.

[0202]

As the insulating film 110_0, a dense silicon oxide film or a dense silicon oxynitride film can be formed under the following conditions: the substrate placed in a vacuum-evacuated

treatment chamber of the PECVD apparatus is held at a temperature higher than or equal to 280 °C and lower than or equal to 400 °C; the pressure in the treatment chamber into which a source gas is introduced is set to be higher than or equal to 20 Pa and lower than or equal to 250 Pa, preferably higher than or equal to 100 Pa and lower than or equal to 250 Pa; and a high-frequency power is supplied to an electrode provided in the treatment chamber.

[0203]

The insulating film 110_0 may be formed by a PECVD method using a microwave. A microwave refers to a wave in the frequency range of 300 MHz to 300 GHz. In the case of using a microwave, electron temperature and electron energy are low. Furthermore, in supplied power, the proportion of power used for acceleration of electrons is low, and therefore, much more power can be used for dissociation and ionization of molecules. Thus, plasma with a high density (high-density plasma) can be excited. This method causes little plasma damage to the deposition surface or a deposit, so that the insulating film 110_0 having few defects can be formed.

[0204]

Alternatively, the insulating film 110_0 can also be formed by a CVD method using an organosilane gas. As the organosilane gas, any of the following silicon-containing compound can be used: tetraethyl orthosilicate (TEOS) (chemical formula: $Si(OC_2H_5)_4$); tetramethylsilane (TMS) (chemical formula: $Si(CH_3)_4$); tetramethylcyclotetrasiloxane (TMCTS); octamethylcyclotetrasiloxane (OMCTS); hexamethyldisilazane (HMDS); triethoxysilane ($SiH(OC_2H_5)_3$); trisdimethylaminosilane ($SiH(N(CH_3)_2)_3$); or the like. The insulating film 110_0 having high coverage can be formed by a CVD method using an organosilane gas.

[0205]

In this embodiment, as the insulating film 110_0, a 100-nm-thick silicon oxynitride film is formed with the PECVD apparatus.

[0206]

Subsequently, a mask is formed by lithography in a desired position over the insulating film 110_0, and then the insulating film 110_0 and the insulating film 104 are partly etched, so that the opening 143 reaching the conductive film 106 is formed (see FIG. 6C).

[0207]

To form the opening 143, a wet etching method and/or a dry etching method can be used. In this embodiment, the opening 143 is formed by a dry etching method.

[0208]

Next, a conductive film 112_0 is formed over the conductive film 106 and the insulating

film 110_0 so as to cover the opening 143. In the case where a metal oxide film is used as the conductive film 112_0, for example, oxygen might be added to the insulating film 110_0 during the formation of the conductive film 112_0 (see FIG. 6D).

[0209]

In FIG. 6D, oxygen added to the insulating film 110_0 is schematically shown by arrows. Furthermore, the conductive film 112_0 formed to cover the opening 143 is electrically connected to the conductive film 106.

[0210]

In the case where a metal oxide film is used as the conductive film 112_0, the conductive film 112_0 is preferably formed by a sputtering method in an atmosphere containing an oxygen gas. Formation of the conductive film 112_0 in an atmosphere containing an oxygen gas allows suitable addition of oxygen to the insulating film 110_0. Note that a method for forming the conductive film 112_0 is not limited to a sputtering method, and another method such as an ALD method may be used.

[0211]

In this embodiment, a 100-nm-thick IGZO film containing an In-Ga-Zn oxide (In:Ga:Zn = 4:2:4.1 (atomic ratio)) is formed as the conductive film 112_0 by a sputtering method. Oxygen addition treatment may be performed on the insulating film 110_0 before or after the formation of the conductive film 112_0. The oxygen addition treatment can be performed in a manner similar to that of the oxygen addition treatment that can be performed after the formation of the insulating film 104.

[0212]

Subsequently, a mask 140 is formed by a lithography process in a desired position over the conductive film 112_0 (see FIG. 7A).

[0213]

Next, etching is performed from above the mask 140 to process the conductive film 112_0 and the insulating film 110_0. After the processing of the conductive film 112_0 and the insulating film 110_0, the mask 140 is removed. As a result of the processing of the conductive film 112_0 and the insulating film 110_0, the island-shaped conductive film 112 and the island-shaped insulating film 110 are formed (see FIG. 7B).

[0214]

In this embodiment, the conductive film 112_0 and the insulating film 110_0 are processed by a dry etching method.

[0215]

In the processing of the conductive film 112_0 and the insulating film 110_0, the thickness of the oxide semiconductor film 108a in a region not overlapping with the conductive film 112 is decreased in some cases. In other cases, in the processing of the conductive film 112_0 and the insulating film 110_0, the thickness of the insulating film 104 in a region not overlapping with the oxide semiconductor film 108a is decreased. In the processing of the conductive film 112_0 and the insulating film 110_0, an etchant or an etching gas (e.g., chlorine) might be added to the oxide semiconductor film 108a or the constituent element of the conductive film 112_0 or the insulating film 110_0 might be added to the oxide semiconductor film 108.

[0216]

Next, the insulating film 116 is formed over the insulating film 104, the oxide semiconductor film 108, and the conductive film 112. By the formation of the insulating film 116, part of the oxide semiconductor film 108a that is in contact with the insulating film 116 becomes the regions 108n. Here, the oxide semiconductor film 108a overlapping with the conductive film 112 is the oxide semiconductor film 108 (see FIG. 7C).

[0217]

The insulating film 116 can be formed using a material selected from the above-mentioned materials. In this embodiment, as the insulating film 116, a 100-nm-thick silicon nitride oxide film is formed with a PECVD apparatus. In the formation of the silicon nitride oxide film, two steps, i.e., plasma treatment and deposition treatment, are performed at a temperature of 220 °C. The plasma treatment is performed under the following conditions: an argon gas at a flow rate of 100 sccm and a nitrogen gas at a flow rate of 1000 sccm are introduced into a chamber before deposition; the pressure in the chamber is set to 40 Pa; and a power of 1000 W is supplied to an RF power source (27.12 MHz). The deposition treatment is performed under the following conditions: a silane gas at a flow rate of 50 sccm, a nitrogen gas at a flow rate of 5000 sccm, and an ammonia gas at a flow rate of 100 sccm are introduced into the chamber; the pressure in the chamber is set to 100 Pa; and a power of 1000 W is supplied to the RF power source (27.12 MHz).

[0218]

When a silicon nitride oxide film is used as the insulating film 116, nitrogen or hydrogen in the silicon nitride oxide film can be supplied to the regions 108n in contact with the insulating film 116. In addition, when the formation temperature of the insulating film 116 is the above temperature, release of excess oxygen contained in the insulating film 110 to the outside can be suppressed.

[0219]

Next, the insulating film 118 is formed over the insulating film 116 (see FIG. 8A).

[0220]

The insulating film 118 can be formed using a material selected from the above-mentioned materials. In this embodiment, as the insulating film 118, a 300-nm-thick silicon oxynitride film is formed with a PECVD apparatus.

[0221]

Subsequently, a mask is formed by lithography in a desired position over the insulating film 118, and then the insulating film 118 and the insulating film 116 are partly etched, so that the opening 141a and the opening 141b reaching the regions 108n are formed (see FIG. 8B).

[0222]

To etch the insulating film 118 and the insulating film 116, a wet etching method and/or a dry etching method can be used. In this embodiment, the insulating film 118 and the insulating film 116 are processed by a dry etching method.

[0223]

Next, a conductive film is formed over the regions 108n and the insulating film 118 so as to cover the openings 141a and 141b, and the conductive film is processed into a desired shape, whereby the conductive films 120a and 120b are formed (see FIG. 8C).

[0224]

The conductive films 120a and 120b can be formed using a material selected from the above-mentioned materials. In this embodiment, for the conductive films 120a and 120b, a stack including a 50-nm-thick tungsten film and a 400-nm-thick copper film is formed with a sputtering apparatus.

[0225]

To process the conductive film to be the conductive films 120a and 120b, a wet etching method and/or a dry etching method can be used. In this embodiment, in the processing of the conductive film into the conductive films 120a and 120b, the copper film is etched by a wet etching method, and then the tungsten film is etched by a dry etching method.

[0226]

Then, the insulating film 122 is formed to cover the conductive films 120a and 120b and the insulating film 118.

[0227]

Through the above steps, the transistor 150 in FIGS. 4A to 4C can be manufactured.

[0228]

Note that the films included in the transistor 150 (the insulating film, the metal oxide film, the oxide semiconductor film, the conductive film, and the like) can be formed by, other

than the above methods, a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, a pulsed laser deposition (PLD) method, or an ALD method. Alternatively, a coating method or a printing method can be used. Although a sputtering method and a PECVD method are typical examples of the deposition method, a thermal CVD method may be used. As an example of a thermal CVD method, a metal organic chemical vapor deposition (MOCVD) method can be given.

[0229]

Deposition by the thermal CVD method may be performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, and a source gas and an oxidizer are supplied to the chamber at a time and react with each other in the vicinity of the substrate or over the substrate. Thus, no plasma is generated in the deposition; therefore, the thermal CVD method has an advantage that no defect due to plasma damage is caused.

[0230]

The films such as the conductive films, the insulating films, the oxide semiconductor films, and the metal oxide films that are described above can be formed by a thermal CVD method such as an MOCVD method.

[0231]

For example, in the case where a hafnium oxide film is formed with a deposition apparatus employing an ALD method, two kinds of gases are used, namely, ozone (O_3) as an oxidizer and a source gas that is obtained by vaporizing liquid containing a solvent and a hafnium precursor (hafnium alkoxide or hafnium amide such as tetrakis(dimethylamide)hafnium (TDMAH, $Hf[N(CH_3)_2]_4$) or tetrakis(ethylmethylamide)hafnium).

[0232]

In the case where an aluminum oxide film is formed with a deposition apparatus employing an ALD method, two kinds of gases are used, namely, H_2O as an oxidizer and a source gas that is obtained by vaporizing liquid containing a solvent and an aluminum precursor (e.g., trimethylaluminum (TMA, $Al(CH_3)_3$)). Examples of another material include tris(dimethylamide)aluminum, triisobutylaluminum, and aluminum tris(2,2,6,6-tetramethyl-3,5-heptanedionate).

[0233]

In the case where a silicon oxide film is formed with a deposition apparatus employing an ALD method, hexachlorodisilane is adsorbed on a surface on which a film is to be formed, and radicals of an oxidizing gas (O_2 or dinitrogen monoxide) are supplied to react with the adsorbate.

[0234]

In the case where a tungsten film is formed with a deposition apparatus employing an ALD method, a WF_6 gas and a B_2H_6 gas are sequentially introduced to form an initial tungsten film, and then, a WF_6 gas and an H_2 gas are used to form a tungsten film. Note that an SiH_4 gas may be used instead of a B_2H_6 gas.

[0235]

In the case where an oxide semiconductor film such as an In-Ga-Zn-O film is formed with a deposition apparatus employing an ALD method, an $In(CH_3)_3$ gas and an O_3 gas are used to form an In-O layer, a $Ga(CH_3)_3$ gas and an O_3 gas are used to form a Ga-O layer, and then, a $Zn(CH_3)_2$ gas and an O_3 gas are used to form a Zn-O layer. Note that the order of these layers is not limited to this example. A mixed compound layer such as an In-Ga-O layer, an In-Zn-O layer, or a Ga-Zn-O layer may be formed by using these gases. Note that although an H_2O gas that is obtained by bubbling water with an inert gas such as Ar may be used instead of an O_3 gas, it is preferable to use an O_3 gas, which does not contain H.

[0236]

<Structure example 4 of transistor>

FIG. 9A is a top view of a transistor 300A. FIG. 9B is a cross-sectional view taken along dashed-dotted line X1–X2 in FIG. 9A. FIG. 9C is a cross-sectional view taken along dashed-dotted line Y1–Y2 in FIG. 9A. Note that in FIG. 9A, some components of the transistor 300A (e.g., an insulating film functioning as a gate insulating film) are not illustrated to avoid complexity. The direction of the dashed-dotted line X1–X2 may be referred to as a channel length direction, and the direction of the dashed-dotted line Y1–Y2 may be referred to as a channel width direction. As in FIG. 9A, some components are not illustrated in some cases in top views of transistors described below.

[0237]

The transistor 300A illustrated in FIGS. 9A to 9C includes a conductive film 304 over a substrate 302, an insulating film 306 over the substrate 302 and the conductive film 304, an insulating film 307 over the insulating film 306, an oxide semiconductor film 308 over the insulating film 307, a conductive film 312a over the oxide semiconductor film 308, and a conductive film 312b over the oxide semiconductor film 308. Over the transistor 300A, specifically, over the conductive films 312a and 312b and the oxide semiconductor film 308, an insulating film 314, an insulating film 316, and an insulating film 318 are provided.

[0238]

In the transistor 300A, the insulating films 306 and 307 function as the gate insulating films of the transistor 300A, and the insulating films 314, 316, and 318 function as protective insulating films of the transistor 300A. Furthermore, in the transistor 300A, the conductive film

304 functions as a gate electrode, the conductive film 312a functions as a source electrode, and the conductive film 312b functions as a drain electrode.

[0239]

In this specification and the like, the insulating films 306 and 307 may be referred to as a first insulating film, the insulating films 314 and 316 may be referred to as a second insulating film, and the insulating film 318 may be referred to as a third insulating film.

[0240]

The transistor 300A illustrated in FIGS. 9A to 9C is a channel-etched transistor. The oxide semiconductor film of one embodiment of the present invention is suitable for a channel-etched transistor.

[0241]

<Structure example 5 of transistor>

FIG. 10A is a top view of a transistor 300B. FIG. 10B is a cross-sectional view taken along dashed-dotted line X1–X2 in FIG. 10A. FIG. 10C is a cross-sectional view taken along dashed-dotted line Y1–Y2 in FIG. 10A.

[0242]

The transistor 300B illustrated in FIGS. 10A to 10C includes the conductive film 304 over the substrate 302, the insulating film 306 over the substrate 302 and the conductive film 304, the insulating film 307 over the insulating film 306, the oxide semiconductor film 308 over the insulating film 307, the insulating film 314 over the oxide semiconductor film 308, the insulating film 316 over the insulating film 314, the conductive film 312a electrically connected to the oxide semiconductor film 308 through an opening 341a provided in the insulating films 314 and 316, and the conductive film 312b electrically connected to the oxide semiconductor film 308 through an opening 341b provided in the insulating films 314 and 316. Over the transistor 300B, specifically, over the conductive films 312a and 312b and the insulating film 316, the insulating film 318 is provided.

[0243]

In the transistor 300B, the insulating films 306 and 307 each function as a gate insulating film of the transistor 300B, the insulating films 314 and 316 each function as a protective insulating film of the oxide semiconductor film 308, and the insulating film 318 functions as a protective insulating film of the transistor 300B. Moreover, in the transistor 300B, the conductive film 304 functions as a gate electrode, the conductive film 312a functions as a source electrode, and the conductive film 312b functions as a drain electrode.

[0244]

The transistor 300A illustrated in FIGS. 9A to 9C has a channel-etched structure,

whereas the transistor 300B in FIGS. 10A to 10C has a channel-protective structure. The oxide semiconductor film of one embodiment of the present invention is suitable for a channel-protective transistor as well.

[0245]

<Structure example 6 of transistor>

FIG. 11A is a top view of a transistor 300C. FIG. 11B is a cross-sectional view taken along dashed-dotted line X1–X2 in FIG. 11A. FIG. 11C is a cross-sectional view taken along dashed-dotted line Y1–Y2 in FIG. 11A.

[0246]

The transistor 300C illustrated in FIGS. 11A to 11C is different from the transistor 300B in FIGS. 10A to 10C in the shapes of the insulating films 314 and 316. Specifically, the insulating films 314 and 316 of the transistor 300C have island shapes and are provided over a channel region of the oxide semiconductor film 308. Other components are similar to those of the transistor 300B.

[0247]

<Structure example 7 of transistor>

FIG. 12A is a top view of a transistor 300D. FIG. 12B is a cross-sectional view taken along dashed-dotted line X1–X2 in FIG. 12A. FIG. 12C is a cross-sectional view taken along dashed-dotted line Y1–Y2 in FIG. 12A.

[0248]

The transistor 300D illustrated in FIGS. 12A to 12C includes the conductive film 304 over the substrate 302, the insulating film 306 over the substrate 302 and the conductive film 304, the insulating film 307 over the insulating film 306, the oxide semiconductor film 308 over the insulating film 307, the conductive film 312a over the oxide semiconductor film 308, the conductive film 312b over the oxide semiconductor film 308, the insulating film 314 over the oxide semiconductor film 308 and the conductive films 312a and 312b, the insulating film 316 over the insulating film 314, the insulating film 318 over the insulating film 316, and conductive films 320a and 320b over the insulating film 318.

[0249]

In the transistor 300D, the insulating films 306 and 307 function as first gate insulating films of the transistor 300D, and the insulating films 314, 316, and 318 function as second gate insulating films of the transistor 300D. Furthermore, in the transistor 300D, the conductive film 304 functions as a first gate electrode, the conductive film 320a functions as a second gate electrode, and the conductive film 320b functions as a pixel electrode used for a display device. The conductive film 312a functions as a source electrode, and the conductive film 312b

functions as a drain electrode.

[0250]

As illustrated in FIG. 12C, the conductive film 320b is connected to the conductive film 304 in an opening 342b and an opening 342c provided in the insulating films 306, 307, 314, 316, and 318. Thus, the same potential is applied to the conductive film 320b and the conductive film 304.

[0251]

The structure of the transistor 300D is not limited to that described above, in which the openings 342b and 342c are provided so that the conductive film 320b is connected to the conductive film 304. For example, a structure in which only one of the openings 342b and 342c is provided so that the conductive film 320b is connected to the conductive film 304, or a structure in which the conductive film 320b is not connected to the conductive film 304 without providing the openings 342b and 342c may be employed. Note that in the case where the conductive film 320b is not connected to the conductive film 304, it is possible to apply different potentials to the conductive film 320b and the conductive film 304.

[0252]

The conductive film 320b is connected to the conductive film 312b through an opening 342a provided in the insulating films 314, 316, and 318.

[0253]

Note that the transistor 300D has the S-channel structure described above.

[0254]

At least part of this embodiment can be implemented in combination with any of the other embodiments described in this specification as appropriate.

[Example 1]

[0255]

In this example, measurement results of an oxide semiconductor of one embodiment of the present invention over a substrate are described. A variety of methods were used for the measurement. Note that in this example, Samples 1A, 1B, 1C, 1D, 1E, 1F, 1G, 1H, and 1J were fabricated.

[0256]

<<Structure of samples and fabrication method thereof>>

Samples 1A to 1H and 1J relating to one embodiment of the present invention are described below. Samples 1A to 1H and 1J each include a substrate and an oxide semiconductor over the substrate.

[0257]

Samples 1A to 1H and 1J were fabricated at different temperatures and different oxygen flow rate ratios in formation of the oxide semiconductor. The temperatures and the oxygen flow rate ratios in formation of the oxide semiconductors of Samples 1A to 1H and 1J are shown in Table 1 below.

[0258]

[Table 1]

	Flow rate [sccm]		Percentage of O_2 [%]	Deposition temperature [°C]
	O_2	Ar		
Sample 1A	30	270	10	R.T.
Sample 1B	90	210	30	R.T.
Sample 1C	300	0	100	R.T.
Sample 1D	30	270	10	130
Sample 1E	90	210	30	130
Sample 1F	300	0	100	130
Sample 1G	30	270	10	170
Sample 1H	90	210	30	170
Sample 1J	300	0	100	170

[0259]

Next, methods for fabricating the samples will be described.

[0260]

A glass substrate was used as the substrate. Over the substrate, a 100-nm-thick In-Ga-Zn oxide was formed as an oxide semiconductor with a sputtering apparatus. The formation conditions were as follows: the pressure in a chamber was 0.6 Pa; and a metal oxide target (where an atomic ratio In:Ga:Zn is 4:2:4.1) was used as a target. The metal oxide target provided in the sputtering apparatus was supplied with an AC power of 2500 W to form the oxide semiconductor.

[0261]

The formation temperatures and oxygen flow rate ratios shown in the above table were used as the conditions for forming oxide semiconductors to fabricate Samples 1A to 1H and 1J.

[0262]

Through the above steps, Samples 1A to 1H and 1J of this example were fabricated.

[0263]

<Analysis by X-ray diffraction>

In this section, results of X-ray diffraction (XRD) measurement performed on the oxide semiconductors over the glass substrates are described. As an XRD apparatus, D8 ADVANCE manufactured by Bruker AXS was used. The conditions were as follows: scanning was performed by an out-of-plane method at $\theta/2\theta$, the scanning range was 15 deg. to 50 deg.; the step width was 0.02 deg.; and the scanning speed was 3.0 deg./min.

[0264]

FIG. 14 shows an XRD spectrum of the samples measured by an out-of-plane method.

[0265]

In the XRD spectra shown in FIG. 14, the higher the substrate temperature at the time of formation is or the higher the oxygen gas flow rate ratio at the time of formation is, the higher the intensity of the peak at around $2\theta = 31°$ is. Note that it is found that the peak at around $2\theta = 31°$ is derived from a crystalline IGZO compound whose c-axes are aligned in a direction substantially perpendicular to a formation surface or a top surface of the crystalline IGZO compound (such a compound is also referred to as CAAC-IGZO).

[0266]

As shown in the XRD spectra in FIG. 14, as the substrate temperature at the time of formation is lower or the oxygen gas flow rate ratio at the time of formation is lower, a peak becomes less clear. Accordingly, it is found that there are no alignment in the a-b plane direction and c-axis alignment in the measured areas of the samples that are formed at a lower substrate temperature or with a lower oxygen gas flow rate ratio.

[0267]

<TEM images and electron diffraction>

This section describes the observation and analysis results of Samples 1A, 1D, and 1J with a high-angle annular dark-field scanning transmission electron microscope (HAADF-STEM). An image obtained with an HAADF-STEM is also referred to as a TEM image.

[0268]

This section describes electron diffraction patterns obtained by irradiation of Samples 1A, 1D, and 1J with an electron beam with a probe diameter of 1 nm (also referred to as a nanobeam).

[0269]

The plan-view TEM images were observed with a spherical aberration corrector function. The HAADF-STEM images were obtained using an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd. under the following conditions: the acceleration voltage was 200 kV; and irradiation with an electron beam with a

diameter of approximately 0.1 nmφ was performed.

[0270]

Note that the electron diffraction patterns were observed while an electron beam irradiation was performed at a constant rate for 35 seconds.

[0271]

FIG. 15A shows a cross-sectional TEM image of Sample 1A, and FIG. 15B shows an electron diffraction pattern of Sample 1A. FIG. 15C shows a cross-sectional TEM image of Sample 1D, and FIG. 15D shows an electron diffraction pattern of Sample 1D. FIG. 15E shows a cross-sectional TEM image of Sample 1J, and FIG. 15F shows an electron diffraction pattern of Sample 1J.

[0272]

It is known that, for example, when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an $InGaZnO_4$ crystal in a direction parallel to the sample surface, a diffraction pattern including a spot derived from the (009) plane of the $InGaZnO_4$ crystal is obtained. That is, the CAAC-OS has c-axis alignment and the c-axes are aligned in the direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS. Meanwhile, a ring-like diffraction pattern is shown when an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. That is, it is found that the CAAC-OS has neither a-axis alignment nor b-axis alignment.

[0273]

Furthermore, a diffraction pattern like a halo pattern is observed when an oxide semiconductor including a nanocrystal (a nanocrystalline oxide semiconductor (hereinafter referred to as nc-OS)) is subjected to electron diffraction using an electron beam with a large probe diameter (e.g., 50 nm or larger). Meanwhile, bright spots are shown in a nanobeam electron diffraction pattern of the nc-OS obtained using an electron beam with a small probe diameter (e.g., smaller than 50 nm). Furthermore, in a nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS, a plurality of bright spots are shown in a ring-like shape in some cases.

[0274]

As shown in FIG. 15A, a nanocrystal (hereinafter, also referred to as nc) is observed in Sample 1A by cross-sectional TEM. In addition, as shown in FIG. 15B, the observed electron diffraction pattern of Sample 1A has a region with high luminance in a circular (ring) pattern. Furthermore, a plurality of spots can be shown in the ring-shaped region.

[0275]

As shown in FIG. 15C, a CAAC structure and a nanocrystal are observed in Sample 1D by cross-sectional TEM. In addition, as shown in FIG. 15D, the observed electron diffraction pattern of Sample 1D has a region with high luminance in a circular (ring) pattern. Furthermore, a plurality of spots can be shown in the ring-shaped region. In the diffraction pattern, spots derived from the (009) plane are slightly observed.

[0276]

In contrast, as shown in FIG. 15E, layered arrangement of a CAAC structure is observed in Sample 1J by cross-sectional TEM.

[0277]

The features observed in the cross-sectional TEM images and the plan-view TEM images are one aspect of a structure of an oxide semiconductor.

[0278]

Next, electron diffraction patterns obtained by irradiation of Sample 1A with an electron beam with a probe diameter of 1 nm (also referred to as a nanobeam) are shown in FIGS. 16A to 16L.

[0279]

Electron diffraction patterns of points indicated by black dots a1, a2, a3, a4, and a5 in the plan-view TEM image of Sample 1A in FIG. 16A are observed. Note that the electron diffraction patterns are observed while electron beam irradiation is performed at a constant rate for 35 seconds. FIGS. 16C, 16D, 16E, 16F, and 16G show the results of the points indicated by the black dots a1, a2, a3, a4, and a5, respectively.

[0280]

In FIGS. 16C to 16G, regions with high luminance in a ring pattern were shown. Furthermore, a plurality of spots are shown in the ring-shaped regions.

[0281]

Electron diffraction patterns of points indicated by black dots b1, b2, b3, b4, and b5 in the cross-sectional TEM image of Sample 1A in FIG. 16B are observed. FIGS. 16H, 16I, 16J, 16K, and 16L show the results of the points indicated by the black dots b1, b2, b3, b4, and b5, respectively.

[0282]

In FIGS. 16H to 16L, regions with high luminance in a ring pattern are shown. Furthermore, a plurality of spots are shown in the ring-shaped regions.

[0283]

In other words, it is found that Sample 1A has an nc structure and has characteristics

distinctly different from those of an oxide semiconductor film having an amorphous structure and an oxide semiconductor film having a single crystal structure.

[0284]

According to the above description, the electron diffraction patterns of Sample 1A and Sample 1D each have the region with high luminance in a ring pattern and the plurality of bright spots appear in the ring-shaped region. Thus, it is found that Sample 1A exhibits an electron diffraction pattern of the nc-OS and does not show alignment in the plane direction and the cross-sectional direction. In addition, it is found that Sample 1D has an nc structure and a CAAC structure.

[0285]

In the electron diffraction pattern of Sample 1J, spots derived from the (009) plane of an $InGaZnO_4$ crystal are included. Thus, Sample 1J has c-axis alignment and the c-axes are aligned in the direction substantially perpendicular to the formation surface or the top surface of Sample 1J.

[0286]

<Analysis of TEM image>

This section describes the observation and analysis results of Samples 1A, 1C, 1D, 1F, 1G, and 1J with an HAADF-STEM.

[0287]

The results of image analysis of plan-view TEM images are described. The plan-view TEM images were obtained with a spherical aberration corrector function. The plan-view TEM images were obtained using an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd. under the following conditions: the acceleration voltage was 200 kV; and irradiation with an electron beam with a diameter of approximately 0.1 nmφ was performed.

[0288]

In FIG. 17, the plan-view TEM images of Samples 1A, 1C, 1D, 1F, 1G, and 1J and images obtained through image processing of the plan-view TEM images are shown. Note that in a table in FIG. 17, left views are the plan-view TEM images and right views are the images obtained through image processing of the plan-view TEM images on the left side.

[0289]

Image processing and image analyzing methods are described. Image processing was performed as follows. The plan-view TEM image in FIG. 17 was subjected to fast Fourier transform (FFT), so that an FFT image was obtained. Then, the obtained FFT image was subjected to mask processing except for a range from 2.8 nm^{-1} to 5.0 nm^{-1}. After that, the FFT

image subjected to mask processing was subjected to inverse fast Fourier transform (IFFT) to obtain an FFT filtering image.

[0290]

To conduct the image analysis, lattice points were extracted from the FFT filtering image in the following manner. First, noise in the FFT filtering image was removed. To remove the noise, the luminance of a region within a 0.05-nm radius was smoothed using Formula 1.

[0291]

[Formula 1]

$$S_Int(x,y) = \sum_{r \le 0.05} \frac{Int(x',y')}{r} \qquad (1)$$

[0292]

Note that $S_Int(x,y)$ represents the smoothed luminance at the coordinates (x,y), r represents the distance between the coordinates (x,y) and the coordinates (x',y'), and $Int(x',y')$ represents the luminance at the coordinates (x',y'). In the calculation, r is regarded as 1 when it is 0.

[0293]

Then, a search for lattice points was conducted. The coordinates with the highest luminance among candidate lattice points within a 0.22-nm radius were regarded as the lattice point. At this point, a candidate lattice point was extracted. Within a 0.22-nm radius, detection errors of lattice points due to noise can be less frequent. Note that adjacent lattice points are a certain distance away from each other in the TEM image; thus, two or more lattice points are unlikely to be observed within a 0.22-nm radius.

[0294]

Subsequently, coordinates with the highest luminance within a 0.22-nm radius from the extracted candidate lattice point were extracted to redetermine a candidate lattice point. The extraction of a candidate lattice point was repeated in this manner until no new candidate lattice point appeared; the coordinates at that point were determined as a lattice point. Similarly, determination of another lattice point was performed at a position 0.22 nm or more away from the determined lattice point; thus, lattice points were determined in the entire region. The determined lattice points are collectively called a lattice point group.

[0295]

Here, a method for deriving an orientation of a hexagonal lattice from the extracted lattice point group is described with reference to schematic diagrams in FIGS. 18A to 18C and a flow chart in FIG. 18D. First, a reference lattice point was determined and the six closest

lattice points to the reference lattice point were connected to form a hexagonal lattice (see FIG. 18A and Step S101 in FIG. 18D). After that, an average distance R between the reference lattice point, which was the center point of the hexagonal lattice, and each of the lattice points, which is a vertex, was calculated. Then, a regular hexagon was formed with the use of the reference lattice point as the center point and the calculated distance R as the distance from the center point to each vertex (see Step S102 in FIG. 18D). The distances from the vertices of the regular hexagon to their respective closest lattice points were regarded as a distance d1, a distance d2, a distance d3, a distance d4, a distance d5, and a distance d6 (see FIG. 18B and Step S103 in FIG. 18D). Next, the regular hexagon was rotated around the center point through 60° by 0.1°, and the average deviation between the hexagonal lattice and the rotated regular hexagon [D = (d1 + d2 + d3 + d4 + d5 + d6)/6] was calculated (see Step S104 in FIG. 18D). Then, a rotation angle θ of the regular hexagon when the average deviation D becomes minimum was calculated as the orientation of the hexagonal lattice (see FIG. 18C and Step S105 in FIG. 18D).

[0296]

Next, an observation area of the plan-view TEM image was adjusted so that hexagonal lattices whose orientations were 30° account for the highest percentage. In such a condition, the average orientation of hexagonal lattice within a 1-nm radius was calculated. The plan-view TEM image obtained through image processing was shown where color or gradation changes in accordance with the angle of the hexagonal lattice in the region. The image obtained through image processing of the plan-view TEM image in FIG. 17 is an image obtained by performing image analysis on the plan-view TEM image in FIG. 17 by the above method and applying color in accordance with the angle of the hexagonal lattice. In other words, the image obtained through the image processing of the plan-view TEM image is an image in which the orientations of lattice points in certain wavenumber ranges are extracted by color-coding the certain wavenumber ranges in an FFT filtering image of the plan-view TEM image.

[0297]

As shown in FIG. 17, in Samples 1A and 1D in which nc is observed, the hexagons are oriented randomly and distributed in a mosaic pattern. In Sample 1J in which a layered structure is observed in the cross-sectional TEM image, regions with uniformly oriented hexagons exist in a large area of several tens of nanometers. In Sample 1D, it is found that an nc region in a random mosaic pattern and a large-area region with uniformly oriented hexagons as in Sample 1J are included.

[0298]

It is found from FIG. 17 that as the substrate temperature at the time of formation is lower or the oxygen gas flow rate ratio at the time of formation is lower, regions in which the

hexagons are oriented randomly and distributed in a mosaic pattern are likely to exist.

[0299]

Through the analysis of a plan-view TEM image of a CAAC-OS, a boundary portion where angles of hexagonal lattices change can be examined.

[0300]

Next, Voronoi diagrams were formed using lattice point groups in Sample 1A. A Voronoi diagram is an image partitioned by regions including a lattice point group. Each lattice point is closer to regions surrounding the lattice point than to any other lattice point. A method for forming a Voronoi diagram is described below in detail using schematic diagrams in FIGS. 19A to 19D and a flow chart in FIG. 19E.

[0301]

First, a lattice point group was extracted by the method described using FIGS. 18A to 18D or the like (see FIG. 19A and Step S111 in FIG. 19E). Next, adjacent lattice points were connected with segments (see FIG. 19B and Step S112 in FIG. 19E). Then, perpendicular bisectors of the segments were drawn (see FIG. 19C and Step S113 in FIG. 19E). Subsequently, points where three perpendicular bisectors intersect were extracted (see Step S114 in FIG. 19E). The points are called Voronoi points. After that, adjacent Voronoi points were connected with segments (see FIG. 19D and Step S115 in FIG. 19E). A polygonal region surrounded by the segments at this point is called a Voronoi region. In the above method, a Voronoi diagram was formed.

[0302]

FIG. 20 shows the proportions of the shapes of Voronoi regions (tetragon, pentagon, hexagon, heptagon, octagon, and enneagon) in Samples 1A, 1C, 1D, 1F, 1G, and 1J. Bar graphs show the numbers of the shapes of Voronoi regions (tetragon, pentagon, hexagon, heptagon, octagon, and enneagon) in the samples. Furthermore, tables show the proportions of the shapes of Voronoi regions (tetragon, pentagon, hexagon, heptagon, octagon, and enneagon) in the samples.

[0303]

It is found from FIG. 20 that there is a tendency that the proportion of hexagons is high in Sample 1J with a high degree of crystallinity and the proportion of hexagons is low in Sample 1A with a low degree of crystallinity. The proportion of hexagons in Sample 1D is between those in Samples 1J and 1A. Accordingly, it is found from FIG. 20 that the crystal state of the oxide semiconductor significantly differs under different formation conditions.

[0304]

It is found from FIG. 20 that as the substrate temperature at the time of formation is

lower or the oxygen gas flow rate ratio at the time of formation is lower, the degree of crystallinity is lower and the proportion of hexagons is lower.

[0305]

<Elementary analysis>

This section describes the analysis results of elements included in Sample 1A. For the analysis, by energy dispersive X-ray spectroscopy (EDX), EDX mapping images are obtained. An energy dispersive X-ray spectrometer AnalysisStation JED-2300T manufactured by JEOL Ltd. is used as an elementary analysis apparatus in the EDX measurement. A Si drift detector is used to detect an X-ray emitted from the sample.

[0306]

In the EDX measurement, an EDX spectrum of a point is obtained in such a manner that electron beam irradiation is performed on the point in a detection target region of a sample, and the energy of characteristic X-ray of the sample generated by the irradiation and its frequency are measured. In this example, peaks of an EDX spectrum of the point were attributed to electron transition to the L shell in an In atom, electron transition to the K shell in a Ga atom, and electron transition to the K shell in a Zn atom and the K shell in an O atom, and the proportions of the atoms in the point are calculated. An EDX mapping image indicating distributions of proportions of atoms can be obtained through the process in an analysis target region of a sample.

[0307]

FIGS. 21A to 21H show a cross-sectional TEM image, a plan-view TEM image, and EDX mapping images of Sample 1A. In the EDX mapping images, the proportion of an element is indicated by grayscale: the more measured atoms exist in a region, the brighter the region is; the less measured atoms exist in a region, the darker the region is. The magnification of the EDX mapping images in FIGS. 21B to 21D and 21F to 21H is 7,200,000 times.

[0308]

FIG. 21A shows a cross-sectional TEM image, and FIG. 21E shows a plan-view TEM image. FIG. 21B shows a cross-sectional EDX mapping image of In atoms, and FIG. 21F shows a plan-view EDX mapping image of In atoms. In the EDX mapping image in FIG. 21B, the proportion of the In atoms in all the atoms is 9.28 atomic% to 33.74 atomic%. In the EDX mapping image in FIG. 21F, the proportion of the In atoms in all the atoms is 12.97 atomic% to 38.01 atomic%.

[0309]

FIG. 21C shows a cross-sectional EDX mapping image of Ga atoms, and FIG. 21G shows a plan-view EDX mapping image of Ga atoms. In the EDX mapping image in FIG. 21C,

the proportion of the Ga atoms in all the atoms is 1.18 atomic% to 18.64 atomic%. In the EDX mapping image in FIG. 21G, the proportion of the Ga atoms in all the atoms is 1.72 atomic% to 19.82 atomic%.

[0310]

FIG. 21D shows a cross-sectional EDX mapping image of Zn atoms, and FIG. 21H shows a plan-view EDX mapping image of Zn atoms. In the EDX mapping image in FIG. 21D, the proportion of the Zn atoms in all the atoms is 6.69 atomic% to 24.99 atomic%. In the EDX mapping image in FIG. 21H, the proportion of the Zn atoms in all the atoms is 9.29 atomic% to 28.32 atomic%.

[0311]

Note that FIGS. 21A to 21D show the same region in the cross section of Sample 1A. FIGS. 21E to 21H show the same region in the plane of Sample 1A.

[0312]

FIGS. 22A to 22C show enlarged cross-sectional EDX mapping images of Sample 1A. FIG. 22A is an enlarged view of a part in FIG. 21B. FIG. 22B is an enlarged view of a part in FIG. 21C. FIG. 22C is an enlarged view of a part in FIG. 21D.

[0313]

The EDX mapping images in FIGS. 22A to 22C show relative distribution of bright and dark areas, indicating that the atoms have distributions in Sample 1A. Areas surrounded by solid lines and areas surrounded by dashed lines in FIGS. 22A to 22C are examined.

[0314]

As shown in FIG. 22A, a relatively dark region occupies a large area in the area surrounded by the solid line and a relatively bright region occupies in a large area in the area surrounded by the dashed line. As shown in FIG. 22B, a relatively bright region occupies a large area in the area surrounded by the solid line and a relatively dark region occupies a large area in the area surrounded by the dashed line.

[0315]

That is, it is found that the areas surrounded by the solid lines are regions including a relatively large number of In atoms and the areas surrounded by the dashed lines are regions including a relatively small number of In atoms. FIG. 22C shows that a right portion of the area surrounded by the solid line is relatively bright and a left portion thereof is relatively dark. Thus, it is found that the area surrounded by the solid line is a region including $In_{X2}Zn_{Y2}O_{Z2}$, InO_{X1}, or the like as a main component.

[0316]

It is found that the area surrounded by the solid line is a region including a relatively

small number of Ga atoms and the area surrounded by the dashed line is a region including a relatively large number of Ga atoms. FIG. 22C shows that an upper left portion of the area surrounded by the dashed line is relatively dark and a lower right portion thereof is relatively bright. Thus, it is found that the area surrounded by the dashed line is a region including GaO_{X3}, $Ga_{X4}Zn_{Y4}O_{Z4}$, or the like as a main component.

[0317]

Furthermore, as shown in FIGS. 22A to 22C, the In atoms are relatively more uniformly distributed than the Ga atoms, and regions including InO_{X1} as a main component are seemingly joined to each other through a region including $In_{X2}Zn_{Y2}O_{Z2}$ as a main component. It can be thus guessed that the regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component extend like a cloud.

[0318]

An In-Ga-Zn oxide having a composition in which the regions including GaO_{X3} as a main component and the regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are unevenly distributed and mixed can be referred to as CAC-IGZO.

[0319]

As shown in FIGS. 22A to 22C, each of the regions including GaO_{X3} as a main component and the regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component has a size of greater than or equal to 0.5 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 3 nm.

[0320]

As described above, it is confirmed that the CAC-IGZO has a structure different from that of an IGZO compound in which metal elements are evenly distributed, and has characteristics different from those of the IGZO compound. That is, it can be confirmed that in the CAC-IGZO, regions including GaO_{X3} or the like as a main component and regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are separated to form a mosaic pattern.

[0321]

Accordingly, it can be expected that when CAC-IGZO is used for a semiconductor element, the property derived from GaO_{X3} or the like and the property derived from $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} complement each other, whereby high on-state current (I_{on}), high field-effect mobility (μ), and low off-state current (I_{off}) can be achieved. A semiconductor element including CAC-IGZO has high reliability. Thus, CAC-IGZO is suitably used in a variety of semiconductor devices typified by a display.

[0322]

At least part of this example can be implemented in combination with any of

embodiments and the other examples described in this specification as appropriate.

[Example 2]

[0323]

In this example, the transistor 150 including the oxide semiconductor film 108 of one embodiment of the present invention was fabricated and subjected to tests for electrical characteristics and reliability. In this example, nine transistors, i.e., Samples 2A, 2B, 2C, 2D, 2E, 2F, 2G, 2H, and 2J, were fabricated as the transistor 150 including the oxide semiconductor 108.

[0324]

<Structure of samples and fabrication method thereof>

Samples 2A to 2H and 2J relating to one embodiment of the present invention are described below. As Samples 2A to 2H and 2J, the transistors 150 having the structure illustrated in FIGS. 3A to 3C were fabricated by the fabrication method described in Embodiment 2 with reference to FIGS. 6A to 6D, FIGS. 7A to 7C, and FIGS. 8A to 8C.

[0325]

Samples 2A to 2H and 2J were fabricated at different temperatures and different oxygen flow rate ratios in formation of the oxide semiconductor 108. The temperatures and the oxygen flow rate ratios in formation of the oxide semiconductors of Samples 2A to 2H and 2J are shown in Table 2 below.

[0326]

[Table 2]

	Formation conditions of oxide semiconductor film 108			
	Flow rate [sccm]		Percentage of O_2 [%]	Deposition temperature [°C]
	O_2	Ar		
Sample 2A	30	270	10	R.T.
Sample 2B	90	210	30	R.T.
Sample 2C	300	0	100	R.T.
Sample 2D	30	270	10	130
Sample 2E	90	210	30	130
Sample 2F	300	0	100	130
Sample 2G	30	270	10	170
Sample 2H	90	210	30	170
Sample 2J	300	0	100	170

[0327]

The samples were fabricated by the fabrication method described in Embodiment 2. The oxide semiconductor 108 was formed using a metal oxide target (In:Ga:Zn = 4:2:4.1 [atomic ratio]).

[0328]

The transistor 150 had a channel length of 2 μm and a channel width of 3 μm (hereinafter, also referred to as L/W = 2/3 μm) or a channel length of 2 μm and a channel width of 50 μm (hereinafter, also referred to as L/W = 2/50 μm).

[0329]

<I_d-V_g characteristics of transistors>

Next, I_d-V_g characteristics of the transistors (L/W = 2/3 μm) in Samples 2A to 2H and 2J were measured. As conditions for measuring the I_d-V_g characteristics of each transistor, a voltage applied to the conductive film 112 serving as a first gate electrode (hereinafter the voltage is also referred to as gate voltage (V_g)) and a voltage applied to the conductive film 106 serving as a second gate electrode (hereinafter the voltage is also referred to as back gate voltage (V_{bg})) were changed from −10 V to +10 V in increments of 0.25 V. A voltage applied to the conductive film 120a serving as a source electrode (the voltage is also referred to as source voltage (V_s)) was 0 V (comm), and a voltage applied to the conductive film 120b serving as a drain electrode (the voltage is also referred to as drain voltage (V_d)) was 0.1 V and 20 V.

[0330]

In FIG. 23, the results of I_d-V_g characteristics and field-effect mobilities of Samples 2A to 2H and 2J are shown. The solid line and the dashed-dotted line represent I_d at V_d = 20 V and I_d at V_d = 0.1 V, respectively. The dashed line represents field-effect mobility. In FIG. 23, the first vertical axis represents I_d [A], the second vertical axis represents field-effect mobility (μFE) [cm^2/Vs], and the horizontal axis represents V_g [V]. The field-effect mobility was calculated from the value measured at V_d = 20 V.

[0331]

As shown in FIG. 23, it is found that Samples 2A to 2H and 2J have different on-state currents (I_{on}) and different field effect mobilities, particularly different field effect mobilities in saturation regions. In particular, the maximum saturation mobilities and the rising characteristics of the field-effect mobilities around 0 V differ distinctly.

[0332]

It is found from FIG. 23 that as the substrate temperature at the time of formation is lower or the oxygen flow rate ratio at the time of formation is lower, the on-state current (I_{on}) becomes higher and the field effect mobility rises more steeply around 0 V. In particular, Sample 2A has a maximum field-effect mobility close to 70 cm^2/Vs.

[0333]

<Gate bias-temperature stress test (GBT test)>

Next, the reliability of the transistors (L/W = 2/50 μm) of Samples 2A to 2H and 2J was evaluated. As the reliability evaluation, GBT tests were used.

[0334]

The conditions for GBT tests in this example were as follows. A voltage applied to the conductive film 112 serving as the first gate electrode and the conductive film 106 serving as the second gate electrode (hereinafter referred to as gate voltage (V_g)) was ±30 V, and a voltage applied to the conductive film 120a serving as the source electrode and the conductive film 120b serving as a drain electrode (hereinafter referred to as source voltage (V_s) and drain voltage (V_d), respectively) was 0 V (COMMON). The stress temperature was 60 °C, the time for stress application was 1 hour, and two kinds of measurement environments, a dark environment and a photo environment (irradiation with light at approximately 10,000 lx from a white LED), were employed.

[0335]

In other words, the conductive film 120a serving as the source electrode of the transistor 150 and the conductive film 120b serving as the drain electrode of the transistor 150 were set at the same potential, and a potential different from that of the conductive film 120a serving as the source electrode and the conductive film 120b serving as the drain electrode was applied to the

conductive film 112 serving as the first gate electrode and the conductive film 106 serving as the second gate electrode for a certain time (here, one hour).

[0336]

A case where the potential applied to the conductive film 112 serving as the first gate electrode and the conductive film 106 serving as the second gate electrode is higher than the potential applied to the conductive film 120a serving as the source electrode and the conductive film 120b serving as the drain electrode is called positive stress, and a case where the potential applied to the conductive film 112 serving as the first gate electrode and the conductive film 106 serving as the second gate electrode is lower than the potential applied to the conductive film 120a serving as the source electrode and the conductive film 120b serving as the drain electrode is called negative stress. Thus, the reliability evaluation was performed under four conditions in total, i.e., positive GBT (dark), negative GBT (dark), positive GBT (light irradiation), and negative GBT (light irradiation).

[0337]

Note that the positive GBT (dark) can be referred to as positive bias temperature stress (PBTS), the negative GBT (dark) as negative bias temperature stress (NBTS), the positive GBT (light irradiation) as positive bias illumination temperature stress (PBITS), and the negative GBT (light irradiation) as negative bias illumination temperature stress (NBITS).

[0338]

FIG. 24 shows the GBT test results of Samples 2A to 2H and 2J. In FIG. 24, the vertical axis represents the amount of shift in the threshold voltage (ΔV_{th}) of the transistors.

[0339]

The results in FIG. 24 indicate that the amount of shift in the threshold voltage (ΔV_{th}) of each of the transistors included in Samples 2A to 2H and 2J was within ±3 V in the GBT tests. Thus, it is confirmed that the transistors included in Samples 2A to 2H and 2J each have high reliability.

[0340]

Thus, even the IGZO film having low crystallinity is presumed to have a low density of defect states like an IGZO film having high crystallinity.

[0341]

At least part of this example can be implemented in combination with any of embodiments and the other examples described in this specification as appropriate.

[Example 3]

[0342]

In this example, measurement results of an oxide semiconductor of one embodiment of

the present invention formed over a substrate are described. A variety of methods were used for the measurement. Note that in this example, Samples 3A, 3D, and 3J were fabricated.

[0343]

<<Structure of samples and fabrication method thereof>>

Samples 3A, 3D, and 3J relating to one embodiment of the present invention are described below. Samples 3A, 3D, and 3J each include a substrate and an oxide semiconductor over the substrate.

[0344]

Samples 3A, 3D, and 3J were fabricated at different temperatures and different oxygen flow rate ratios in formation of the oxide semiconductor. The temperatures and the oxygen flow rate ratios in formation of the oxide semiconductors of Samples 3A, 3D, and 3J are shown in Table 3 below.

[0345]

[Table 3]

	Flow rate [sccm]		Percentage of O_2 [%]	Deposition temperature [°C]
	O_2	Ar		
Sample 3A	30	270	10	R.T.
Sample 3D	30	270	10	130
Sample 3J	150	150	50	170

[0346]

Next, methods for fabricating the samples will be described.

[0347]

A glass substrate was used as the substrate. Over the substrate, a 100-nm-thick In-Ga-Zn oxide semiconductor was formed as an oxide semiconductor with a sputtering apparatus. The formation conditions were as follows: the pressure in a chamber was 0.6 Pa, and a metal oxide target (where an atomic ratio In:Ga:Zn is 1:1:1.2) was used as a target. The metal oxide target provided in the sputtering apparatus was supplied with an AC power of 2500 W.

[0348]

The formation temperatures and oxygen flow rate ratios shown in the above table were used as the conditions for forming oxide semiconductors to fabricate Samples 3A, 3D, and 3J.

[0349]

Through the above steps, Samples 3A, 3D, and 3J of this example were fabricated.

[0350]

<TEM images and electron diffraction>

This section describes the TEM observation and analysis results of Samples 3A, 3D, and 3J.

[0351]

This section describes electron diffraction patterns obtained by irradiation of Samples 3A, 3D, and 3J with an electron beam with a probe diameter of 1 nm (also referred to as a nanobeam).

[0352]

The plan-view TEM images were observed with a spherical aberration corrector function. The HAADF-STEM images were obtained using an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd. under the following conditions: the acceleration voltage was 200 kV, and irradiation with an electron beam with a diameter of approximately 0.1 nmφ was performed.

[0353]

Note that the electron diffraction patterns were observed while an electron beam irradiation was performed at a constant rate for 35 seconds.

[0354]

FIG. 25A shows a cross-sectional TEM image of Sample 3A, and FIG. 25B shows an electron diffraction pattern of Sample 3A. FIG. 25C shows a cross-sectional TEM image of Sample 3D, and FIG. 25D shows an electron diffraction pattern of Sample 3D. FIG. 25E shows a cross-sectional TEM image of Sample 3J, and FIG. 25F shows an electron diffraction pattern of Sample 3J.

[0355]

As shown in FIG. 25A, a nanocrystal is observed in Sample 3A by cross-sectional TEM. In addition, as shown in FIG. 25B, the observed electron diffraction pattern of Sample 3A has a region with high luminance in a circular (ring) pattern. Furthermore, a plurality of spots can be shown in the ring-shaped region.

[0356]

As shown in FIG. 25C, a CAAC structure and a nanocrystal are observed in Sample 3D by cross-sectional TEM. In addition, as shown in FIG. 25D, the observed electron diffraction pattern of Sample 3D has a region with high luminance in a circular (ring) pattern. Furthermore, a plurality of spots can be shown in the ring-shaped region. In the diffraction pattern, spots derived from the (009) plane are slightly observed.

[0357]

In contrast, as shown in FIG. 25E, layered arrangement of a CAAC structure is observed

in Sample 3J by cross-sectional TEM. Furthermore, spots derived from the (009) plane are included in the electron diffraction pattern of Sample 3J in FIG. 25F.

[0358]

The features observed in the cross-sectional TEM images and the plan-view TEM images are one aspect of a structure of an oxide semiconductor.

[0359]

According to the above description, the electron diffraction patterns of Sample 3A and Sample 3D each have a region with high luminance in a ring pattern and a plurality of bright spots appear in the ring-shaped region. Accordingly, Samples 3A and 3D each exhibit an electron diffraction pattern of the nc-OS and do not show alignment in the plane direction and the cross-sectional direction. Sample 3D is found to be a mixed material of the nc structure and the CAAC structure.

[0360]

In the electron diffraction pattern of Sample 3J, spots derived from the (009) plane of an $InGaZnO_4$ crystal are included. Thus, Sample 3J has c-axis alignment and the c-axes are aligned in the direction substantially perpendicular to the formation surface or the top surface of Sample 3J.

[0361]

<Analysis of TEM image>

This section describes the observation and analysis results of Samples 3A, 3D, and 3J with an HAADF-STEM.

[0362]

The results of image analysis of plan-view TEM images are described. The plan-view TEM images were obtained with a spherical aberration corrector function. The plan-view TEM images were obtained using an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd. under the following conditions: the acceleration voltage was 200 kV, and irradiation with an electron beam with a diameter of approximately 0.1 nmφ was performed.

[0363]

FIG. 26A shows a plan-view TEM image of Sample 3A, and FIG. 26B shows an image obtained through image processing of the plan-view TEM image of Sample 3A. FIG. 26C shows a plan-view TEM image of Sample 3D and FIG. 26D shows an image obtained through image processing of the plan-view TEM image of Sample 3D. FIG. 26E shows a plan-view TEM image of Sample 3J and FIG. 26F shows an image obtained through image processing of the plan-view TEM image of Sample 3J.

[0364]

The images obtained through image processing of the plan-view TEM images in FIGS. 26B, 26D, and 26F are images obtained through image analysis of the plan-view TEM images in FIGS. 26A, 26C, and 26E by the method described in Example 1 and applying color in accordance with the angle of the hexagonal lattice. In other words, the images obtained through the image processing of the plan-view TEM images are each an image in which the orientations of lattice points in certain wavenumber ranges are extracted by color-coding the certain wavenumber ranges and providing gradation in the ranges in an FFT filtering image of the plan-view TEM image.

[0365]

As shown in FIGS. 26A to 26F, in Samples 3A and 3D in which nc is observed, the hexagons are oriented randomly and distributed in a mosaic pattern. In Sample 3J in which a layered structure is observed in the cross-sectional TEM image, regions with uniformly oriented hexagons exist in a large area of several tens of nanometers. In Sample 3D, it is found that an nc region in a random mosaic pattern and a large-area region with uniformly oriented hexagons as in Sample 3J are included.

[0366]

It is found from FIGS. 26A to 26F that as the substrate temperature at the time of formation is lower or the oxygen gas flow rate ratio at the time of formation is lower, regions in which the hexagons are oriented randomly and distributed in a mosaic pattern are likely to exist.

[0367]

Through the analysis of a plan-view TEM image of a CAAC-OS, a boundary portion where angles of hexagonal lattices change can be examined.

[0368]

Next, Voronoi diagrams were formed using lattice point groups in Sample 3A. The Voronoi diagrams were obtained by the method described in Example 1.

[0369]

FIGS. 27A to 27C show the proportions of the shapes of Voronoi regions (tetragon, pentagon, hexagon, heptagon, octagon, and enneagon) in Samples 3A, 3D, and 3J, respectively. Bar graphs show the numbers of the shapes of Voronoi regions (tetragon, pentagon, hexagon, heptagon, octagon, and enneagon) in the samples. Furthermore, tables show the proportions of the shapes of Voronoi regions (tetragon, pentagon, hexagon, heptagon, octagon, and enneagon) in the samples.

[0370]

It is found from FIGS. 27A to 27C that there is a tendency that the proportion of hexagons is high in Sample 3J with a high degree of crystallinity and the proportion of hexagons

is low in Sample 3A with a low degree of crystallinity. The proportion of hexagons in Sample 3D is between those in Samples 3J and 3A. Accordingly, it is found from FIGS. 27A to 27C that the crystal state of the oxide semiconductor significantly differs under different formation conditions.

[0371]

It is found from FIGS. 27A to 27C that as the substrate temperature at the time of formation is lower or the oxygen gas flow rate ratio at the time of formation is lower, the degree of crystallinity is lower and the proportion of hexagons is lower.

[0372]

<Elementary analysis>

This section describes the analysis results of elements included in Sample 3A. For the analysis, by energy dispersive X-ray spectroscopy (EDX), EDX mapping images are obtained. An energy dispersive X-ray spectrometer AnalysisStation JED-2300T manufactured by JEOL Ltd. is used as an elementary analysis apparatus in the EDX measurement. A Si drift detector is used to detect an X-ray emitted from the sample.

[0373]

In the EDX measurement, an EDX spectrum of a point is obtained in such a manner that electron beam irradiation is performed on the point in a detection target region of a sample, and the energy of characteristic X-ray of the sample generated by the irradiation and its frequency are measured. In this example, peaks of an EDX spectrum of the point were attributed to electron transition to the L shell in an In atom, electron transition to the K shell in a Ga atom, and electron transition to the K shell in a Zn atom and the K shell in an O atom, and the proportions of the atoms in the point are calculated. An EDX mapping image indicating distributions of proportions of atoms can be obtained through the process in an analysis target region of a sample.

[0374]

FIGS. 28A to 28H show a cross-sectional TEM image, a plan-view TEM image, and EDX mapping images of Sample 3A. In the EDX mapping images, the proportion of an element is indicated by grayscale: the more measured atoms exist in a region, the brighter the region is; the less measured atoms exist in a region, the darker the region is. The magnification of the EDX mapping images in FIGS. 28B to 28D and 28F to 28H is 7,200,000 times.

[0375]

FIG. 28A shows a cross-sectional TEM image, and FIG. 28E shows a plan-view TEM image. FIG. 28B shows a cross-sectional EDX mapping image of In atoms, and FIG. 28F shows a plan-view EDX mapping image of In atoms. In the EDX mapping image in FIG. 28B,

the proportion of the In atoms in all the atoms is 8.64 atomic% to 34.91 atomic%. In the EDX mapping image in FIG. 28F, the proportion of the In atoms in all the atoms is 5.76 atomic% to 34.69 atomic%.

[0376]

FIG. 28C shows a cross-sectional EDX mapping image of Ga atoms, and FIG. 28G shows a plan-view EDX mapping image of Ga atoms. In the EDX mapping image in FIG. 28C, the proportion of the Ga atoms in all the atoms is 2.45 atomic% to 25.22 atomic%. In the EDX mapping image in FIG. 28G, the proportion of the Ga atoms in all the atoms is 1.29 atomic% to 27.64 atomic%.

[0377]

FIG. 28D shows a cross-sectional EDX mapping image of Zn atoms, and FIG. 28H shows a plan-view EDX mapping image of Zn atoms. In the EDX mapping image in FIG. 28D, the proportion of the Zn atoms in all the atoms is 5.05 atomic% to 23.47 atomic%. In the EDX mapping image in FIG. 28H, the proportion of the Zn atoms in all the atoms is 3.69 atomic% to 27.86 atomic%.

[0378]

Note that FIGS. 28A to 28D show the same region in the cross section of Sample 3A. FIGS. 28E to 28H show the same region in the plane of Sample 3A.

[0379]

FIGS. 29A to 29C show enlarged cross-sectional EDX mapping images of Sample 3A. FIG. 29A is an enlarged view of a part in FIG. 28B. FIG. 29B is an enlarged view of a part in FIG. 28C. FIG. 29C is an enlarged view of a part in FIG. 28D.

[0380]

The EDX mapping images in FIGS. 29A to 29C show relative distribution of bright and dark areas, indicating that the atoms have distributions in Sample 3A. Areas surrounded by solid lines and areas surrounded by dashed lines in FIGS. 29A to 29C are examined.

[0381]

As shown in FIG. 29A, a relatively dark region occupies a large area in the area surrounded by the solid line and a relatively bright region occupies a large area in the area surrounded by the dashed line. As shown in FIG. 29B, a relatively bright region occupies a large area in the area surrounded by the solid line and a relatively dark region occupies a large area in the area surrounded by the dashed line.

[0382]

That is, it is found that the areas surrounded by the solid lines are regions including a

relatively large number of In atoms and the areas surrounded by the dashed lines are regions including a relatively small number of In atoms. FIG. 29C shows that an upper portion of the area surrounded by the solid line is relatively bright and a lower portion thereof is relatively dark. Thus, it is found that the area surrounded by the solid line is a region including $In_{X2}Zn_{Y2}O_{Z2}$, InO_{X1}, or the like as a main component.

[0383]

It is found that the area surrounded by the solid line is a region including a relatively small number of Ga atoms and the area surrounded by the dashed line is a region including a relatively large number of Ga atoms. As shown in FIG. 29C, a relatively bright region occupies a large area in a right portion in the area surrounded by the upper dashed line and a dark region occupies a large area in a left portion therein. As shown in FIG. 29C, a relatively bright region occupies a large area in an upper left portion in the area surrounded by the lower dashed line and a dark region occupies a large area in a lower right portion therein. Thus, it is found that the area surrounded by the dashed line is a region including GaO_{X3}, $Ga_{X4}Zn_{Y4}O_{Z4}$, or the like as a main component.

[0384]

Furthermore, as shown in FIGS. 29A to 29C, the In atoms are relatively more uniformly distributed than the Ga atoms, and regions including InO_{X1} as a main component are seemingly joined to each other through a region including $In_{X2}Zn_{Y2}O_{Z2}$ as a main component. It can be thus guessed that the regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component extend like a cloud.

[0385]

An In-Ga-Zn oxide having a composition in which the regions including GaO_{X3} as a main component and the regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are unevenly distributed and mixed can be referred to as CAC-IGZO.

[0386]

As shown in FIGS. 29A to 29C, each of the regions including GaO_{X3} as a main component and the regions including $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component has a size of greater than or equal to 0.5 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 3 nm.

[0387]

As described above, it is confirmed that the CAC-IGZO has a structure different from that of an IGZO compound in which metal elements are evenly distributed, and has characteristics different from those of the IGZO compound. That is, it can be confirmed that in the CAC- IGZO, regions including GaO_{X3} or the like as a main component and regions including

$In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} as a main component are separated to form a mosaic pattern.

[0388]

Accordingly, it can be expected that when CAC-IGZO is used for a semiconductor element, the property derived from GaO_{X3} or the like and the property derived from $In_{X2}Zn_{Y2}O_{Z2}$ or InO_{X1} complement each other, whereby high on-state current (I_{on}), high field-effect mobility (μ), and low off-state current (I_{off}) can be achieved. A semiconductor element including CAC-IGZO has high reliability. Thus, CAC-IGZO is suitably used in a variety of semiconductor devices typified by a display.

[0389]

At least part of this example can be implemented in combination with any of embodiments and the other examples described in this specification as appropriate.

[Example 4]

[0390]

In this example, the transistor 150 including the oxide semiconductor 108 of one embodiment of the present invention was fabricated and subjected to tests for electrical characteristics and reliability. In this example, nine transistors, i.e., Samples 4A, 4B, 4C, 4D, 4E, 4F, 4G, 4H, and 4J, were fabricated as the transistor 150 including the oxide semiconductor 108.

[0391]

<<Structure of samples and fabrication method thereof>>

Samples 4A to 4H and 4J relating to one embodiment of the present invention are described below. As Samples 4A to 4H and 4J, the transistors 150 having the structure illustrated in FIGS. 3A to 3C were fabricated by the fabrication method described in Embodiment 2 with reference to FIGS. 6A to 6D, FIGS. 7A to 7C, and FIGS. 8A to 8C.

[0392]

Samples 4A to 4H and 4J were fabricated at different temperatures and different oxygen flow rate ratios in formation of the oxide semiconductor 108. The temperatures and the oxygen flow rates in formation of the oxide semiconductor of Samples 4A to 4H and 4J are shown in Table 4 below.

[0393]

[Table 4]

	Formation conditions of oxide semiconductor film 108			
	Flow rate [sccm]		Percentage of O_2 [%]	Deposition temperature [°C]
	O_2	Ar		
Sample 4A	30	270	10	R.T.
Sample 4B	90	210	30	R.T.
Sample 4C	150	150	50	R.T.
Sample 4D	30	270	10	130
Sample 4E	90	210	30	130
Sample 4F	150	150	50	130
Sample 4G	30	270	10	170
Sample 4H	90	210	30	170
Sample 4J	150	150	50	170

[0394]

The samples were fabricated by the fabrication method described in Embodiment 2. The oxide semiconductor 108 was formed using a metal oxide target (In:Ga:Zn = 1:1:1.2 [atomic ratio]).

[0395]

The transistor 150 had a channel length of 2 μm and a channel width of 3 μm (hereinafter, also referred to as L/W = 2/3 μm).

[0396]

<I_d-V_g characteristics of transistors>

Next, I_d-V_g characteristics of the transistors (L/W = 2/3 μm) in Samples 4A to 4J were measured. As conditions for measuring the I_d-V_g characteristics of each transistor, a voltage applied to the conductive film 112 serving as a first gate electrode (hereinafter the voltage is also referred to as gate voltage (V_g)) and a voltage applied to the conductive film 106 serving as a second gate electrode (hereinafter the voltage is also referred to as back gate voltage (V_{bg})) were changed from −10 V to +10 V in increments of 0.25 V. A voltage applied to the conductive film 120a serving as a source electrode (the voltage is also referred to as source voltage (V_s)) was 0 V (comm), and a voltage applied to the conductive film 120b serving as a drain electrode (the voltage is also referred to as drain voltage (V_d)) was 0.1 V and 20 V.

[0397]

In FIG. 30, the results of I_d-V_g characteristics and field-effect mobilities of Samples 4A

to 4H and 4J are shown. The solid line and the dashed-dotted line represent I_d at V_d = 20 V and I_d at V_d = 0.1 V, respectively. The dashed line represents field-effect mobility. In FIG. 30, the first vertical axis represents I_d [A], the second vertical axis represents field-effect mobility (μFE) [cm^2/Vs], and the horizontal axis represents V_g [V]. The field-effect mobility is calculated from a value measured at V_d = 20 V.

[0398]

As shown in FIG. 30, the transistors 150 of Samples 4A to 4H and 4J have normally-off characteristics. As shown in FIG. 30, it is found that Samples 4A to 4H and 4J have different on-state currents (I_{on}) and different field effect mobilities, particularly different field effect mobilities in saturation regions. In particular, the maximum saturation mobilities and the rising characteristics of the field-effect mobilities around 0 V differ distinctly.

[0399]

It is found from FIG. 30 that as the substrate temperature at the time of formation is lower or the oxygen gas flow rate ratio at the time of formation is lower, the field-effect mobility at low V_g is significantly higher. In particular, Sample 4A has a maximum field-effect mobility close to 40 cm^2/Vs. Having high mobility at low V_g means being suitable for high-speed driving at low voltage; therefore, application to a variety of semiconductor devices typified by a display can be expected.

[0400]

At least part of this example can be implemented in combination with any of embodiments and the other examples described in this specification as appropriate.

REFERENCE NUMERALS

[0401]

001: region, 002: region, 003: region, 100: transistor, 102: substrate, 104: insulating film, 106: conductive film, 108: oxide semiconductor film, 108a: oxide semiconductor film, 108n: region, 110: insulating film, 110_0: insulating film, 112: conductive film, 112_0: conductive film, 112_1: conductive film, 112_2: conductive film, 116: insulating film, 118: insulating film, 120a: conductive film, 120b: conductive film, 122: insulating film, 140: mask, 141a: opening, 141b: opening, 143: opening, 150: transistor, 160: transistor, 300A: transistor, 300B: transistor, 300C: transistor, 300D: transistor, 302: substrate, 304: conductive film, 306: insulating film, 307: insulating film, 308: oxide semiconductor film, 312a: conductive film, 312b: conductive film, 314: insulating film, 316: insulating film, 318: insulating film, 320a: conductive film, 320b: conductive film, 341a: opening, 341b: opening, 342a: opening, 342b: opening, 342c: opening.

This application is based on Japanese Patent Application Serial No. 2016-100939 filed with Japan Patent Office on May 19, 2016, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A composite oxide semiconductor comprising:
a first region comprising indium; and
a second region comprising an element *M*,
wherein:
the element *M* comprises one or more of Ga, Al, Hf, Y, and Sn, and
the first region and the second region are arranged in a mosaic pattern.

2. A composite oxide semiconductor comprising:
a first region comprising indium oxide or indium zinc oxide;
a second region comprising gallium oxide or gallium zinc oxide; and
a third region comprising zinc oxide,
wherein the first region and the second region are arranged in a mosaic pattern.

3. The composite oxide semiconductor according to claim 2, wherein one of the first region, the second region, and the third region has a blurred periphery and a cloud-like composition.

4. The composite oxide semiconductor according to claim 1, wherein a diameter of the second region is greater than or equal to 0.5 nm and less than or equal to 10 nm, or in a neighborhood thereof.

5. The composite oxide semiconductor according to claim 2, wherein a diameter of the second region is greater than or equal to 0.5 nm and less than or equal to 10 nm, or in a neighborhood thereof.

6. The composite oxide semiconductor according to claim 1, wherein a diameter of the second region is greater than or equal to 1 nm and less than or equal to 2 nm, or in a neighborhood thereof.

7. The composite oxide semiconductor according to claim 2, wherein a diameter of the second region is greater than or equal to 1 nm and less than or equal to 2 nm, or in a neighborhood thereof.

8. The composite oxide semiconductor according to claim 1, wherein an atomic ratio between indium, the element *M*, and zinc is 4:2:3, or in a neighborhood thereof.

9. The composite oxide semiconductor according to claim 2, wherein an atomic ratio between indium, gallium, and zinc is 4:2:3, or in a neighborhood thereof.

10. The composite oxide semiconductor according to claim 1, wherein an atomic ratio between indium, the element *M*, and zinc is 5:1:6, or in a neighborhood thereof.

11. The composite oxide semiconductor according to claim 2, wherein an atomic ratio between indium, gallium, and zinc is 5:1:6, or in a neighborhood thereof.

12. The composite oxide semiconductor according to claim 1, wherein an atomic ratio between indium, the element *M*, and zinc is 1:1:1, or in a neighborhood thereof.

13. The composite oxide semiconductor according to claim 2, wherein an atomic ratio between indium, gallium, and zinc is 1:1:1, or in a neighborhood thereof.

14. A transistor comprising the composite oxide semiconductor according to claim 1.

15. A transistor comprising the composite oxide semiconductor according to claim 2.

FIG. 1

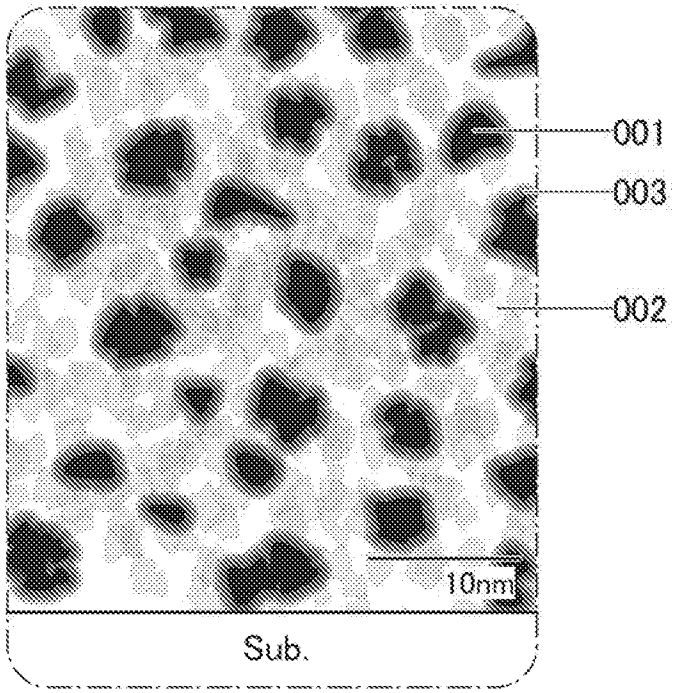


FIG. 2

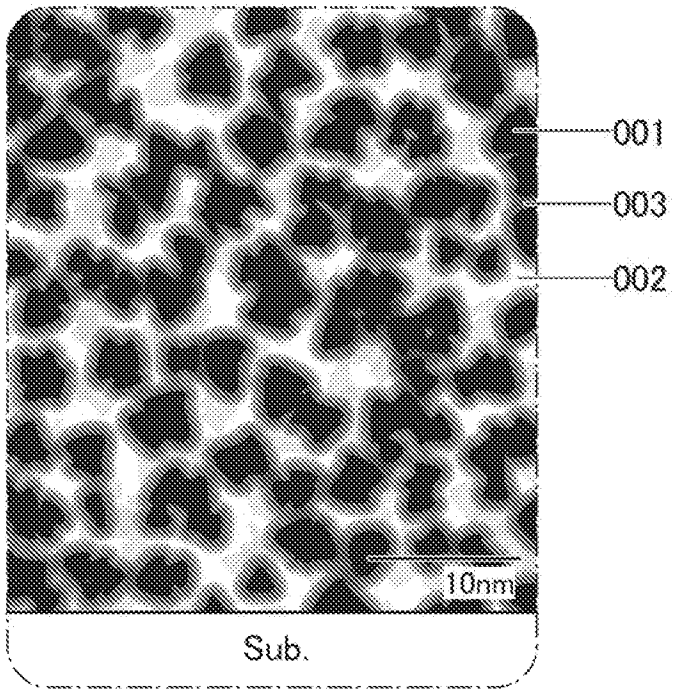


FIG. 3A

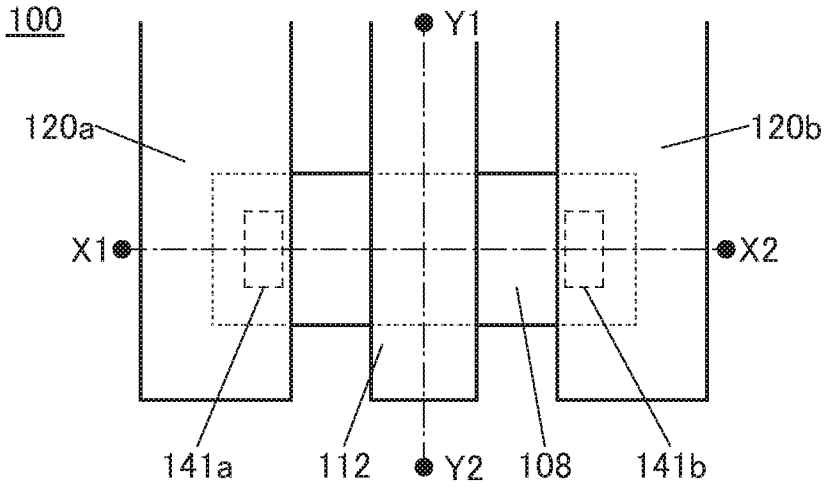


FIG. 3B

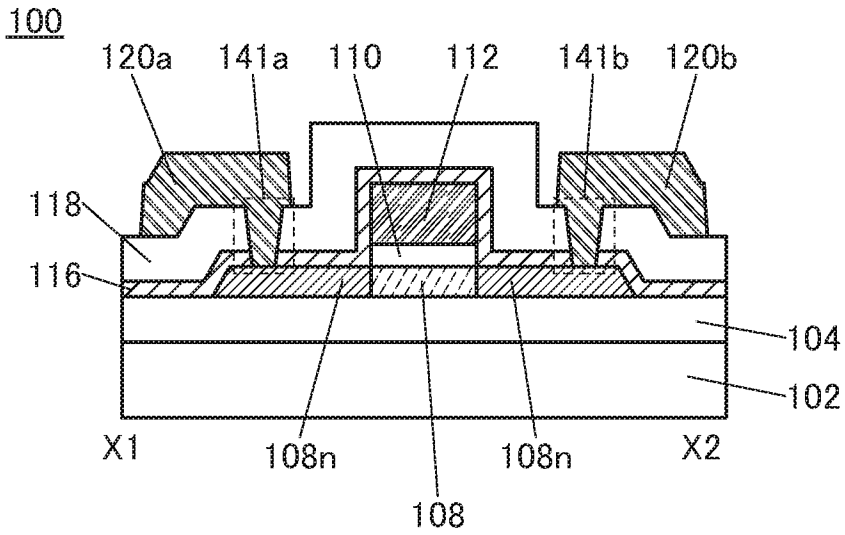


FIG. 3C

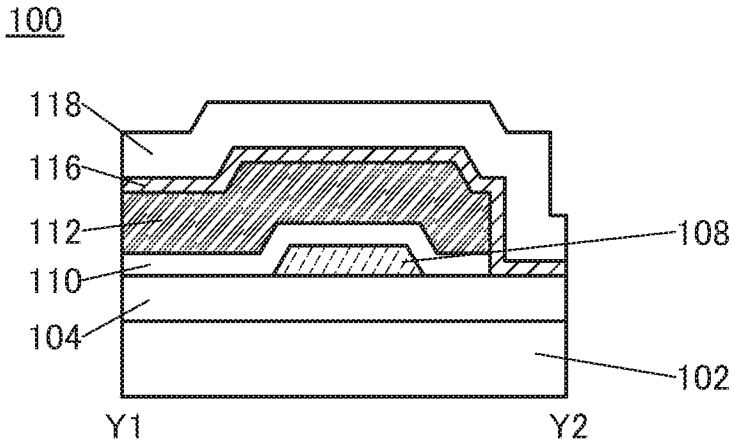


FIG. 4A

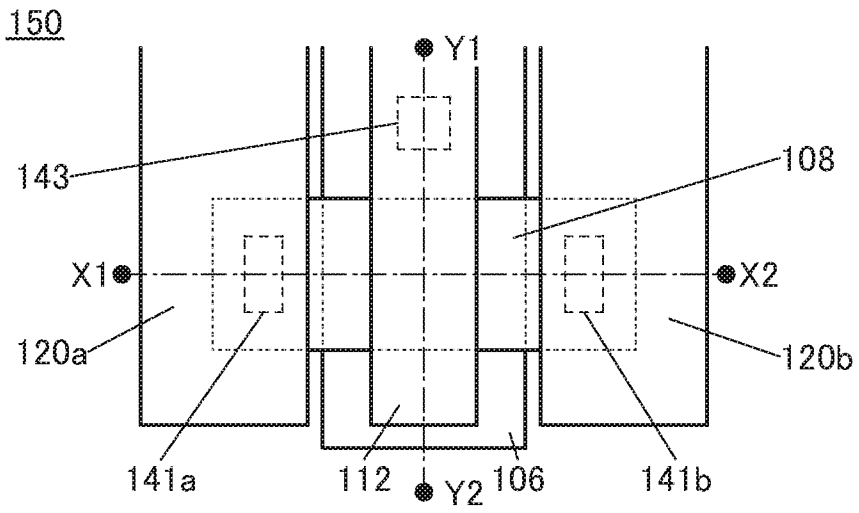


FIG. 4B

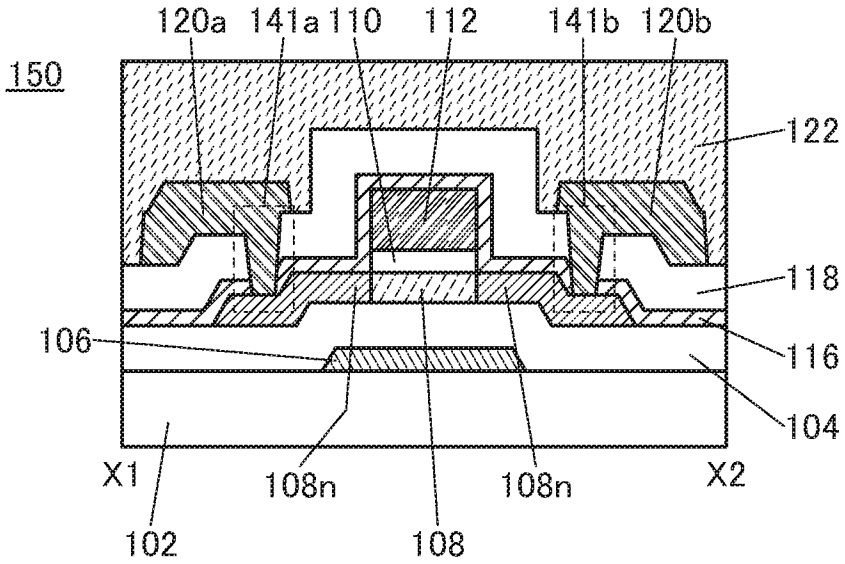


FIG. 4C

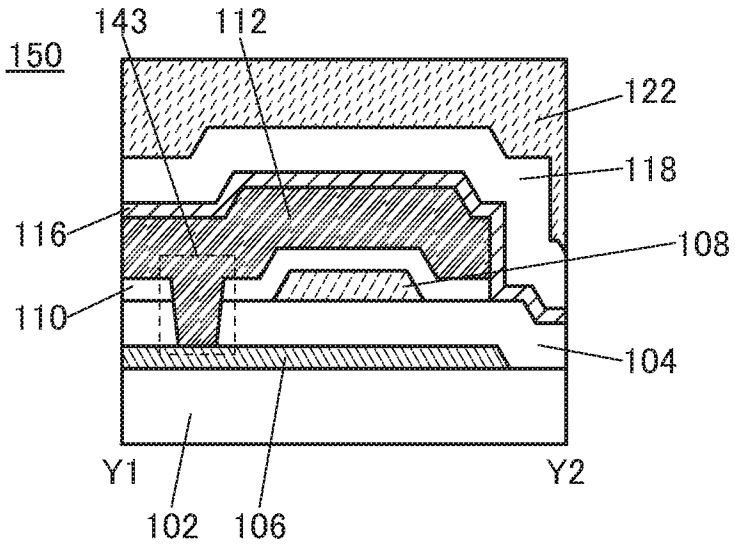


FIG. 5A

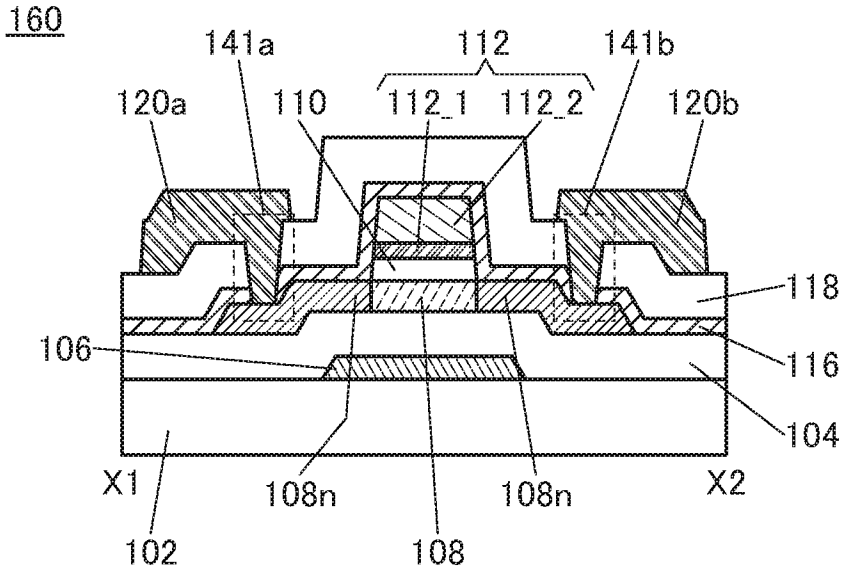

160
141a
112
141b
120a
110
112_1
112_2
120b
118
106
116
104
X1
108n
108n
X2
102
108

FIG. 5B

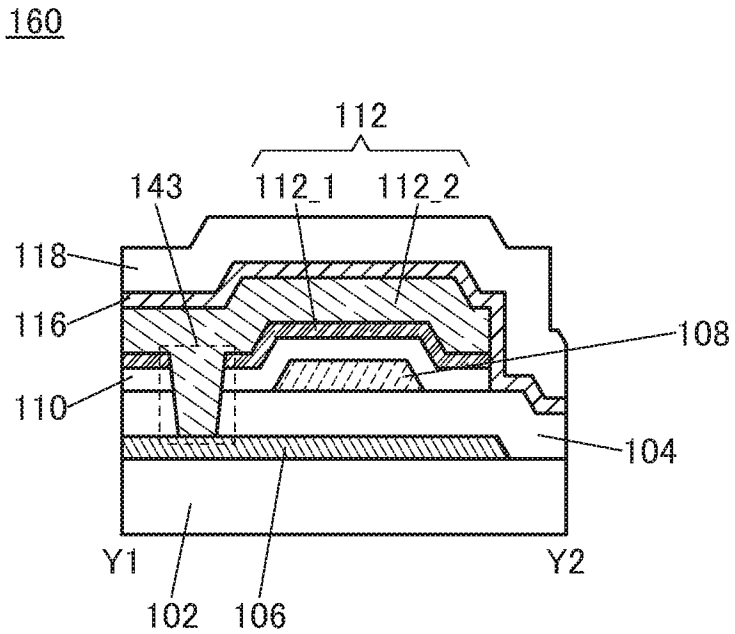

160
112
143
112_1
112_2
118
116
108
110
104
Y1
Y2
102
106

FIG. 6A

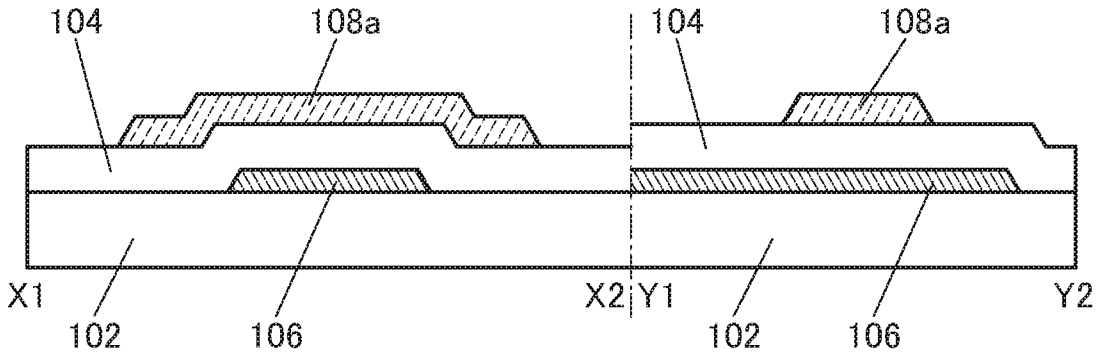


FIG. 6B

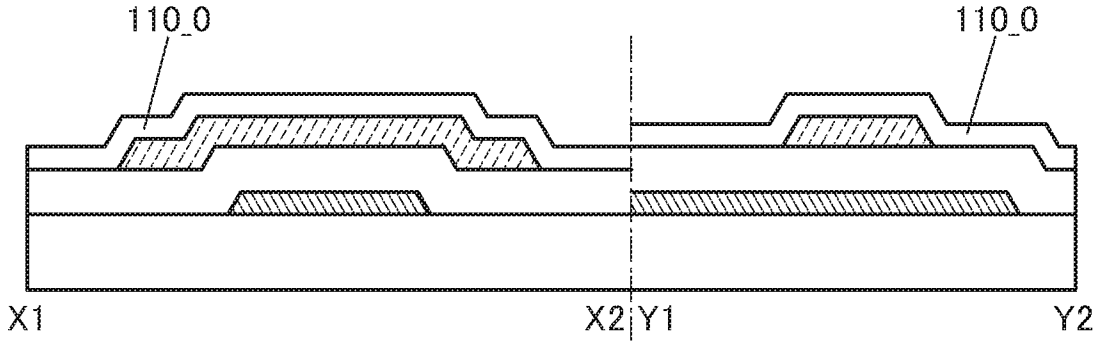


FIG. 6C

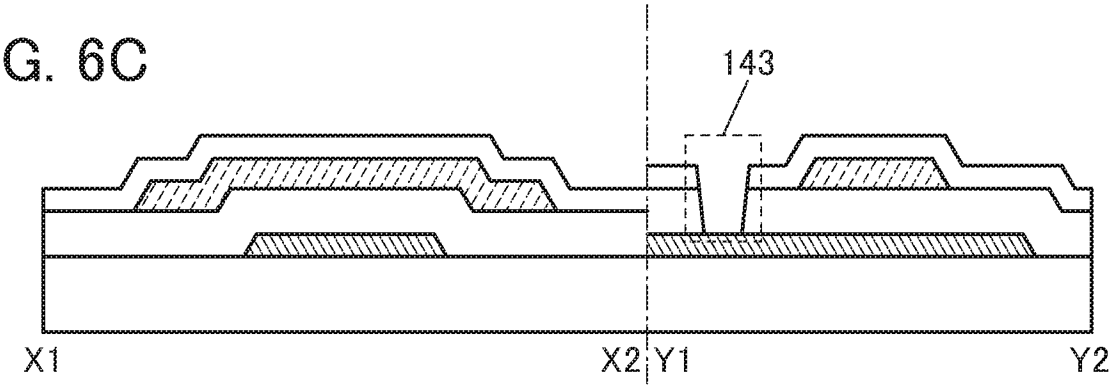


FIG. 6D

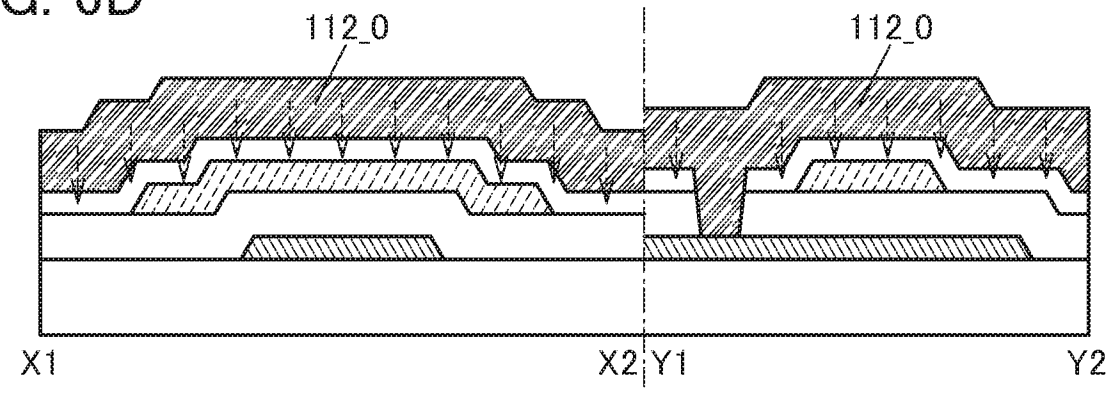


FIG. 7A

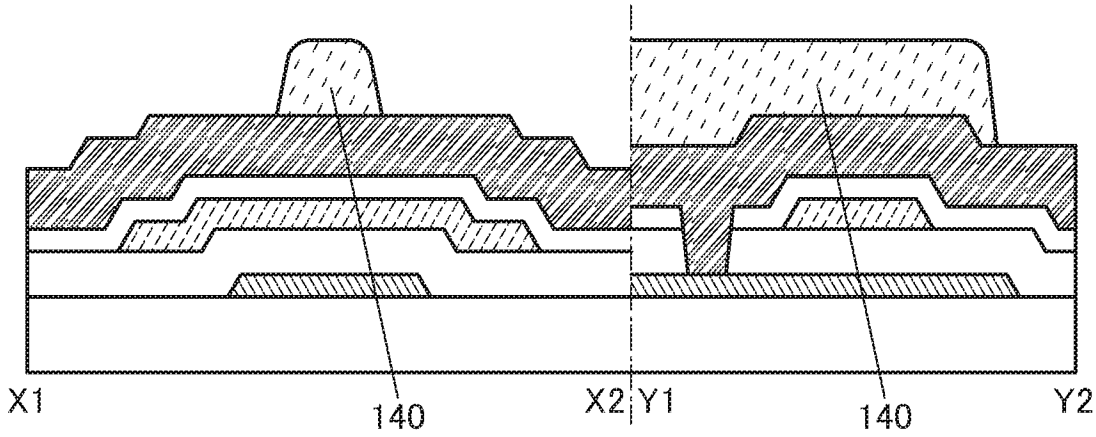


FIG. 7B

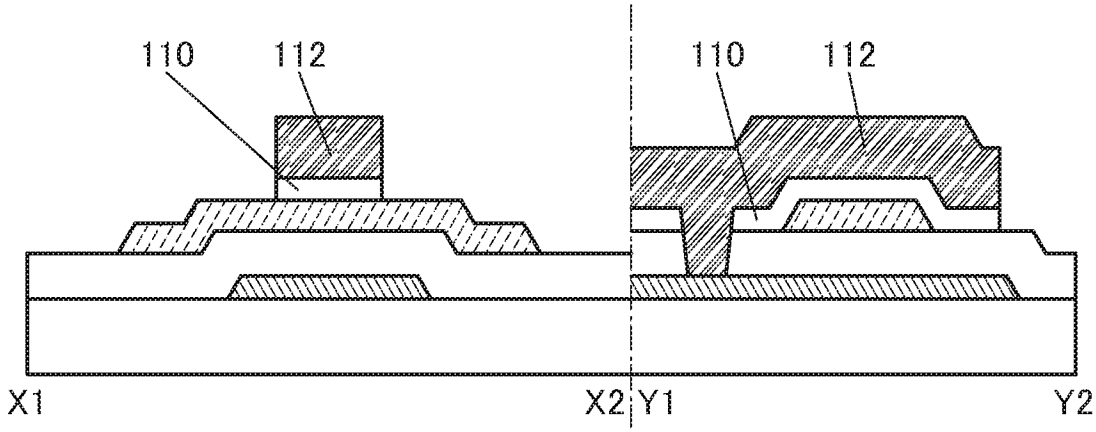


FIG. 7C

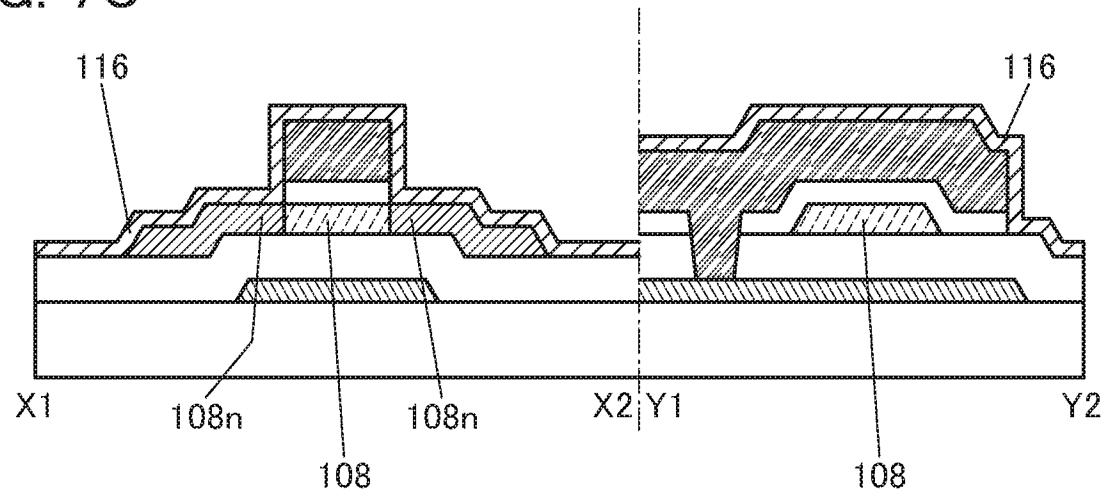


FIG. 8A

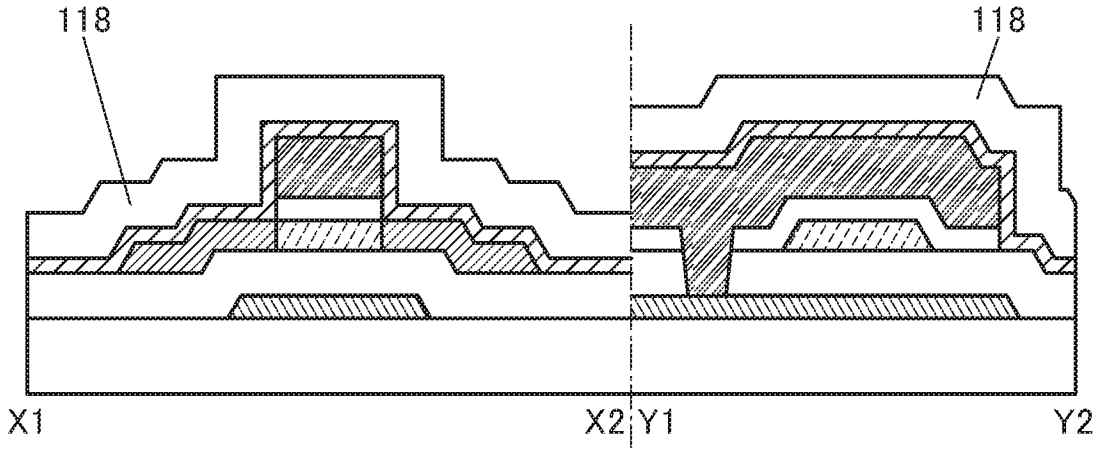


FIG. 8B

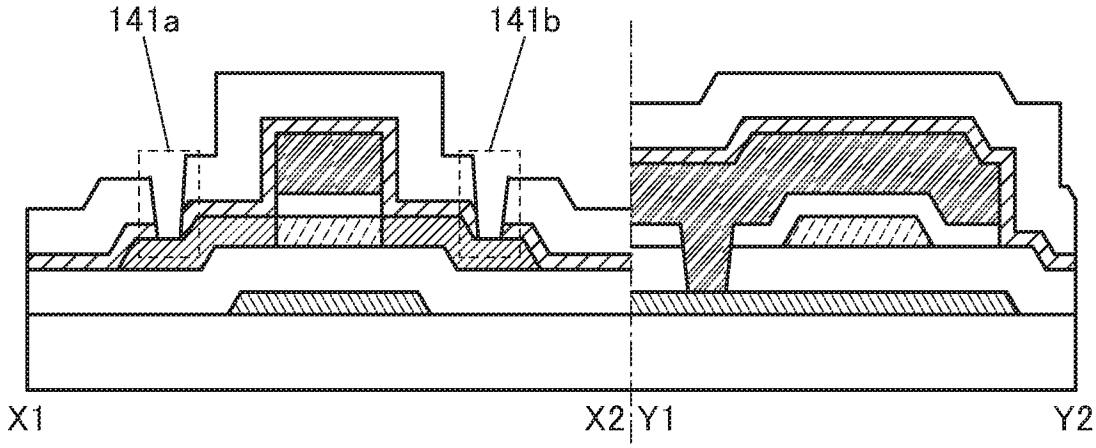


FIG. 8C

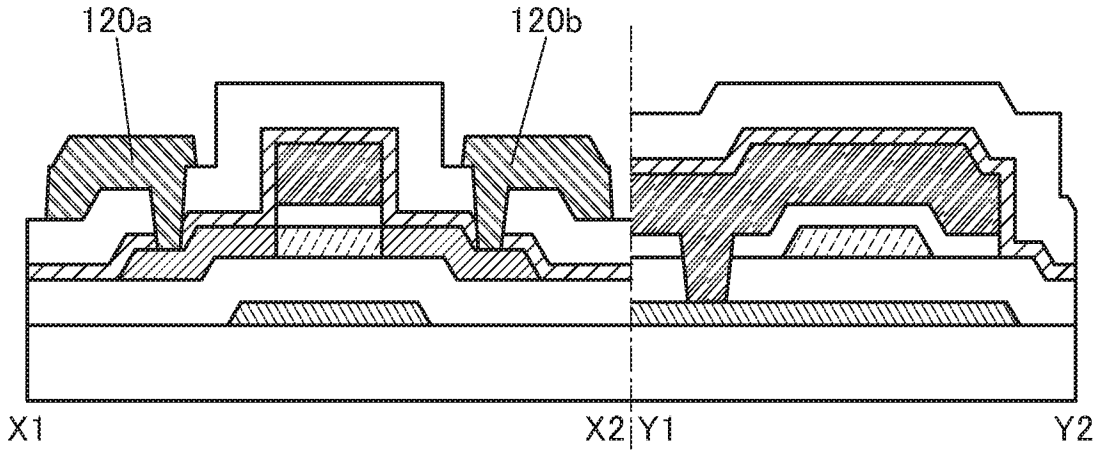


FIG. 9A

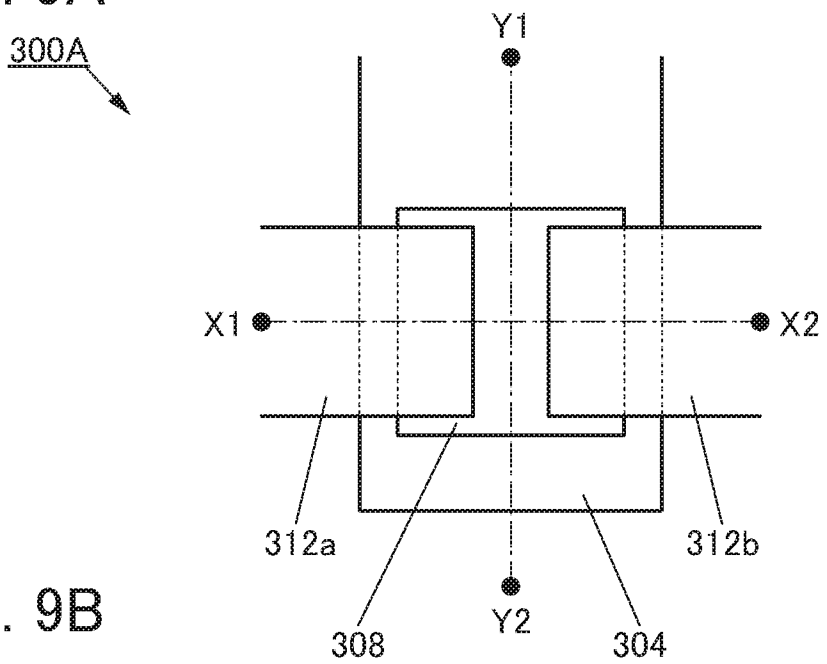


FIG. 9B

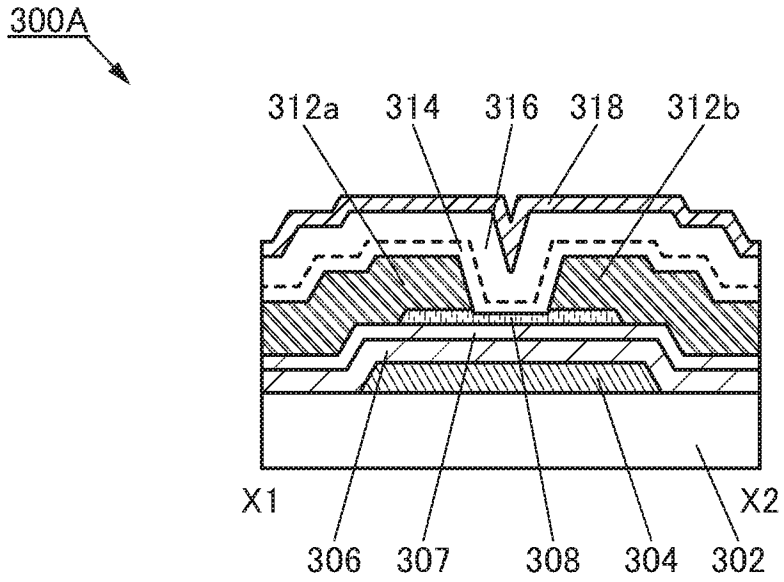


FIG. 9C

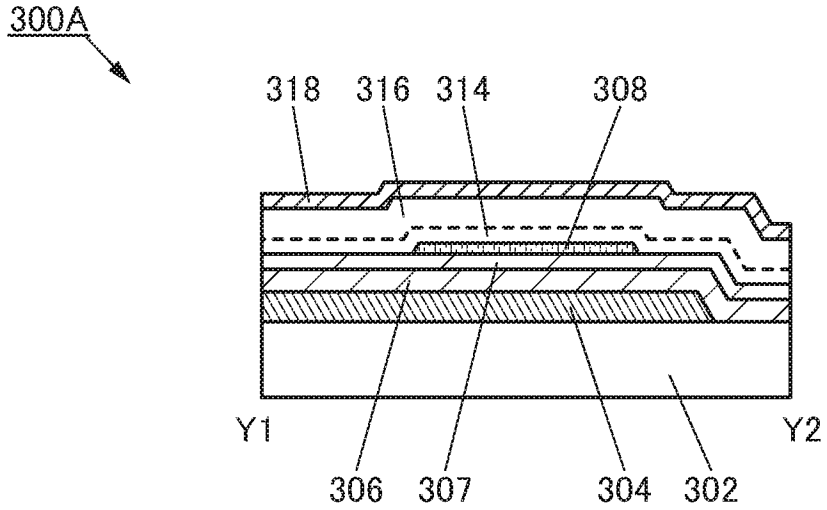


FIG. 10A

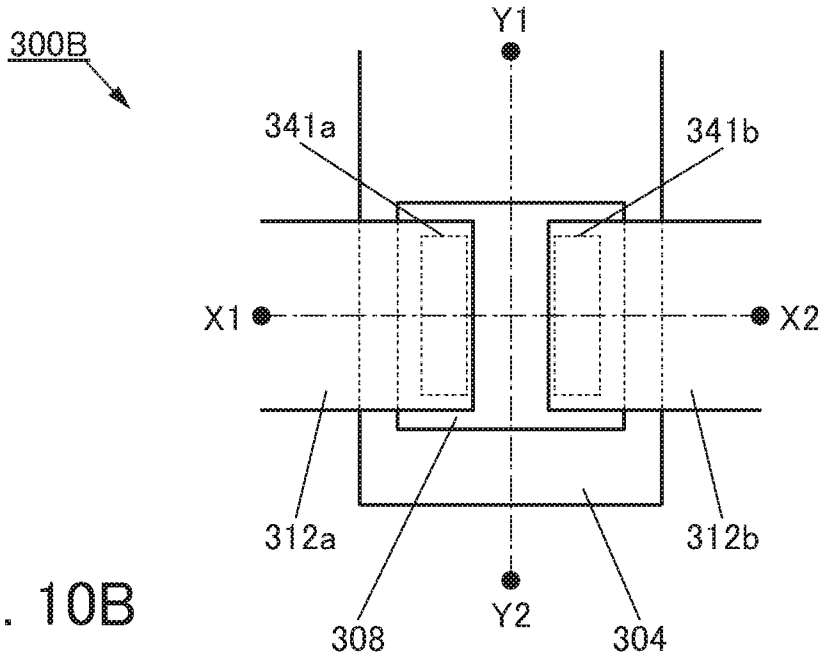


FIG. 10B

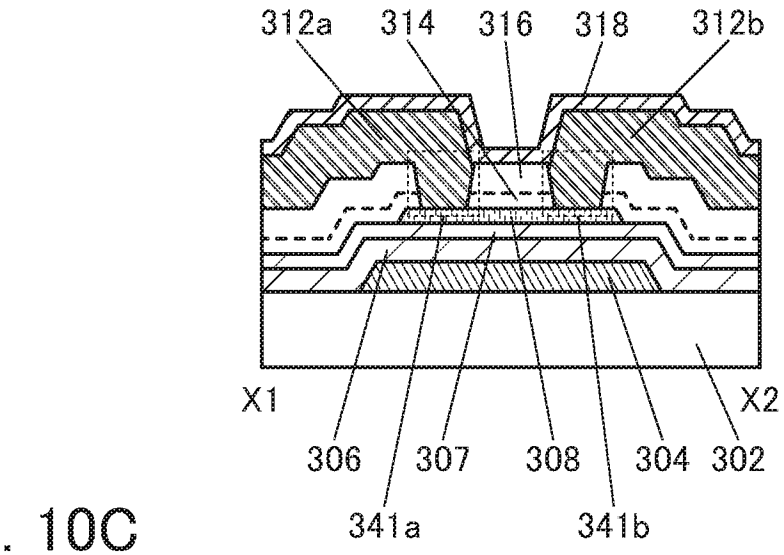


FIG. 10C

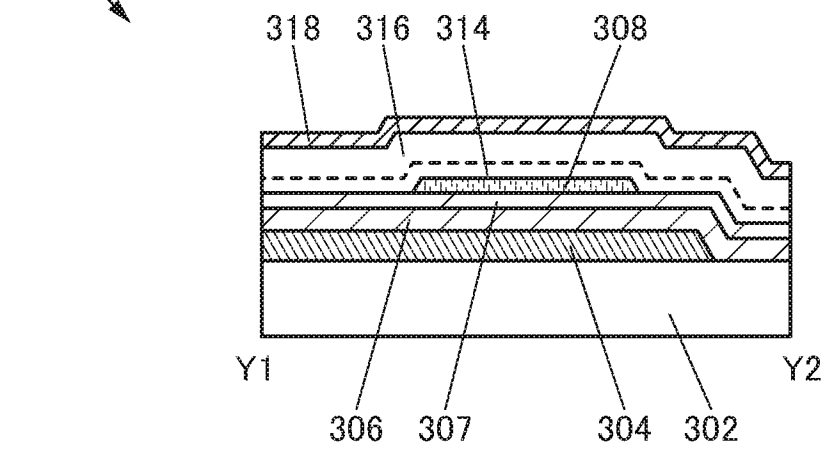


FIG. 11A

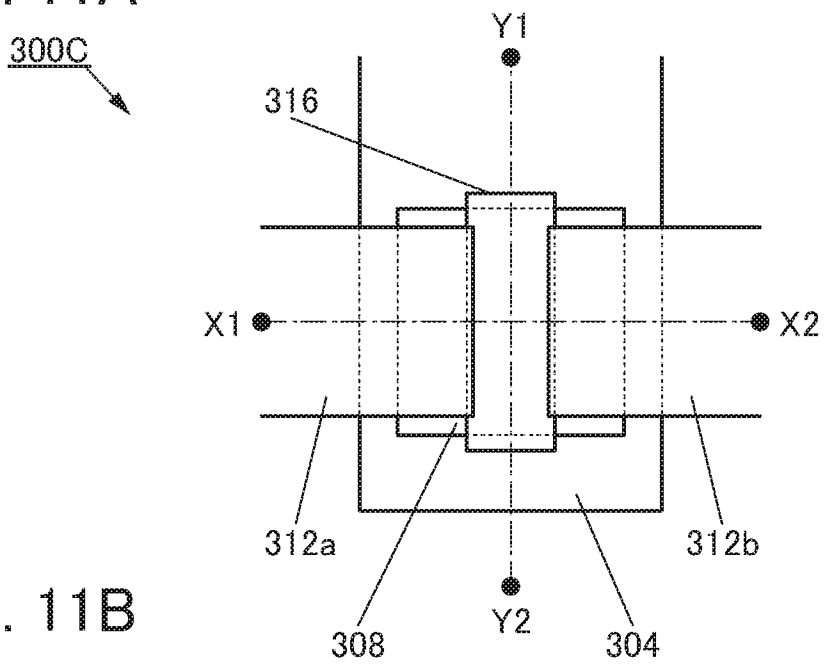


FIG. 11B

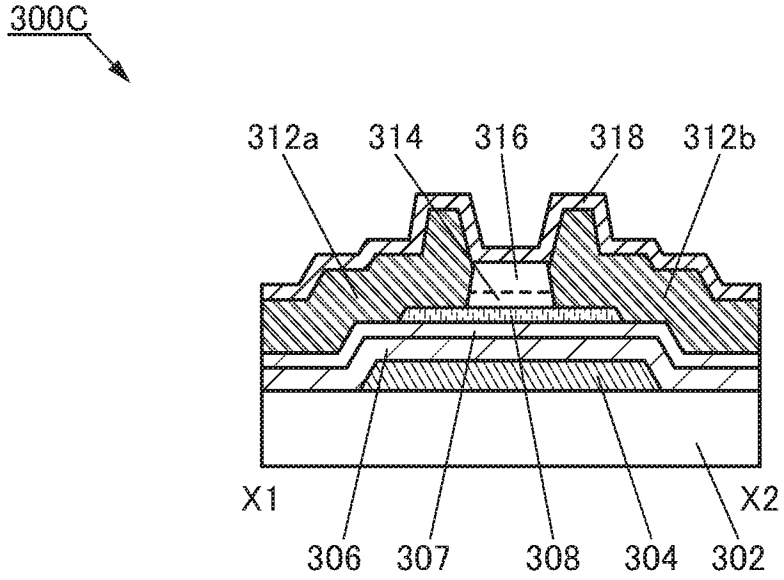


FIG. 11C

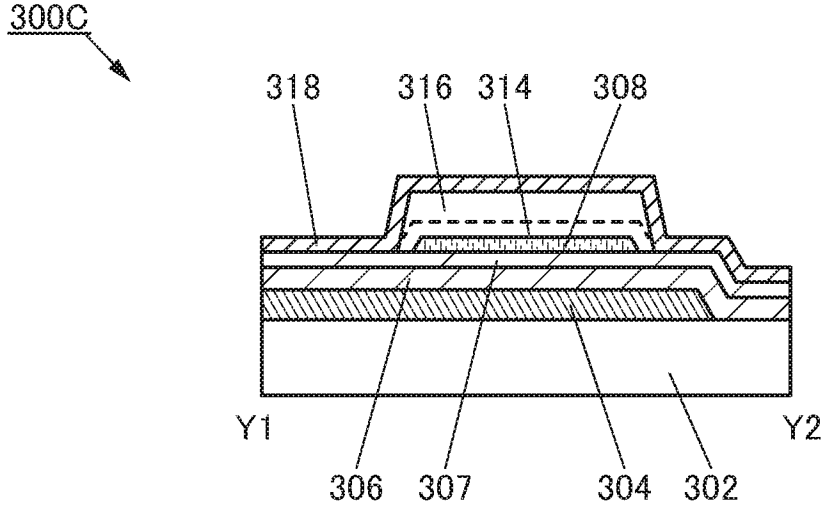


FIG. 12A

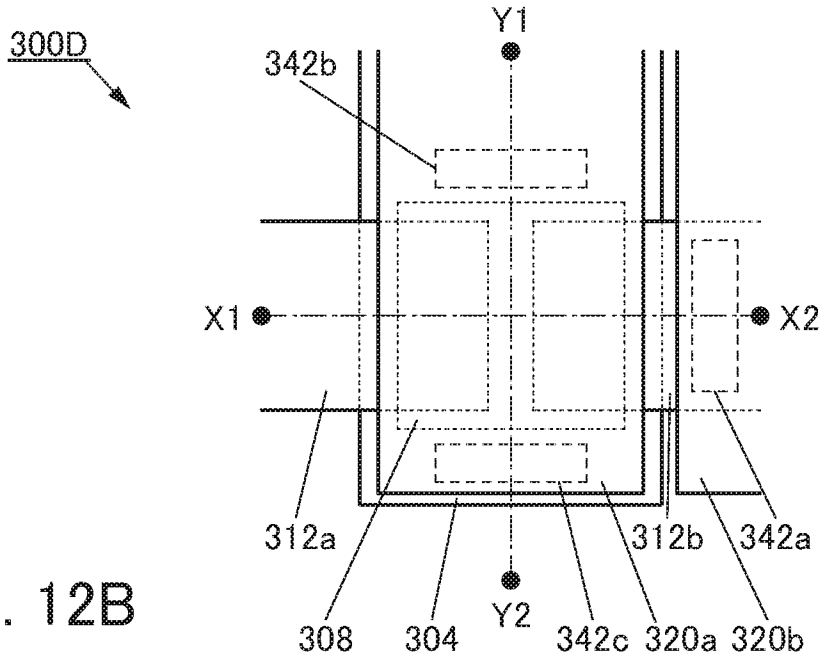


FIG. 12B

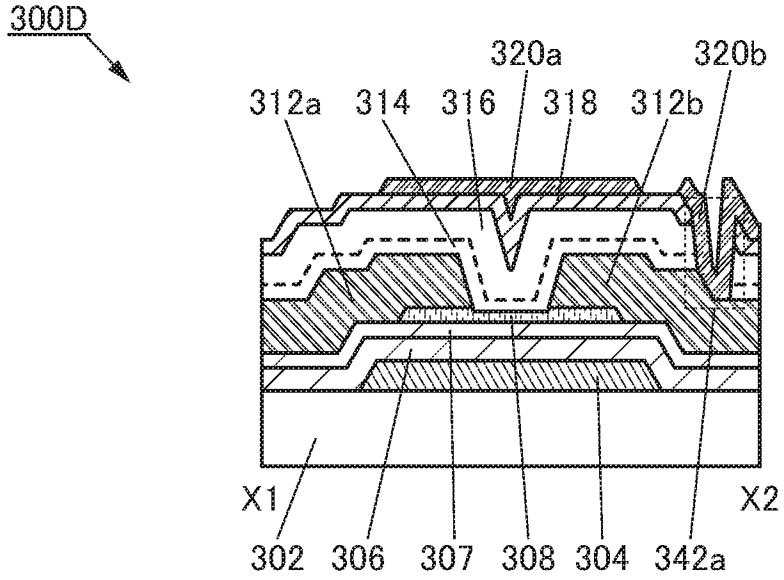


FIG. 12C

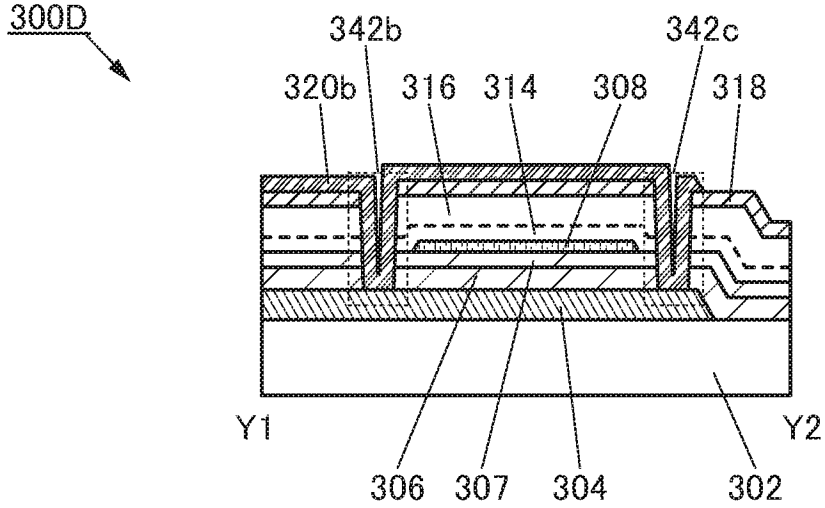


FIG. 13A

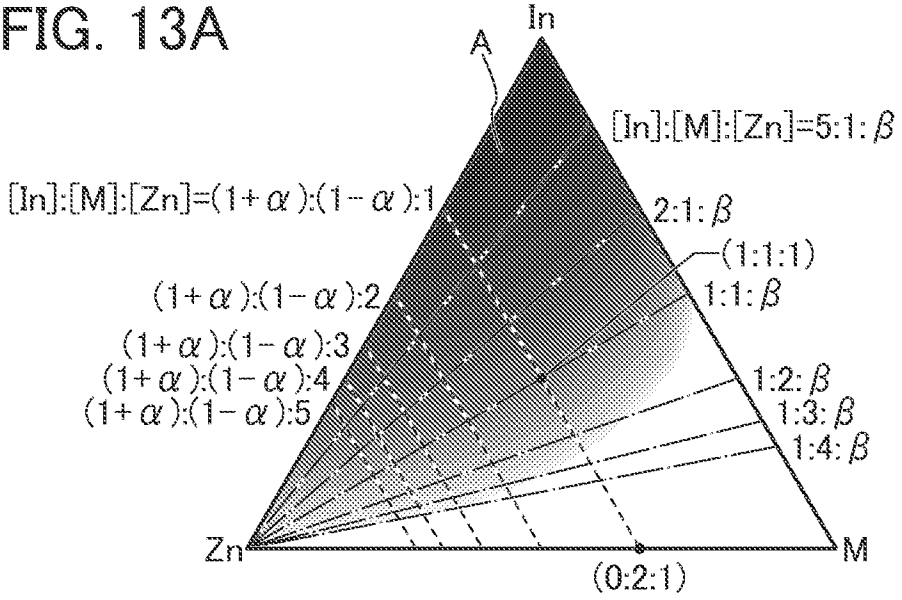


FIG. 13B

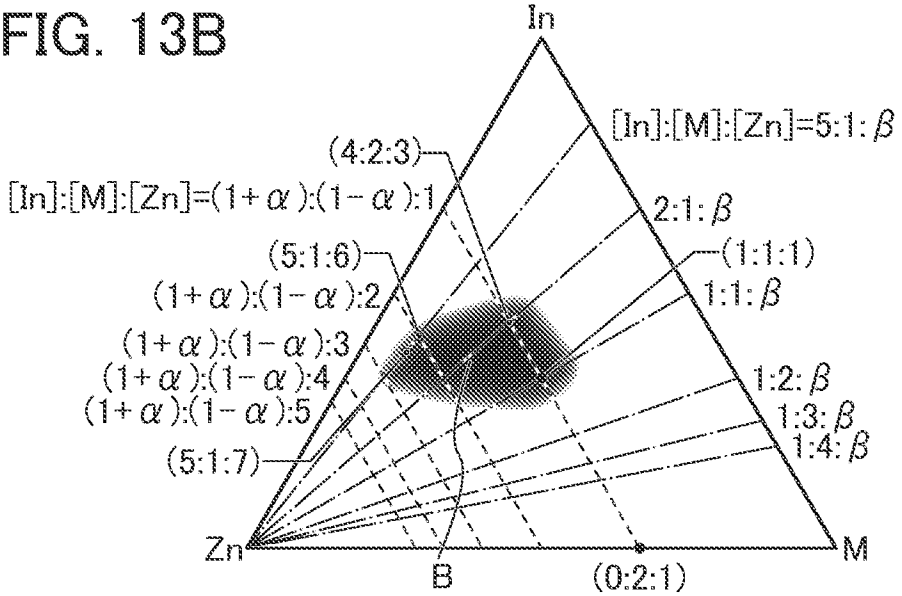


FIG. 13C

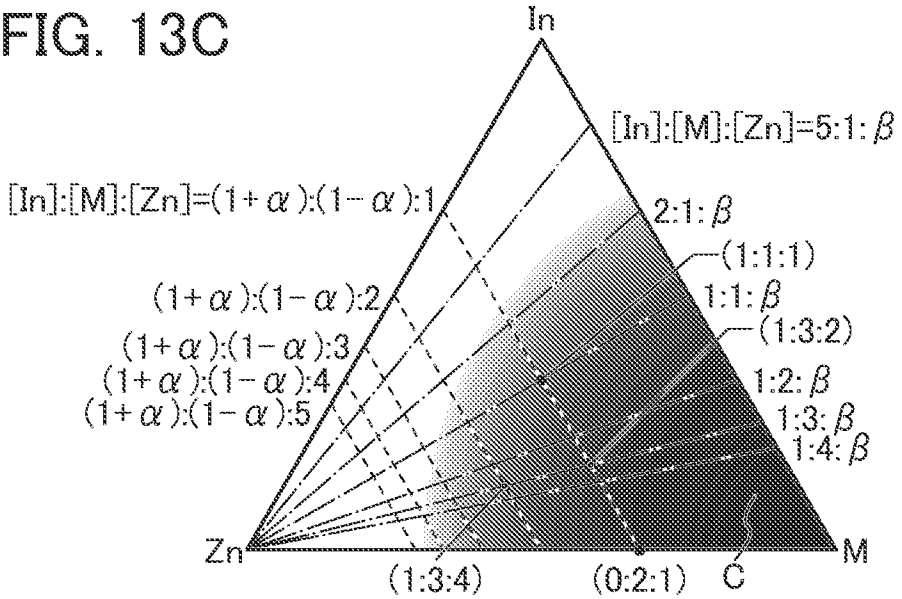


FIG. 14

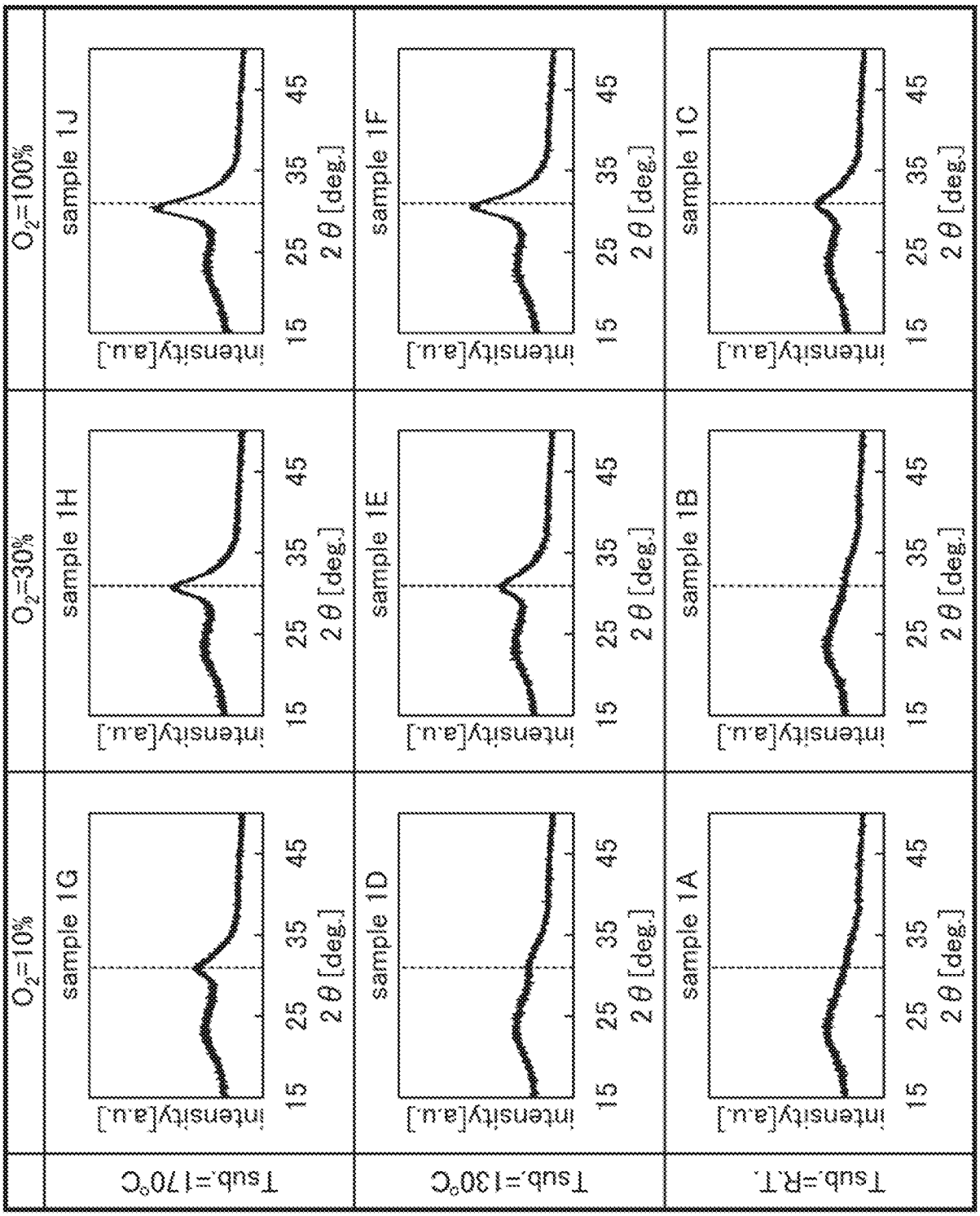

O_2=10%
O_2=30%
O_2=100%
$T_{sub.}$=R.T.
$T_{sub.}$=130°C
$T_{sub.}$=170°C
sample 1A
sample 1B
sample 1C
sample 1D
sample 1E
sample 1F
sample 1G
sample 1H
sample 1J
intensity[a.u.]
15 25 35 45
2θ [deg.]

FIG. 15A

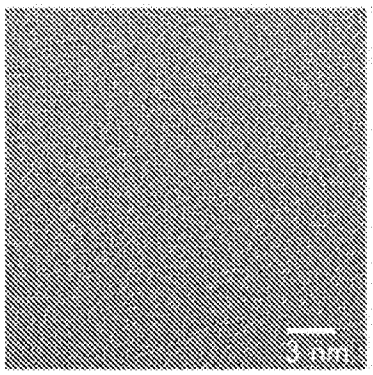


FIG. 15B

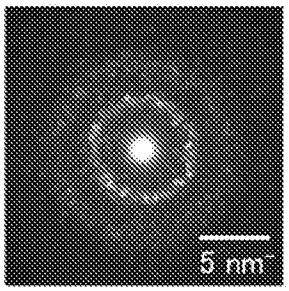


FIG. 15C

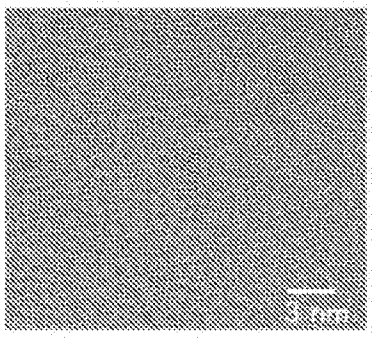


FIG. 15D

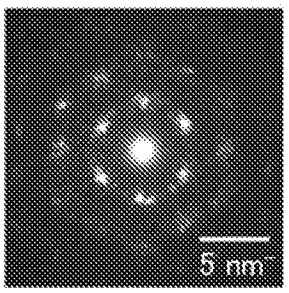


FIG. 15E

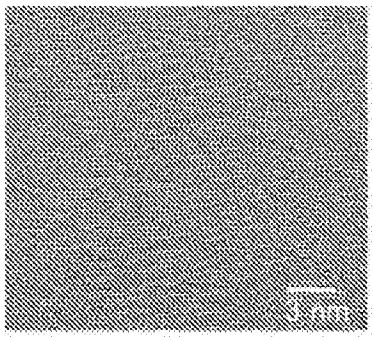


FIG. 15F

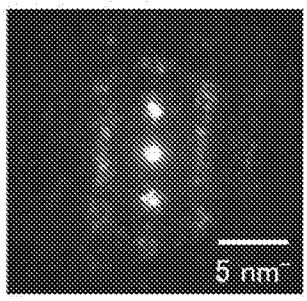


FIG. 16A

plan-view TEM image

FIG. 16B

cross-sectional TEM image

FIG. 16C

FIG. 16D

FIG. 16E

FIG. 16F

FIG. 16G

FIG. 16H

FIG. 16I

FIG. 16J

FIG. 16K

FIG. 16L

FIG. 17

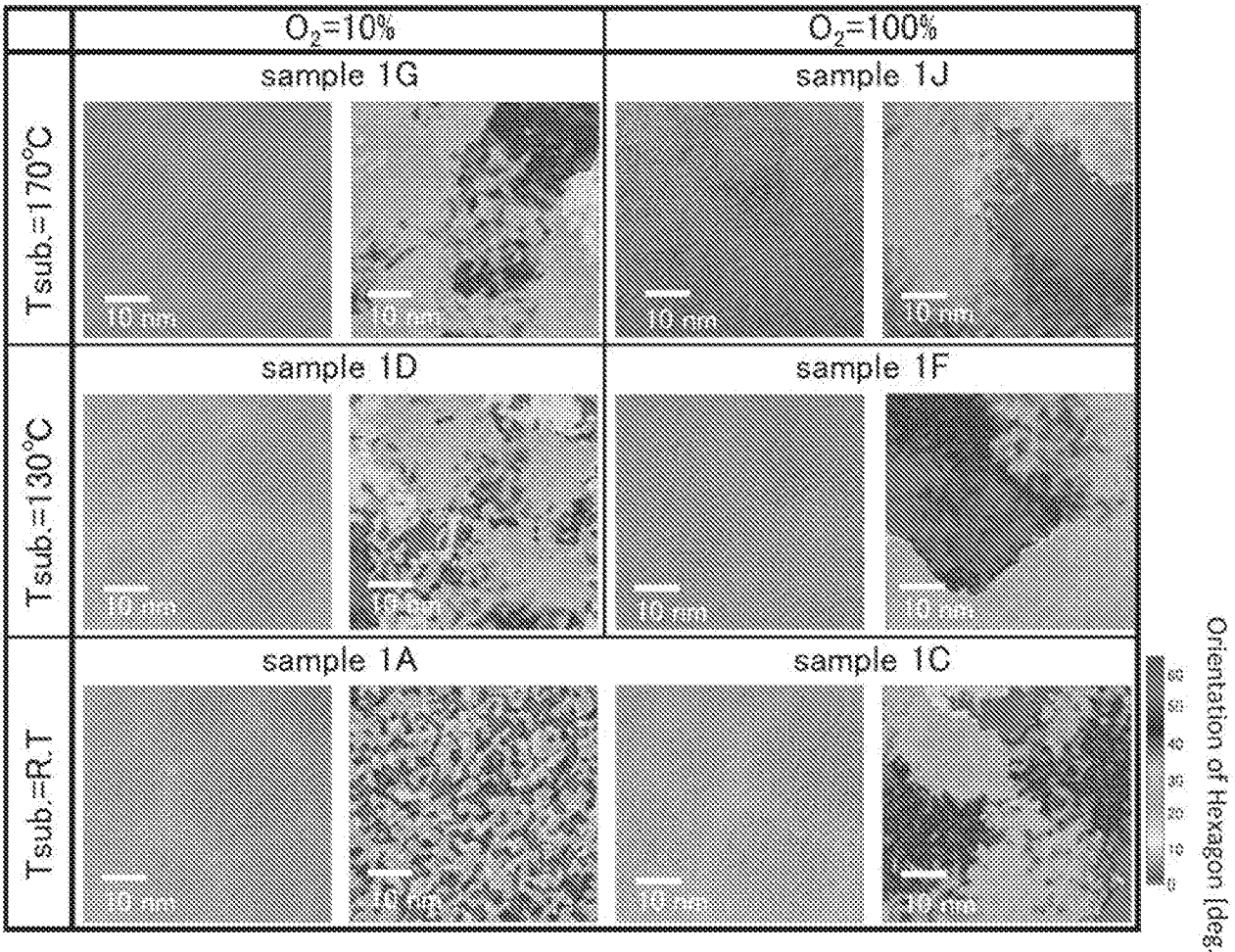

O2=10%
O2=100%
Tsub.=170°C
Tsub.=130°C
Tsub.=R.T
sample 1G
sample 1J
sample 1D
sample 1F
sample 1A
sample 1C
10 nm
Orientation of Hexagon [deg.]

FIG. 18A

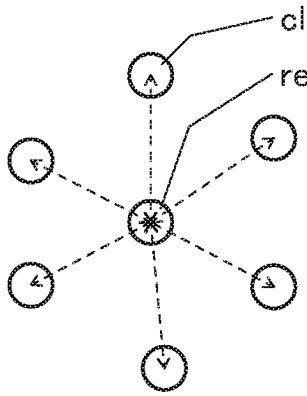


FIG. 18B

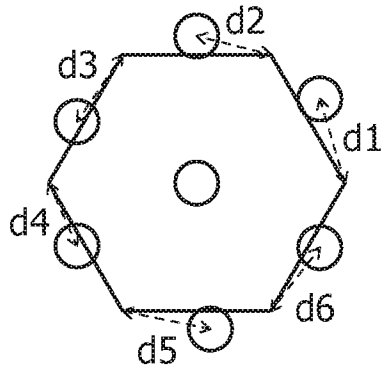


FIG. 18C

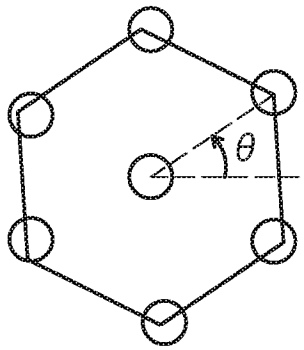


FIG. 18D

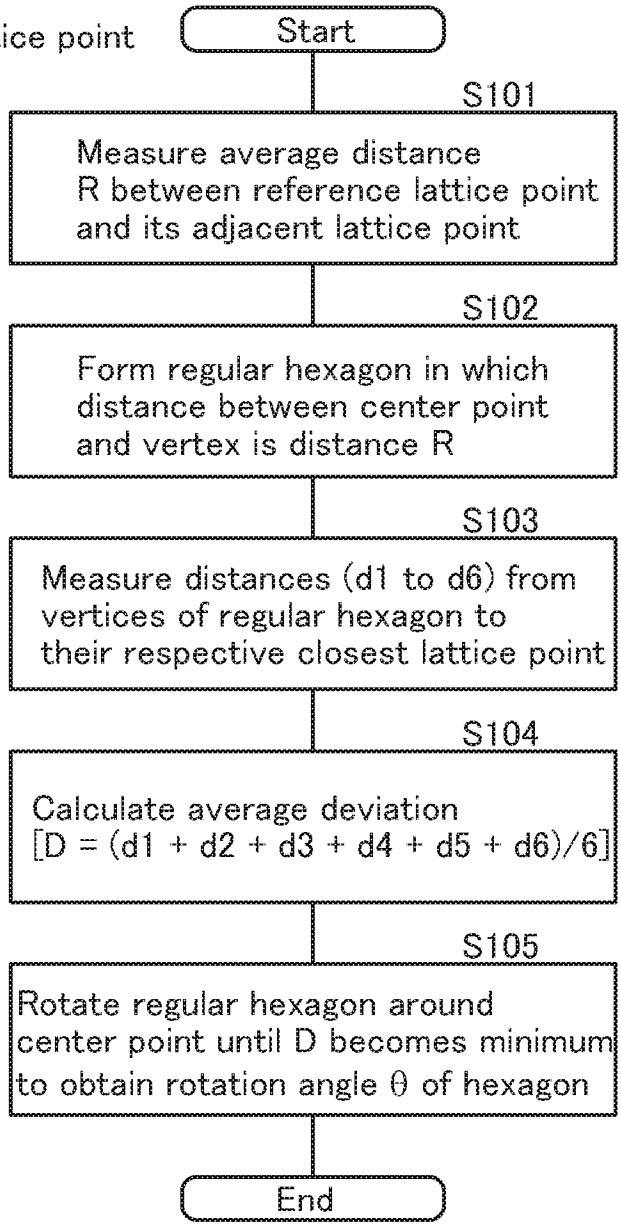


FIG. 19A

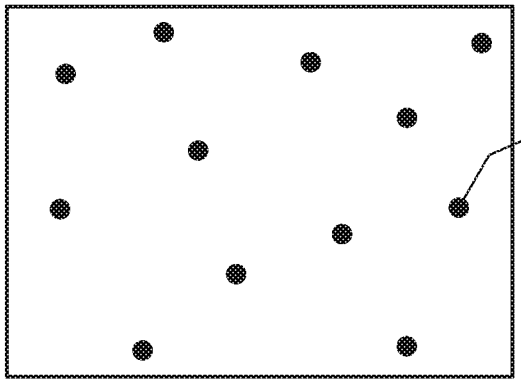


FIG. 19B

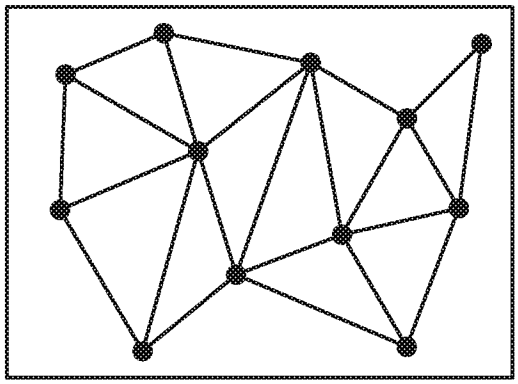


FIG. 19C

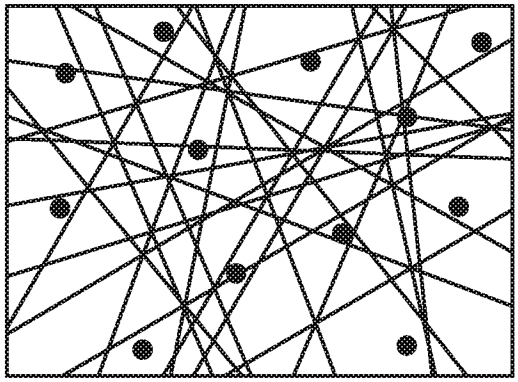


FIG. 19D

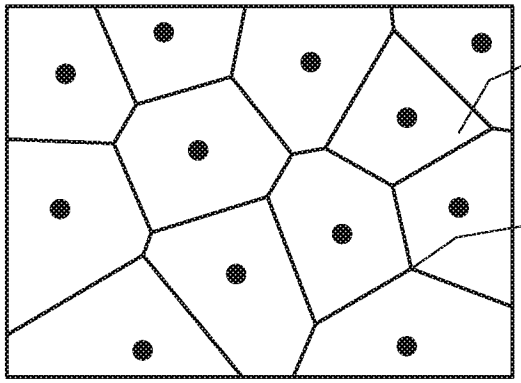


FIG. 19E

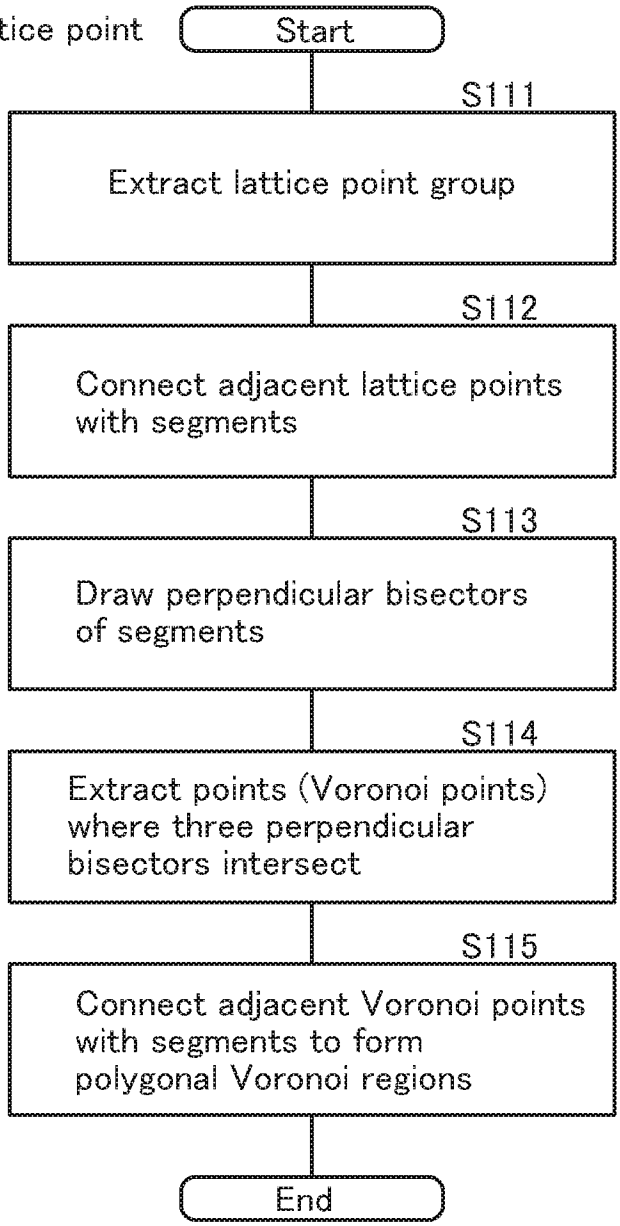
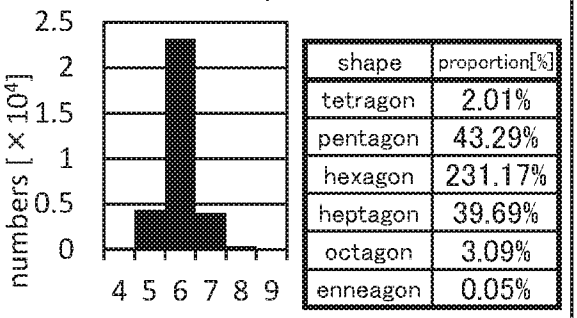
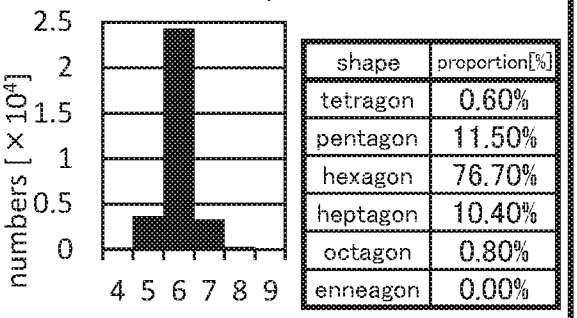


FIG. 20

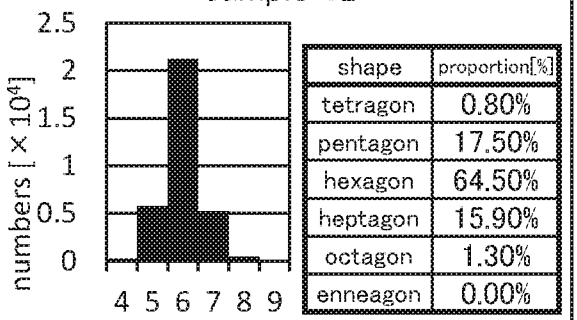
	O_2=10%	O_2=100%
Tsub.=170°C	sample 1G	sample 1J
Tsub.=130°C	sample 1D	sample 1F
Tsub.=R.T.	sample 1A	sample 1C



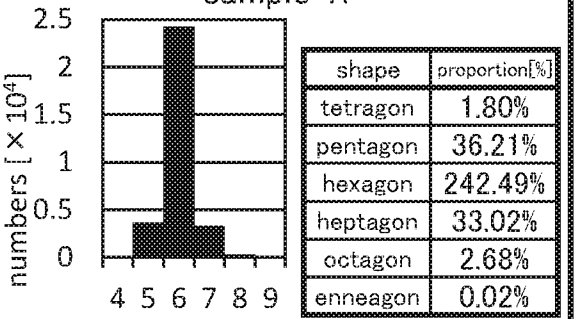
shape	proportion[%]
tetragon	2.01%
pentagon	43.29%
hexagon	231.17%
heptagon	39.69%
octagon	3.09%
enneagon	0.05%



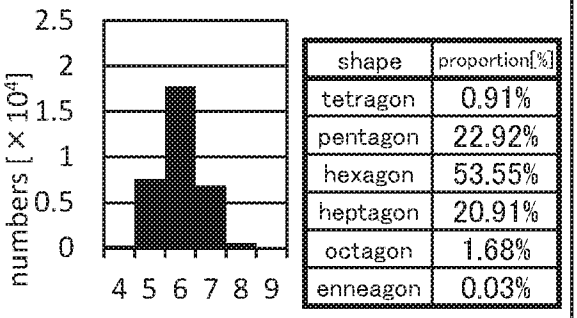
shape	proportion[%]
tetragon	0.60%
pentagon	11.50%
hexagon	76.70%
heptagon	10.40%
octagon	0.80%
enneagon	0.00%



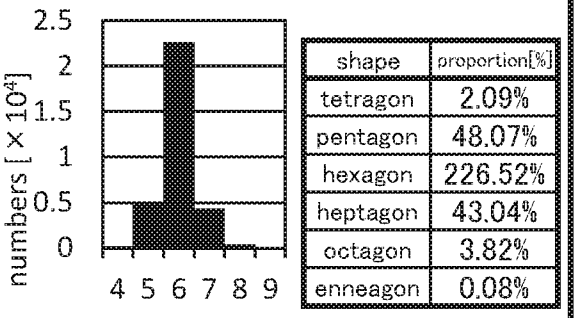
shape	proportion[%]
tetragon	0.80%
pentagon	17.50%
hexagon	64.50%
heptagon	15.90%
octagon	1.30%
enneagon	0.00%



shape	proportion[%]
tetragon	1.80%
pentagon	36.21%
hexagon	242.49%
heptagon	33.02%
octagon	2.68%
enneagon	0.02%



shape	proportion[%]
tetragon	0.91%
pentagon	22.92%
hexagon	53.55%
heptagon	20.91%
octagon	1.68%
enneagon	0.03%



shape	proportion[%]
tetragon	2.09%
pentagon	48.07%
hexagon	226.52%
heptagon	43.04%
octagon	3.82%
enneagon	0.08%

FIG. 21A

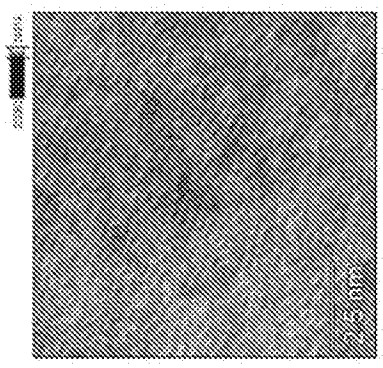


FIG. 21B

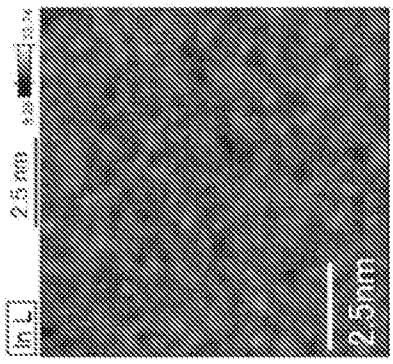


FIG. 21C

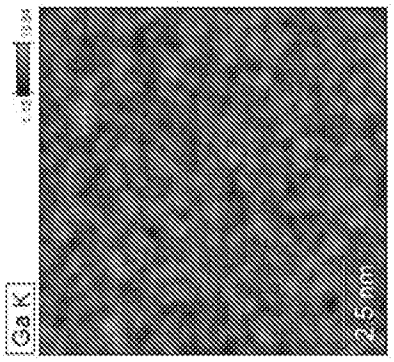


FIG. 21D

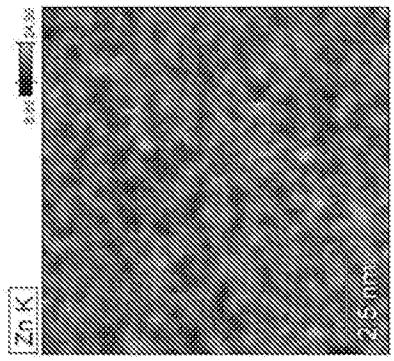


FIG. 21E

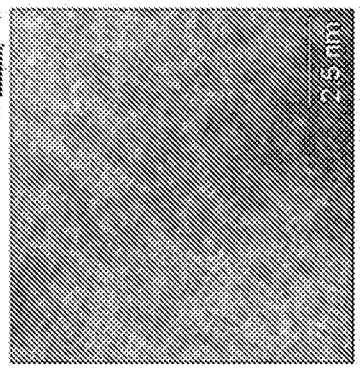


FIG. 21F

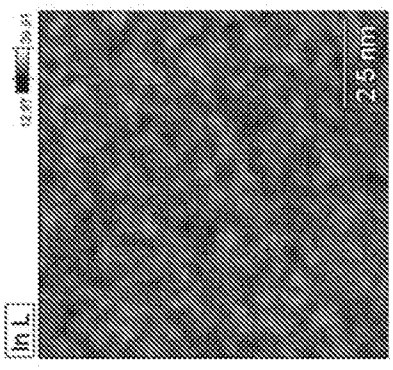


FIG. 21G

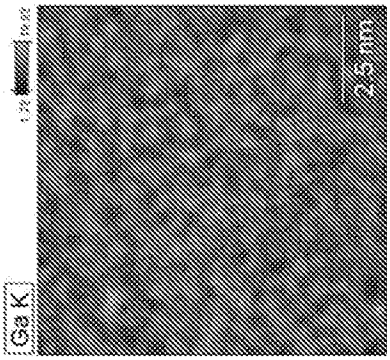


FIG. 21H

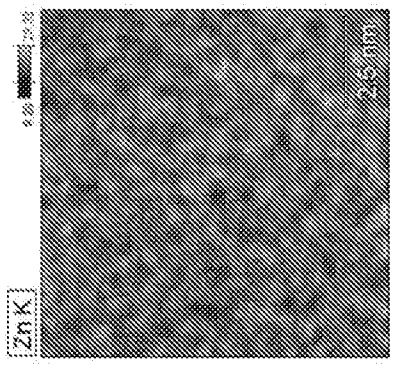


FIG. 22A

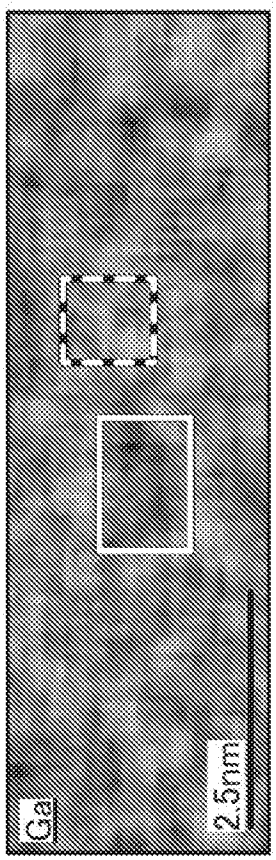


FIG. 22B

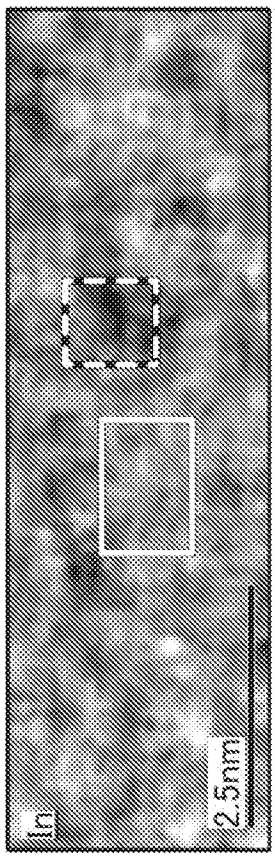


FIG. 22C

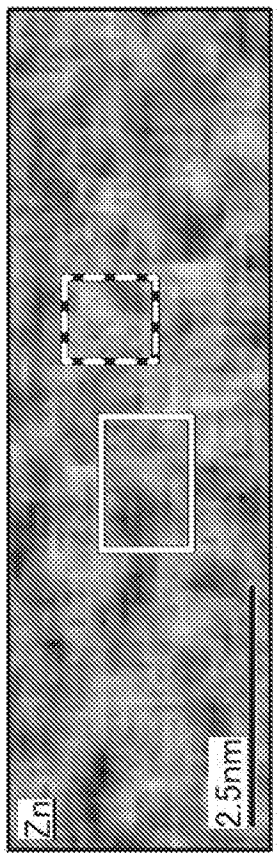


FIG. 23

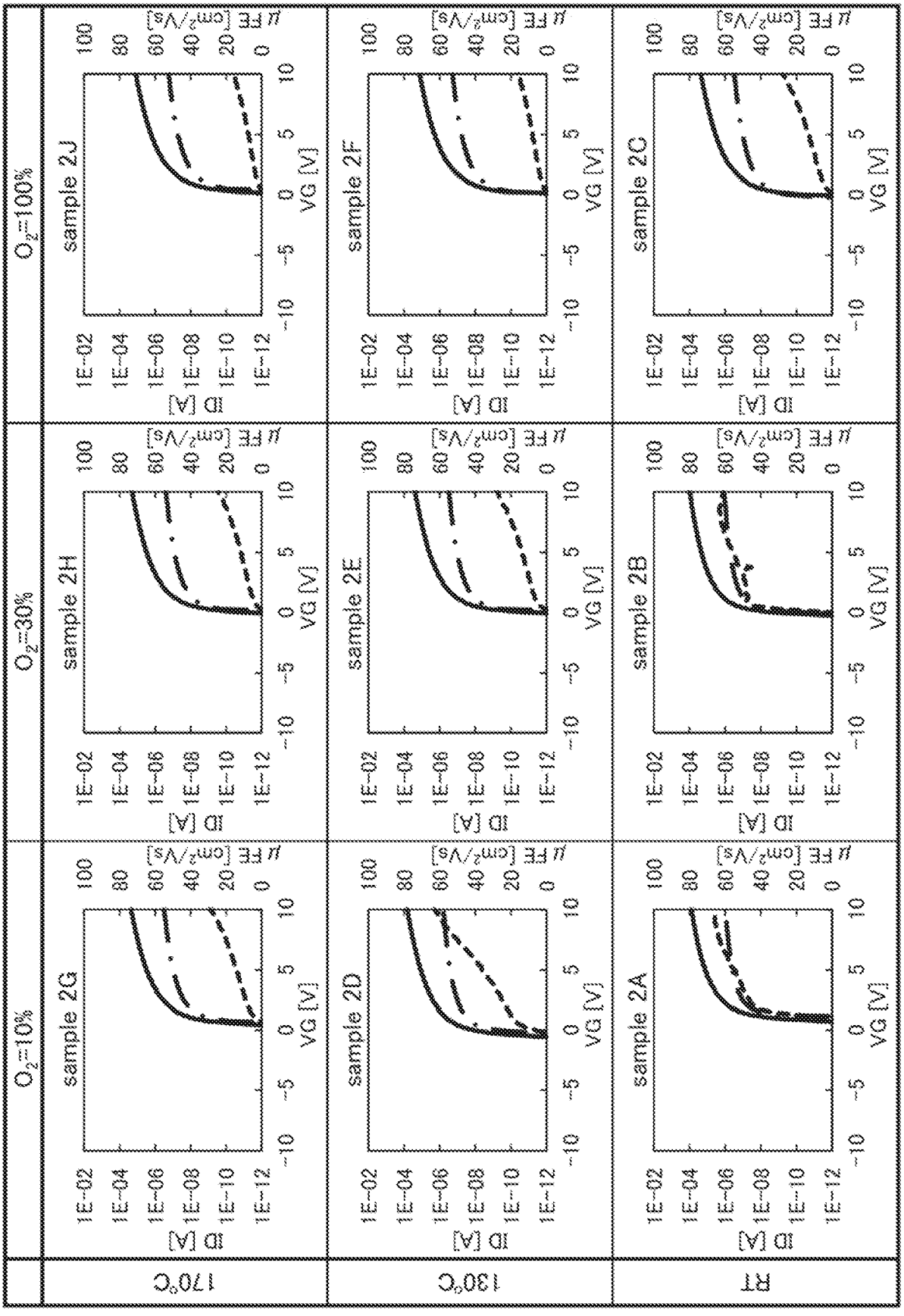

RT
130°C
170°C
O2=10%
O2=30%
O2=100%
sample 2A
sample 2B
sample 2C
sample 2D
sample 2E
sample 2F
sample 2G
sample 2H
sample 2J
ID [A]
μ FE [cm²/Vs]
VG [V]

FIG. 24

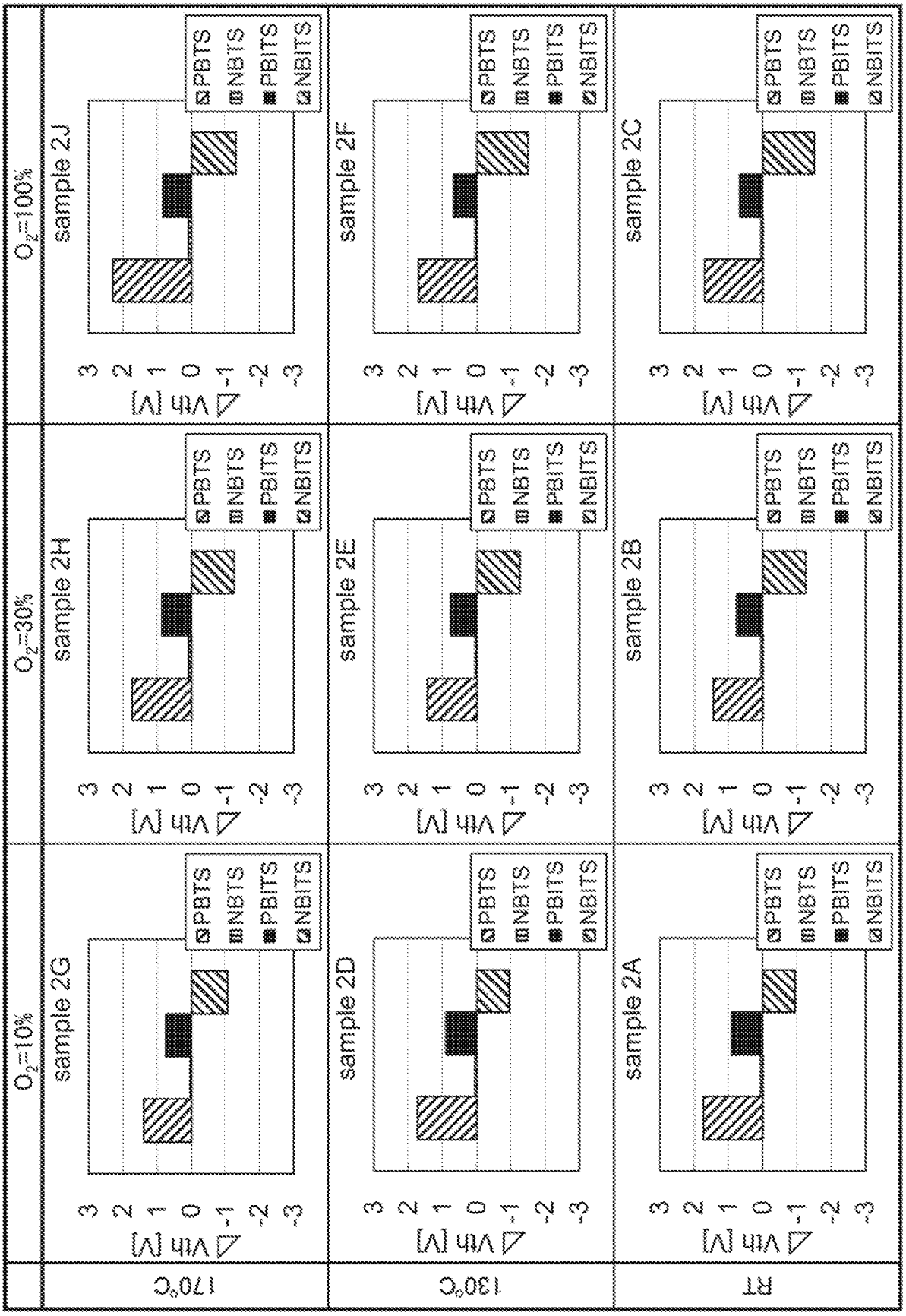

RT
130°C
170°C
O2=10%
O2=30%
O2=100%
sample 2A
sample 2B
sample 2C
sample 2D
sample 2E
sample 2F
sample 2G
sample 2H
sample 2J
PBTS
NBTS
PBITS
NBITS
ΔVth [V]
3
2
1
0
-1
-2
-3

FIG. 25A

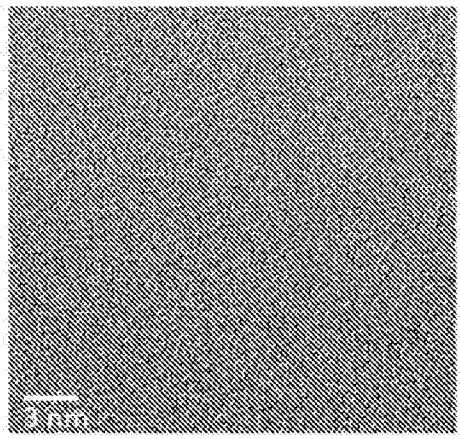


FIG. 25B

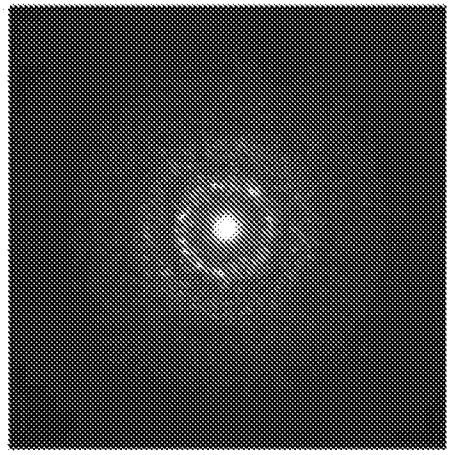


FIG. 25C

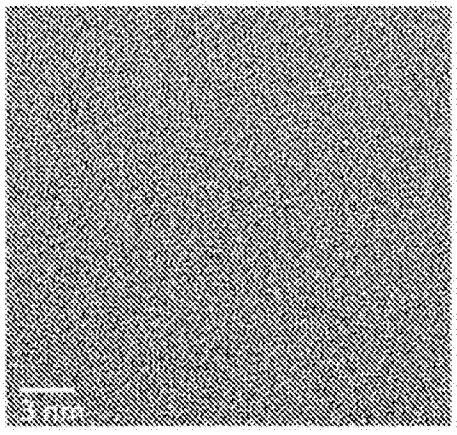


FIG. 25D

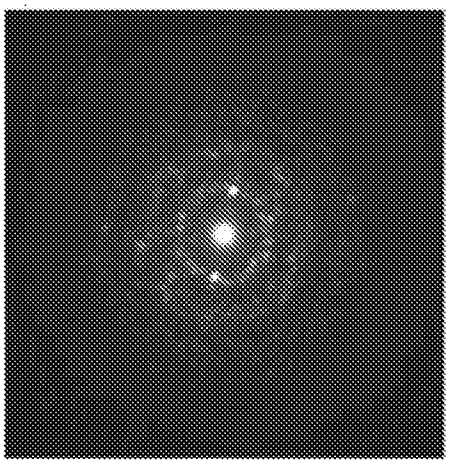


FIG. 25E

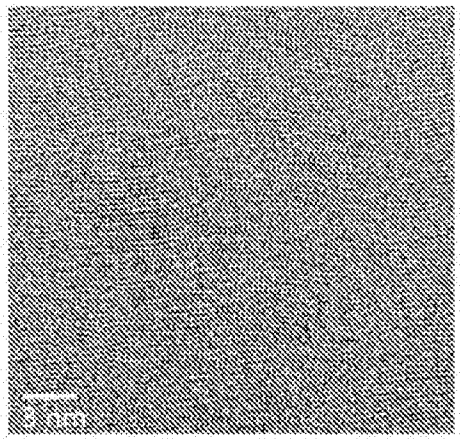


FIG. 25F

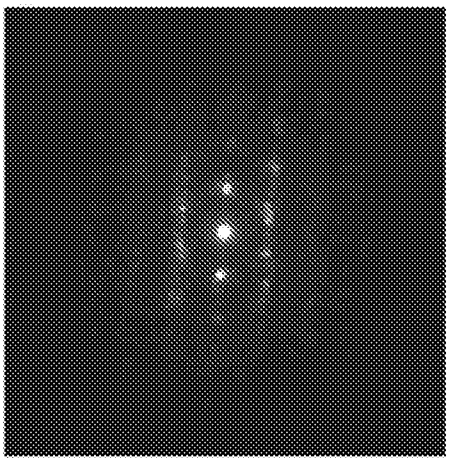


FIG. 26A

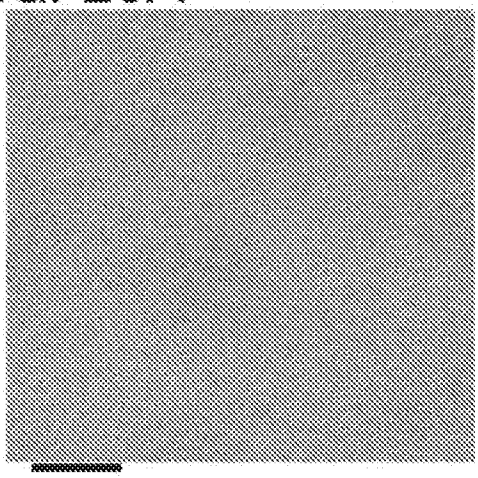


FIG. 26B

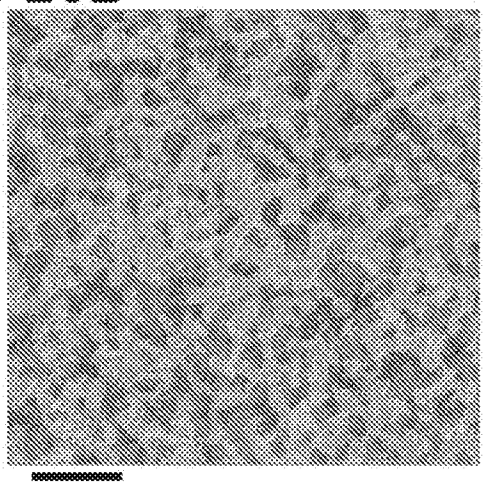


FIG. 26C

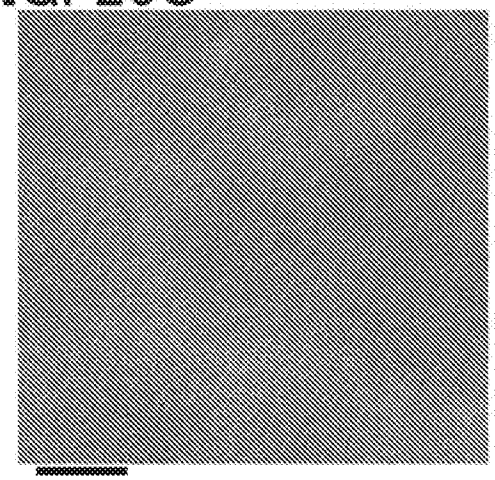


FIG. 26D

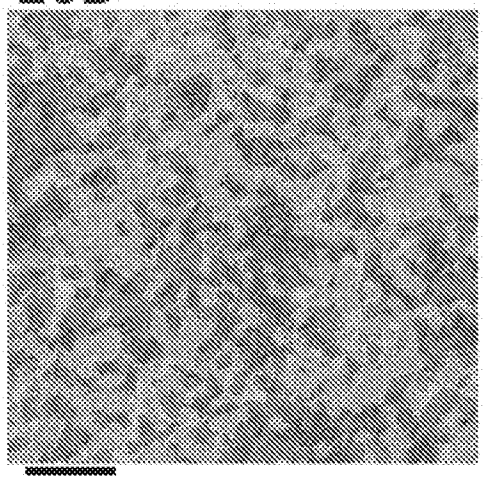


FIG. 26E

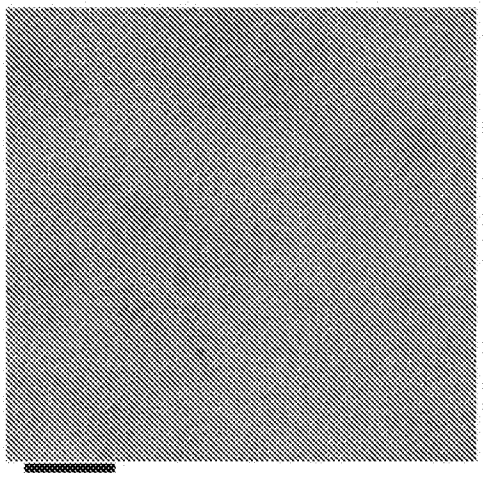


FIG. 26F

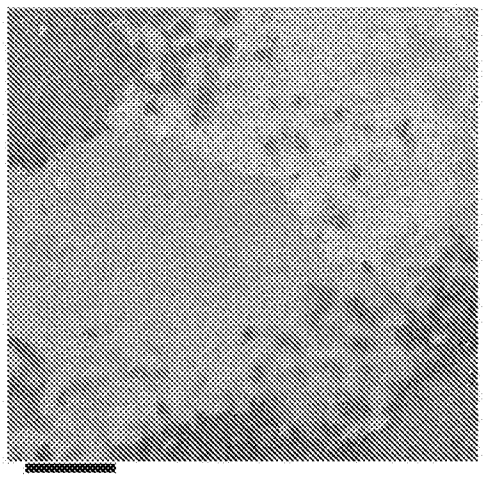
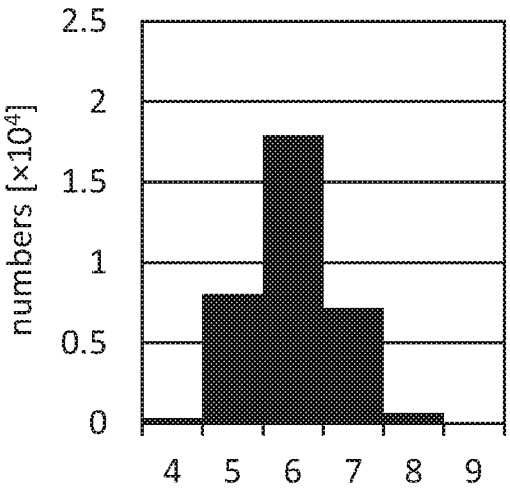
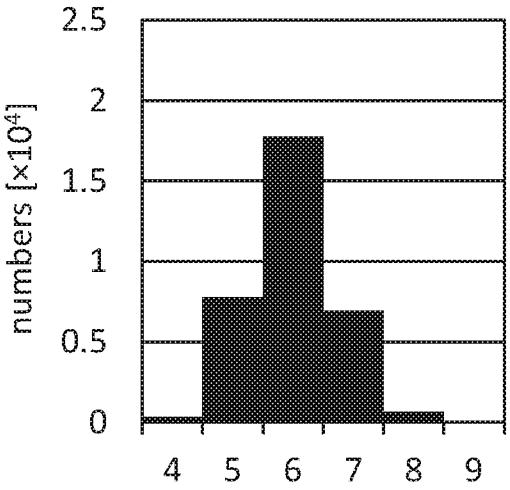


FIG. 27A



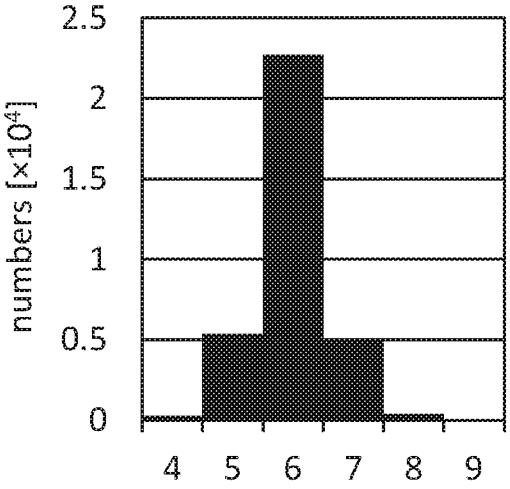
shape	proportion[%]
pentagon	23.6%
hexagon	52.5%
heptagon	21.1%
others	2.8%

FIG. 27B



shape	proportion[%]
pentagon	23.3%
hexagon	53.0%
heptagon	20.7%
others	3.0%

FIG. 27C



shape	proportion[%]
pentagon	15.9%
hexagon	67.3%
heptagon	14.8%
others	2.0%

FIG. 28A

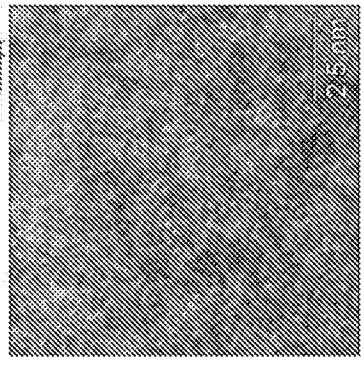


FIG. 28B

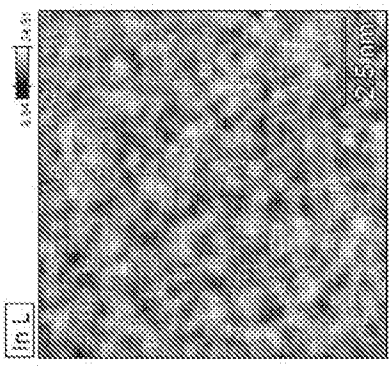


FIG. 28C

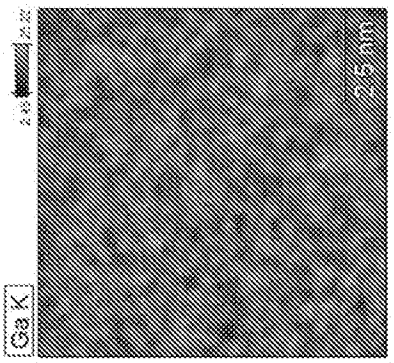


FIG. 28D

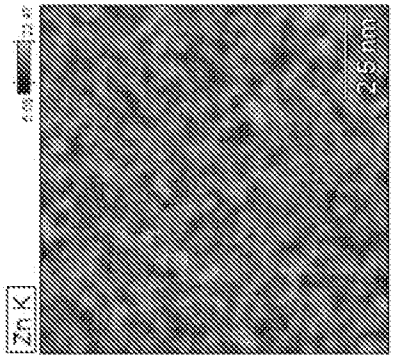


FIG. 28E

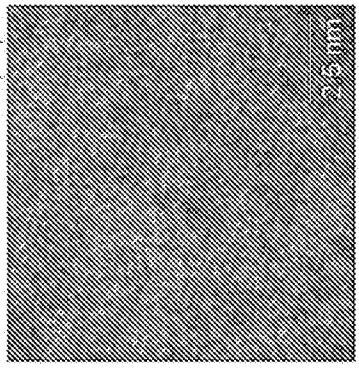


FIG. 28F

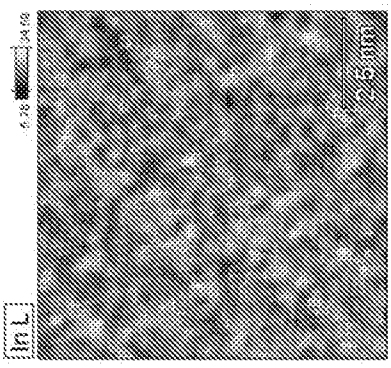


FIG. 28G

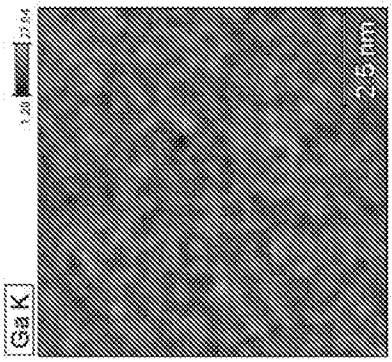


FIG. 28H

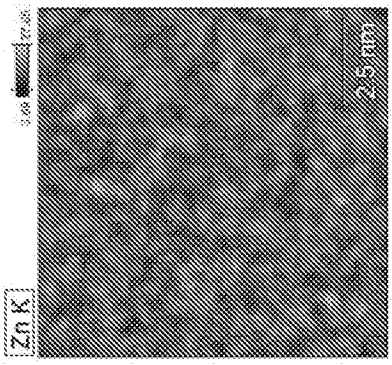


FIG. 29A

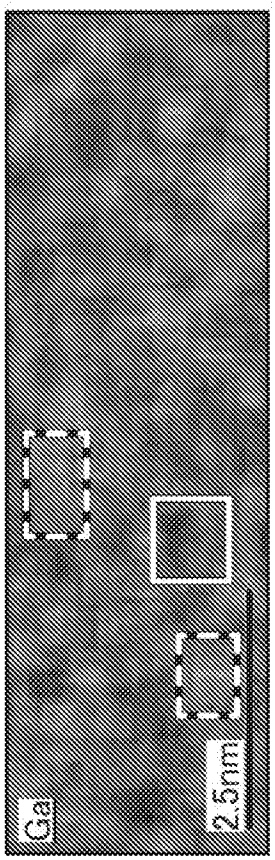


FIG. 29B

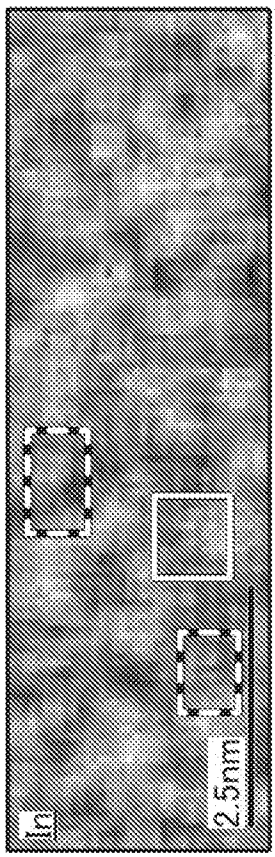


FIG. 29C

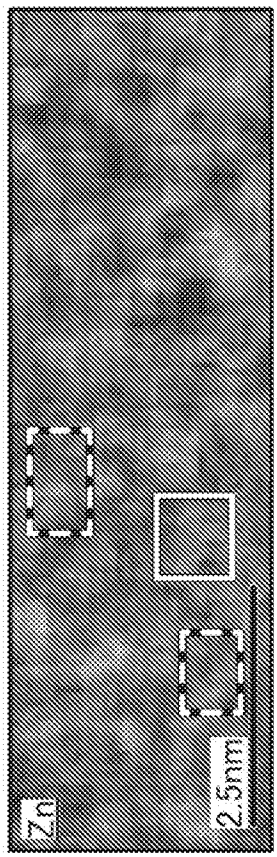
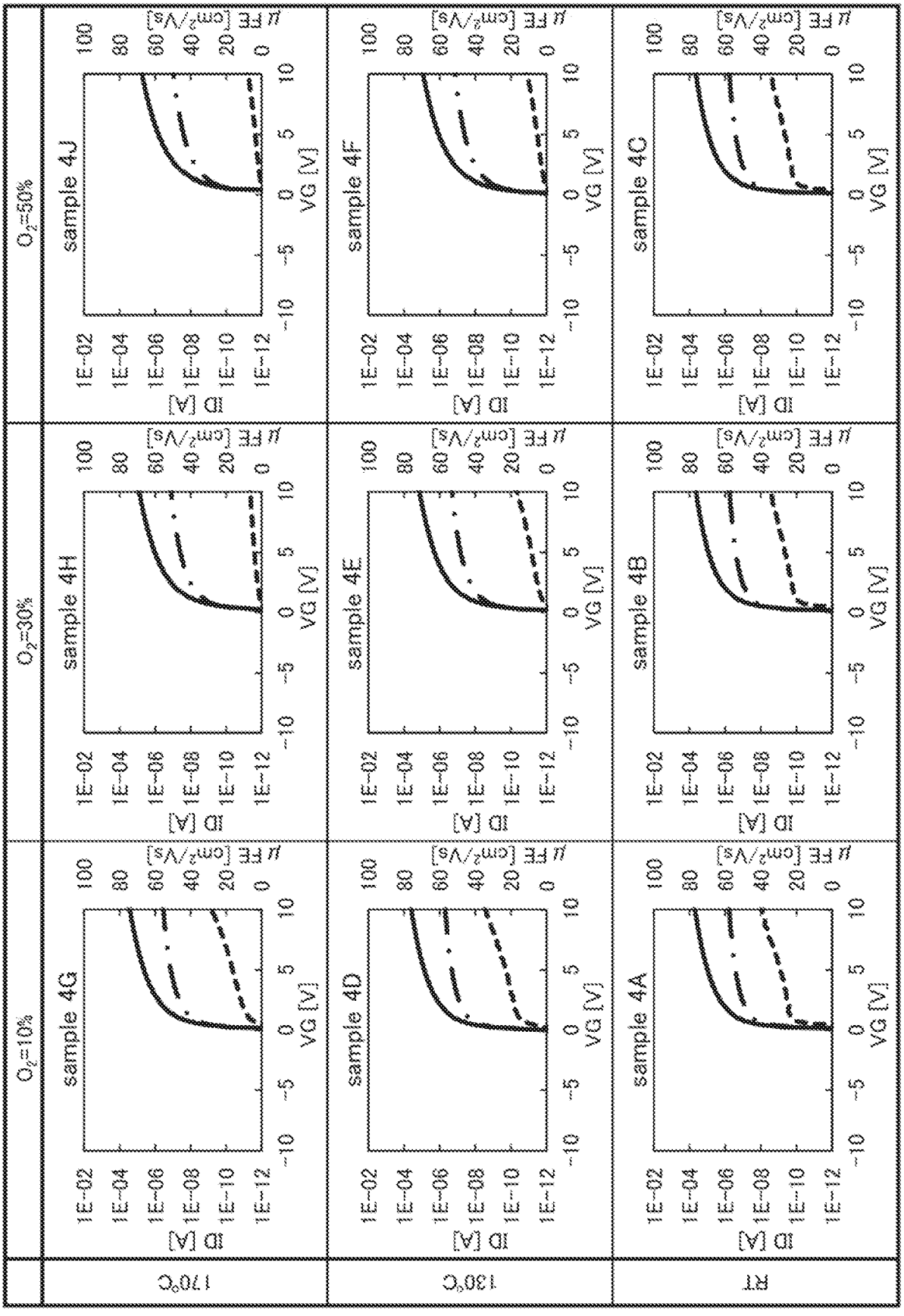


FIG. 30


O2=10%
O2=30%
O2=50%
170°C
130°C
RT
sample 4G
sample 4H
sample 4J
sample 4D
sample 4E
sample 4F
sample 4A
sample 4B
sample 4C
ID [A]
μ FE [cm²/Vs]
VG [V]

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2017/052714

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786(2006.01)i, C23C14/08(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, C23C14/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2017
Registered utility model specifications of Japan 1996-2017
Published registered utility model applications of Japan 1994-2017

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/0318359 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2015.11.05, Pars. [0103]-[0628], Figs. 1, 12 & JP 2016-66776 A & KR 10-2015-0125555 A	1-15
A	WO 2005/093847 A1 (HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.) 2005.10.06, pp. 6-8 & JP 2007-529117 A & US 2005/0199879 A1 & EP 1733433 A1 & KR 10-2007-0006770 A & CN 1930692 A & TW 200534367 A	1-15
A	US 2015/0318171 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2015.11.05, Pars. [0408]-[0413] & JP 2016-56446 A & KR 10-2015-0126272 A	1-15

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15.08.2017	22.08.2017

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2017/052714

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/0123130 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2010.05.20, Pars. [0036]-[0073], Fig. 1 & JP 2010-153802 A & KR 10-2010-0056970 A & CN 101740637 A & TW 201036160 A	1-15
A	JP 2010-027808 A (RICOH COMPANY, LTD.) 2010.02.04, Pars. [0033]-[0095], Fig. 1 (No Family)	1-15
A	JP 2015-189631 A (IDEMITSU KOSAN CO., LTD.) 2015.11.02, Pars. [0011]-[0050], Fig. 1 (No Family)	1-15