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(54) Title: IGBT STRUCTURE FOR WIDE BAND-GAP SEMICONDUCTOR MATERIALS

(57) Abstract: An IGBT device includes an IGBT stack, a collector contact, a gate contact, and an emitter contact. The IGBT stack includes an injector region, a drift region over the injector region, a spreading region over the drift region, and a pair of junction implants in the spreading region. The spreading region provides a first surface of the IGBT stack, which is opposite the drift region. The pair of junction implants is separated by a channel, and extends from the first surface of the IGBT stack along a lateral edge of the IGBT stack towards the drift region to a first depth, such that the thickness of the spreading region is at least one and a half times greater than the first depth.

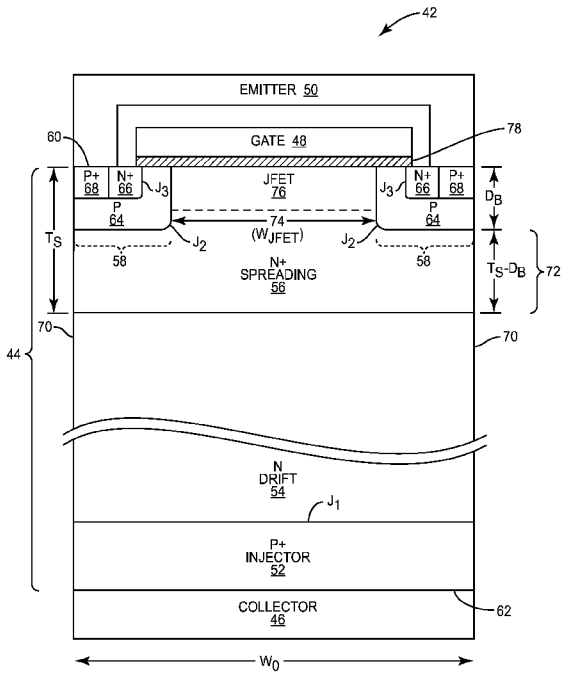

FIG. 2

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IGBT STRUCTURE FOR WIDE BAND-GAP SEMICONDUCTOR MATERIALS

Government Support

[0001] This invention was made with government funds under contract number W911NF-10-2-0038 awarded by the United States Army. The U.S. Government has rights in this invention.

Field of the Disclosure

[0002] The present disclosure relates to insulated gate bipolar transistor (IGBT) devices and structures.

Background

[0003] The insulated gate bipolar transistor (IGBT) is a semiconductor device that combines many of the desirable properties of a field-effect transistor (FET) with those of a bipolar junction transistor (BJT). An exemplary conventional IGBT device 10 is shown in Figure 1. The conventional IGBT device shown in Figure 1 represents a single IGBT cell that includes an IGBT stack 12, a collector contact 14, a gate contact 16, and an emitter contact 18. The IGBT stack 12 includes an injector region 20 adjacent to the collector contact 14, a drift region 22 over the injector region 20 and adjacent to the gate contact 16 and the emitter contact 18, and a pair of junction implants 24 in the drift region 22. The drift region 22 provides a first surface 26 of the IGBT stack 12 on which the gate contact 16 and the emitter contact 18 are located. Further, the injector region 20 provides a second surface 28 of the IGBT stack 12 opposite the first surface 26 on which the collector contact 14 is located.

[0004] Each one of the junction implants 24 is generally formed by an ion implantation process, and includes a base well 30, a source well 32, and an ohmic well 34. Each base well 30 is implanted in the first surface 26 of the IGBT stack 12, and extends down towards the injector region 20 along a lateral edge 36 of the IGBT stack 12. The source well 32 and the ohmic well 34 are formed in a shallow portion on the first surface 26 of the IGBT stack 12, and are

surrounded by the base well 30. A JFET gap 38 separates each one of the junction implants 24, and defines a JFET gap width W_{JFET} as the distance between each one of the junction implants 24 in the conventional IGBT device 10.

[0005] A gate oxide layer 40 is positioned on the first surface 26 of the IGBT stack 12, and extends laterally between a portion of the surface of each one of the source wells 32, such that the gate oxide layer 40 partially overlaps and runs between the surface of each source well 32 in the junction implants 24. The gate contact 16 is positioned over the gate oxide layer 40. The emitter contact 18 is a "U" shape, and includes two portions in contact with the first surface 26 of the IGBT stack 12. Each portion of the emitter contact 18 on the first surface 26 of the IGBT stack 12 partially overlaps both the source well 32 and the ohmic well 34 of one of the junction implants 24, respectively, without contacting the gate contact 16 or the gate oxide layer 40.

[0006] A first junction J_1 between the injector region 20 and the drift region 22, a second junction J_2 between each base well 30 and the drift region 22, and a third junction J_3 between each source well 32 and each base well 30 are controlled to operate in one of a forward-bias mode of operation or a reverse-bias mode of operation based on the biasing of the conventional IGBT device 10. Accordingly, the flow of current between the collector contact 14 and the emitter contact 18 is controlled.

[0007] The conventional IGBT device 10 has three primary modes of operation. When a positive bias is applied to the gate contact 16 and the emitter contact 18, and a negative bias is applied to the collector contact 14, the conventional IGBT device 10 operates in a reverse blocking mode. In the reverse blocking mode of the conventional IGBT device 10, the first junction J_1 and the third junction J_3 are reverse-biased, while the second junction J_2 is forward biased. As will be understood by those of ordinary skill in the art, the reverse-biased junctions J_1 and J_3 prevent current from flowing from the collector contact 14 to the emitter contact 18. Accordingly, the drift region 22 supports the majority of the voltage across the collector contact 14 and the emitter contact 18.

[0008] When a negative bias is applied to the gate contact 16 and the emitter contact 18, and a positive bias is applied to the collector contact 14, the conventional IGBT device 10 operates in a forward blocking mode. In the forward blocking mode of the conventional IGBT device 10, the first junction J_1 and the third junction J_3 are forward biased, while the second junction J_2 is reverse-biased. As will be understood by those of ordinary skill in the art, the reverse-bias of the second junction J_2 generates a depletion region, which effectively pinches off the JFET gap 38 of the IGBT device 10 and prevents current from flowing from the collector contact 14 to the emitter contact 18. Accordingly, the drift region 22 supports the majority of the voltage across the collector contact 14 and the emitter contact 18.

[0009] When a positive bias is applied to the gate contact 16 and the collector contact 14, and a negative bias is applied to the emitter contact 18, the conventional IGBT device 10 operates in a forward conduction mode of operation. In the forward conduction mode of operation of the conventional IGBT device 10, the first junction J_1 and the third junction J_3 are forward-biased, while the second junction J_2 is reverse-biased. Accordingly, current can flow from the collector contact 14 to the emitter contact 18. Specifically, the positive bias applied to the gate contact 16 generates an inversion channel on the first surface 26 of the IGBT stack 12, thereby creating a low-resistance path for electrons to flow from the emitter contact 18 through each one of the source wells 32 and each one of the base wells 30 into the drift region 22. As electrons flow into the drift region 22, the potential of the drift region 22 is decreased, thereby placing the first junction J_1 in a forward-bias mode of operation. When the first junction J_1 becomes forward-biased, holes are allowed to flow from the injector region 20 into the drift region 22. The holes effectively increase the doping concentration of the drift region 22, thereby increasing the conductivity thereof. Accordingly, electrons from the emitter contact 18 may flow more easily through the drift region 22 and to the collector contact 14.

[0010] The IGBT stack 12 of the conventional IGBT device 10 is Silicon (Si), the advantages and shortcomings of which are well known to those of ordinary

skill in the art. In an attempt to further increase the performance of IGBT devices, many have focused their efforts on using wide band-gap materials such as Silicon Carbide (SiC) for the IGBT stack 12. Although promising, conventional IGBT structures such as the one shown in Figure 1 are generally unsuitable for use with wide band-gap materials such as SiC. Due to inherent limitations in SiC fabrication processes, the carrier mobility and/or carrier concentration in the injector region 20 in a SiC IGBT device may be significantly diminished. Specifically, the conductivity in the injector region 20 will be low in a SiC device due to difficulties in growing high quality P-type epitaxial layers with low defect density. Further, due to damage in the drift region 22 caused by the ion implantation of the junction implants 24, the lifetime of carriers in the area directly below each junction implant 24 is significantly diminished. The result of the aforementioned conditions in a SiC IGBT device is that holes from the injector region 20 do not adequately modulate the conductivity of the portion of the drift region 22 above a certain distance from the injector region 20. Accordingly, electrons from the emitter contact 18 are met with a high-resistance path in the upper portion of the drift region 22, thereby increasing the on resistance R_{ON} of the conventional IGBT device 10 significantly, or cutting off current flow in the device altogether. Accordingly, an IGBT structure is needed that is suitable for use with wide band-gap semiconductor materials such as SiC.

Summary

[0011] The present disclosure relates to insulated gate bipolar transistor (IGBT) devices and structures. According to one embodiment, an IGBT device includes an IGBT stack, a collector contact, a gate contact, and an emitter contact. The IGBT stack includes an injector region, a drift region over the injector region, a spreading region over the drift region, and a pair of junction implants in the spreading region. The spreading region provides a first surface of the IGBT stack, which is opposite the drift region. The pair of junction implants is separated by a JFET gap, and extends from the first surface of the IGBT stack along a lateral edge of the IGBT stack towards the drift region to a first depth,

such that the thickness of the spreading region is at least one and a half times greater than the first depth. By including the spreading layer that is at least one and a half times thicker than the depth of each junction implant, the ON resistance R_{ON} and front-side injection capabilities of the IGBT device may be improved.

[0012] According to various embodiments, the thickness of the spreading layer is at least 2 to 4 times greater than that of the first depth of the junction implants.

[0013] According to one embodiment, the IGBT stack is formed of a wide band-gap semiconductor material. For example, the IGBT stack may be a Silicon Carbide (SiC) substrate.

[0014] According to one embodiment, the drift region is a lightly doped N region, the injector region is a highly doped P region, and the spreading region is a highly doped N region.

[0015] According to one embodiment, an IGBT device includes an IGBT stack, a collector contact, a gate contact, and an emitter contact. The IGBT stack includes an injector region, a drift region over the injector region, a spreading region over the drift region, and a pair of junction implants in the spreading region. The spreading region provides a first surface of the IGBT stack, which is opposite the drift region. The pair of junction implants are separated by a JFET gap, and extend from the first surface of the IGBT stack along a lateral edge of the IGBT stack towards the drift region to a first depth, such that the spreading region extends at least 1.5 µm beyond the first depth so that at least 1.5 µm of the spreading region exists between the bottom of each junction implant and the drift region. As discussed above, by including the spreading layer that extends at least 1.5 µm beyond the depth of each junction implant, the ON resistance R_{ON} and front-side injection capabilities of the IGBT device may be improved.

[0016] According to various embodiments, the spreading region is from at least 2.0 µm to at least 10.0 µm thicker than the first depth of each junction implant.

[0017] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0018] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0019] Figure 1 shows a two-dimensional representation of a conventional IGBT device.

[0020] Figure 2 shows a two-dimensional representation of an IGBT device suitable for wide band-gap semiconductor materials according to one embodiment of the present disclosure.

[0021] Figure 3 shows a flow-chart describing a method for manufacturing the IGBT device shown in Figure 2 according to one embodiment of the present disclosure.

[0022] Figures 4A-4I illustrate the method for manufacturing the IGBT device described in Figure 2 according to one embodiment of the present disclosure.

[0023] Figure 5 shows a two-dimensional representation of an IGBT device suitable for wide band-gap semiconductor materials according to one embodiment of the present disclosure.

[0024] Figure 6 shows a flow-chart describing a method for manufacturing the IGBT device shown in Figure 5 according to one embodiment of the present disclosure.

[0025] Figures 7A-7F illustrate the method for manufacturing the IGBT device described in Figure 5 according to one embodiment of the present disclosure.

Detailed Description

[0026] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the

best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0027] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0028] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0029] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one

element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0030] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0031] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0032] Turning now to Figure 2, an IGBT device 42 suitable for use with wide band-gap semiconductor materials systems is shown according to one embodiment of the present disclosure. The IGBT device 42 shown in Figure 2 represents a single IGBT cell, which may be part of a larger IGBT device including multiple cells. The IGBT device 42 includes an IGBT stack 44, a collector contact 46, a gate contact 48, and an emitter contact 50. The IGBT stack 44 includes an injector region 52 adjacent to the collector contact 46, a drift region 54 over the injector region 52, a spreading region 56 over the drift region 54 and adjacent to the gate contact 48 and the emitter contact 50, and a pair of junction implants 58 in the spreading region 56. The spreading region 56 provides a first surface 60 of the IGBT stack 44 on which the gate contact 48 and

the emitter contact 50 are located. Further, the injector region 52 provides a second surface 62 of the IGBT stack 44 opposite the first surface 60 on which the collector contact 46 is located. A thickness (T_S) of the spreading region 56 is defined as the distance between the junction of the spreading region 56 and the drift region 54 and the first surface 60 of the IGBT stack 44.

[0033] Each one of the junction implants 58 may be formed by an ion implantation process, and may include a base well 64, a source well 66, and an ohmic well 68. Each base well 64 is implanted in the first surface 60 of the IGBT stack 44, and extends down towards the injector region 52 along a lateral edge 70 of the IGBT stack 44 to a first depth (D_B). Notably, the first depth (D_B) represents the portion of each junction implant 58 that is closest to the drift region 54, which is substantially less than the thickness (T_S) of the spreading region 56, thereby leaving a spreading layer buffer 72 between each one of the junction implants 58 and the drift region 54 in order to mitigate the effects of one or more damaged regions located below the junction implants 58, as discussed in further detail below. The thickness of the spreading layer buffer 72 is the thickness (T_S) of the spreading region 56 less the first depth (D_B) of the base well 64. The source well 66 and the ohmic well 68 are formed in a shallow portion of the first surface 60 of the IGBT stack 44, and are surrounded by the base well 64. A JFET gap 74 separates each one of the junction implants 58, and defines a JFET gap width W_{JFET} as the distance between each one of the junction implants in the IGBT device 42. An additional junction field-effect transistor (JFET) implant 76 may be provided in the JFET gap 74, as discussed in further detail below.

[0034] According to one embodiment, the thickness (T_S) of the spreading region 56 is between about 1.5 µm to 10 µm. The first depth (D_B) of the base well 64 may be between about 0.5 µm to 1.5 µm. As discussed in further detail below, the thickness (T_S) of the spreading region 56 is substantially greater than the first depth (D_B) of the base well 64 of each junction implant 58 in order to provide the spreading layer buffer 72, which mitigates the effects of one or more damaged regions located below the junction implants 58. For example, the

thickness (T_S) of the spreading region 56 may be between one and a half to four times greater than the first depth (D_B) of each one of the base wells 64. As an additional example, the thickness (T_S) of the spreading region 56 may be at least 1.5 µm to 10.0 µm greater than the first depth (D_B) of the base wells 64, such that the spreading layer buffer 72 is at least 1.5 µm to 10.0 µm.

[0035] A gate oxide layer 78 may be positioned on the first surface 60 of the IGBT stack 44, and may extend laterally between a portion of the surface of each one of the source wells 66, such that the gate oxide layer 78 partially overlaps and runs between the surface of each source well 66 in the junction implants 58. The emitter contact 50 may be a "U" shape, and may include two portions in contact with the first surface 60 of the IGBT stack 44. Each portion of the emitter contact 50 on the first surface 60 of the IGBT stack 44 may partially overlap both the source well 66 and the ohmic well 68 of one of the junction implants 58, respectively, without contacting the gate contact 48 of the gate oxide layer 78.

[0036] A first junction J_1 between the injector region 52 and the drift region 54, a second junction J_2 between each base well 64 and the drift region 54, and a third junction J_3 between each source well 66 and each base well 64 are controlled to operate in one of a forward-bias mode of operation or a reverse-bias mode of operation based on the biasing of the IGBT device 42. Accordingly, the flow of current between the collector contact 46 and the emitter contact 50 is controlled.

[0037] According to one embodiment, the injector region 52 is a highly doped P region 52 with a doping concentration between 1E16 cm^{-3} to 1E21 cm^{-3}. The drift region 54 may be a lightly doped N region with a doping concentration between 1E13 cm^{-3} to 1E15 cm^{-3}. In some embodiments, the drift region 54 may include a notably light concentration of dopants, in order to improve one or more performance parameters of the IGBT device 42 as discussed in further detail below. The spreading region 56 may be a highly doped N region with a doping concentration between 5E15 cm^{-3} to 5E16 cm^{-3}. Further, in some embodiments, the spreading region 56 may include a graduated doping concentration, such that as the spreading region 56 extends away from the first surface 60 of the IGBT

stack 44, the doping concentration of the spreading region 56 gradually decreases. For example, the portion of the spreading region 56 directly adjacent to the first surface 60 of the IGBT stack 44 may be doped at a concentration of about 5E16 cm^{-3}, while the portion of the spreading region directly adjacent to the drift region 54 may be doped at a concentration of about 5E15 cm^{-3}. The JFET region 76 may be also be a highly doped N region with a doping concentration between 1E16 cm^{-3} to 1E17 cm^{-3}. Further, the base well 64 may be a P doped region with a doping concentration between 5E17 cm^{-3} and 1E19 cm^{-3}, the source well 66 may be a highly doped N region with a doping concentration between 1E19 cm^{-3} and 1E21 cm^{-3}, and the ohmic well 68 may be a highly doped P layer with a doping concentration between1E19 cm^{-3} and 1E21 cm^{-3}.

[0038] The injector region 52 may be doped aluminum, boron, or the like. Those of ordinary skill in the art will appreciate that many different dopants exist that may be suitable for doping the injector region 52, all of which are contemplated herein. The drift region 54, the spreading region 56, and the JFET region 76 may be doped with nitrogen, phosphorous, or the like. Those of ordinary skill in the art will appreciate that many different dopants exist that may be suitable for doping the drift region 54, the spreading region 56, and the JFET region, all of which are contemplated herein.

[0039] According to one embodiment, the injector region 52 is generated by an epitaxy process. According to an additional embodiment, the injector region 52 is formed by an ion implantation process. Those of ordinary skill in the art will appreciate that numerous different processes exist for generating the injector region 52, all of which are contemplated herein. The spreading region 56 and the JFET region 76 may similarly be formed by either an epitaxy process or an ion implantation process. Those of ordinary skill in the art will appreciate that numerous different processes exist for generating the spreading region 56 and the JFET region 76, all of which are contemplated herein.

[0040] According to one embodiment, the IGBT stack 44 is a wide band-gap semiconductor material. For example, the IGBT stack 44 may be Silicon Carbide (SiC). As discussed above, manufacturing limitations inherent in current SiC

technologies will generally result in a diminished carrier lifetimes and/or carrier concentration in the injector region of a SiC IGBT device. As a result, SiC IGBT devices generally suffer from a reduced amount of "backside injection", which results in poor conductivity modulation and an increased ON resistance (R_{ON}) of the SiC IGBT device. Further, in attempting to design a wide band-gap IGBT device, it was discovered by the inventors that damaged regions below each one of the junction implants of a SiC IGBT device result in a significantly degraded carrier lifetime at or near these damaged regions. These so-called "end-of-range" defects effectively prevent the modulation of current in the upper portion of the drift layer in a SiC IGBT device, which in turn significantly increases the resistance in this area. As a result of the increased resistance in the upper portion of the drift region, current flow in the SiC IGBT device may be significantly reduced, and may even be cut off altogether. The spreading region 56 of the IGBT device 42 is therefore provided to bypass the damaged regions below each one of the junction implants 58, thereby improving the performance of the SiC IGBT device 42.

[0041] By bypassing the damaged regions below each one of the junction implants 58, electrons from the emitter contact 50 are delivered directly to a region of high conductivity modulation in the drift region 54. Accordingly, electrons easily pass into the drift region 54 and to the collector contact 46 of the IGBT device 42. Those of ordinary skill in the art will recognize that the ON resistance (R_{ON}) is significantly reduced in the IGBT device 42, thereby improving the performance thereof.

[0042] While the spreading region 56 effectively reduces the ON resistance (R_{ON}) of the IGBT device 42, the introduction of the spreading region 56 also results in a decrease in the blocking voltage (V_{BLK}) of the IGBT device 42. In order to compensate for this fact, the doping concentration in the drift region 54 may be decreased, such that the doping concentration in the drift region 54 is exceptionally light, as discussed above. Accordingly, a balance between the on resistance (R_{ON}) and the blocking voltage (V_{BLK}) of the IGBT device 42 may be struck.

[0043] In addition to the advantages described above, the IGBT device 42 further benefits from the predominant use of "front-side" injection. That is, the IGBT device 42 shown in Figure 2 transfers current from the collector contact 46 to the emitter contact 50 primarily through the use of electrons supplied from the emitter contact 50, rather than as a result of hole injection from the injector region 52. As will be appreciated by those of ordinary skill in the art, the use of predominant backside injection, as is common among conventional IGBT devices, often results in significant switching losses, thereby degrading the performance of the IGBT device. Accordingly, numerous techniques have been developed to reduce the amount of hole injection provided at the back-side of the device, while simultaneously increasing the amount of electrons supplied from the emitter contact. Due to the arrangement of the various regions in the IGBT stack 44, the IGBT device 42 inherently operates in a predominant "front-side" injection mode, thereby improving the performance of the device.

[0044] Further, providing the spreading region 56 also allows the JFET gap width (W_{JFET}) and the overall device width (W_D) to be significantly reduced when compared to conventional IGBT devices. For example, the JFET gap width (W_{JFET}) of the IGBT device 42 may be between 1 µm to 4 µm, and the overall device width (W_D) of the IGBT device 42 may be between 5 µm to 15 µm.

[0045] Finally, providing the spreading region 56 results in desirable thermal properties of the IGBT device 42. As will be appreciated by those of ordinary skill in the art, conventional IGBT devices generally suffer from a significant amount of temperature dependence. That is, the performance characteristics of a conventional IGBT generally change with temperature. Specifically, as the temperature of an IGBT device increases, so does the lifetime of carriers in the drift region, thereby resulting in increased current flow through the device. This can result in a dangerous cycle, in which increased current flow through the IGBT device further raises the temperature of the device, until the IGBT device can no longer handle the amount of current through the device and fails. By providing the spreading region 56 in the IGBT device 42, a large unmodulated region is generated below the first surface 60 of the IGBT stack 44, as discussed above.

As will be appreciated by those of ordinary skill in the art, this unmodulated region has an inverse relationship between the current flow therein and temperature. By carefully choosing the dimensions of the drift region 54 and the spreading region 56, a designer can thus effectively cancel the effects of temperature on current flow in the IGBT device 42, thereby significantly increasing the performance thereof.

[0046] Figures 3 and 4A-4I illustrate a method for manufacturing the IGBT device 42 shown in Figure 2 according to one embodiment of the present disclosure. First, the injector region 52 is grown via an epitaxy process on a sacrificial substrate 80 (step 100 and Figure 4A). As will be appreciated by those of ordinary skill in the art, the sacrificial substrate 80 must be used to generate the IGBT device 42 shown in Figure 2 due to a lack of available P-substrates for SiC materials systems. The drift region 54 is then grown on top of the injector region 52 opposite the substrate 80 (step 102 and Figure 4B). Next, the spreading region 56 is grown via an epitaxy process over the drift region 54 opposite the injector region 52 (step 104 and Figure 4C). The spreading region 56 provides the first surface 60, which is opposite the drift region 54. The junction implants 58 are then provided in the first surface 60 of the IGBT stack 44 (step 106 and Figure 4D), such that the junction implants 58 extend to a first depth D_B from the first surface 60 of the IGBT stack 44. The junction implants 58 are generally provided via one or more ion implantation processes, however, any suitable method may be used to provide the junction implants 58 without departing from the principles disclosed herein. Notably, as discussed above, the spreading region 56 and the junction implants 58 are provided such that the spreading region 56 has a thickness T_S that is between one and a half to four times thicker than the first depth D_B, thereby improving the performance of the completed IGBT device 42.

[0047] The JFET region 76 is then provided in the channel 74 between the junction implants 58 (step 108 and Figure 4E). The JFET region 76 may be provided by an epitaxy process, an ion implantation process, or any other suitable process. Next, the gate oxide 78 and the gate contact 48 are provided

on the first surface 60 of the IGBT stack 44 (step 110 and Figure 4F). Specifically, the gate oxide 78 is provided such that the gate oxide 78 partially overlaps and runs between each source well 66 in the pair of junction implants 58, and the gate contact 48 is provided on top of the gate oxide layer 78. As will be appreciated by those of ordinary skill in the art, several different oxidation and metallization techniques exist for providing the gate oxide 78 and the gate contact 48, respectively, all of which are contemplated herein. The emitter contact 50 is then provided on the first surface 60 of the IGBT stack 44 (step 112 and Figure 4G). Specifically, the emitter contact 50 is provided such that the emitter partially overlaps the source well 66 and the ohmic well 68 in each one of the pair of junction implants 58, respectively, without contacting the gate contact 48. The emitter contact 50 may be provided by any suitable metallization process. Next, the substrate 80 is removed from the IGBT stack 44 (step 114 and Figure 4H). The substrate 80 may be removed, for example, by an etching or grinding process. Finally, the collector contact 46 is provided over the entire second surface 62 of the IGBT stack 44 (step 116 and Figure 4I). The collector contact 46 may be provided by any suitable metallization process.

[0048] Although the process illustrated in Figures 3 and 4A-4I is illustrated in a particular number of discrete steps, which are arranged in a particular order, the present disclosure is not so limited. Each illustrated step may in fact comprise one or more steps, and may be accomplished in any order with respect to the other steps without departing from the principles described herein.

[0049] Figure 5 shows the IGBT device 42 according to an additional embodiment of the present disclosure. While the IGBT device 42 shown above with respect to Figure 2 is an N-IGBT, the IGBT device 42 of Figure 5 is a P-IGBT device. Accordingly, the doping of each one of the separate regions in the IGBT device 42 are the opposite of that shown in Figure 2, such that the injector region 52 may be a heavily doped N region with a doping concentration between 1E18 cm^{-3} and 1E21 cm^{-3}, the drift region 54 may be a lightly doped P region with a doping concentration between 1E13 cm^{-3} and 1E15 cm^{-3}, the spreading region 56 may be a heavily doped P region with a doping concentration between 5E15

cm^{-3} to 5E16 cm^{-3}, and the JFET region 76 may be a highly doped P region with a doping concentration between 1E16 cm^{-3} and 1E17 cm^{-3}. Further, the base well 64 may be an N doped region with a doping concentration between 5E17 cm^{-3} and 1E19 cm^{-3}, the source well 66 may be a highly doped P region with a doping concentration between 1E19 cm^{-3} and 1E21 cm^{-3}, and the ohmic well 68 may be a highly doped N layer with a doping concentration between 1E19 cm^{-3} and 1E21 cm^{-3}. The IGBT device 42 shown in Figure 5 may function substantially similarly to the IGBT device 42 described above with respect to Figure 2, with differences that will be readily appreciated by those of ordinary skill in the art.

[0050] Figures 6 and 7A-7F illustrate a method for manufacturing the IGBT device 42 shown in Figure 5 according to one embodiment of the present disclosure. First, the drift region 54 is grown on top of the injector region 52 (step 200 and Figure 7A). As will be appreciated by those of ordinary skill in the art, because the injector region 52 in the IGBT device 42 is an N-doped layer, the injector region can serve as the substrate for growing the other regions in the IGBT stack 44. The spreading region 56 is then grown on top of the drift region 54 opposite the injector region 52 (step 202 and Figure 7B). The spreading region 56 provides the first surface 60, which is opposite the IGBT stack 44. Next, the junction implants 58 are provided in the first surface 60 of the IGBT stack 44 (step 204 and Figure 7C), such that the junction implants 58 extend to a first depth D_B from the first surface 60 of the IGBT stack 44. The junction implants 58 are generally provided via one or more implantation processes, however, any suitable method may be used to provide the junction implants 58 without departing from the principles disclosed herein. Notably, as discussed above, the spreading region 56 and the junction implants 58 are provided such that the spreading region 56 has a thickness T_S that is between one half to four times thicker than the first depth D_B, thereby improving the performance of the completed IGBT device 42.

[0051] The JFET region 76 is then provided in the channel 74 between the junction implants 58 (step 206 and Figure 7D). The JFET region 76 may be

provided by an epitaxy process, an ion implantation process, or any other suitable process. Next, the gate oxide 78 and the gate contact 48 are provided on the first surface 60 of the IGBT stack 44 (step 208 and Figure 7E). Specifically, the gate oxide 78 is provided such that the gate oxide 78 partially overlaps and runs between each source well 66 in the pair of junction implants 58, and the gate contact 48 is provided on top of the gate oxide layer 78. As will be appreciated by those of ordinary skill in the art, several different oxidation and metallization techniques exist for providing the gate oxide 78 and the gate contact 48, respectively, all of which are contemplated herein. Finally, the collector contact 46 is provided on the second surface 62 of the IGBT stack 44, and the emitter contact 50 is provided on the first surface 60 of the IGBT stack 44 (step 210 and Figure 4F). Specifically, the emitter contact 50 is provided such that the emitter contact 50 partially overlaps the source well 66 and the ohmic well 68 in each one of the pair of junction implants, respectively, without contacting the gate contact 48, while the collector contact 46 is provided over the entire second surface 62 of the IGBT stack 44. The collector contact 46 and the emitter contact 50 may be provided by any suitable metallization process.

[0052] Although the process illustrated in Figures 6 and 7A-7F is illustrated in a particular number of discrete steps, which are arranged in a particular order, the present disclosure is not so limited. Each illustrated step may in fact comprise one or more steps, and may be accomplished in any order with respect to the other steps without departing from the principles described herein.

[0053] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. An insulated gate bipolar transistor (IGBT) device comprising:
   - an IGBT stack, wherein the IGBT stack includes:
     - an injector region;
     - a drift region over the injector region;
     - a spreading region over the drift region, the spreading region providing a first surface of the IGBT stack opposite the drift region; and
     - a pair of junction implants in the spreading region, wherein:
       - the pair of junction implants are separated by a channel and extend from the first surface of the IGBT stack along a lateral edge of the IGBT stack towards the drift region to a first depth; and
       - the thickness of the spreading region is at least one and a half times greater than the first depth;
   - a gate contact and an emitter contact on the first surface of the IGBT stack; and
   - a collector contact on a second surface of the IGBT stack, which is provided by the injector region opposite the drift region.

2. The IGBT device of claim 1 wherein the thickness of the spreading region is less than four times greater than the first depth.

3. The IGBT device of claim 1 wherein the thickness of the spreading region is at least two times greater than the first depth.

4. The IGBT device of claim 1 wherein the IGBT stack is a wide band-gap semiconductor material.

5. The IGBT device of claim 1 wherein the IGBT stack is Silicon Carbide (SiC).

6. The IGBT device of claim 1 wherein each one of the pair of junction implants comprises:

- a base well;
- a source well; and
- an ohmic well, wherein the doping concentration of the base well, the source well, and the ohmic well are different from one another.

7. The IGBT device of claim 6 wherein:

- the gate contact partially overlaps and runs between each source well in the pair of junction implants; and
- the emitter contact partially overlaps both the source well and the ohmic well in each one of the pair of junction implants, respectively, without contacting the gate contact.

8. The IGBT device of claim 7 further comprising a gate oxide layer between the gate contact and the first surface of the IGBT stack.

9. The IGBT device of claim 1 wherein:

- the drift region is a lightly doped N region;
- the injector region is a highly doped P region; and
- the spreading region is a highly doped N region.

10. The IGBT device of claim 1 wherein:

- the drift region is a lightly doped P region;
- the injector region is a highly doped N region; and
- the spreading region is a highly doped P region.

11. The IGBT device of claim 1 wherein:

- the first depth is in the range of about 0.3 µm to about 1.0 µm; and
- the thickness of the spreading region is in the range of about 1.5 µm to about 10 µm.

12. The IGBT device of claim 1 wherein a width of the IGBT stack is between about 1µm to 4µm.

13. An insulated gate bipolar transistor (IGBT) device comprising:

- an IGBT stack, wherein the IGBT stack includes:
  - an injector region;
  - a drift region over the injector region;
  - a spreading region over the drift region, the spreading region providing a first surface of the IGBT stack opposite the drift region; and
  - a pair of junction implants in the spreading region, wherein:
    - the pair of junction implants are separated by a junction field-effect transistor (JFET) region and extend from the first surface of the IGBT stack along a lateral edge of the IGBT stack towards the drift region to a first depth; and
    - the spreading region extends beyond the first depth by at least 1.5 µm;
- a gate contact and an emitter contact on the first surface of the IGBT stack; and
- a collector contact on a second surface of the IGBT stack, which is provided by the injector region opposite the drift region.

14. The IGBT device of claim 13 wherein the spreading region extends beyond the first depth by less than about 10.0 µm.

15. The IGBT device of claim 13 wherein the spreading region extends beyond the first depth by at least 2.0 µm.

16. The IGBT device of claim 13 wherein the IGBT stack comprises a wide band-gap semiconductor material.

17. The IGBT device of claim 13 wherein the IGBT stack comprises Silicon Carbide (SiC).

18. The IGBT device of claim 13 wherein each one of the pair of junction implants comprises:

- a base well;
- a source well; and
- an ohmic well, wherein the doping concentration of the base well, the source well, and the ohmic well are different from one another.

19. The IGBT device of claim 18 wherein:

- the gate contact partially overlaps and runs between each source well in the pair of junction implants; and
- the emitter contact partially overlaps both the source well and the ohmic well in each one of the pair of junction implants, respectively, without contacting the gate contact.

20. The IGBT device of claim 19 further comprising a gate oxide layer between the gate contact and the first surface of the IGBT stack.

21. The IGBT device of claim 13 wherein:

- the drift region is a lightly doped N region;
- the injector region is a highly doped P region; and
- the spreading region is a highly doped N region.

22. The IGBT device of claim 13 wherein:

- the drift region is a lightly doped P region;
- the injector region is a highly doped N region; and
- the spreading region is a highly doped P region.

23. The IGBT device of claim 13 wherein the first depth is in the range of about 0.3 µm to about 1.5 µm.

24. The IGBT device of claim 13 wherein a width of the IGBT stack is between about 1µm to 4µm.

25. A method comprising:

- providing an IGBT stack including an injector region, a drift region over the injector region, and a spreading region over the drift region, such that the spreading region provides a first surface of the IGBT stack opposite the drift layer;
- providing a pair of junction implants in the first surface of the IGBT stack such that the pair of junction implants are separated by a channel and extend from a first surface of the IGBT stack towards the drift region to a first depth, wherein the thickness of the spreading region is at least one and a half times greater than the first depth;
- providing a gate contact and an emitter contact on the first surface of the IGBT stack; and
- providing a collector contact on a second surface of the IGBT stack, which is provided by the injector region opposite the drift region.

26. The method of claim 25 wherein the thickness of the spreading region is less than four times greater than the first depth.

27. The method of claim 25 wherein the thickness of the spreading region is at least two times greater than the first depth.

28. The method of claim 25 wherein the IGBT stack is Silicon Carbide (SiC).

29. An insulated gate bipolar transistor (IGBT) device comprising:

- an IGBT stack, wherein the IGBT stack includes:
  - an injector region;
  - a drift region over the injector region;
  - a spreading region over the drift region; and
  - a pair of junction implants in the spreading region, each of the pair of junction implants separated by a channel;
- wherein the spreading region enables the width of the IGBT stack to remain less than about 4µm.

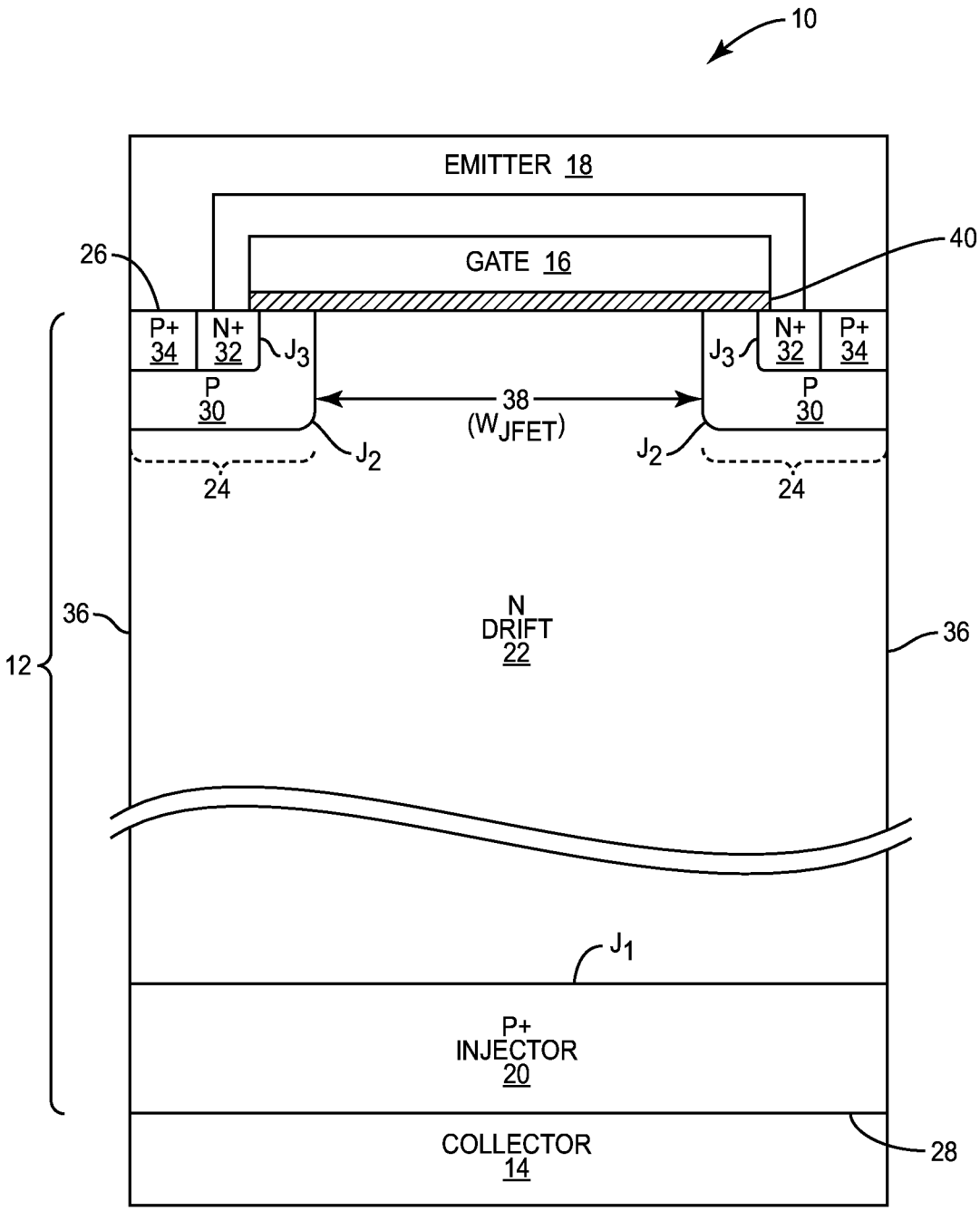

FIG. 1
(RELATED ART)

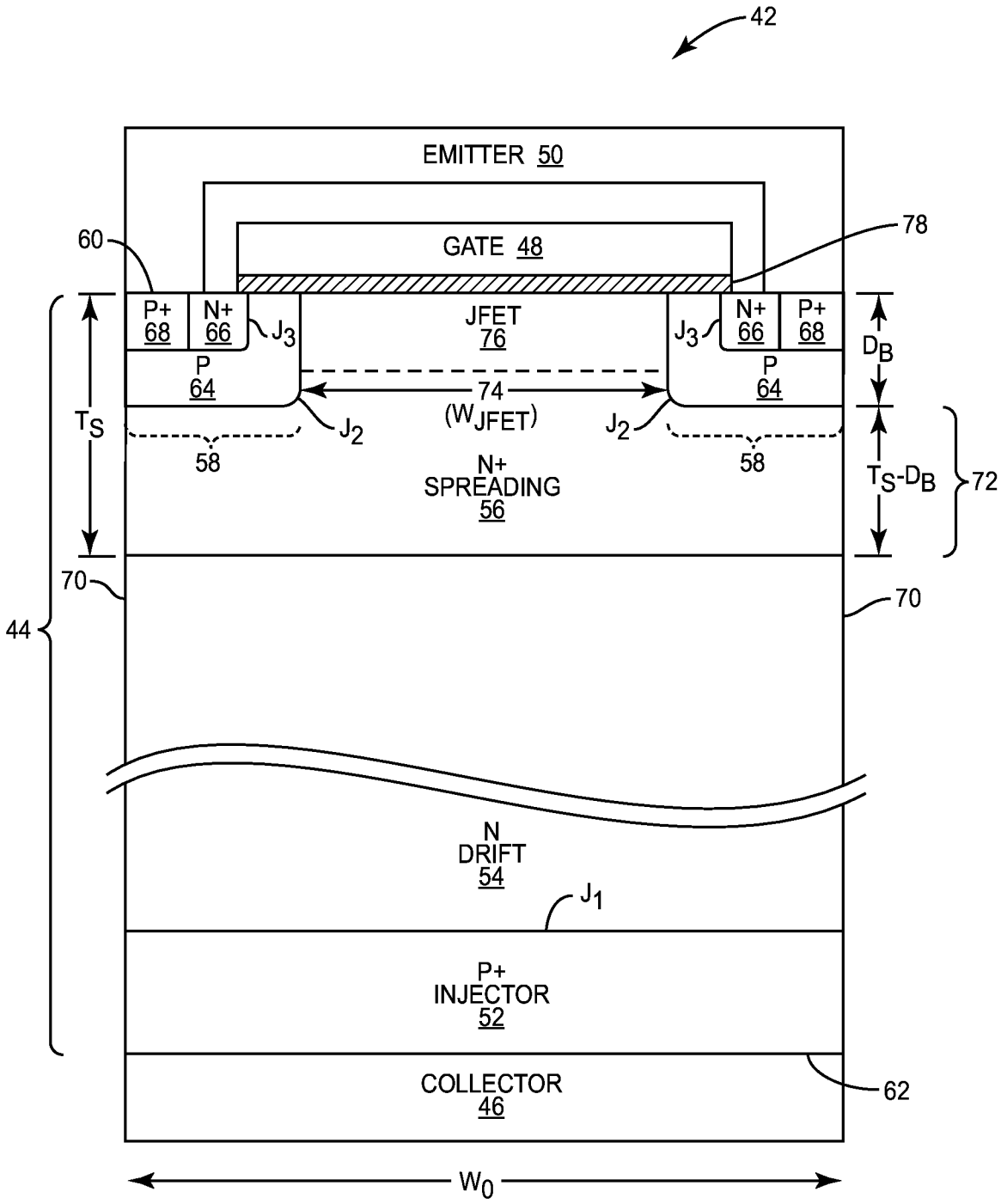
42
EMITTER 50
GATE 48
60
78
P+ 68
N+ 66
J3
JFET 76
J3
N+ 66
P+ 68
P 64
P 64
74 (WJFET)
TS
J2
J2
58
58
N+ SPREADING 56
DB
TS-DB
72
70
70
44
N DRIFT 54
J1
P+ INJECTOR 52
COLLECTOR 46
62
W0

FIG. 2

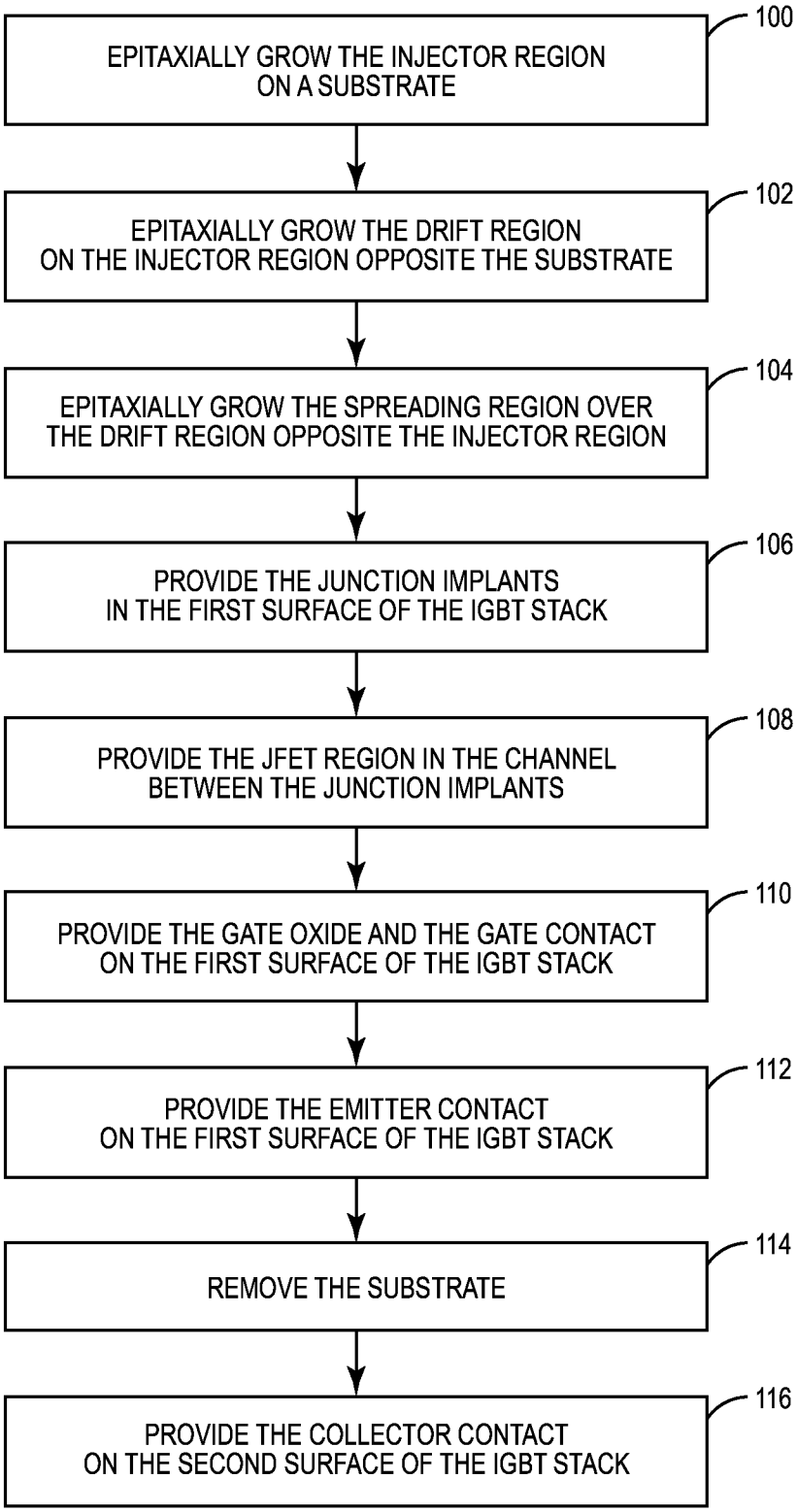
EPITAXIALLY GROW THE INJECTOR REGION ON A SUBSTRATE
100
EPITAXIALLY GROW THE DRIFT REGION ON THE INJECTOR REGION OPPOSITE THE SUBSTRATE
102
EPITAXIALLY GROW THE SPREADING REGION OVER THE DRIFT REGION OPPOSITE THE INJECTOR REGION
104
PROVIDE THE JUNCTION IMPLANTS IN THE FIRST SURFACE OF THE IGBT STACK
106
PROVIDE THE JFET REGION IN THE CHANNEL BETWEEN THE JUNCTION IMPLANTS
108
PROVIDE THE GATE OXIDE AND THE GATE CONTACT ON THE FIRST SURFACE OF THE IGBT STACK
110
PROVIDE THE EMITTER CONTACT ON THE FIRST SURFACE OF THE IGBT STACK
112
REMOVE THE SUBSTRATE
114
PROVIDE THE COLLECTOR CONTACT ON THE SECOND SURFACE OF THE IGBT STACK
116

FIG. 3

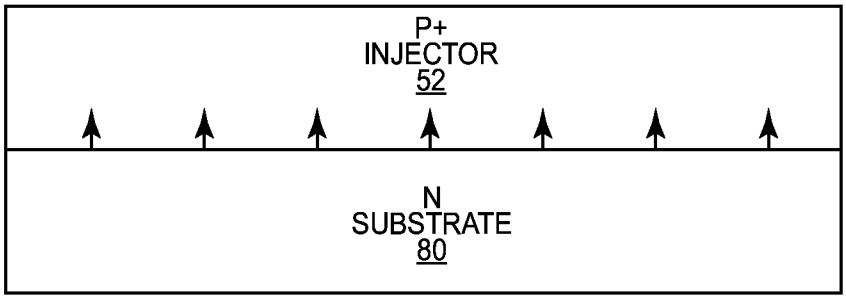

FIG. 4A

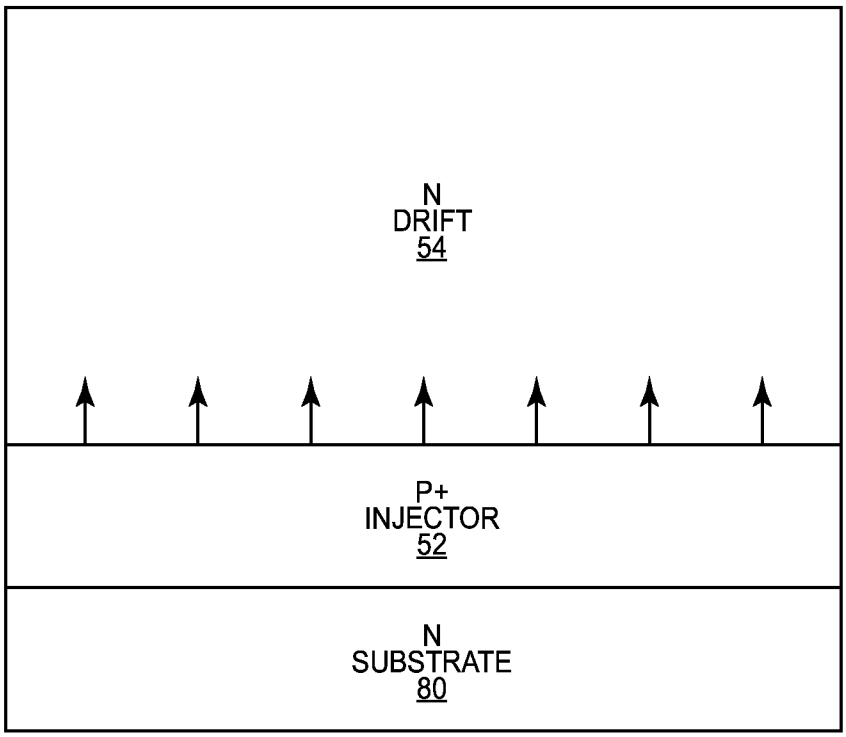

FIG. 4B

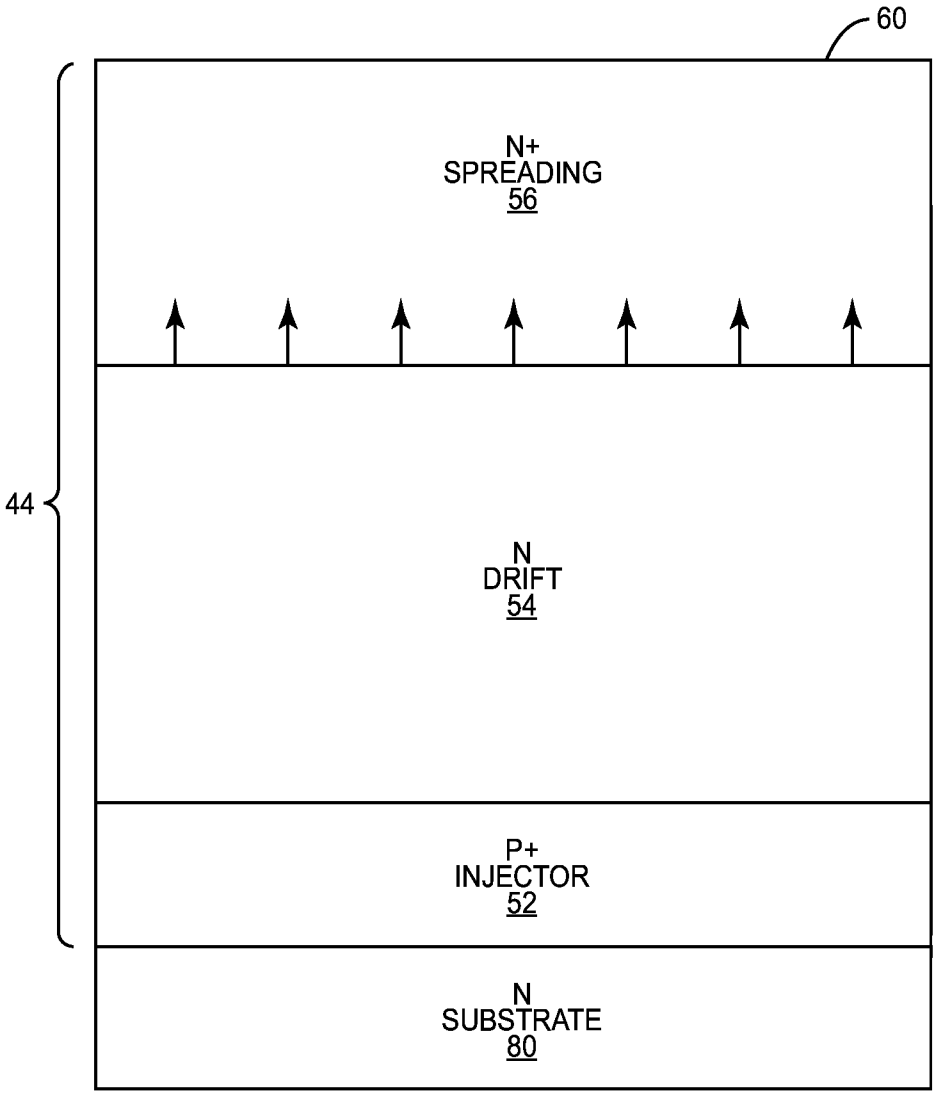

FIG. 4C

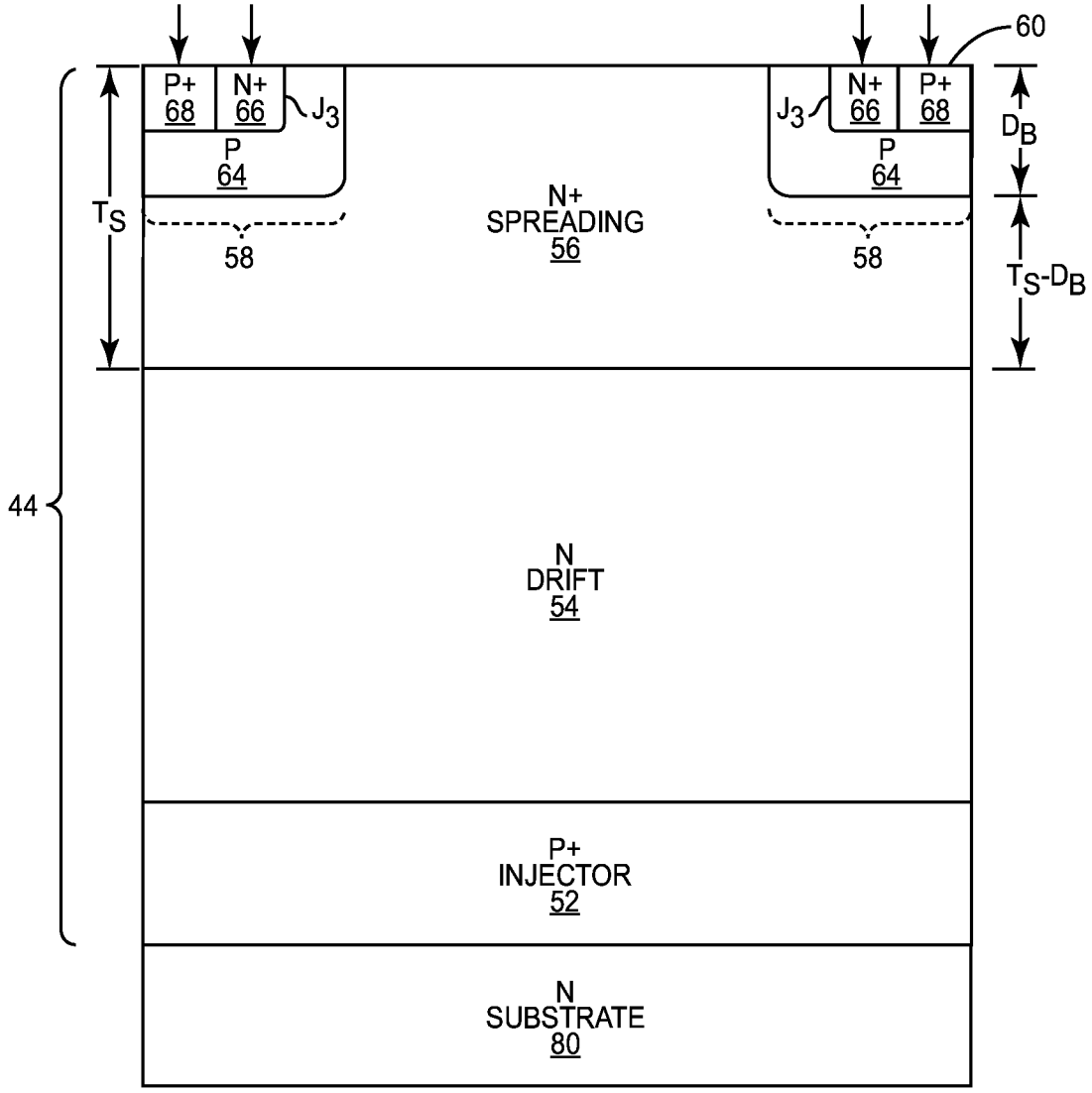
60
P+
68
N+
66
J3
P
64
TS
58
N+
SPREADING
56
J3
N+
66
P+
68
P
64
58
DB
TS-DB
44
N
DRIFT
54
P+
INJECTOR
52
N
SUBSTRATE
80

FIG. 4D

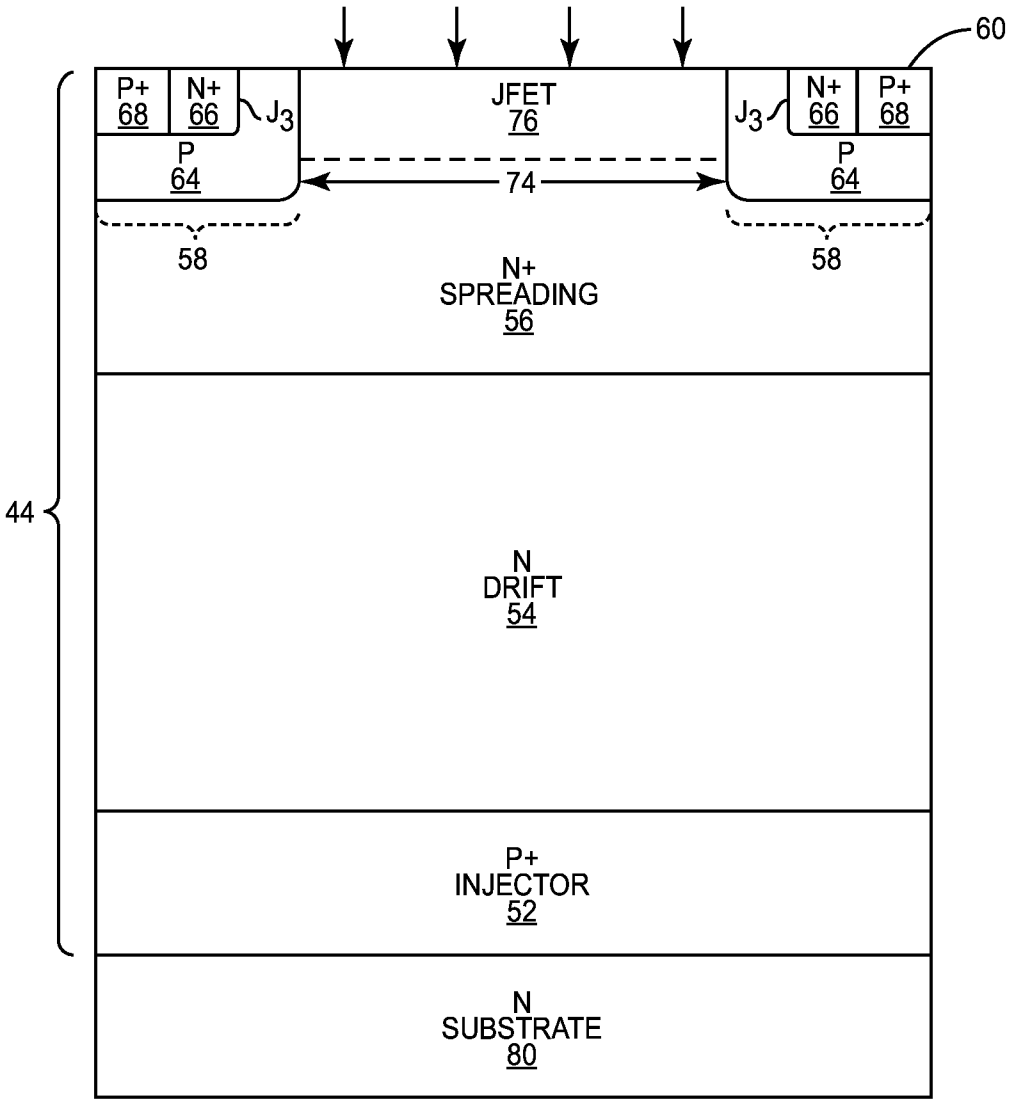
60
P+
68
N+
66
J3
JFET
76
J3
N+
66
P+
68
P
64
74
P
64
58
58
N+
SPREADING
56
44
N
DRIFT
54
P+
INJECTOR
52
N
SUBSTRATE
80

FIG. 4E

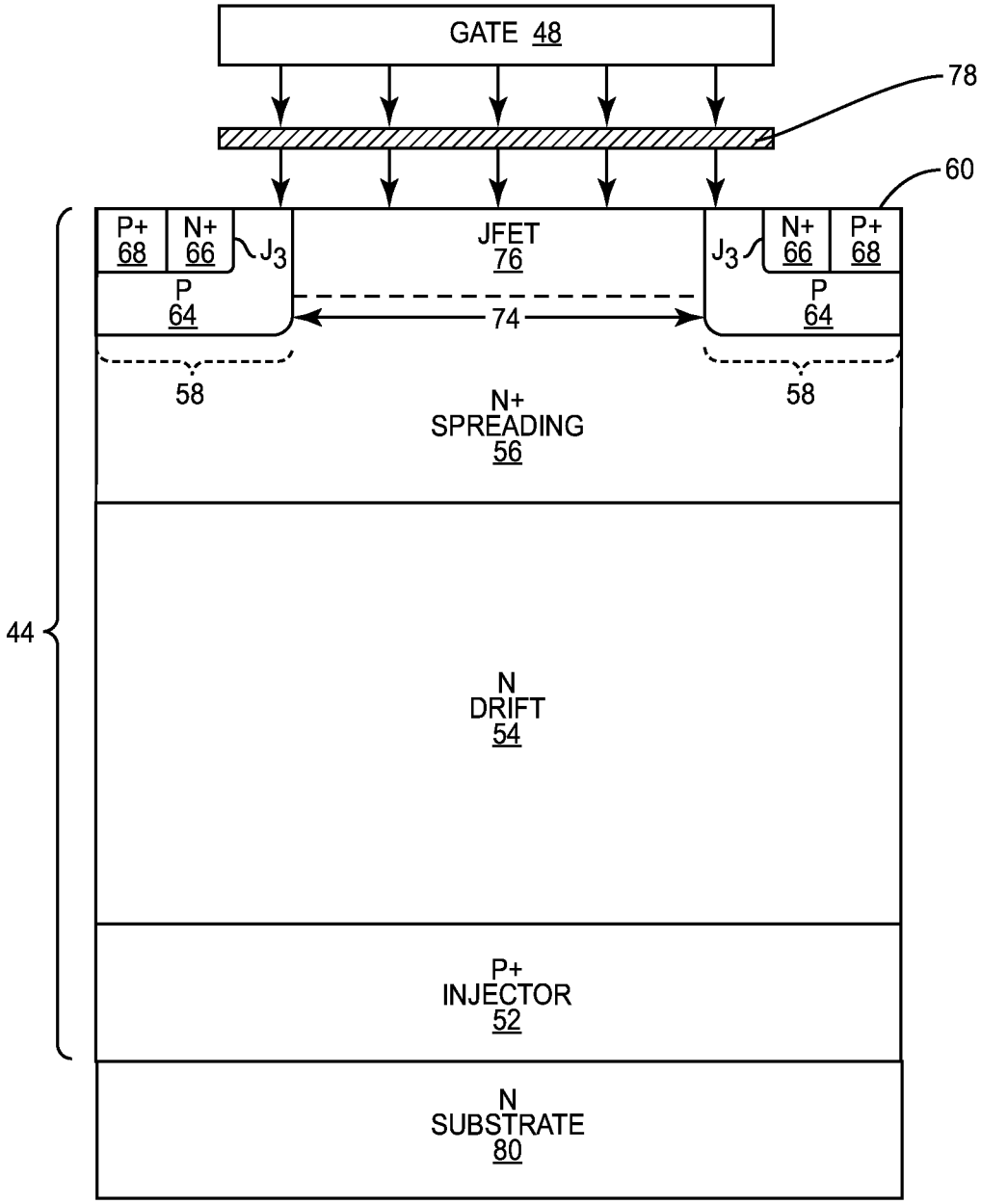
GATE 48
78
60
P+
68
N+
66
J3
JFET
76
J3
N+
66
P+
68
P
64
74
P
64
58
58
N+
SPREADING
56
44
N
DRIFT
54
P+
INJECTOR
52
N
SUBSTRATE
80

FIG. 4F

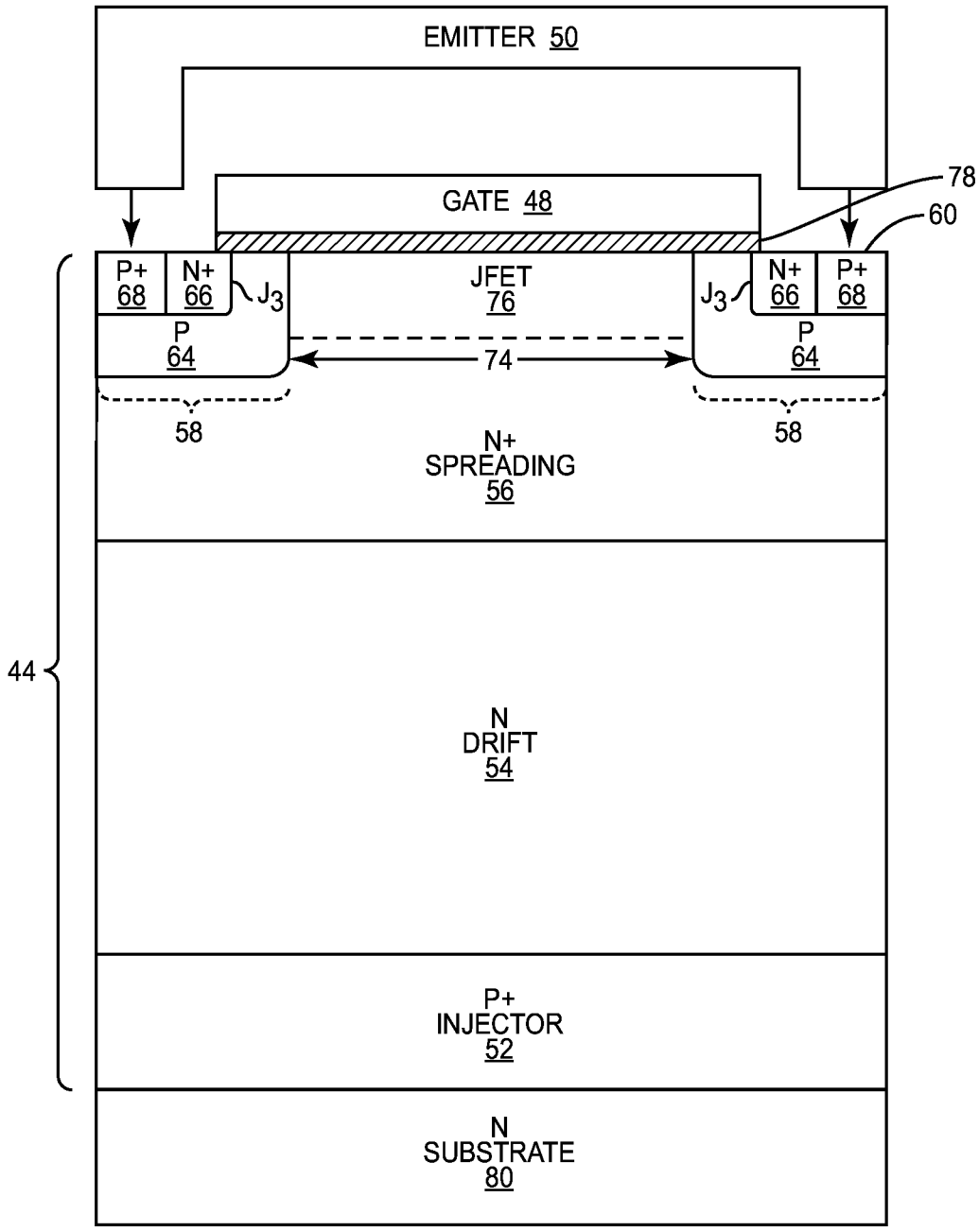
EMITTER 50
GATE 48
78
60
P+ 68
N+ 66
J_3
JFET 76
J_3
N+ 66
P+ 68
P 64
74
P 64
58
58
N+ SPREADING 56
44
N DRIFT 54
P+ INJECTOR 52
N SUBSTRATE 80

FIG. 4G

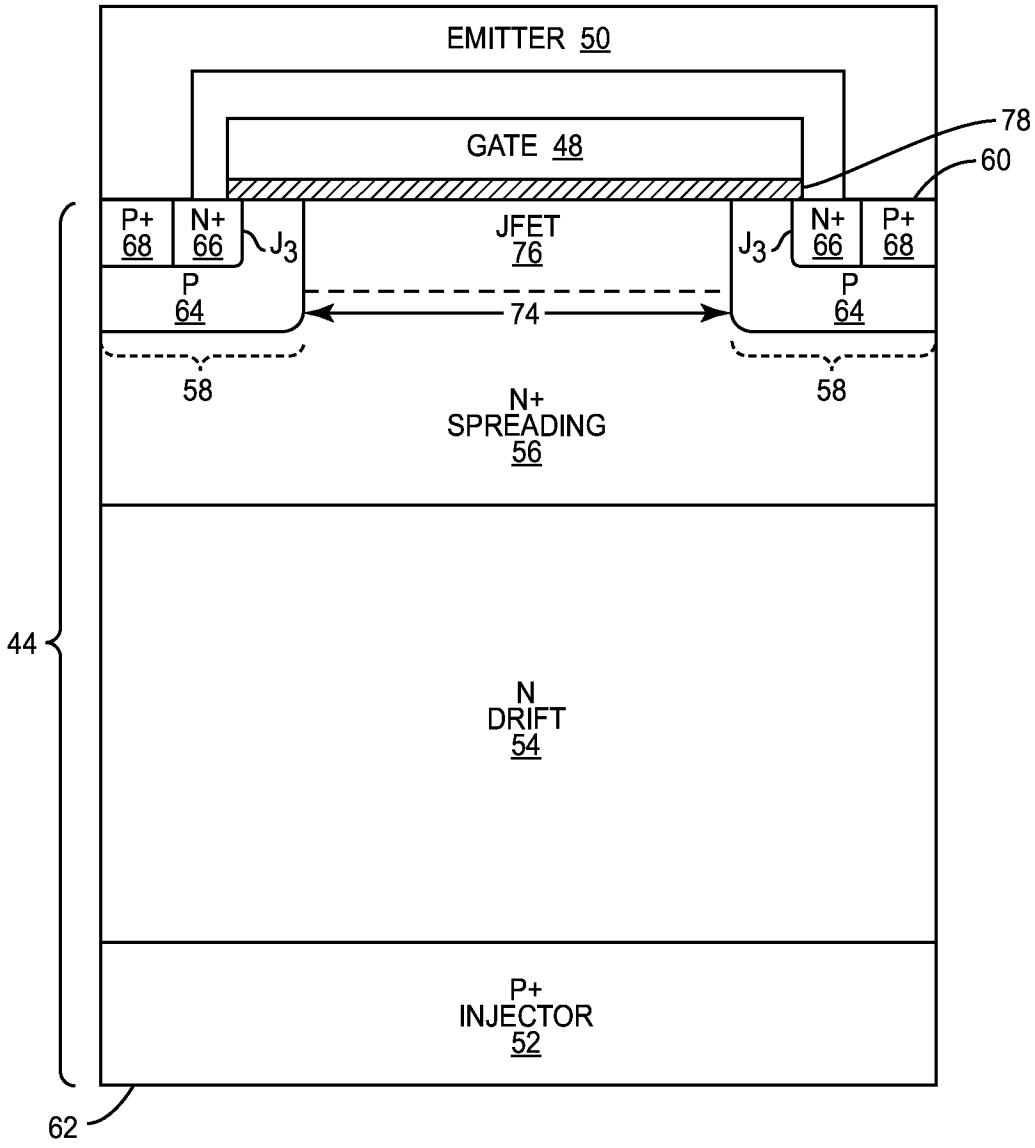
EMITTER 50
GATE 48
78
60
P+ 68
N+ 66
J3
JFET 76
J3
N+ 66
P+ 68
P 64
74
P 64
58
58
N+ SPREADING 56
44
N DRIFT 54
P+ INJECTOR 52
62

FIG. 4H

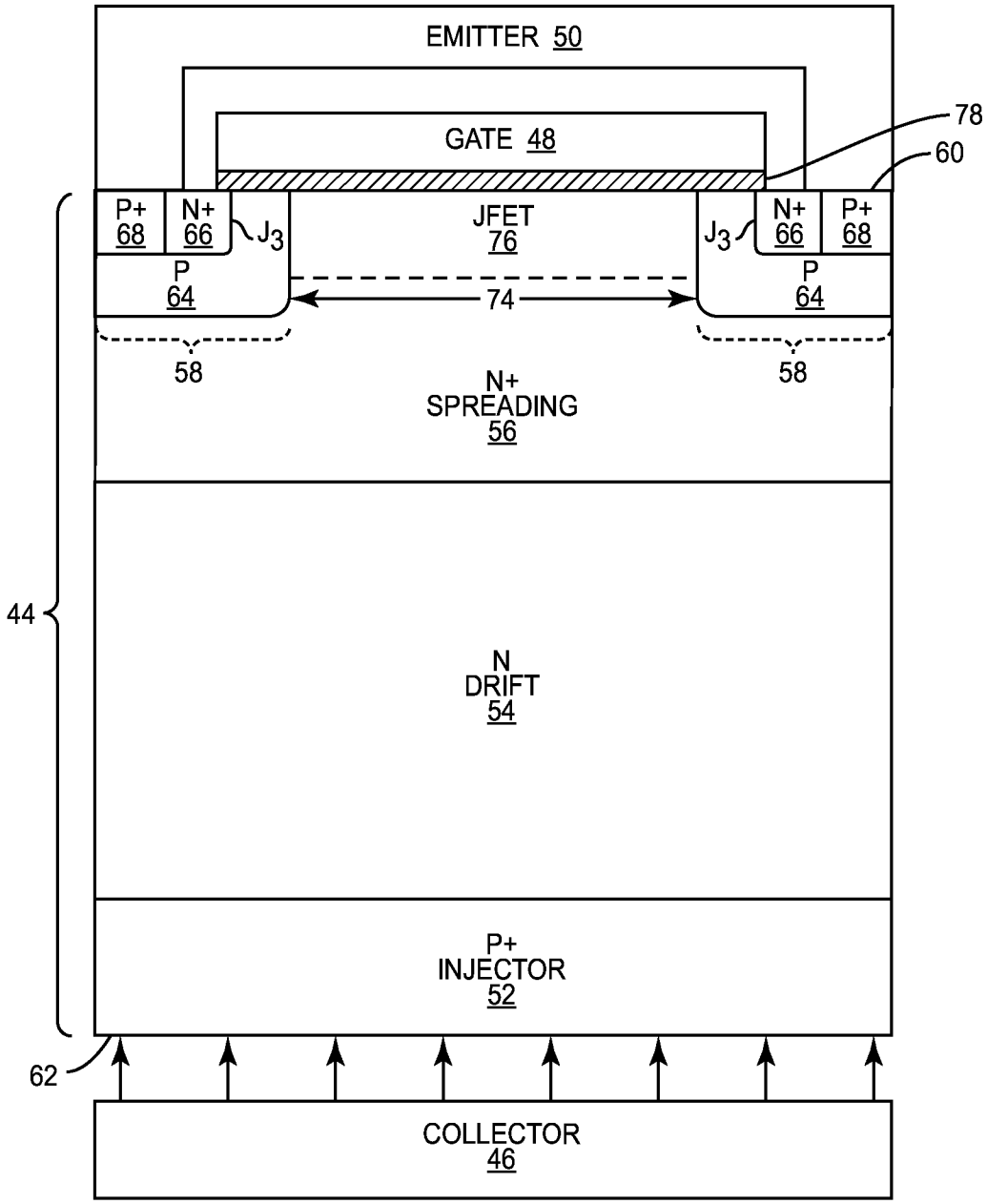
EMITTER 50
GATE 48
78
60
P+ 68
N+ 66
J3
JFET 76
J3
N+ 66
P+ 68
P 64
74
P 64
58
58
N+ SPREADING 56
44
N DRIFT 54
P+ INJECTOR 52
62
COLLECTOR 46

FIG. 4I

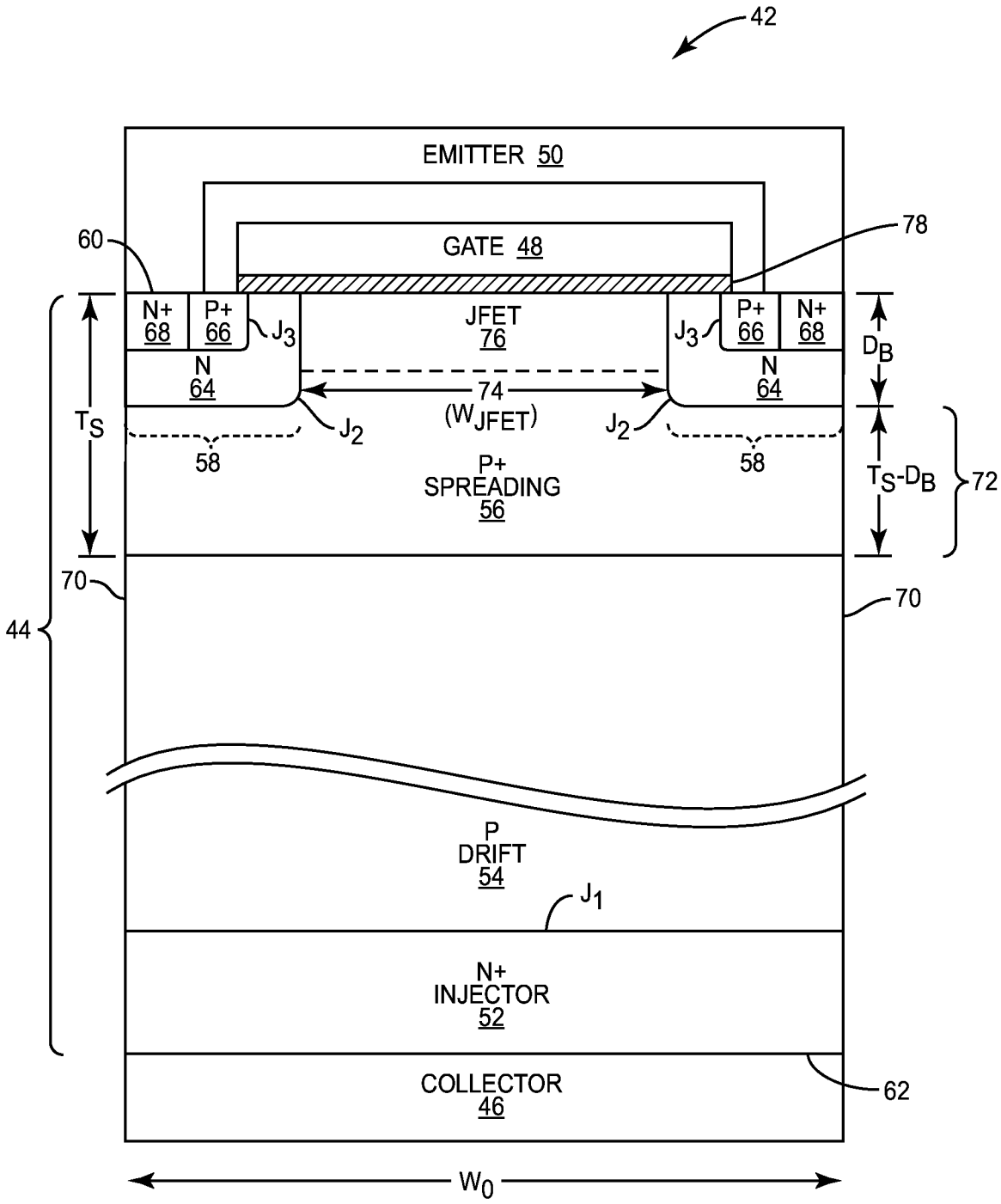
42
EMITTER 50
GATE 48
60
78
N+ 68
P+ 66
J3
JFET 76
J3
P+ 66
N+ 68
N 64
N 64
74 (WJFET)
TS
J2
J2
58
58
P+ SPREADING 56
DB
TS-DB
72
70
70
44
P DRIFT 54
J1
N+ INJECTOR 52
COLLECTOR 46
62
W0

FIG. 5

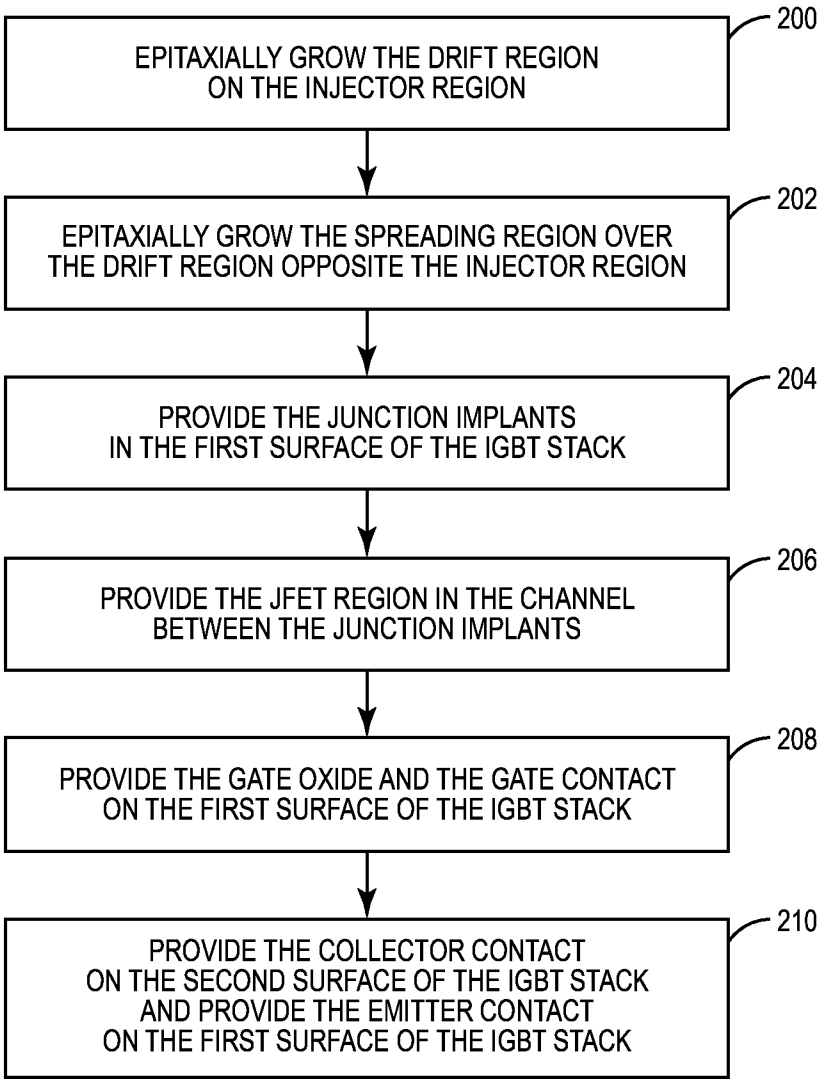
EPITAXIALLY GROW THE DRIFT REGION ON THE INJECTOR REGION
200
EPITAXIALLY GROW THE SPREADING REGION OVER THE DRIFT REGION OPPOSITE THE INJECTOR REGION
202
PROVIDE THE JUNCTION IMPLANTS IN THE FIRST SURFACE OF THE IGBT STACK
204
PROVIDE THE JFET REGION IN THE CHANNEL BETWEEN THE JUNCTION IMPLANTS
206
PROVIDE THE GATE OXIDE AND THE GATE CONTACT ON THE FIRST SURFACE OF THE IGBT STACK
208
PROVIDE THE COLLECTOR CONTACT ON THE SECOND SURFACE OF THE IGBT STACK AND PROVIDE THE EMITTER CONTACT ON THE FIRST SURFACE OF THE IGBT STACK
210

FIG. 6

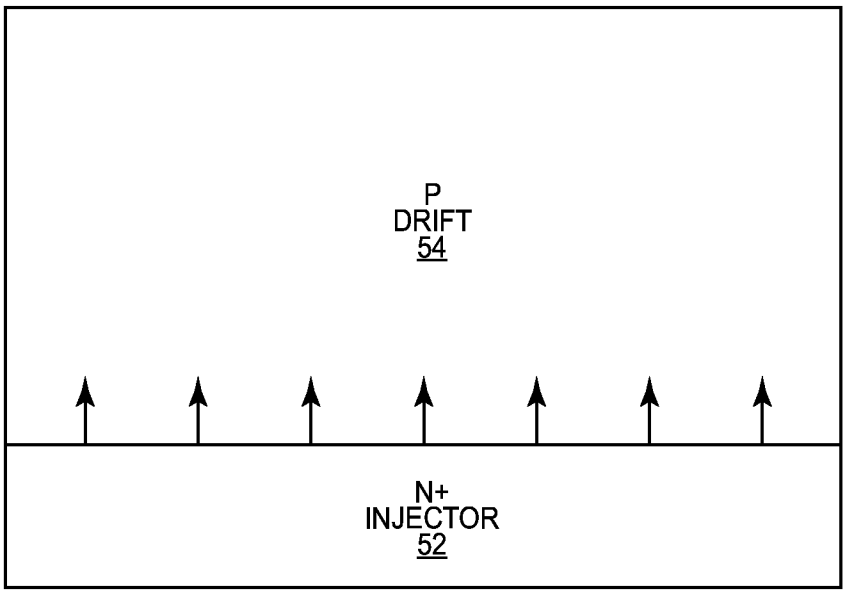

FIG. 7A

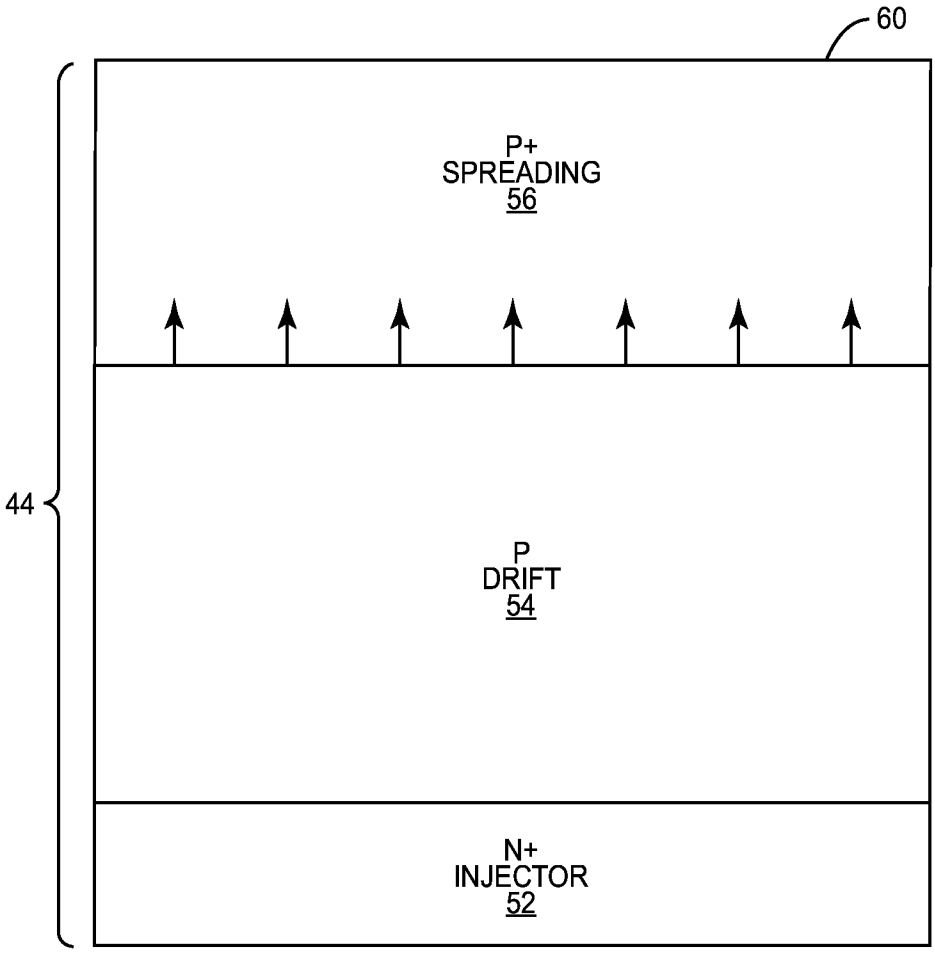

FIG. 7B

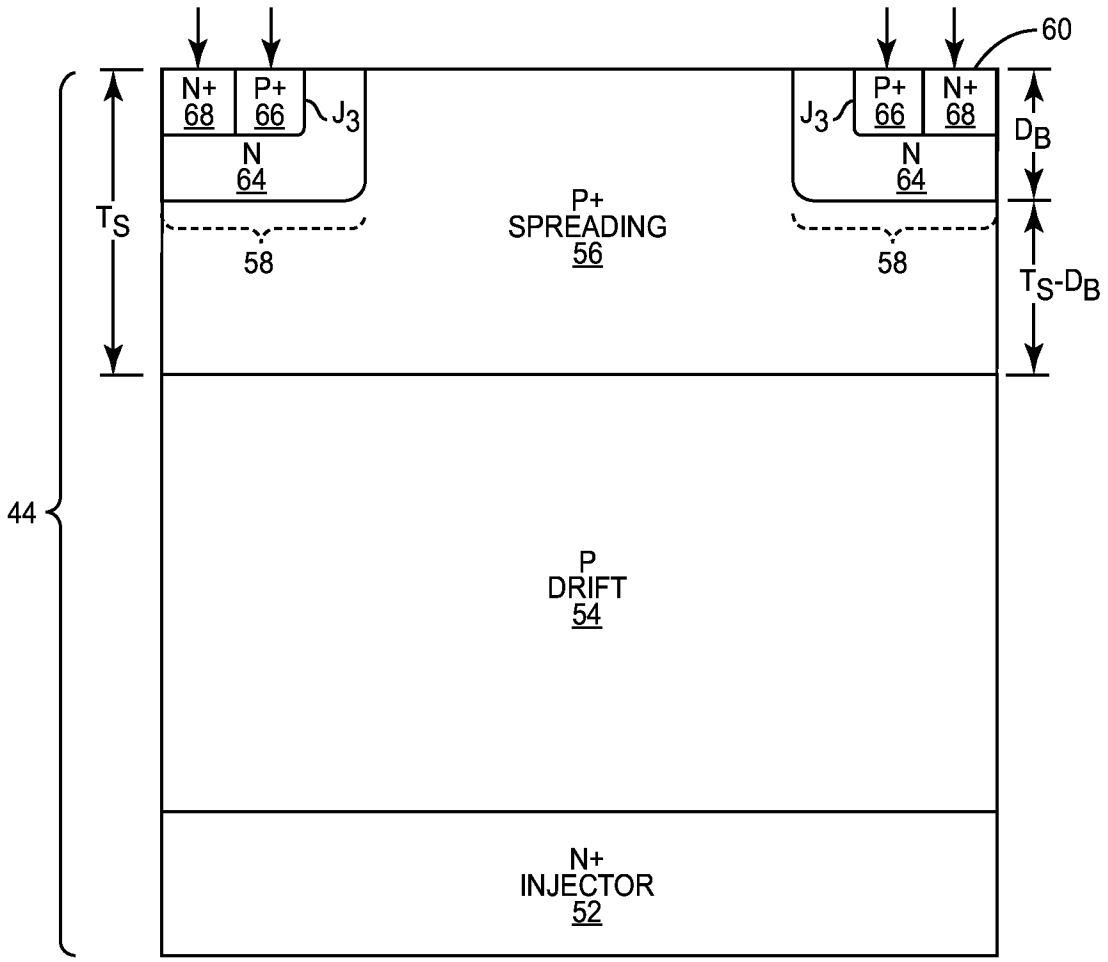
60
N+
68
P+
66
J3
N
64
P+
66
N+
68
J3
N
64
DB
TS
P+
SPREADING
56
58
58
TS-DB
44
P
DRIFT
54
N+
INJECTOR
52

FIG. 7C

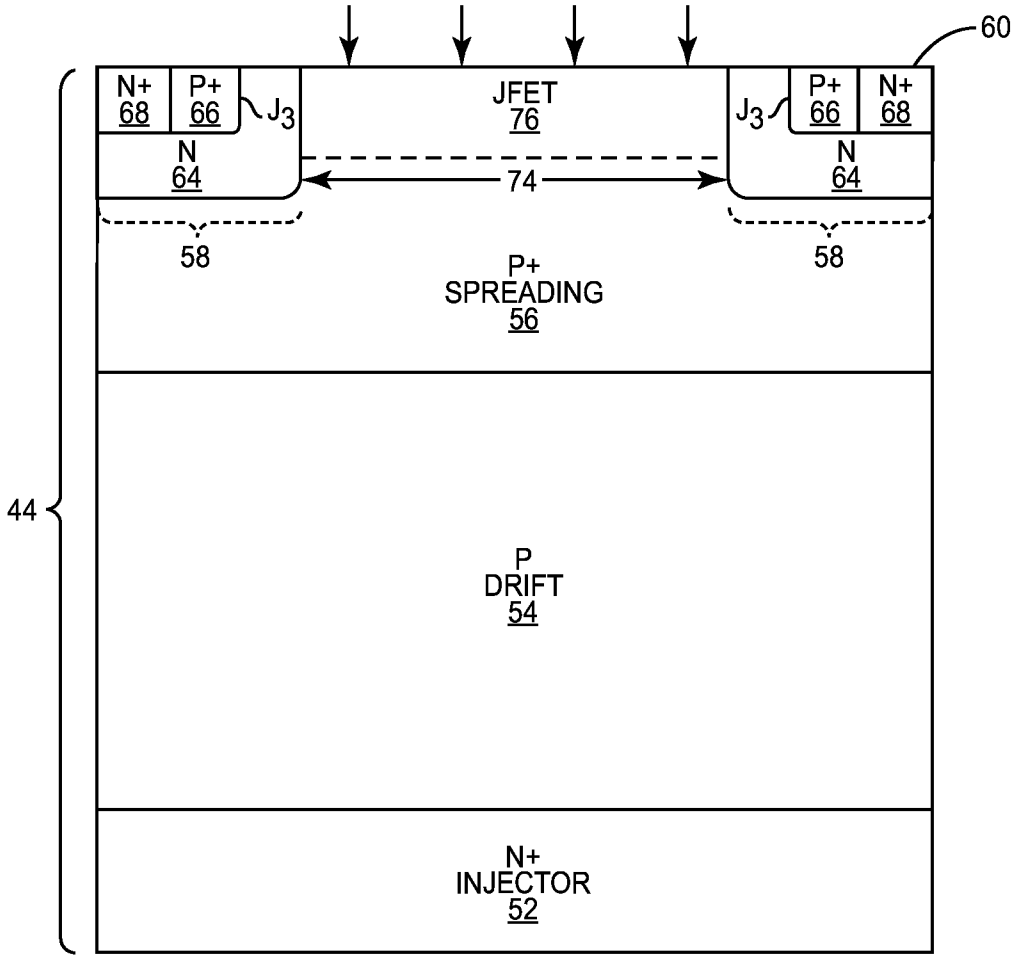
60
N+
68
P+
66
J3
JFET
76
J3
P+
66
N+
68
N
64
74
N
64
58
58
P+
SPREADING
56
44
P
DRIFT
54
N+
INJECTOR
52

FIG. 7D

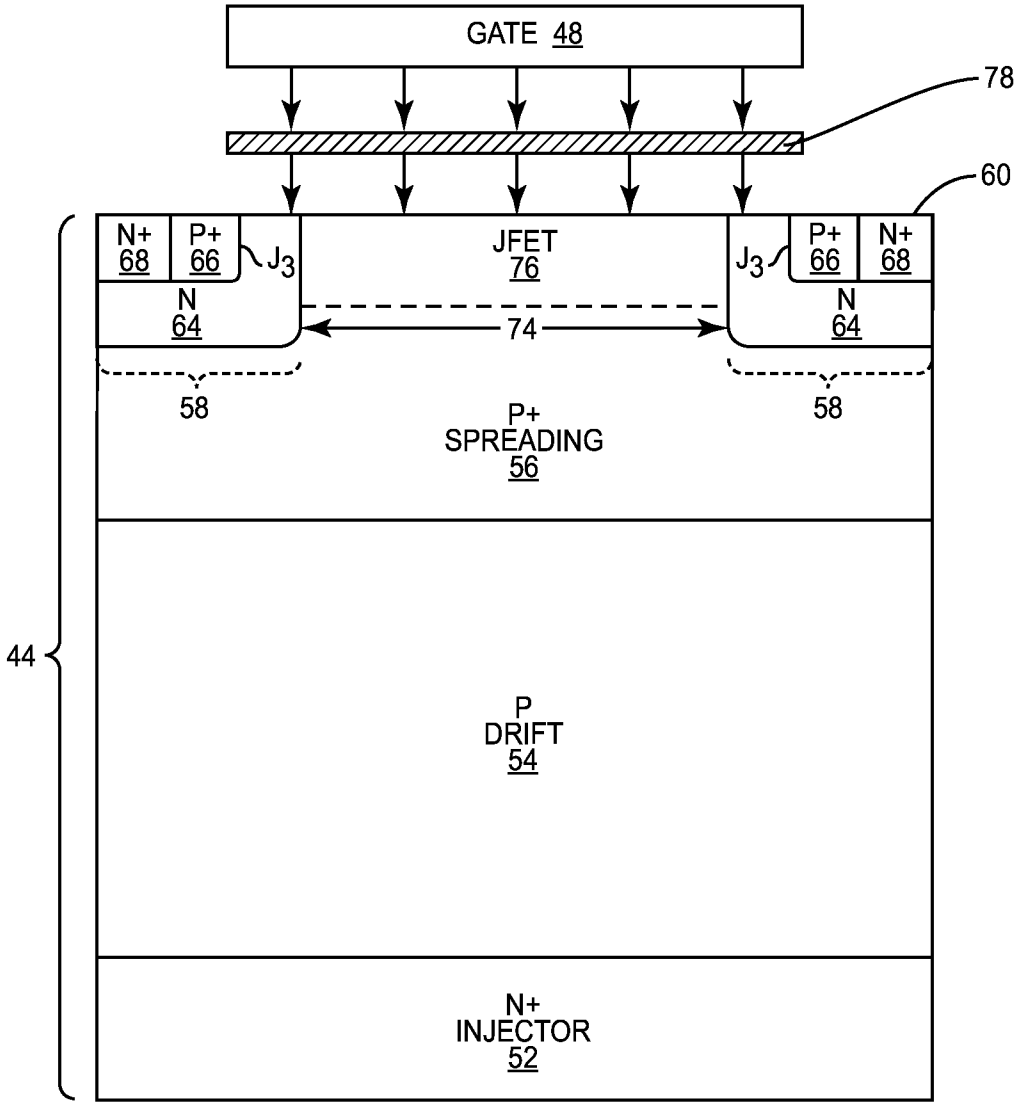
GATE 48
78
60
N+
68
P+
66
J3
JFET
76
J3
P+
66
N+
68
N
64
74
N
64
58
58
P+
SPREADING
56
P
DRIFT
54
N+
INJECTOR
52
44

FIG. 7E

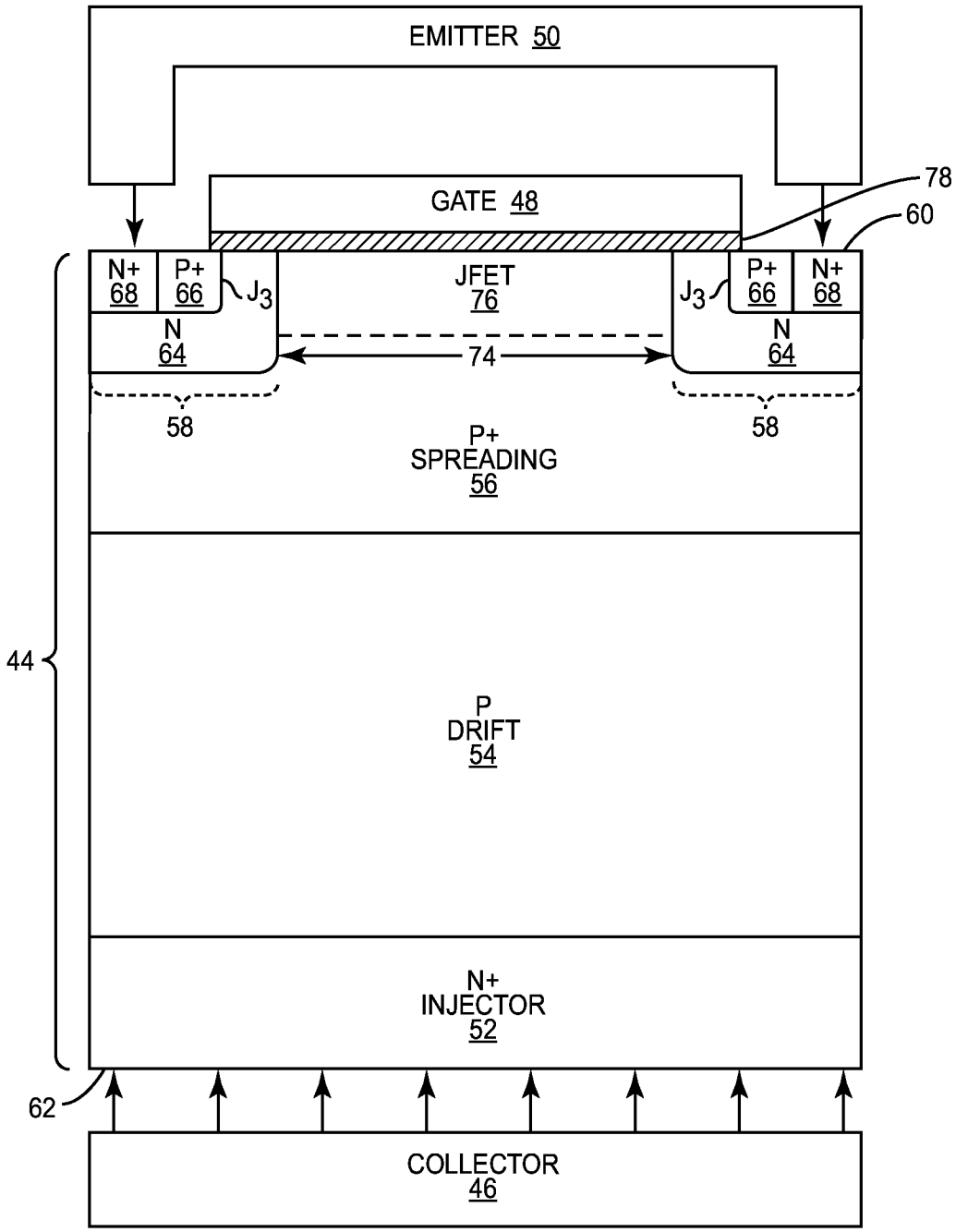
EMITTER 50
GATE 48
78
60
N+
68
P+
66
J3
JFET
76
J3
P+
66
N+
68
N
64
74
N
64
58
58
P+
SPREADING
56
44
P
DRIFT
54
N+
INJECTOR
52
62
COLLECTOR
46

FIG. 7F

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/011015

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/16 H01L29/10 H01L29/739 H01L29/66
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 965 432 A1 (CREE INC [US]) 3 September 2008 (2008-09-03) paragraph [0031] - paragraph [0049] paragraph [0054] figures 1,2 ----- -/--	1-29

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 September 2015	30/09/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kostrzewa, Marek

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/011015

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TAMAKI T ET AL: "Optimization of on -State and Switching Performances for 15-20-kV 4H-SiC IGBTs", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 55, no. 8, 1 August 2008 (2008-08-01) , pages 1920-1927, XP011231879, ISSN: 0018-9383, DOI: 10.1109/TED.2008.926965 page 1920, paragraph I. Introduction - page 1921 page 1923, paragraph B. Design of the CSL and JFET Regions figures 1,7	1-29
X	US 2012/292742 A1 (ITOH SATOMI [JP] ET AL) 22 November 2012 (2012-11-22) paragraph [0021] - paragraph [0032] paragraph [0040] figure 1	1-29
X	GB 2 243 952 A (INT RECTIFIER CORP [US]) 13 November 1991 (1991-11-13) page 24, line 4 - page 35, line 3 figures 9-20	1-29
X	US 2011/101375 A1 (ZHANG QINGCHUN [US]) 5 May 2011 (2011-05-05) paragraph [0041] - paragraph [0057] figures 1-5	1-29
A	US 2004/119076 A1 (RYU SEI-HYUNG [US]) 24 June 2004 (2004-06-24) the whole document	1-29

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Information on patent family members

International application No
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