(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 October 2017 (05.10.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/172536 A1

(51) International Patent Classification:
H01L 21/3065 (2006.01) *H01L 21/67* (2006.01)
H01L 21/66 (2006.01) *H05H 1/46* (2006.01)
H01L 21/02 (2006.01)

(21) International Application Number:
PCT/US2017/024138

(22) International Filing Date:
24 March 2017 (24.03.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/316,021 31 March 2016 (31.03.2016) US

(71) Applicant: **TOKYO ELECTRON LIMITED** [JP/JP]; Akasaka Biz Tower, 3-1 Akasaka 5-chome, Minato-ku, Tokyo 107-6325 (JP).

(71) Applicant *(for JP only)*: **TOKYO ELECTRON U.S. HOLDINGS, INC.** [US/US]; 2400 Grove Boulevard, Austin, Texas 78741 (US).

(72) Inventors: **COPPA, Brian J.**; 709 Spyglass Way, Eagle, Idaho 83616 (US). **VEDHACHALAM, Deepak**; 6488 S Liveoak Pl., Boise, Idaho 83716 (US). **DASSAPA, Francois C.**; 42055 Camino Santa Barbara, Fremont, California 94539 (US).

(74) Agent: **MITROVIC, Andrej**; Tokyo Electron U.S. Holdings, Inc., 2400 Grove Blvd., Austin, Texas 78741 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA,

[Continued on next page]

(54) Title: CONTROLLING DRY ETCH PROCESS CHARACTERISTICS USING WAFERLESS DRY CLEAN OPTICAL EMISSION SPECTROSCOPY

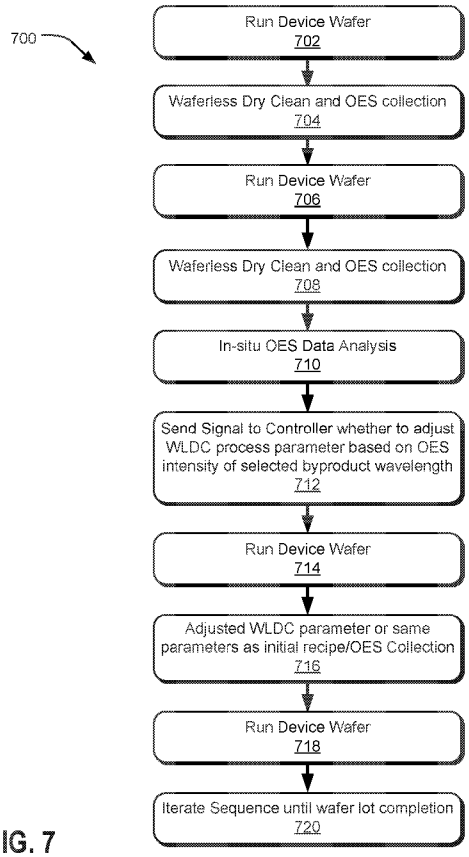

FIG. 7

(57) Abstract: Described herein are architectures, platforms and methods for acquiring optical emission spectra from an optical emission spectroscopy system by flowing a dry cleaning gas into a plasma processing chamber of the plasma processing system and igniting a plasma in the plasma processing chamber to initiate the waferless dry cleaning process.

WO 2017/172536 A1

MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

CONTROLLING DRY ETCH PROCESS CHARACTERISTICS USING WAFERLESS DRY CLEAN OPTICAL EMISSION SPECTROSCOPY

RELATED APPLICATIONS

[0001] This application is based on and claims priority to U.S. Provisional Patent Application No. 61/316,021, entitled "METHOD FOR CONTROLLING DRY ETCH PROCESS CHARACTERISTICS USING WAFERLESS DRY CLEAN OPTICAL EMISSION SPECTROSCOPY" (Ref. No. TEA-136US1-PRO), filed on March 31, 2016.

BACKGROUND

[0002] One of the problems with dry etch processes for via and trench features is the variation in the etch profile during the processing of a full lot of wafers. This may be due to the build-up of carbon (C) and fluorine (F) (collectively referred to as CF)-based etch gas constituents used for passivation and etch selectivity, which are used to form specific etch profiles for patterned wafers in semiconductor processing. If these constituents are not effectively removed from the chamber to the same degree during dry clean cycles between wafers, polymer deposition can accumulate in a chamber leading to the build-up of a film layer which can lead to particle formation and peeling, and can generate defects and device failure on a wafer. In addition, ineffective or inconsistent waferless dry cleaning (WLDC) of the chamber between device wafers, can lead to varying residual CF constituents in the chamber, which subsequently are introduced during a successive dry etch process of a device wafer that affects the uniformity of etch profile characteristics from one wafer lot to the next. The wafers making up a lot.

SUMMARY OF INVENTION

[0003] This invention relates to the optimization of a waferless dry clean (WLDC) process in order to reduce the dry etch wafer-to-wafer process variation of patterned device wafers of a lot. Optical Emission Spectroscopy (OES) is used to monitor light emission from a plasma, such as a dry cleaning process that is performed between each process wafer of a lot, to minimize deposition build-up in a plasma processing chamber. The OES of various constituents, such as chlorine (C) and fluorine (F) being exhausted during a dry clean cycle is indicative of the effectiveness of the cleaning process. The OES of the constituents can be used to gauge and optimize the WLDC process in order to improve etch wafer process control.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The detailed description is described with reference to accompanying figures. In the figures, the left-most digit(s) of a reference number identifies the figure in which the reference number first appears. The same numbers are used throughout the drawings to reference like features and components.

[0005] FIG. 1 is a cross-sectional view showing an example schematic configuration of a capacitively coupled plasma (CCP) processing system in accordance with embodiments herein.

[0006] FIG. 2 is an example schematic block diagram of an example plasma processing system implementing optical emission spectroscopy (OES) to determine OES spectra, as part of an overall monitoring system to monitor gas constituents inside the plasma chamber.

[0007] FIG. 3 are example graphs that illustrate a peak in optical emission spectroscopy (OES) spectra of a residual constituent fluorine (F) by-product during a non-optimized WLDC clean process and the constant increase of the

amount of the residual constituent over the time period of the dry clean process.

[0008] FIG. 4 is an example flowchart that illustrates a particular dry clean process condition.

[0009] FIG. 5 is a process chart illustrating an example process flow for monitoring and controlling a waferless dry cleaning process in a plasma processing system based on optical emission spectroscopy (OES) as described herein.

[0010] FIG. 6 is an example graph that illustrates optical emission spectroscopy (OES) detection of an endpoint for a residual fluorine (F) by-product constituent during an optimized waferless dry clean associated with clean chamber states.

[0011] FIG. 7 is a process chart illustrating an example process flow for optical emission spectroscopy (OES) process control.

DETAILED DESCRIPTION

[0012] Described herein are architectures, platforms and methods for analyzing residue constituents in a waferless dry clean (WLDC) process, and in particular analysis using Optical Emission Spectroscopy (OES). A process control monitor/metric such as OES can be utilized to analyze the effectiveness of a WLDC process by evaluation of carbon (C) and fluorine (F) based wavelengths in the spectra for a batch of wafers.

[0013] Moreover, a WLDC process can be optimized based on OES spectra of undesirable residue constituents being removed by the dry cleaning process following one particular device wafer process. Typically, an ineffective WLDC process will never show the leveling out in OES intensity for the wavelength examined of a constituent that is intended to be removed by the WLDC. However, the OES spectra of this constituent

would show the leveling out in intensity once the endpoint was reached for the WLDC process; this endpoint time can be utilized for determining the ideal completion time for the WLDC process in order to optimize production throughput. In other words, by optimizing the WLDC process (e.g., minimizing the time to perform the WLDC process), optimal usage and production may be realized.

[0014] Wet cleans of a plasma processing chamber may be routinely performed. By optimizing the WLDC process, the time or period between such wet cleans may be also be optimized. Optimization of the herein described parameters for a WLDC process can maximize the time between wet cleans. Furthermore, useful life of components in a plasma processing chamber or system may be prolonged with an optimized WLDC process.

[0015] Furthermore, by reducing the variation in the C and F intensity levels between device wafers collectively for a wafer lot using a more optimal WLDC process, the uniformity of the etch profile characteristics of the wafer lot can be improved. Excess or inconsistent C and F constituents due to an inconsistent WLDC process can cause variations in the subsequent plasma etch performance for patterned device wafers that can lead to an insufficient critical dimension variation across patterned device wafers of a wafer lot.

[0016] OES can be used to optimize the consistency and effectiveness of a WLDC for removing undesirable remnant constituents resulting from a device wafer etch process. Thus, OES of C and F based species in an OES spectra within a wafer lot are directly correlated to key metrics such as the etch profile uniformity of a device wafer lot. In addition, it has been found that bare silicon wafers exposed to the same etch process as a device wafer can be used to optimize the WLDC, since OES shows the same response and trends with respect to adjustment of WLDC process parameters. Examples of process

parameters include, but are not limited to radio frequency (RF) or microwave power supplied to a plasma processing chamber of a plasma processing system; RF or microwave power pulse frequency supplied to the plasma processing chamber; RF or microwave pulse duty cycle to the plasma processing chamber; RF power supplied to a substrate holder in the plasma processing chamber; magnetic field of one of more magnets proximate the substrate holder; DC bias of the substrate holder; DC bias voltage supplied to at least one electrode arranged proximate the substrate holder; dry cleaning gas flow rate; wafer chuck temperature, dry cleaning gas pressure; and duration of the waferless dry cleaning process.

[0017] Improvement in a WLDC process for removal of C and F such as using a higher oxygen plasma power may be found between either bare silicon or device wafers based on the resulting OES spectra; allowing optimization of a WLDC process without consuming high-cost device wafers. In certain implementations, a dummy substrate or wafer may be used as described herein. Therefore, an optimal time for a WLDC process may be achieved, where a minimal time is determined for such a WLDC process. Furthermore, an optimal WLDC process can enhance etch profile wafer-to-wafer uniformity for wafer lots.

[0018] It has been found that OES can be used to optimize the consistency and effectiveness of a WLDC for removing undesirable remnant constituents resulting from a device wafer etch process. Thus, OES of C and F constituent spectra within a wafer lot are directly correlated to key metrics such as the wafer-to-wafer etch profile uniformity of a device wafer lot. In addition, it has been found that bare silicon wafers exposed to the same etch process as a device wafer, can be used to optimize the WLDC since OES shows the same response and trend with respect to adjustment of WLDC process parameters including but not limited to gas pressures, gas flows, plasma exposure time, plasma power, bias voltage, and temperature.

[0019] For example, improvement in a WLDC process for the removal of C and F and CF polymer deposition accomplished by using a higher oxygen plasma power may be found both in bare silicon and device wafers based on a resulting OES spectra; allowing optimization of a WLDC process without consuming high-cost device production wafers. Therefore, the use of higher oxygen plasma power accelerates the time (and subsequent wafer output) and lessens the cost for optimization of a WLDC based on OES analysis to determine the optimal WLDC process or device wafers to enhance the wafer-to-wafer etch profile uniformity within the wafer lot. The use of OES spectra analysis may also be found to be indicative of cleaning effectiveness for a wide variety of etch process conditions, as the variation in undesirable remnant species for a batch of wafers can be used to predict changes in the uniformity of subsequently formed etch profiles for multiple wafers within a wafer lot.

[0020] Furthermore, a more effective WLDC process reduces the need for additional bare silicon dummy wafers to be run between device wafers to achieve better etch process control to remove residue accumulating in a chamber or conditioning to stabilize the chamber environment; thus reducing overall process time and cost. In addition an optimal WLDC process that keeps the chamber cleaner long-term lessens the frequency of wet clean preventive maintenance cycles, which ultimately improves chamber utilization and productivity.

[0021] In certain instances, an etch process may introduce a wide variety of gas species into the chamber such as C and F, which ultimately lead to polymer deposition within the plasma processing chamber that can form particles within the plasma processing chamber and on the wafer surface. OES spectra can be collected during the subsequent clean to evaluate the gas species removed from the chamber during a WLDC process that runs in the chamber after processing a device wafer.

[0022] In comparison between a wafer lot having a process with a less effective WLDC process with less effective residual constituent (CF) removal, versus a wafer lot having a more effective WLDC process with more effective residual constituent (CF) removal, the less effective WLDC process may not show a leveling out of OES intensity for the F wavelength examined over WLDC process time. In contrast, the more effective WLDC process can indicate an OES endpoint for this exact same F constituent for all WLDC processes occurring between each device wafer etch process for the lot that could be categorized as a clean condition for the chamber. In addition, particle monitor wafers may be cycled through the plasma processing chamber before and after each wafer lot to analyze particle levels. A long-term benefit of a more effective WLDC process may be seen in reducing increasing trends of particle levels in a chamber, since polymer deposition can accumulate over time leading to peeling from chamber surfaces for an insufficient WLDC.

[0023] For a more effective WLDC process, when using higher oxygen or O2 pressure, higher O2 power and higher bias voltage may significantly improve within-lot etch uniformity. A reduction in the range and standard deviation of the means of the bottom via critical dimension or CD of an etch profile across a lot of wafers may be realized with the more effective WLDC. Furthermore, a wafer lot using this more effective WLDC may also have a lower within-wafer etch uniformity for various CDs such as a bottom via width CD. Particle levels may reduce for the more effective WLDC in addition to less added defects being measured for the wafer lot with the enhanced WLDC process. A need for adding additional bare silicon dummy chamber conditioning wafers to be processed during overall wafer lot processing with a particular recipe may be eliminated, saving on overall wafer lot processing time.

[0024] OES analysis during the WLDC processes running between device wafers for wafer lots may show the more effective WLDC process operating at

higher O2 pressure, higher O2 power and with DC bias voltage. A more effective and consistent F removal from the plasma processing chamber, as the main constituent remaining after a device wafer etch process, generated from higher power oxygen radicals and ions, may create a cleaner and more consistent environment in the plasma processing chamber for successive wafers in the wafer lot. The overall within-wafer and within-lot etch uniformity can improve. A one to one correlation may be realized between the reduction of the within-lot F variation in the WLDC OES and the reduction in the standard deviation of the mean bottom CD per wafer in the lot. For example, OES WLDC processes can be used as an in-situ diagnostic to enhance etch process control, when OES WLDC processes are linked with process automation features of plasma processing systems/chambers to optimize etch uniformity in a manufacturing fab.

[0025] In addition, other optical diagnostic methods, such as laser induced fluorescence (LIF), laser interferometry, mass spectrometry, residual gas analysis, FTIR, etc., can be used instead of OES for monitoring the WLDC process with the same or similar outcome.

[0026] FIG. 1 shows a schematic cross-sectional view of an example of a capacitively coupled plasma (CCP) processing apparatus or plasma processing system 100 in accordance with embodiments herein. It is to be understood that other processing systems can be implemented, such as radial line slot antenna (RLSA) and inductively coupled plasma (ICP) processing systems may be implemented. In particular implementations, the plasma processing system 100 is used for a WLDC process, which may implement an OES spectra analysis of residual constituents, such as C and F. Furthermore, plasma analysis may be performed. In addition, endpoint analysis may be performed. Duration of the WLDC process can be a parameter that may be optimized during a WLDC process using OES data of residual constituents.

[0027] The plasma processing system 100 may be used for multiple operations including ashing, etching, deposition, cleaning, plasma polymerization, plasma-enhanced chemical vapor deposition (PECVD), plasma-enhanced atomic layer deposition (PEALD) and so forth. Plasma processing can be executed within plasma processing chamber 102, which can be a vacuum chamber made of a metal such as aluminum or stainless steel. The plasma processing chamber 102 is grounded such to ground(s) 104. The plasma processing chamber 102 defines a processing vessel providing a process space PS 106 for plasma generation. An inner wall of the plasma processing chamber 102 can be coated with alumina, yttria, or other protectant. The plasma processing chamber 102 can be cylindrical in shape or have other geometric configurations.

[0028] At a lower, central area within the plasma processing chamber 102, a substrate holder or susceptor 108 (which can be disc-shaped) can serve as a mounting table on which, for example, a substrate W 110 to be processed (such as a semiconductor wafer) can be mounted. Substrate W 110 can be moved into the plasma processing chamber 102 through loading/unloading port 112 and gate valve 114. Susceptor 108 forms part of a lower electrode 116 (lower electrode assembly) as an example of a second electrode acting as a mounting table for mounting substrate W 110 thereon. Specifically, the susceptor 108 is supported on a susceptor support 118, which is provided at substantially a center of the bottom of plasma processing chamber 102 via an insulating plate 120. The susceptor support 118 can be cylindrical. The susceptor 108 can be formed of, e.g., an aluminum alloy. Susceptor 108 is provided thereon with an electrostatic chuck 122 (as part of the lower electrode assembly 116) for holding the substrate W 110. The electrostatic chuck 122 is provided with an electrode 124. Electrode 124 is electrically connected to DC power source 126 (direct current power source). The electrostatic chuck 122 attracts the substrate W 110 thereto via an

electrostatic force generated when DC voltage from the DC power source 126 is applied to the electrode 124. DC bias of the substrate holder or susceptor 108, and DC bias voltage supplied to at least one of electrodes 116 and 124, can be parameters that may be optimized during a WLDC process using OES data of residual constituents.

[0029] The susceptor 108 can be electrically connected with a high-frequency power source 130 via a matching unit 132. This high-frequency power source 130 (a second power source) can output a high-frequency voltage in a range from, for example, 2 MHz to 20 MHz. Applying high frequency bias power causes ions, in the plasma, generated in the plasma processing chamber 102, to be attracted to substrate W 110. A focus ring 134 is provided on an upper surface of the susceptor 108 to surround the electrostatic chuck 122. In addition, RF or microwave power (not shown) may be provided to the plasma processing chamber 102. RF or microwave power supplied to the plasma processing chamber; RF or microwave power pulse frequency; RF or microwave pulse duty cycle; and RF power supplied to a substrate holder or susceptor 108, in the plasma processing chamber 102 can be parameters that may be optimized during a WLDC process using OES data of residual constituents.

[0030] An inner wall member 136, which can be cylindrical and formed of, e.g., quartz, is attached to the outer peripheral side of the electrostatic chuck 122 and the susceptor support 118. The susceptor support 118 includes a coolant flow path 138. The coolant flow path 138 communicates with a chiller unit (not shown), installed outside the plasma processing chamber 102. Coolant flow path 138 is supplied with coolant (cooling liquid or cooling water) circulating through corresponding lines. Accordingly, a temperature of the substrate W 110 mounted on/above the susceptor 108 can be accurately controlled. A gas supply line 140, which passes through the susceptor 108 and the susceptor support 118, is

configured to supply heat transfer gas to an upper surface of the electrostatic chuck 122. A heat transfer gas (also known as backside gas) such as helium (He) can be supplied between the substrate W 110 and the electrostatic chuck 122 via the gas supply line 140 to assist in heating substrate W 110.

[0031] An exhaust path 142 can be formed along an outer periphery of inner wall member 136 and an inner sidewall surface of the plasma processing chamber 102. An exhaust port 144 (or multiple exhaust ports) is provided in a bottom portion of the exhaust path 142. A gas exhaust unit 146 is connected to each exhaust port via gas exhaust line 148. The gas exhaust unit 146 can include a vacuum pump such as a turbo molecular pump configured to decompress the plasma processing space within the plasma processing chamber 102 to a desired vacuum condition. The gas exhaust unit 146 evacuates the inside of the plasma processing chamber 102 to thereby depressurize an inner pressure thereof up to a desired degree of vacuum.

[0032] An upper electrode 150 (that is, an upper electrode assembly), is an example of a first electrode and is positioned vertically above the lower electrode 116 to face the lower electrode 116 in parallel. The plasma generation space or process space PS 106 is defined between the lower electrode 116 and the upper electrode 150. The upper electrode 150 includes an inner upper electrode 152 having a disk shape, and an outer upper electrode 154 can be annular and surrounding a periphery of the inner upper electrode 152. The inner upper electrode 152 also functions as a processing gas inlet for injecting a specific amount of processing gas into the process space PS 106 above substrate W 110 mounted on the lower electrode 116.

[0033] More specifically, the inner upper electrode 152 includes electrode plate 156 (which is typically circular) having gas injection

openings 158. Inner upper electrode 152 also includes an electrode support 160 detachably supporting an upper side of the electrode plate 156. The electrode support 160 can be formed in the shape of a disk having substantially a same diameter as the electrode plate 156 (when electrode plate 156 is embodied as circular in shape). In alternative embodiments, electrode plate 156 can be square, rectangular, polygonal, etc. The electrode plate 156 can be formed of a conductor or semiconductor material, such as Si, SiC, doped Si, Aluminum, and so forth. The electrode plate 156 can be integral with upper electrode 150 or detachably supported by electrode support 160 for convenience in replacing a given plate after surface erosion. The upper electrode 150 can also include a cooling plate or cooling mechanism (not shown) to control temperature of the electrode plate 156.

[0034] The electrode support 160 can be formed of, e.g., aluminum, and can include a buffer chamber 162. Buffer chamber 162 is used for diffusing process gas and can define a disk-shaped space. Processing gas from a process gas supply system 164 supplies gas to the upper electrode 150. The process gas supply system 164 can be configured to supply a processing gas for performing specific processes, such as film-forming, etching, and the like, on the substrate W 110. The process gas supply system 164 is connected with a gas supply line 166 forming a processing gas supply path. The gas supply line 166 is connected to the buffer chamber 162 of the inner upper electrode 152. The processing gas can then move from the buffer chamber 162 to the gas injection openings 158 at a lower surface thereof. A flow rate of processing gas introduced into the buffer chamber 162 can be adjusted by, e.g., by using a mass flow controller. Further, the processing gas introduced is uniformly discharged from the gas injection openings 158 of the electrode plate 156 (showerhead electrode) to the process space PS 106. The inner upper electrode 152 then functions in part to provide a showerhead electrode

assembly. Dry cleaning gas flow rate, and dry cleaning gas pressure can be parameters that may be optimized during a WLDC process using OES data of residual constituents. Dry cleaning gases can include oxygen, an oxygen-containing gas, HCl, F2, Cl2, hydrogen, nitrogen, argon, SF6, C2F6, NF3, CF4, or a mixture of two or more of such gases.

[0035] A dielectric 168, having a ring shape, can be interposed between the inner upper electrode 152 and the outer upper electrode 154. An insulator 170, which can be a shield member having a ring shape and being formed of, e.g., alumina, is interposed between the outer upper electrode 154 and an inner peripheral wall of the plasma processing chamber 102 in an air tight manner.

[0036] The outer upper electrode 154 is electrically connected with a high-frequency power source 172 (first high-frequency power source) via a power feeder 174, an upper power feed rod 176, and a matching unit 178. The high-frequency power source 172 can output a high-frequency voltage having a frequency of 13 MHz (megahertz) or higher (e.g. 60 MHz), or can output a very high frequency (VHF) voltage having a frequency of 30-300 MHz. This power source 172 can be referred to as the main power supply as compared to a bias power supply. The power feeder 174 can be formed into, e.g., a substantially cylindrical shape having an open lower surface. The power feeder 174 can be connected to the outer upper electrode 154 at the lower end portion thereof. The power feeder 174 is electrically connected with the lower end portion of the upper power feed rod 176 at the center portion of an upper surface thereof. The upper power feed rod 176 is connected to the output side of the matching unit 178 at the upper end portion thereof. The matching unit 178 is connected to the high-frequency power source 172 and can match load impedance with the internal impedance of the high-frequency power source 172.

Note, however, that outer upper electrode 154 is optional and embodiments can function with a single upper electrode.

[0037] Power feeder 174 can be cylindrical having a sidewall whose diameter is substantially the same as that of the plasma processing chamber 102. The ground conductor 180 is connected to the upper portion of a sidewall of the plasma processing chamber 102 at the lower end portion thereof. The upper power feed rod 176 passes through a center portion of the upper surface of the ground conductor 180. An insulating member 182 is interposed at the contact portion between the ground conductor 180 and the upper power feed rod 176.

[0038] The electrode support 160 is electrically connected with a lower power feed rod 184 on the upper surface thereof. The lower power feed rod 184 is connected to the upper power feed rod 176 via a connector. The upper power feed rod 176 and the lower power feed rod 184 form a power feed rod for supplying high-frequency electric power from the high-frequency power source 172 to the upper electrode 150. A variable condenser 186 is provided in the lower power feed rod 184. By adjusting the capacitance of the variable condenser 186, when the high-frequency electric power is applied from the high-frequency power source 160, the relative ratio of an electric field strength formed directly under the outer upper electrode 154 to an electric field strength formed directly under the inner upper electrode 172 can be adjusted. The inner upper electrode 152 of the upper electrode 150 is electrically connected with a low pass filter (LPF) 188. The LPF 188 blocks high frequencies from the high-frequency power source 172 while passing low frequencies from the high-frequency power source 130 to ground. A lower portion of the system, the susceptor 108, forming part of the lower electrode 120, is electrically connected with a high pass filter (HPF) 190. The HPF 190 passes high frequencies from the high-frequency power source 172 to ground.

[0039] High-frequency electric power in a range from about 3 MHz to 150 MHz, is applied from the high-frequency power source 172 to the upper electrode 150. This results in a high-frequency electric field being generated between the upper electrode 150 and the susceptor 108 or lower electrode 116. Processing gas delivered to process space PS 106 can then be dissociated and converted into a plasma. A low frequency electric power in a range from about 0.2 MHz to 20 MHz can be applied from the high-frequency power source 130 to the susceptor 108 forming the lower electrode 116. In other words, a dual frequency system can be used. As a result, ions in the plasma are attracted toward the susceptor 108, and thus anisotropy of etching is increased by ion assistance. Note that for convenience, FIG. 1 shows the high-frequency power source 172 supplying power to the upper electrode 150. In alternative embodiments, the high-frequency power source 172 can be supplied to the lower electrode 116. Thus, both main power (energizing power) and the bias power (ion acceleration power) can be supplied to the lower electrode.

[0040] Components of the plasma processing system 100 can be connected to, and controlled by, a control unit 192, which in turn can be connected to a corresponding storage unit 194 and user interface 196. Various plasma processing operations can be executed via the user interface 196, and various plasma processing recipes and operations can be stored in storage unit 194. Accordingly, a given substrate can be processed within the plasma processing chamber with various microfabrication techniques. In operation, the plasma processing apparatus uses the upper and lower electrodes to generate a plasma in the processing space PS 106. This generated plasma can then be used for processing a target substrate (such as substrate W 110 or any material to be processed) in various types of treatments such as plasma etching, chemical vapor deposition, treatment of glass material and treatment of

large panels such as thin-film solar cells, other photovoltaic cells, and organic/inorganic plates for flat panel displays, etc. In certain implementations described herein, a dummy substrate, which may be a non-production wafer may be used as wafer W 110.

[0041] The control unit 192 may include one or more processors, microcomputers, computing units and the like. The storage unit 194 may include memory, and is an example of non-transitory computer-readable storage media for storing instructions which are executed by the control unit 192, to perform the various functions described herein. For example, the storage unit 194 may generally include both volatile memory and non-volatile memory (e.g., RAM, ROM, or the like). Memory may be referred to as memory or computer-readable storage media herein. Memory is capable of storing computer-readable, processor-executable program instructions as computer program code that may be executed by the control unit 190 as a particular machine configured for carrying out the operations and functions described in the implementations herein.

[0042] Memory may further store one or more applications (not shown). The applications may include preconfigured/installed and downloadable applications. In addition, memory may store the OES spectral data used for processes as described herein.

[0043] The plasma processing system 100 can further include a spectrometer 198 and a window 199. The spectrometer 196 is used for gathering light used for process endpoint analysis and OES spectra. The spectrometer 198 may be connected to control unit 192, or other controllers/systems.

[0044] FIG. 2 is an example schematic block diagram of an example plasma processing system implementing optical emission spectroscopy (OES) to determine OES spectra, and plasma monitoring. As discussed above, the

plasma processing chamber 102 provides for the processing space PS 106 above the substrate W 110 mounted on the lower electrode 116. In a WLDC process to determine and gather OES spectra and/or endpoint calculation of residue constituents (e.g, CF), a production substrate W 110 may be absent. In other implementations, a dummy or non-production substrate is in place for substrate W 110.

[0045] In this example, the spectrometer 198 collects light, as represented by light volume 200. During the monitoring of OES spectra in a WLDC process, light volume 200 provides for the OES spectra data, which can include OES spectra of CF constituents.

[0046] The spectrometer 198 may be part of a monitoring system 202. The monitoring system may be part of the plasma processing system 100. The monitoring system 202 can be particularly used in plasma monitoring in the plasma processing chamber 102. Other example systems and components that can be part of monitoring system 202, include and are not limited to, an optical emission spectroscopy system 204, laser induced fluorescence system 206, laser interferometer 208, mass spectrometer 210, and Fourier transform infrared (FTIR) system 212. In particular, the spectrometer 196 can be part of the optical emission spectroscopy system 204. The optical emission spectroscopy system 204 may acquire OES during a WLDC process.

[0047] As discussed, a metric, such as OES spectra can be utilized to analyze the effectiveness of a WLDC process by evaluation of undesirable species or residual constituents, such as wavelengths of C and F constituents in an OES spectra for a batch or lot of wafers. Furthermore, a WLDC process can be optimized based on OES spectra of undesirable residue constituents being removed by the dry cleaning process following one particular device wafer process (in situ process). Typically, an ineffective WLDC process may not show the leveling out in OES intensity for the wavelength examined of a constituent

that is intended to be removed by the WLDC process or even the feed-in dry cleaning gas such as oxygen. However, the OES spectra of this constituent can show the leveling out in intensity once the endpoint was reached for the WLDC process; this endpoint time can be utilized for determining the ideal completion time for the WLDC in order to optimize throughput. By reducing the variation in the C and F intensity levels between device wafers collectively for a lot using a more effective WLDC process, the uniformity of the etch profile characteristics of that lot can be improved such as the bottom via width (bottom critical dimension or CD). Excess or inconsistent CF or carbon densities in a chamber or polymer deposition build-up remaining from an inconsistent WLDC process can cause variations in the subsequent plasma etch performance for patterned device wafers that could lead to critical dimension variation across a lot outside the control limits for manufacturing specifications. These undesirable constituents residing in a chamber can lead to clogging of the features being etched during a subsequent device wafer etch process, which is the build-up of polymer residue in a trench or via feature which prevents uniform etching of a feature profile. Similarly, an accumulation of fluorine by-product in a chamber can lead to an increasing etch rate from one wafer to the next, since it tends to remove sidewall polymer passivation, which ultimately causes an increasing trend toward wider etch profiles. This mechanism was deemed the basis why a more effective WLDC process was found to improve wafer-to-wafer and within-wafer etch profile uniformity as well.

[0048] FIG. 3 shows an example graph 300 that illustrate a peak in OES spectra of a residual constituent, and in particular fluorine (F). The OES spectral peak of fluorine for a particular WLDC is represented by 302 in graph 300. Using the intensity vs. time trend of a particular WLDC by-product OES peak such as fluorine, which happens to be shown in graph 304, and implementing an endpoint analysis, a determination may be made as to if

and when the residual constituent fluorine levels off or not in a plasma processing chamber. Fluorine residual by-product background build-up within a chamber, as measured by OES, while processing wafers of a wafer lot involving polymer shrink based dry etching may cause an increasing trend in the etch profile width CD, as sidewall polymer is being removed to a higher degree for the same given etch process for consecutively processed device wafers of a lot. An endpoint analysis that may be implemented may be found in U.S. Patent 9,330,990 entitled "METHOD OF ENDPOINT DETECTION OF PLASMA ETCHING PROCESS USING MULTIVARIATE ANALYSIS" which is included in its entirety by reference.

[0049] It is realized that the plasma processing chamber is not absolutely devoid of residual constituents, and an acceptable amount of constituents may reside in the plasma processing chamber.

[0050] FIG. 4 shows an example chart 400 that provides optimized values for a particular dry clean process, such as a WLDC. In this example, OES spectra and endpoint analysis can be collected for residual constituent F. Several acronyms noted include: radical gas-distribution control (RDC) referring to the center to edge gas zone flow ratio/percent, brine or chiller temperature for the plasma system, direct current (DC) electrode voltage, low-frequency (LF) power, high-frequency (HF) power, and advanced temperature controlled chuck (ATCC) temperature in proximity to the substrate or wafer holder.

[0051] A particular process is identified under the heading "Recipe" as represented by 402. In this example, a WLDC process is identified as represented by 404. Step 406 furthers identifies the process as an oxygen (O2) clean 408. A pre-set recipe time of 20 seconds 410 is identified as the maximum WLDC process time. Other parameters as shown in chart 400 may be identified for this optimized process. Such parameters can include "gas pressure", "power", "DC bias", etc.

[0052] FIG. 5 shows an example process 500 for monitoring and controlling a waferless dry cleaning process in a plasma processing system. The order in which the method is described is not intended to be construed as a limitation, and any number of the described method blocks can be combined in any order to implement the method, or alternate method. Additionally, individual blocks may be deleted from the method without departing from the spirit and scope of the subject matter described herein. Furthermore, the method may be implemented in any suitable hardware, software, firmware, or a combination thereof, without departing from the scope of the invention.

[0053] At block 502, flowing a dry cleaning gas into a plasma processing chamber is performed. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0054] At block 504, igniting a plasma in the plasma processing chamber to initiate a waferless dry cleaning (WLDC) process is performed. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0055] At block 506, acquiring optical emission spectra (OES) data is performed. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100. In addition, in reference to FIG. 2 above, this block may be performed by the optical emission spectroscopy system 204. In other implementations, the acquiring may be a monitoring act that monitors the plasma in the plasma processing chamber 102.

[0056] At block 508, optimizing at least one parameter of the WLDC process based on the acquired OES data. The parameters may be those described above. In addition, the parameters may be optimized in-situ or ex-situ.

[0057] FIG. 6 shows an example graph 600 of optical emission spectroscopy (OES) detection of a residual constituent for an optimized WLDC condition. The residual constituent F is represented by the OES peak 602. OES analysis is performed on residual constituent F as described herein indicating an OES endpoint by virtue of the leveling in intensity over time for this by-product. An array of OES endpoint time values 604 when the residual constituent F intensity stabilizes were found with steadily shorter times as the WLDC cleaned the chamber more and more of residual etch by-products such as fluorine over the course of wafer lot processing. These values may be used as the duration as to when a WLDC process (i.e., recipe) ends. The total variation in OES intensity of this F peak at the end of the optimized WLDC condition process time is reduced by 50 percent compared to the non-optimized WLDC OES spectra noted in FIG. 3; which subsequently led to over 50 percent less wafer-to-wafer via CD width variation across the lot.

[0058] FIG. 7 shows an example process 700 for optical emission spectroscopy (OES) process control. In particular, the process 700 may be used for dry etch process control. Process 700 can be considered an in situ process, wherein in feedback may be sent to a plasma processing system, as described in reference to FIG. 1. Adjustment may be performed based on the determined feedback data.

[0059] The order in which the method is described is not intended to be construed as a limitation, and any number of the described method blocks can be combined in any order to implement the method, or alternate method. Additionally, individual blocks may be deleted from the method without departing from the spirit and scope of the subject matter described herein. Furthermore, the method may be implemented in any suitable hardware, software, firmware, or a combination thereof, without departing from the scope of the invention.

[0060] At block 702, a production process of a wafer lot is performed. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0061] At block 704, a WLDC and OES trace data collection as described herein is performed. In reference to FIG. 1 and FIG. 2 above, this block may be performed by the described components of plasma processing system 100, and monitoring system 200.

[0062] At block 706, the production process of a wafer lot is continued. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0063] At block 708, a WLDC and OES trace data collection as described herein is performed. In reference to FIG. 1 and FIG. 2 above, this block may be performed by the described components of plasma processing system 100, and monitoring system 200.

[0064] At block 710, an in situ OES data analysis is performed. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0065] At block 712, data/signals are sent to the plasma processing system (i.e., controllers), to determine whether to adjust a WLDC process parameter based on OES intensity of the selected by-product (i.e., residual constituent) or cleaning feed gas wavelength.

[0066] At block 714, the production process of a wafer lot is continued. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0067] At block 716, an adjustment to the WLDC process parameters may be performed. Alternatively, the same parameters may be used. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0068] At block 718, the production process of a wafer lot is continued. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

[0069] At block 720, the sequence is iterated until the wafer lot production is complete. In reference to FIG. 1 above, this block may be performed by the described components of plasma processing system 100.

CLAIMS

What is claimed is:

1. A method for monitoring and controlling a waferless dry cleaning process in a plasma processing system, the method comprising:

flowing a dry cleaning gas into a plasma processing chamber of the plasma processing system;

igniting a plasma in the plasma processing chamber to initiate the waferless dry cleaning process; and

acquiring optical emission spectra from an optical emission spectroscopy system attached to the plasma processing chamber, during the waferless dry cleaning process.

2. The method of claim 1, wherein the plasma processing system is a plasma etching system.

3. The method of claim 1, wherein the plasma processing system is a plasma deposition system.

4. The method of claim 1, wherein the acquiring of optical emission spectra is performed during a waferless dry cleaning process absent production substrates present in the plasma processing chamber.

5. The method of claim 4, wherein the acquiring of optical emission spectra is performed with dummy substrates placed in the plasma processing chamber.

6. The method of claim 1, further comprising:

optimizing at least one parameter of the waferless dry cleaning process based on the acquired optical emission spectra.

7. The method of claim 6, wherein the at least one parameter of the waferless dry cleaning process is selected from the group consisting of:

radio frequency (RF) or microwave power supplied to the plasma processing chamber;

RF or microwave power pulse frequency;

RF or microwave pulse duty cycle;

RF power supplied to a substrate holder in the plasma processing chamber;

magnetic field of one of more magnets proximate the substrate holder;

direct current (DC) bias of the substrate holder;

DC bias voltage supplied to at least one electrode arranged proximate the substrate holder;

dry cleaning gas flow rate;

dry cleaning gas pressure; and

duration of the waferless dry cleaning process.

8. The method of claim 6, wherein the optimization of the at least one parameter of the waferless dry cleaning process is performed to maximize the time between wet cleans of the plasma processing chamber.

9. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to minimize the duration of the waferless dry cleaning process.

10. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to maximize the lifetime of a component of the plasma processing chamber.

11. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to minimize particle generation in the plasma processing chamber.

12. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to maximize critical dimension (CD) uniformity of a subsequently processed production substrate or lot of production substrates.

13. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed using optical emission spectra acquired with dummy substrates placed in the plasma processing chamber.

14. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed ex-situ.

15. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed in-situ.

16. The method of claim 6, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to minimize the duration of the waferless dry cleaning process.

17. The method of claim 1, wherein the dry cleaning gas comprises oxygen, an oxygen-containing gas, HCl, F2, Cl2, hydrogen, nitrogen, argon, SF6, C2F6, NF3, CF4, or a mixture of two or more thereof.

18. The method of claim 1, further comprising:

terminating the waferless dry cleaning process when the acquired optical emission spectra substantially match a predetermined target optical emission spectrum,

wherein the target optical emission spectrum is characteristic for a plasma processing chamber for a predetermined acceptable clean condition.

19. The method of claim 1, further comprising:

terminating the waferless dry cleaning process when content of a residual constituent approaches a determined level based on OES endpoint analysis.

20. A non-transitory machine-accessible storage medium having instructions stored thereon which cause a data processing system to perform a method for monitoring and controlling a waferless dry cleaning process in a plasma processing tool, the method comprising:

flowing a dry cleaning gas into a plasma processing chamber of the plasma processing system;

igniting a plasma in the plasma processing chamber to initiate the waferless dry cleaning process; and

acquiring optical emission spectra from an optical emission spectroscopy system attached to the plasma processing chamber, during the waferless dry cleaning process.

21. The storage medium of claim 20, wherein the method for monitoring and controlling a waferless dry cleaning process in a plasma processing tool further comprises:

optimizing at least one parameter of the waferless dry cleaning process based on the acquired optical emission spectra.

22. The storage medium of claim 20, wherein the method for monitoring and controlling a waferless dry cleaning process in a plasma processing tool further comprises:

terminating the waferless dry cleaning process when the acquired optical emission spectra substantially match a predetermined target optical emission spectrum,

wherein the target optical emission spectrum is characteristic for a plasma processing chamber in a clean condition.

23. A plasma processing system comprising:

one or more controllers;

a plasma processing chamber;

a process gas supply system controlled by the one or more controllers, that flows into the plasma processing chamber, wherein the one or more controllers initiate an ignition of a plasma in the plasma processing chamber to initiate the waferless dry cleaning process; and

an optical spectroscopy system attached to the plasma processing chamber that acquires optical emission spectra during the waferless dry cleaning process.

24. An in situ method of monitoring and controlling a waferless dry cleaning (WLDC) process in a plasma processing tool, the method comprising:

initiating a production process of a wafer lot;

collecting in-situ monitoring data during the production process;

performing in-situ data analysis of the wafer lot; and

adjusting parameters of the WLDC process based on the in-situ monitoring data.

25. The method of claim 24, wherein the in-situ monitoring data is collected by performing a method comprising:

flowing a dry cleaning gas into a plasma processing chamber of the plasma processing system;

igniting a plasma in the plasma processing chamber to initiate the waferless dry cleaning process; and

monitoring the plasma in the plasma processing chamber during the waferless dry cleaning process using a monitoring system,

wherein the monitoring system comprises an optical emission spectroscopy system, a laser induced fluorescence system, a laser interferometer, a residual gas analyzer, a mass spectrometer, or a Fourier Transform Infrared (FTIR) system.

26. The method of claim 24, wherein the plasma processing tool is a plasma etching system.

27. The method of claim 24, wherein the plasma processing tool is a plasma deposition system.

28. The method of claim 24, wherein the monitoring the plasma acquires optical emission spectra is performed during the waferless dry cleaning process absent production substrates present in the plasma processing chamber.

29. The method of claim 28, wherein the acquiring of optical emission spectra is performed with dummy substrates placed in the plasma processing chamber.

30. The method of claim 28, further comprising:

optimizing at least one parameter of the waferless dry cleaning process based on the acquired optical emission spectra.

31. The method of claim 30, wherein the at least one parameter of the waferless dry cleaning process is selected from the group consisting of:

radio frequency (RF) or microwave power supplied to the plasma processing chamber;

RF or microwave power pulse frequency;

RF or microwave pulse duty cycle;

RF power supplied to a substrate holder in the plasma processing chamber;

magnetic field of one of more magnets proximate the substrate holder;

direct current (DC) bias of the substrate holder;

DC bias voltage supplied to at least one electrode arranged proximate the substrate holder;

dry cleaning gas flow rate;

dry cleaning gas pressure; and

duration of the waferless dry cleaning process.

32. The method of claim 30, wherein the optimization of the at least one parameter of the waferless dry cleaning process is performed to maximize the time between wet cleans of the plasma processing chamber.

33. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to minimize the duration of the waferless dry cleaning process.

34. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to maximize the lifetime of a component of the plasma processing chamber.

35. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to minimize particle generation in the plasma processing chamber.

36. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to maximize critical dimension (CD) uniformity of a subsequently processed production substrate or lot of production substrates.

37. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed using optical emission spectra acquired with dummy substrates placed in the plasma processing chamber.

38. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed ex-situ.

39. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed in-situ.

40. The method of claim 30, wherein the optimizing of the at least one parameter of the waferless dry cleaning process is performed to minimize the duration of the waferless dry cleaning process.

41. A non-transitory machine-accessible storage medium having instructions stored thereon which cause a data processing system to perform a method for monitoring and controlling a waferless dry cleaning process in a plasma processing tool, the method comprising:

starting a production process of a wafer lot;

gathering in-situ monitoring data during the production process;

analyzing in-situ data of the wafer lot; and

recalculating parameters of the WLDC process based on the in-situ monitoring data.

42. The storage medium of claim 41, wherein the method for monitoring and controlling a waferless dry cleaning process in a plasma processing tool further comprises:

optimizing at least one parameter of the waferless dry cleaning process based on the acquired optical emission spectra.

43. The storage medium of claim 41, wherein the method for monitoring and controlling a waferless dry cleaning process in a plasma processing tool further comprises:

terminating the waferless dry cleaning process when the acquired optical emission spectra substantially match a predetermined target optical emission spectrum,

wherein the target optical emission spectrum is characteristic for a plasma processing chamber in a clean condition.

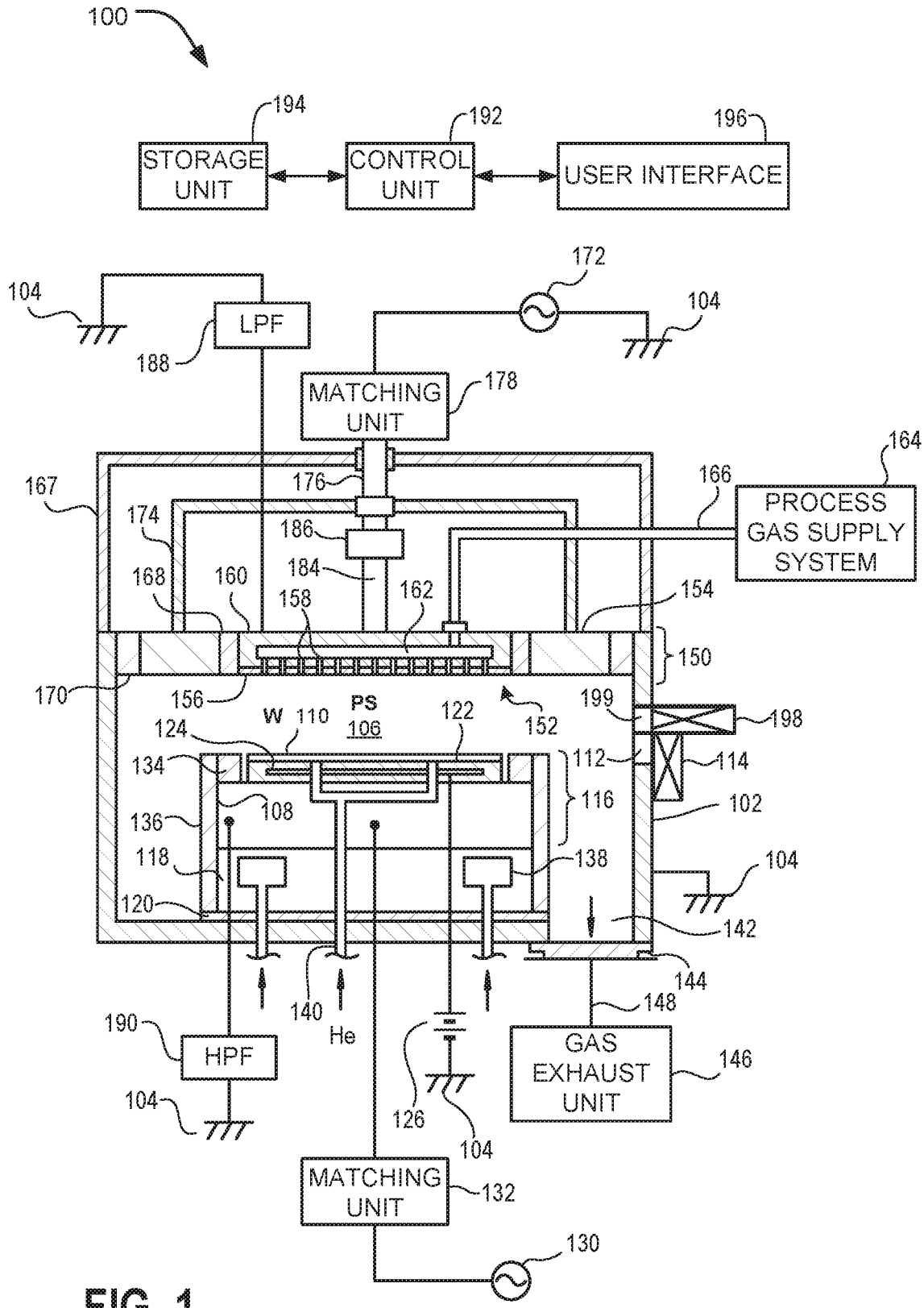
100
194
STORAGE UNIT
192
CONTROL UNIT
196
USER INTERFACE
172
104
LPF
188
104
MATCHING UNIT
178
164
167
176
166
PROCESS GAS SUPPLY SYSTEM
174
186
168
160
184
162
158
154
150
170
156
W
110
PS
106
122
152
199
198
124
134
112
114
116
108
102
136
118
138
104
120
142
144
140
He
148
190
HPF
GAS EXHAUST UNIT
146
104
126
104
MATCHING UNIT
132
130

FIG. 1

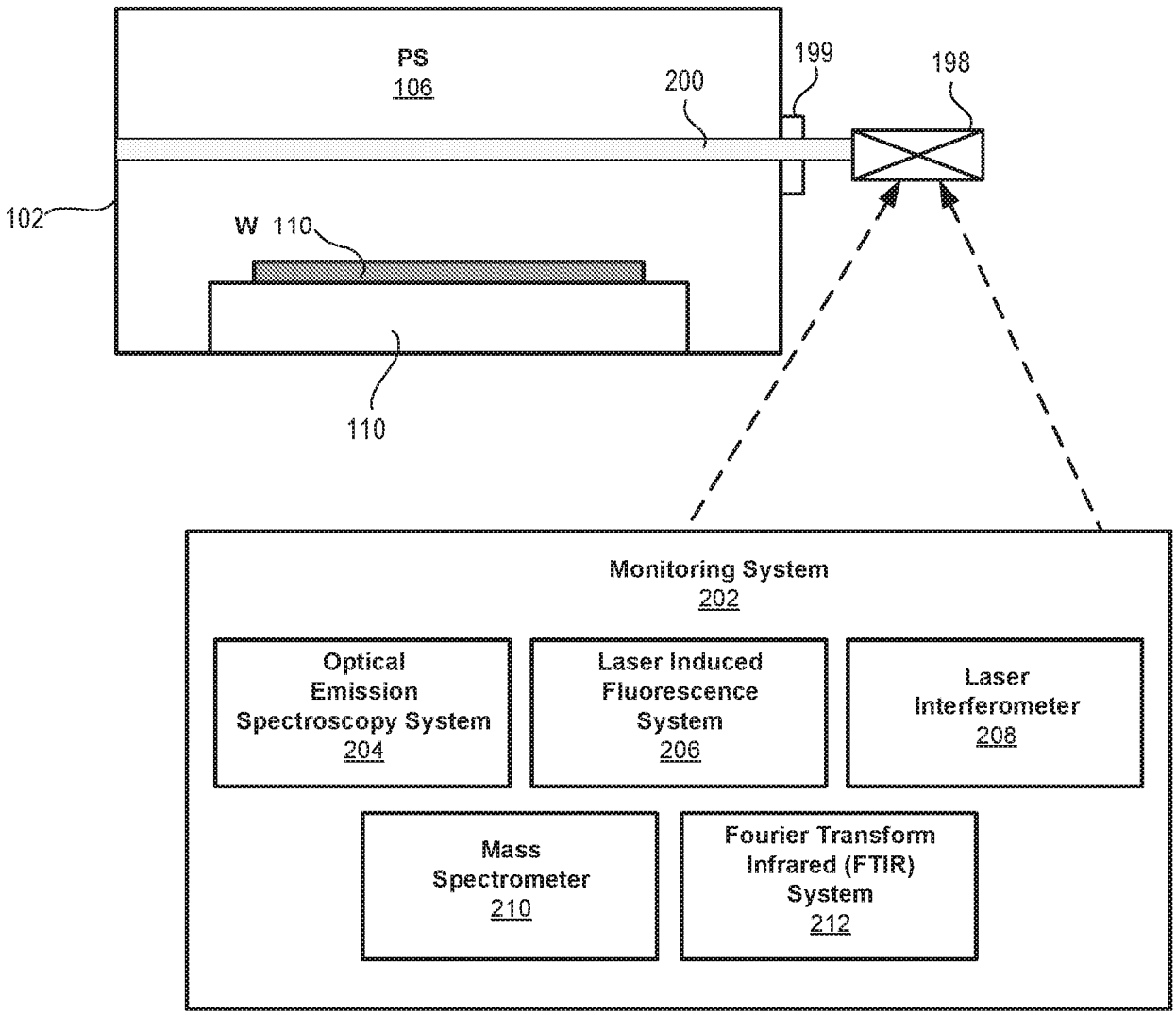
PS
106
200
199
198
102
W 110
110
Monitoring System
202
Optical Emission Spectroscopy System
204
Laser Induced Fluorescence System
206
Laser Interferometer
208
Mass Spectrometer
210
Fourier Transform Infrared (FTIR) System
212

FIG. 2

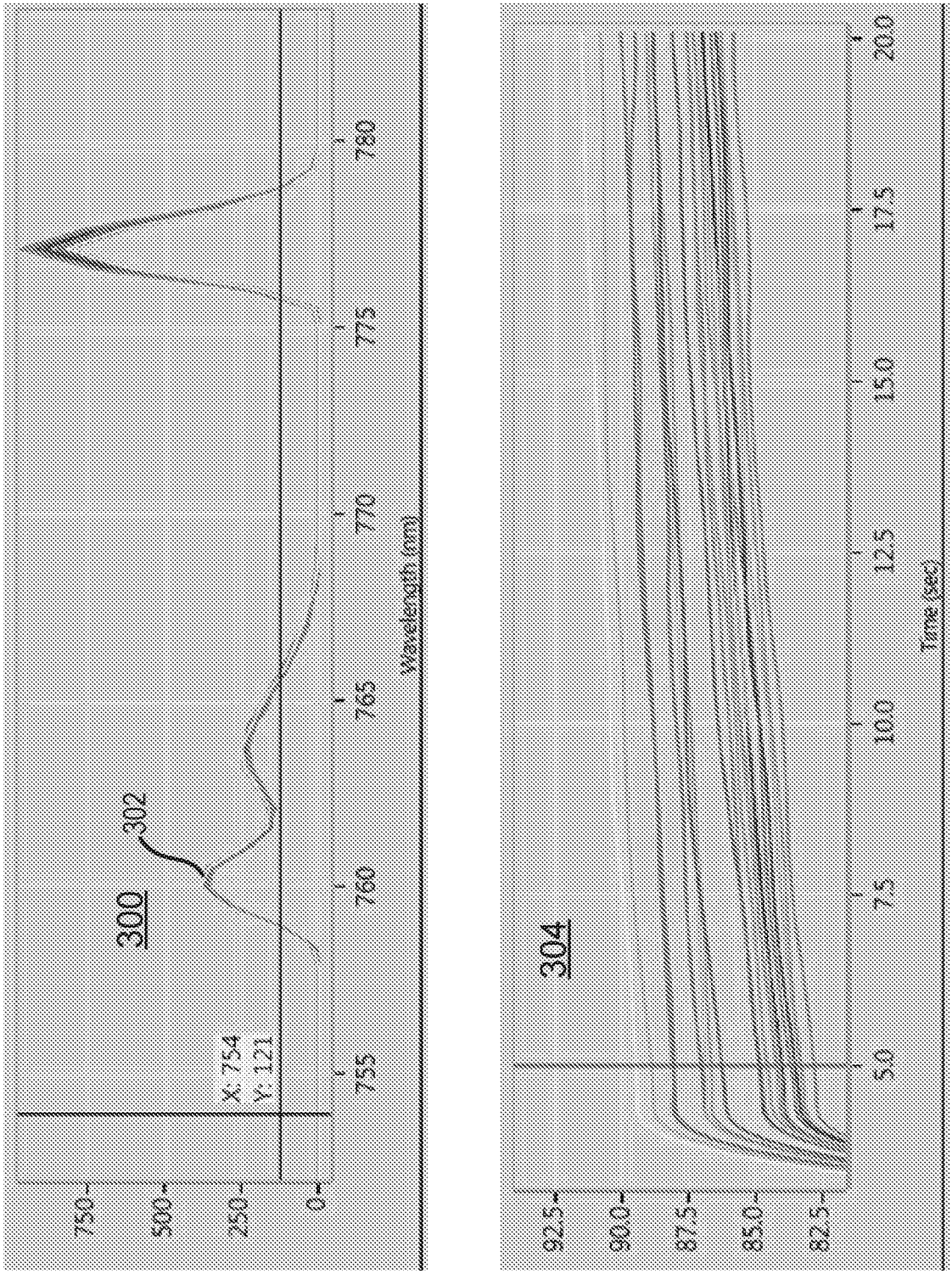
300
302
X: 754
Y: 121
750
500
250
0
755
760
765
770
775
780
Wavelength (nm)
304
92.5
90.0
87.5
85.0
82.5
50
75
100
125
150
175
200
Time (sec)

FIG. 3

400

Recipe 402	Step 406	Etch time [sec]	Press [mT]	Power [W] HF	Power [W] LF	Dc [-V]	N2	O2	RBC [%]	A-RBC C4F8	A-RBC O2	B.He [T] C. E	Temp Brine (deg.C)	ΔTCC (deg.C)
WLDC-Via-4 404	O2 clean 408	20 410	400	200	0	0		1500	50	0	0	0	-10	25, 25
	N2 clean	10	200	700	0	0	480		50	0	0	0	-10	25, 25

FIG. 4

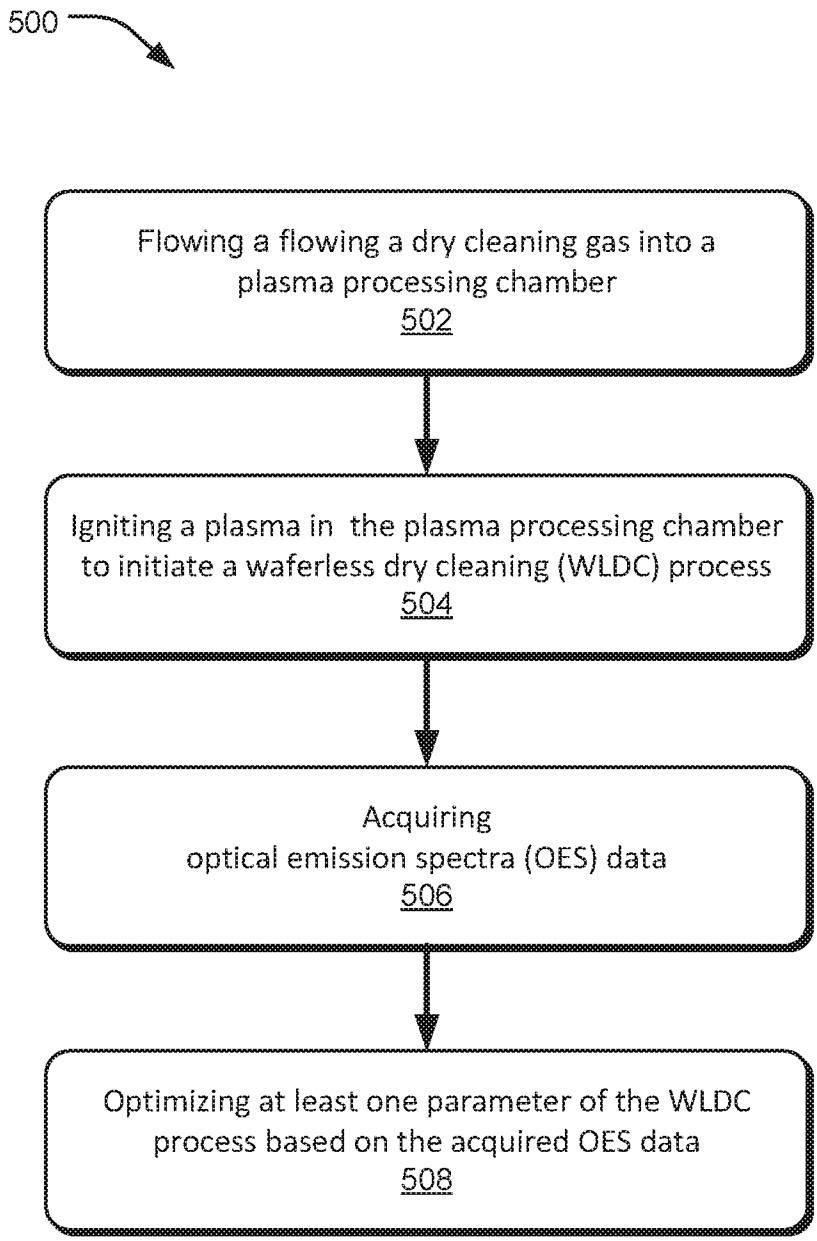
500
Flowing a flowing a dry cleaning gas into a plasma processing chamber
502
Igniting a plasma in the plasma processing chamber to initiate a waferless dry cleaning (WLDC) process
504
Acquiring optical emission spectra (OES) data
506
Optimizing at least one parameter of the WLDC process based on the acquired OES data
508

FIG. 5

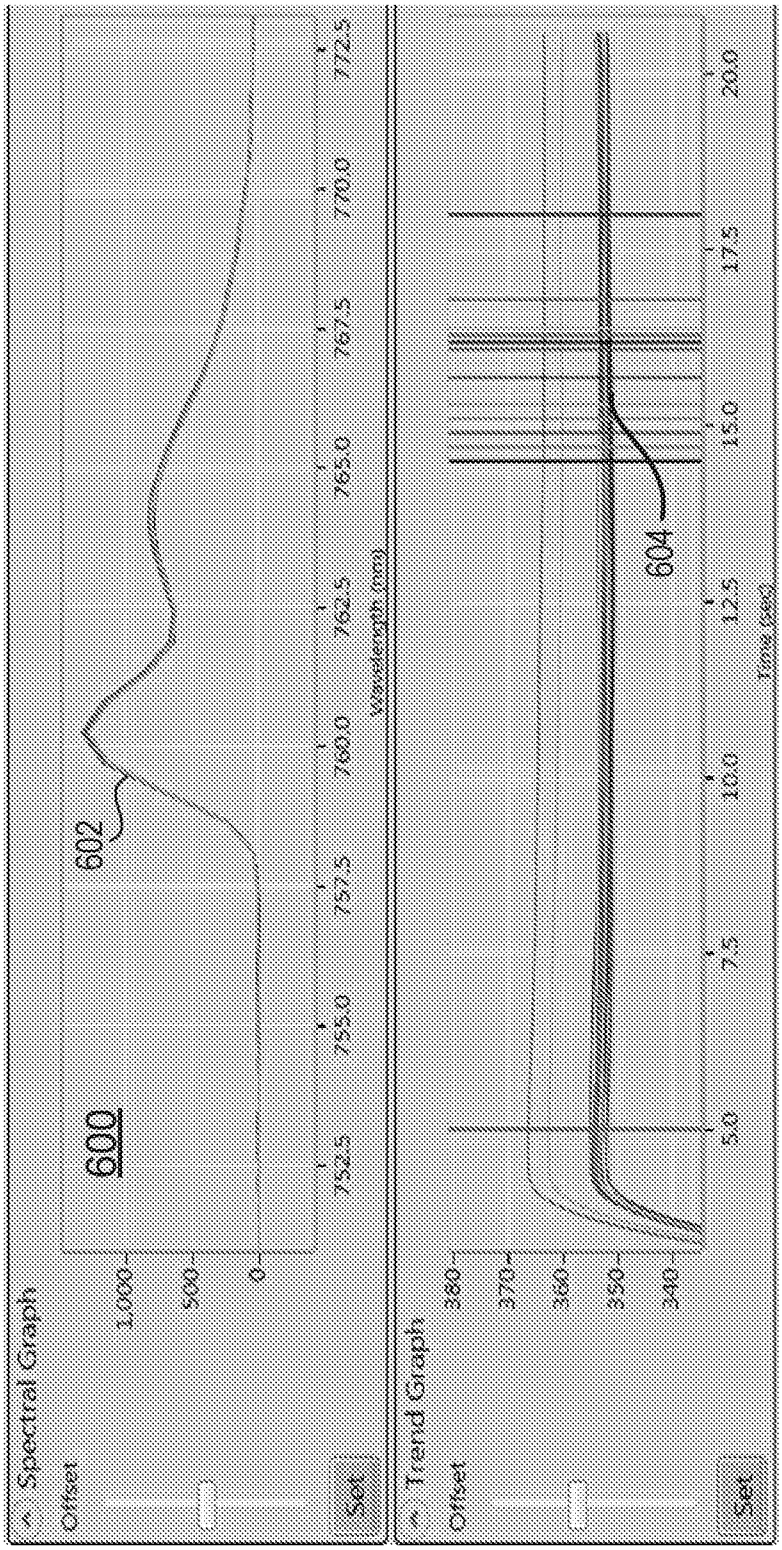
Spectral Graph
Offset
600
602
1,000
500
0
Set
752.5
755.0
757.5
760.0
762.5
765.0
767.5
770.0
772.5
Wavelength (nm)
Trend Graph
Offset
380
370
360
350
340
Set
5.0
7.5
10.0
12.5
15.0
17.5
20.0
Time (sec)
604

FIG. 6

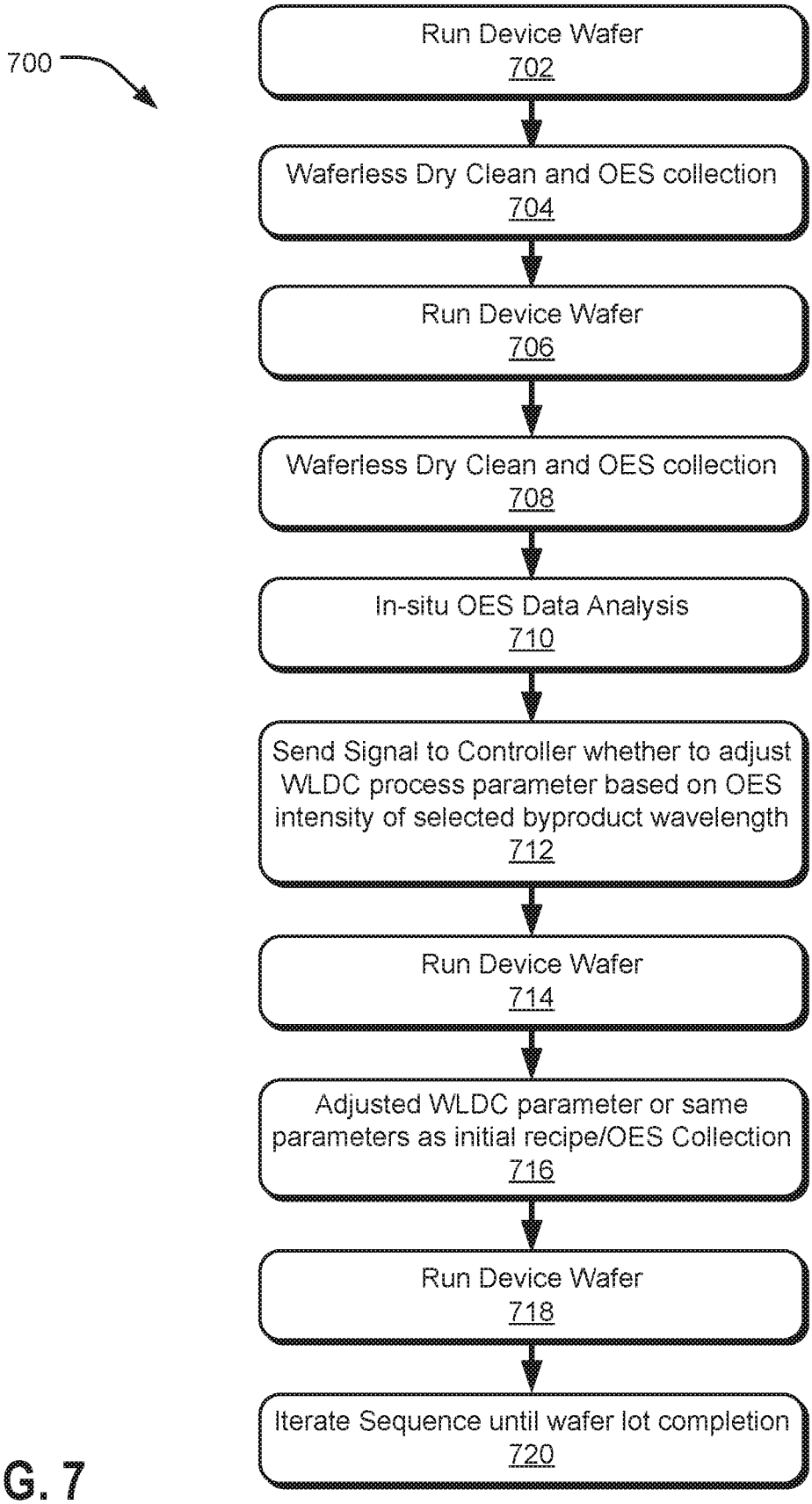
700
Run Device Wafer
702
Waferless Dry Clean and OES collection
704
Run Device Wafer
706
Waferless Dry Clean and OES collection
708
In-situ OES Data Analysis
710
Send Signal to Controller whether to adjust WLDC process parameter based on OES intensity of selected byproduct wavelength
712
Run Device Wafer
714
Adjusted WLDC parameter or same parameters as initial recipe/OES Collection
716
Run Device Wafer
718
Iterate Sequence until wafer lot completion
720

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/024138

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/3065(2006.01)i, H01L 21/66(2006.01)i, H01L 21/02(2006.01)i, H01L 21/67(2006.01)i, H05H 1/46(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/3065; H01L 21/302; B08B 7/00; B08B 6/00; B44C 1/22; C23C 16/00; B01J 19/08; H01L 21/66; H01L 21/02; H01L 21/67; H05H 1/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: waferless dry clesning, plasma, optical emission spectroscopy, chamber

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0238199 A1 (ASAO YAMASHITA) 11 October 2007 See paragraphs [0004], [0011]-[0042], [0057]-[0087], claims 14-15 and figures 1-2.	1-43
Y	US 2005-0241669 A1 (NORMAN WODECKI) 03 November 2005 See paragraphs [0009], [0029], [0040], [0052]-[0064] and figures 2, 12.	1-43
Y	US 2009-0325387 A1 (XIAOYI CHEN et al.) 31 December 2009 See paragraphs [0006], [0033] and figure 2.	5,13,29,37
A	US 2001-0046769 A1 (YU-CHANG CHOW et al.) 29 November 2001 See claim 1 and figure 1.	1-43
A	US 2012-0006351 A1 (HYUN-SU JUN et al.) 12 January 2012 See claim 1 and figure 1.	1-43

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 August 2017 (18.08.2017)	**18 August 2017 (18.08.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM HYEON JIN
Telephone No. +010-4310-7635

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/024138

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0238199 A1	11/10/2007	US 7906032 B2	15/03/2011
		WO 2007-126469 A2	08/11/2007
		WO 2007-126469 A3	23/10/2008
US 2005-0241669 A1	03/11/2005	JP 2007-535169 A	29/11/2007
		TW 200540942 A	16/12/2005
		TW I290743 B	01/12/2007
		WO 2005-111265 A1	24/11/2005
US 2009-0325387 A1	31/12/2009	CN 102077327 A	25/05/2011
		JP 2011-526082 A	29/09/2011
		KR 10-1445153 B1	29/09/2014
		KR 10-2011-0050438 A	13/05/2011
		WO 2009-158311 A2	30/12/2009
		WO 2009-158311 A3	19/08/2010
US 2001-0046769 A1	29/11/2001	TW 439143 B	07/06/2001
		US 6374832 B2	23/04/2002
US 2012-0006351 A1	12/01/2012	KR 10-2012-0004190 A	12/01/2012