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(54) **BI-DIRECTIONAL SINGLE WIRE INTERFACE**

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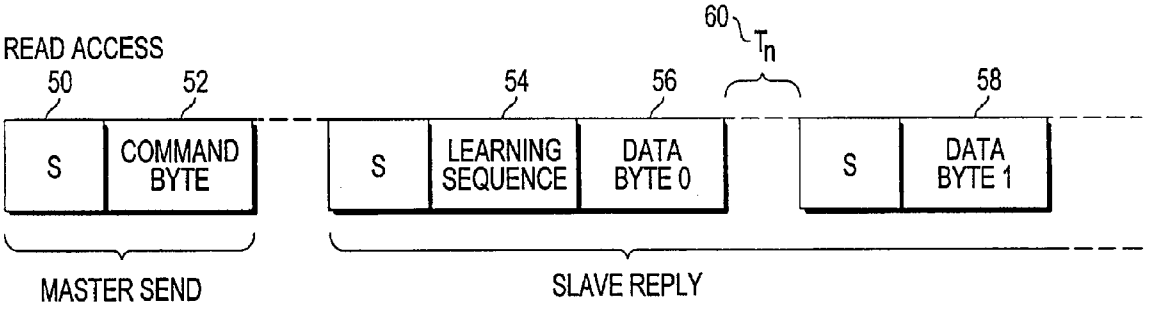
(57) **ABSTRACT**

A single-wire, bi-directional communication protocol is provided in which the sending device transmits its clock frequency and its bit transmission period and data through a predefined waveform pattern or "learning sequence" that is recognizable by the receiving device and in a period of time, as measured in number of sending clock cycles, that is known to the receiving device. By clocking the full length of the predefined waveform pattern using its own internal clock, the receiving device becomes aware of the bit transmission period of the sending device.



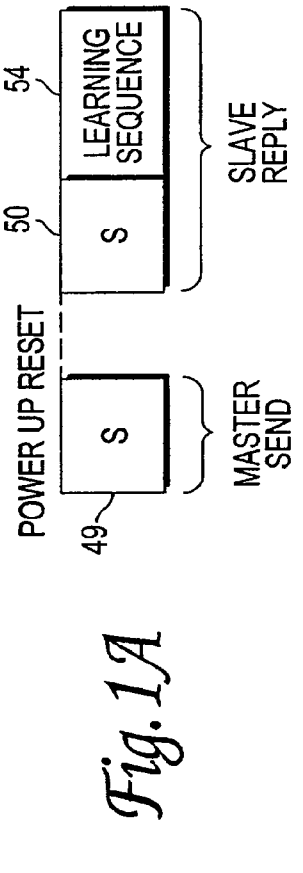


Fig. 1A

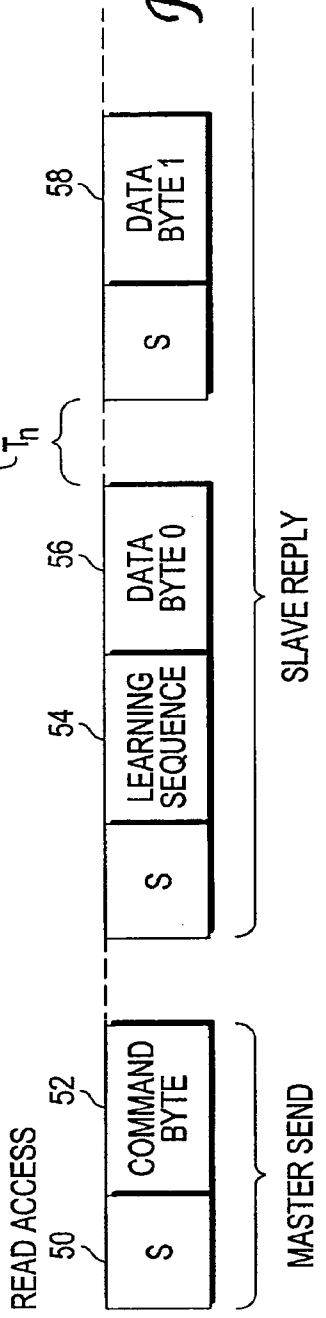


Fig. 1B

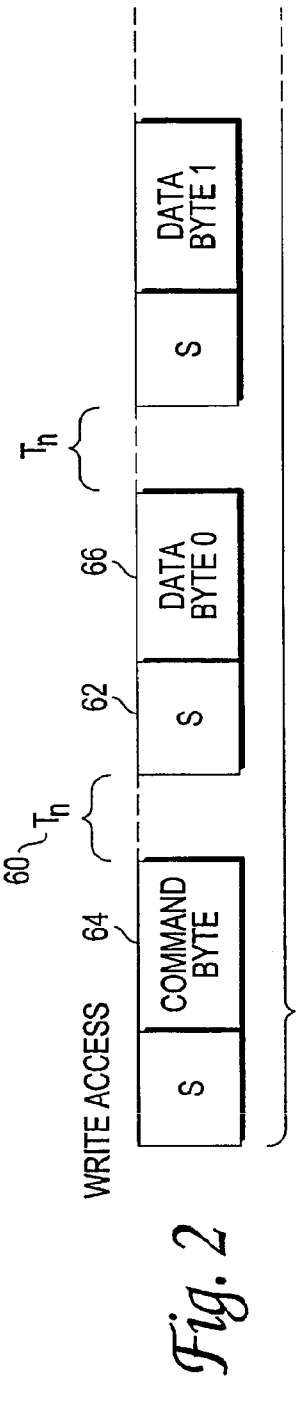


Fig. 2

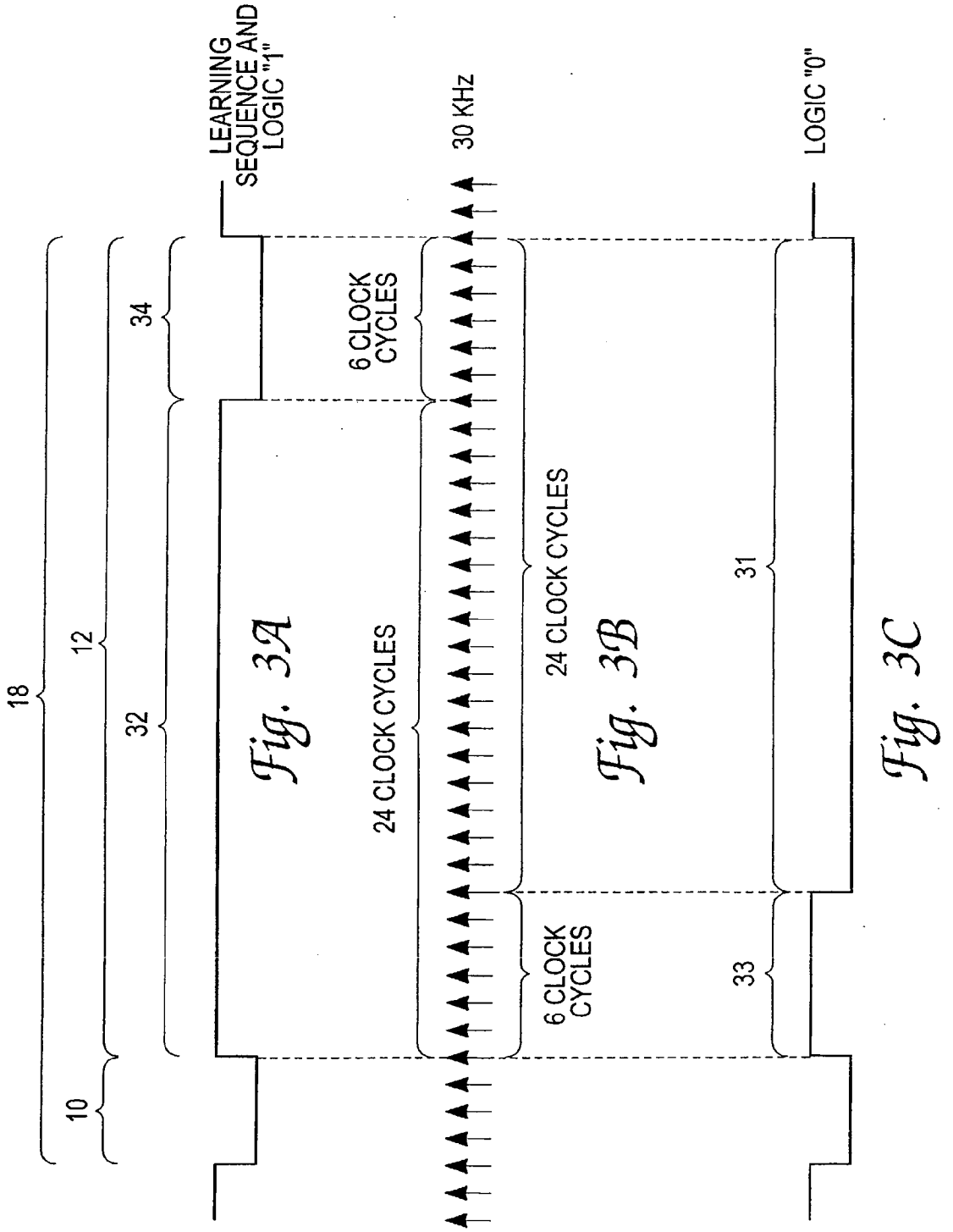


Fig. 3A

Fig. 3B

Fig. 3C

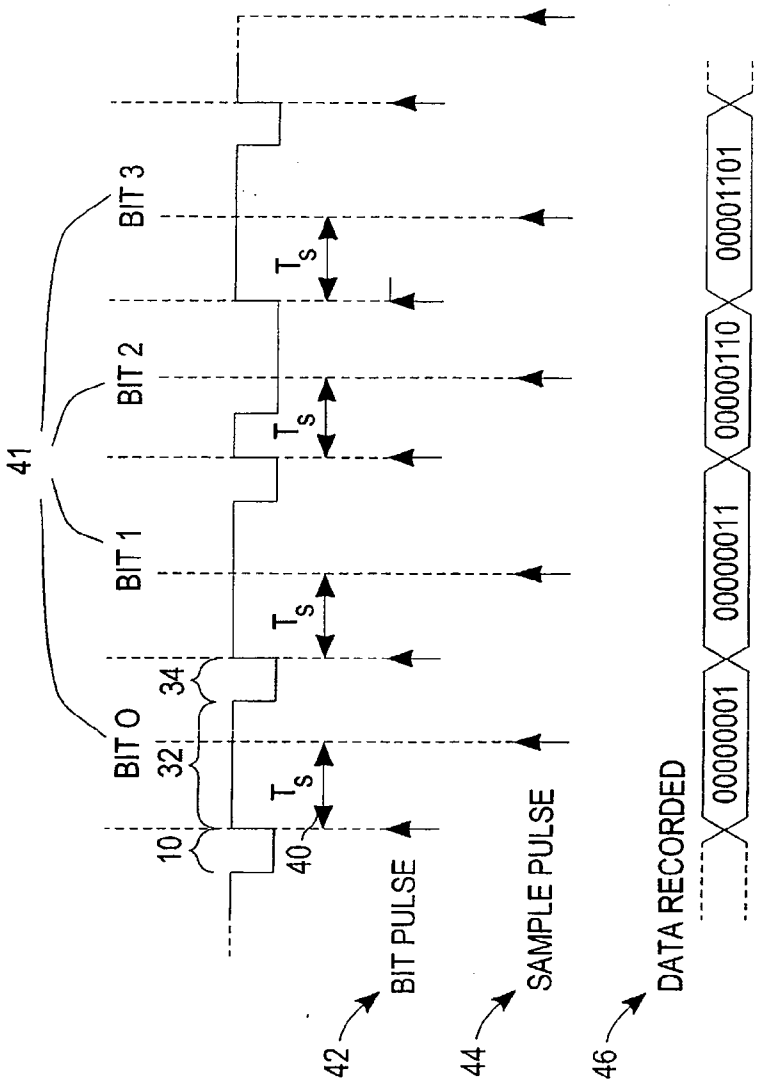

41
BIT 0
BIT 1
BIT 2
BIT 3
10
32
34
40
T_s
BIT PULSE
SAMPLE PULSE
DATA RECORDED
00000001
00000011
00000110
00001101
42
44
46

Fig. 4

10
12
14
16
S
LEARNING SEQUENCE
DATA BYTE 1
DATA BYTE 1
DATA BYTE 2
18
20
20

Fig. 5

BI-DIRECTIONAL SINGLE WIRE INTERFACE

RELATED APPLICATIONS

[0001] This application is a Continuation application of U.S. patent application Ser. No. 10/443,153, filed on May 21, 2003, which incorporated herein by reference in it entirety.

TECHNICAL FIELD

[0002] The present invention relates to communication protocols for the bi-directional transmission and reception of signals between two devices.

BACKGROUND ART

[0003] Conventional single-wire bi-directional communication systems of the prior art call for an accurate separate clock module to ensure synchronized data transmission between the sending device and the receiving device. U.S. Pat. No. 5,237,322 to Heberle describes a master with a separate clock generator tc that is used for generating an internal system clock cl. In addition, the clock signal is also sent through the single wire as a segment of periodic timing signal bt during wait state. The Heberle patent specifies that a specific end signal be used in the communication protocol. It would be desirable to have a simple communication protocol that does not require specific end signal.

DISCLOSURE OF THE INVENTION

[0004] The present invention is a method of transmitting clock frequency information through a single-wire, bi-directional communication system operating in an asynchronous mode through which a master learns the clock frequency of a slave device. Knowing the clock frequency of the slave device allows the master to adjust its data sampling rate and data transmission rate for optimal data reception and transmission.

[0005] At the beginning of each transmission, the slave device makes its clock frequency known to the master device by transmitting a distinctive waveform that has a predefined pattern and a preset duration that is known to both the slave device and the master device. Once the master device recognizes the distinctive waveform, it uses its internal clock to measure the duration. Having the measured duration and the preset duration allows the master device to deduce the clock frequency in the slave device. Using this knowledge, the master device can then set the optimal sampling frequency for subsequent data transmission from the slave device.

[0006] In a preferred embodiment, the slave device transmits a waveform that is representative of a typical logic "1" and with a duration that is representative of the time it takes to send a single bit of data (bit time), as measured by the number of clock cycles that is known to both the slave and the master devices. The master device measures the bit time based on its internal clock, thereby obtaining the clock frequency of the slave device.

BRIEF DESCRIPTION OF THE FIGURES

[0007] FIG. **1***a* is a timing block diagram showing the power-up reset sequence according to an embodiment of the present invention.

[0008] FIG. **1***b* is a timing block diagram showing the sequence for a master to read from a slave device according to an embodiment of the present invention.

[0009] FIG. **2** is a timing block diagram showing the sequence for a master to write to a slave device according to an embodiment of the present invention.

[0010] FIGS. **3***a-c* are timing diagrams showing an embodiment of a learning sequence, logic "1", and logic "0" shown in FIG. **1**.

[0011] FIG. **4** is a timing diagram showing an embodiment of the data detection protocol as described in the present invention.

[0012] FIG. **5** is a timing block diagram showing sequence for transmitting data between two peer devices through a single-wire as described in the present invention.

BEST MODE OF CARRYING OUT THE INVENTION

[0013] In a system where the communication is between a master and a slave device, each communication session is to be initiated by the master through a command sequence indicating whether it is intending to read or write from a memory location in the slave. The master device typically has a reliable clock whose frequency is stable over time while the slave device typically has a low cost oscillator whose frequency may fluctuate significantly from a nominal value. Through a learning sequence, the master device detects the sending frequency of the slave and adjusts its sampling frequency appropriately. Knowing the clock frequency of the slave device also allows the master to adjust its transmission bit time for optimal data detection by a slave with a fixed sampling rate.

[0014] FIG. **1***a* shows a power-up reset sequence by which a master and a slave device establish an initial contact. Upon power up or during reinitialization, the master sends a reset pulse **49**. In reply, the slave sends a start pulse **50** and a learning sequence **54**, which is a distinctive waveform having a clear beginning and end that allows a receiving device to clock its duration.

[0015] FIG. **1***b* shows, as an example, a sequence by which a master device initiates a memory read session and a slave device replies with the requested data. The sequence begins with the master sending a command byte **52** that contains information about the intended operation (to read) and the location of the data to be read (the memory location in the EEPROM in the slave). The slave replies with a learning sequence **54** that allows the master to measure the operating frequency of the clock in slave and the bit time of the slave. The learning sequence is immediately followed by a first data byte (byte **0**). Each subsequent data byte **58** is sent after certain hold period T_h **60**. As shown in the figure, each subsequent transmission of a data byte is preceded by a start pulse **50**.

[0016] FIG. **2** shows the steps taken by the master device for write access to the slave device. The sequence begins with a command byte **64** containing information about the intention to perform a write operation and the location of the memory to be written. After an elapse of a certain hold period T_h **60**, the master proceeds with sending a sequence of data bytes, beginning with the first data byte **66** (byte **0**). As before, each transmission of a data byte is preceded by a start pulse **62** that signifies the beginning of a next byte transmission.

[0017] FIG. **3***a* shows a transmission session **18** that is comprised of a start pulse **10** and a learning sequence **12** that is in the form of a logic bit "1". For a line that carries a high voltage signal when it is idle, a start pulse **10** is a low voltage signal that is held for some predetermined number of clock cycles, signifying the beginning of a transmission session.

The learning sequence **12**, which begins immediately at the end of the start pulse **10**, is a waveform with an initial high signal section **32** followed by a low signal section **34**, with the duration of the high voltage signal being 4 times that of the low voltage signal. With reference to the clock transitions of the slave device shown in FIG. **3***b*, the high signal section **32** takes up 24 clock cycles while the low signal section **34** takes up 6 clock cycles.

[0018] The waveform pattern and duration for a learning sequence is also used for sending a logic bit "1" in subsequent data transmissions. Conversely, logic bit "0" is represented by a high voltage being held for 6 clock cycles **33** followed by a low voltage being held for 24 clock cycles and such a waveform is shown in FIG. **3**C.

[0019] Once the master detects the start pulse, it waits for a rising voltage edge, which indicates the beginning of the learning sequence. Using its internal clock, the master measures the duration of the learning sequence. Knowing the slave always sends the learning sequence at a fixed number of slave clock cycles, the master device can deduce the clock frequency of the slave device. In a preferred embodiment, the slave operates in a nominal clock frequency of 30K Hz though, its frequency may fluctuate by as much as 50%. The master, on the other hand operates in a nominal clock frequency of 300K Hz with negligible variation. Now assume that at certain point during a transmission, the slave clock slows down to 15K Hz. When it sends a learning sequence, it still uses a fixed number, say 30, of clock cycles. To the master's clock, the learning sequence takes up 600 clock cycles (as opposed to the normal 300 clock cycles when the slave clock is running at 30K Hz.) In response, the master device would reduce its sampling rate and transmission rate for subsequent data reception and transmission by half to accommodate for the slower slave clock.

[0020] Since the slave device operates at a fixed sampling rate of 15 clock cycles, and since the clock in the slave device may change after the transmission of learning sequence, it is important that the slave samples any incoming data waveform at its valid portion. The valid portion for logic "1" is the high signal section **32** while the valid portion for the logic "0" is the low signal section **31**. As the slave clock could vary over time, there may be times when the slave clock is running at a frequency that is so far off the nominal rate that sampling at the 15^{th} clock cycle would return an erroneous data. To guard against such errors, it is necessary to set a limit on the acceptable bit time for each bit received. In the preferred embodiment, the bit time tolerance is set at ±30%. For a nominal bit time of 30 clocks cycles, the acceptable bit time would be approximately between 21 and 39 clock cycles. If the bit time of a received bit is outside of this range, the bit will be discarded and communication is reinitiated.

[0021] FIG. **4** shows how a sequence of data bits are detected in the slave device. The sequence of data bits **41** is preceded with a start pulse **10** followed by a first bit (bit **0**) being represented by 24 slave clock cycles of high voltage **32** followed by 6 slave clock cycles of low voltage **34**. The first clock transition coinciding with or immediately following the arrival of low-to-high transition marks the beginning of each data bit and shall be referred to as a 'bit clock pulse" **42**. The clock transition that is 15 clock cycles (Ts **40**) after the bit clock pulse **42** marks the sampling point of the slave device, and shall be referred to as a "sample clock pulse" **44**. For bit **0** in FIG. **4**, sampling after 15 clock cycles returns a high signal, which denotes the receipt of a logic "1". For bit **1**, the voltage level is high when the sample clock pulse appears and thus a bit "1" is recorded. For bit **2**, the voltage level is low when sample clock pulse appears and thus a bit "0" is recorded. For bit **3**, the voltage level is high when the sample clock pulse appears and thus a bit "1" is recorded. The progression of recorded bits **46** is shown at the bottom of the FIG. **4**.

[0022] Although the preferred embodiment described above relates to communication between a master device and a slave, the concept of using a learning sequence to transmit data clocking information may also be used in a single-wire communication system between any two peer devices each having an independent clock, provided that each device has the necessary circuitry to identify and make use of the learning sequence. FIG. **5** shows the sequence by which a sending device may send a series of data bytes **14** and **16**. After the usual power up reset sequence as shown in FIG. **1***a*, the sending device initiate the transmission with a start pulse **10**, which is followed immediately by a learning sequence **12** and data byte **0**. Data may then be transmitted in independent data sequences **20** that begins with a start pulse **10** followed by data byte **114**.

What is claimed is:

1. An apparatus, comprising:

a first device operating at a first clock frequency, the first device to transmit a learning sequence with a predetermined waveform pattern and a predetermined duration that represents a length of time, based on the first clock frequency; and

a second device to receive the learning sequence and analyze the learning sequence to discover the clock frequency of the first device to adjust a sampling frequency based upon the discovered clock frequency.

2. The apparatus of claim **1**, wherein the learning sequence is preceded by a start sequence that signifies a beginning of a transmission and provides a synchronization point.

3. The apparatus of claim **2**, wherein the first device is configured to maintain a first voltage level while communication is idle and initiate the start sequence where the start sequence comprises a waveform at a different voltage level held for at least two clock cycles.

4. The apparatus of claim **1**, wherein the learning sequence comprises a waveform with a first period of a first voltage level and a second period of a second voltage level.

5. The apparatus of claim **4**, wherein the first voltage level is held for a longer time than the second voltage level.

6. The apparatus of claim **5**, wherein the first period of first voltage level takes up about 80% of the duration of the learning sequence while the second period of second voltage level takes up about 20% of the duration of the learning sequence.

7. The apparatus of claim **4**, wherein the first voltage level is higher than the second voltage level.

8. The apparatus of claim **4**, wherein a subsequent signal transmission by a sending device has the first voltage level with a duration that is longer than a duration of the second voltage level for a representation of logic "1," while a duration of the first voltage level is shorter than a duration of the second voltage level for a representation of logic "0."

9. A bi-directional single wire data communication system, comprising:

a master device having a first clock running at a first frequency; and

a slave device having a second clock running at a second frequency, wherein the master device and the slave

device are communicatively coupled, and the master sends a first command sequence that notifies the slave device of an intent to read, and the slave device sends in response, a learning sequence with a predetermined waveform pattern and a predetermined duration that represents a length of time, based on the clock in the slave device, for transmitting a single bit; and

wherein the master device initiates a counting routine having a duration, in number of clock cycles, of the learning sequence is measured based on the first clock in the master device.

10. The system of claim **9**, wherein the master device sends a second command sequence that notifies the slave device of an intent to write, sends a data sequence which comprises a plurality of data bits, wherein at least one of the plurality of data bits has a predetermined waveform pattern and a predetermined duration based on the first clock in the master device.

11. The system of claim **10**, wherein the first and second command sequence is preceded by a start sequence that signifies the beginning of a transmission and provides a synchronization point.

12. The system of claim **9** configured to provide a one time power-up reset sequence when the slave device is connected to the master device.

13. The system of claim **10**, configured to have the first and second command sequences include addresses of memory to which the master device reads from or writes to respectively.

14. The system of claim **12**, wherein the master device sends a reset pulse and the slave device receives the reset pulse and replies with the start sequence and the learning sequence during a power-up reset sequence.

15. The system of claim **10**, configured to have the learning sequence and at least one of the plurality of data bits represented by a waveform having a first voltage level followed by a second voltage level.

16. The system of claim **15**, wherein the learning sequence has the first voltage level that is held for a longer time period than the second voltage level.

17. The system of claim **16**, wherein the time period at the first voltage level takes up about 80% of the duration of the learning sequence, while the time period at the second voltage level takes up about 20% of the duration of the learning sequence.

18. The system of claim **17**, wherein the first voltage level is higher than the second voltage level.

19. The system of claim **15**, wherein at least one of the plurality of data bits has a first voltage level with a duration that is longer than a duration of the second voltage level for the representation of logic "1," while a duration of the first voltage level is shorter than a duration of the second voltage level for the representation of logic "0."

20. The system of claim **19**, wherein at least one of the plurality of data bits is rejected if a duration of a data bit as measured by the clock in the slave device is less than a first preset number or more than a second preset number, with the first preset number being less than the second preset number.

21. The system of claim **10**, wherein the first and the second command sequences are a byte of data including a single bit that indicates a desired operation and a plurality of bits that indicates a memory location on which to operate.

* * * * *