



(51) International Patent Classification:
H03G 3/20 (2006.01) **H03G 3/30** (2006.01)

(21) International Application Number:
PCT/EP2009/064671

(22) International Filing Date:
5 November 2009 (05.11.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
08305787.7 7 November 2008 (07.11.2008) EP

(71) Applicant (for all designated States except US): **ST WIRELESS SA** [CH/CH]; 39 Chemin du Champ des Filles, Plan-les-Ouates, CH-1288 Geneve (CH).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **AZNAR, Jean-Marc** [FR/FR]; Chemin de la Téréhentine, F-06510 Carros (FR). **SESIA, Stefania** [IT/FR]; 12 Rue d'Italie, F-06000 Nice (FR). **NOEL, Laurent** [FR/FR]; 41 Route des Breguieres, F-06110 Le Cannet (FR).

(74) Agent: **DELPRAT, Olivier**; Bureau D.a. Casalonga & Josse, Bayerstrasse 71/73, 80335 Munich (DE).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD AND DEVICE TO CONTROL THE GAIN OF A RADIO RECEIVER

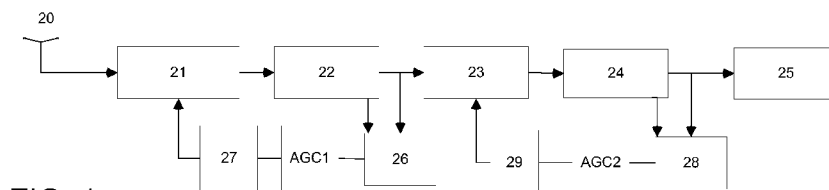


FIG. 1

(57) Abstract: An automatic gain control (AGC) method and system for a radio receiver are proposed in which the AGC comprises two AGC loops; a first loop controlling signal gain in the analogue portion of the radio receiver, a second loop controlling gain in the digital domain after digitization of the received signal. The analogue AGC loop has a slower response time than the digital AGC loop. When applied to a multi-branch diversity receiver, each branch has its own digital AGC loop, but the analogue gain can be common to all branches, based on measurement of the analogue signal in each branch.

METHOD AND DEVICE TO CONTROL THE GAIN OF A RADIO RECEIVER

5 The present disclosure relates to signal processing in radio receivers and in particular to an automatic gain control (AGC) system and method in which the effects of DC current transients on system performance are reduced.

10 Reception of radio signals in a radio apparatus configured therefore and down converting the desired receiving signal from the radio frequency (RF) band into the baseband can generally be done in different ways. A common way is to convert the RF signal down to an intermediate frequency (IF) and in a second step to convert the resulting signal down into the baseband. The converting operation is usually done by a well-known mixing operation with a suitable mixing frequency.

15 For cost reduction, in zero IF receivers, which are broadly used in wireless systems, down conversion from the RF receiving signal to the baseband is done directly without the intermediate frequency step. One drawback in zero-IF receivers is the presence of a residual direct current (DC) offset after the down conversion of the receiving signal, 20 wherein self-mixing of the local oscillators and/or second order intermodulation of the employed mixers creates DC offsets in the baseband signal. Further, even-order distortions may convert strong interfering signals to baseband. Furthermore, $1/f$ noise being inherent in all semiconductor devices and being inversely proportioned to the frequency (f) may mask the baseband signal. Moreover, direct 25 conversion receivers put high demands on the baseband signal processing components because gain control and filtering must be done at baseband frequency range.

30 In modern receiver architectures, the analog RF receiving signal is converted from the analog domain into the digital domain for further processing, since digital signal processing is available with high performance and at low cost. In order to match the signal dynamics required by the system before and after the used analogue-to-digital

converters (ADC), an automatic gain control (AGC) system could be used for control of amplification gain for the receiving signal in the one or more signal amplifiers located in the reception path.

5 The DC offset may be quite large causing saturation of the ADC, e.g. leading to loss of dynamics, and other problems in the receiver. To cope with these effects, so called DC offset compensation circuits are generally employed in the reception (RX) path of radio receivers. Basically, a simple example for DC offset cancellation is application of capacitors, connected in series into the signal path and thus blocking
10 propagation of DC signals. A more complex approach is an active high pass filter configured to remove the unwanted DC components inherent to self-mixing products.

Usually, AGC is implemented by a respective gain control algorithm. Due to the digital nature of most AGC systems, also the
15 analogue gain, i.e. in the receiving path before the ADC, is adjusted by changing the gain of the respective amplifiers in a stepwise manner, i.e. the gain is controlled in discrete gain steps. However, switching of the gain in the signal path generates DC transients in the DC offset, which from a frequency spectrum point of view contain higher frequency
20 components, which cannot be filtered or cancelled by the DC offset compensation or cancellation circuits.

Thus, even that the DC compensation is permanently active, DC transients occur at gain step transitions; every time these gain steps are toggled. Moreover, these transients are heavily RF architecture
25 dependent. Their settling time and peak voltage depend on a variety of RF IC architecture parameters, such as the impedance of the receiving gain chain, the location of the AGC loops with regards to amplifier gain locations and the weight of the gain step.

For instance, link level simulations for UMTS release 5, HSDPA,
30 have shown that DC transients in the order of the frame rate caused by the AGC loop degrade the throughput versa system performance of baseband (BB) integrated circuit (IC), e.g. the signal to noise ratio (SNR).

US 2005/0208916 A1 discloses a direct down conversion receiver architecture comprising a digital variable gain amplifier (DVGA), an automatic gain control (AGC) loop to provide gain control for the DVGA and RF/analog circuitry, and a serial bus interface (SBI) unit to provide controls for the RF/analog circuitry via a serial bus.

US 2003/ 0199264 A1 discloses a system and method for a fast acquiring DC offset cancellation by increasing high pass loop bandwidth and adjusting DC offset levels at baseband. Afterwards the high pass loop bandwidth is decreased in order to fine-tune the previous estimate and to remove small variation in DC.

In view of the foregoing, a method and a system are proposed allowing a reduction of effects of DC current transients on receiver system performance.

According to a first aspect, an automatic gain control system for a radio receiver is proposed, this system having at least one receiving signal path with an analogue and a digital portion.

According to a general feature, the AGC system comprises at least two AGC loops, wherein at least one first AGC loop is configured to control the gain of at least one signal amplifier in the analogue portion of the receiver and has a first cycle time; wherein at least one second AGC loop is configured to control signal amplification of at least one signal processing unit in the digital portion of the receiver and has a second cycle time, and wherein the second cycle time is shorter than the first cycle time.

In certain embodiments, the first cycle time is by orders of magnitude longer than the second cycle time.

In other embodiments, for example if there is no frequent variation of signal reception conditions expected, the first cycle time might not be used at all, but only actually appearing variation of reception conditions lead to a gain control in the analogue portion of the receiver.

In certain embodiments the radio receiver is a multi-branch receiver, which comprises a plurality of generally similar receiving signal paths, each path being equipped with at least two AGC loops, i.e.

at least one arranged in the analogue portion and the at least one other arranged in the digital portion of the respective receiving signal paths of the receiver.

5 Accordingly, according to another feature of the AGC, the radio receiver is a multi-branch receiver having at least two parallel receiving signal paths, each receiving signal path comprises at least one first Automatic Gain Control loop and at least one second Automatic Gain Control loop.

10 In certain embodiments, the arrangement of the multi-branch receiver may be part of a diversity receiver, which operates several antennas for enhancing signal reception capability.

In a further development, the gain of the receiving signal amplification in the analogue portion of each receiving signal path is set or controlled by means of the same gain control signal. For example, in
15 a dual branch diversity receiver, each branch has its own digital AGC loop, but the analogue gain can be arranged as common for both branches, based on measurement of the analogue signal in each branch. This advantageously enables reduction of hardware and firmware (FW) or software (SW), i.e. the embedded code in the baseband, complexity
20 and thus reduces e.g. costs and weight.

The basic idea of the AGC system resides in the perception that DC transients due to gain step transitions in the analog AGC system in radio receivers reduce system performance. The present disclosure provides an improved AGC system and a respective AGC method, by
25 which susceptibility of radio receivers to such DC transients is remarkably reduced. This is achieved by combining at least two AGC loops in the radio receiver signal path, where a first loop is arranged for controlling gain in the analogue domain of the receiver and a second loop is arranged for controlling gain in the digital domain after A/D
30 conversion, i.e. digitization of the received signal. By configuring the analogue AGC loop with a substantial slower cycle time than the digital AGC loop, the occurrence of DC transients can be effectively reduced.

For example, the system is located in a receiving signal path of a mobile communication device or a mobile station.

The mobile communication device or station may thus comprise a receiver for at least one of a wireless communication systems, wireless local loops, wireless LAN applications, and/or cellular systems in accordance with at least one of the following communication standards
5 UMTS, WCDMA, UTRATDD, UTRAFDD, TDSCDMA, CDMA2000, and OFDMA.

For example, the mobile communication device or station is a device capable for High Speed Downlink Packet Access.

According to a second aspect, it is hereby proposed a method for
10 Automatic Gain Control (AGC) in a radio receiver having at least one receiving signal path with an analogue and a digital portion, the method comprising

- at least one first amplifying step, in which an analogue receiving signal is amplified in the analogue portion,
- 15 - digitizing the amplified analogue receiving signal into a digitized receiving signal;
- at least one second amplifying step, in which the digitized receiving signal is amplified in the digital portion,
- controlling a first gain for said first amplifying step based on a
20 first cycle time (t_1), and
- controlling a second gain for said second amplifying step based on a second cycle time (t_2),
wherein the second cycle time is shorter than first cycle time.

According to another feature, the method comprises processing
25 of several receiving signals in a multi-branch receiver having at least two parallel receiving signal paths, the step of controlling the first gain comprising determining one common gain control value in each branch.

For example the second cycle time is by orders of magnitude shorter than the first cycle time.

30 The method may further comprise controlling the first gain independently of the first cycle time based on determining if there is a predetermined change in receiving conditions.

According to a further aspect, it is hereby proposed a computer program comprising program instructions, which, when performed on a

programmable processor, cause the processor to perform the steps of a method as defined above.

Preferred embodiments and further developments of the present disclosure are defined in the dependent claims of the independent
5 claims. It shall be understood that the apparatus and the method of the present disclosure have similar and/or identical preferred embodiments and advantages.

These and other aspects will be apparent from and elucidated with reference to the embodiment(s) described hereinafter. In the
10 following drawings, the figures are schematically drawn and not true to scale, and identical reference numerals in different figures, if any, may refer to corresponding elements. It will be clear for those skilled in the art that alternative but equivalent embodiments are possible without deviating from the true inventive concept.

15 - fig. 1 illustrates an example of a signal path in an embodiment of radio receiver of the first aspect;

- fig. 2 shows a time diagram, illustrating DC offset variation during a gain adjustment operation by the Automatic Gain Control (AGC), causing DC transients;

20 - fig. 3 is a flow chart illustrating the processing of two AGC loops; and

- fig 4 shows a further embodiment of a radio receiver applied to a dual-branch receiver.

The higher the update rate of an AGC loop controlling gain in an
25 analogue portion of a transfer path, the higher is the occurrence or frequentness of DC transients caused by change of the amplification gain of the received analogue signal containing DC offset.

The present disclosure proposes an improvement to the AGC system and respective AGC method in a radio receiver aiming on a
30 significant reduction of such DC transients in the receiving signal.

This is accomplished by, basically, employing at least two separate AGC loops in the radio receiver signal path. The at least one first AGC loop is configured to control solely signal amplification in the analogue portion of the signal path. According to the herein presented

solution, a first cycle rate of the first AGC loop defines the time span between two possible amplification adaptations, i.e. between two possible DC transients. Preferably, the first cycle time is predefined in order to match particular system requirements. For example, the cycle time can be made dependent on the propagation conditions. That is to say, the system may be configured to adapt the cycle time automatically to a predetermined longer value if propagation conditions are static or to a predetermined shorter value in case of multi-path fading conditions. For instance, for the assumption of 3G UMTS environment, under multi-path fading conditions, e.g. two path with about 3km/h, as cycle time of one UMTS frame, i.e. 10 ms, or one slot, i.e. 667 ms, may be used. Further, for static propagation conditions a cycle time of 20 UMTS frames, i.e. 200 ms, or even more may be applied.

The at least one second AGC loop is configured to control signal amplification in the digital portion of the signal path. According to the herein presented solution, this second AGC loop has a second cycle time, which is defined independently from the first cycle time. According to the present disclosure, the analogue first AGC loop has a substantial longer cycle time than the second digital AGC loop.

Fig 1 illustrates a schematic block diagram of a receiving signal path of a radio receiver in accordance with a first embodiment. An antenna 20, for reception of a radio frequency signal of interest, is followed by a radio frequency (RF) receiving signal amplifier 21, e.g. a low noise amplifier (LNA). The amplifier 21 is followed by an analogue to digital converter (ADC) 22.

After the ADC 22, the receiving signal passes a filter 23, e.g. a raised cosine filter (RRC) filter, and a scaler 24 before supplied to an equalizer 25.

Based on the output of the ADC 22, a Pre-Filter RRSS detector 26, detects the signal level of the output of the ADC 22 and/or receives an output of the ADC 22 which indicates if the ADC 22 is saturated by the input signal. Pre-(filter)-RRSS detector 26 is configured to measure the relative receive signal strength (RRSS) of the received (Rx) I/Q baseband signal. Detector 26 measures the I/Q signal received after the

ADC 22 as AGC analog loop related measurement, and thus named Pre-RRSS or Pre-RRC (with reference to the RRC filter). The detector 26 provides an input signal to a slow first AGC loop AGC1. The slow first AGC loop AGC1 operates a serial peripheral interface SPI RF, e.g. a 3-wire bus which vehicles the control words for the radio transceiver, control 27 controlling the radio frequency amplifier 21 by a first gain control signal G1.

After the scaler 24 is a post-(filter)-RRSS detector 28, which provides an input signal to a fast second AGC loop AGC2. Again the post-(filter)-RRSS detector is configured to measure the Rx digital I/Q baseband signal strength received after the scaler 24. Detector 28 measures the root-raised cosine filtered baseband signal as AGC digital loop related measurement, thus also named post-RRSS or post-RRC (with reference to the RRC filter). The fast second AGC loop AGC2 controls the digital implemented gain in the scaler 24 by a gain control signal G2.

Referring now to Fig. 2 the principle of DC offset compensation timing is discussed. Fig. 2 shows a schematic timing diagram, illustrating varying DC offset current 30 in a radio receiver with a stepwise gain control. At a first point in time 31 the analogue signal amplification is toggled boosting the DC share of the signal. This boost contains according to Fourier analysis a large plurality of frequencies not originating from and not associated with the received signal but now propagated via the same transfer path leading to interference and noise.

Further, until the existing DC offset compensation means lower the DC offset current, during time span 32 electric power is wasted, signal dynamic is reduced and generally unwanted heat is produced within the device. Depending on characteristics of the existing DC offset compensation means the graph may look different and thus the impact to the signal may also differ from that depicted in Fig. 2. Nevertheless, the discussed effects generally exist and applying the present teaching can reduce their occurrence frequency.

Now with reference to Fig 3, the operation of the AGC system will be explained in more detail. Thus, fig. 3 shows a flow chart of the

AGC method, which can be implemented in a respective radio receiver. Note, in the flow chart at steps where a condition is checked, “0” corresponds to “NO” and “1” corresponds to “YES”.

5 It goes without saying that the method steps described in the following can be implemented by means of a programmable processor, where the method steps are coded by means of program code instructions, which when run on the processor, cause the processor to perform the steps of the AGC method.

10 At the beginning of the AGC algorithm, at step S100, a timer T1 is started for the first cycle rate or time for control of the first analogue AGC loop, i.e. the slow AGC loop AGC1.

15 The signal gain in at least one amplifier located in the analogue portion of the receiving signal path is adjusted in step S200 in accordance with a certain criteria, e.g. such as based on the result of checking whether the ADC 22 is saturated or not.

20 Then, in step S 300 it is judged whether the amplified receiving signal is in the dynamic range of the receiver or not. If not, the procedure returns to step S200, where a gain adjustment is done. That is to say, the adjustment loop is passed until analogue signal gain matches the dynamic range of the receiver.

Now, until further notice, in step S400 the first analogue AGC loop is deactivated. Hence, no further DC transients will be generated in the analog domain.

25 Next, in step S500 a second timer T2 for timing of the second cycle rate or time of the second digital AGC loop AGC2 is started.

30 In step S600 the signal gain in at least one unit of the digital portion of the receiving signal path is adjusted. In the following step S700 a check is done whether in the meantime an important or significant change in the receiving conditions of the receiving signal has happened, which cannot be coped with by the second digital AGC loop alone. Thus, a gain adjustment is required in the first analog AGC loop, i.e. in the analogue portion of the radio receiver.

If so (YES), the procedure goes to step S800, where the analogue AGC loop is reactivated again.

In the other case (NO), the status of the first timer T1 is checked in step S900. If the first timer T1 has expired (YES), i.e. the first cycle time period is over, the procedure continues at step S800. In other words, the analogue AGC loop is reactivated again in step S800 regardless of the actual set gain control value G1.

If the first timer T1 has not expired (NO), then in step S1000 the second timer T2 is checked. In the case that the second timer T2, i.e. the second cycle time period is over (YES), the second digital AGC loop is recurred by a return of the AGC procedure to step S500.

If the second timer T2 has not expired (NO), then the AGC procedure goes to step S900 and the first timer T1 is again checked in step S900.

It should be noted that fig. 3 in connection with the description above illustrates only one particular embodiment by way of an example. It goes without saying, that the herein disclosed principle can be varied or modified without deviating from the scope of the present disclosure. For instance, the timer T1 could be left and only one time could be used for both AGC loops, implemented by a central AGC control unit. Then, only detection of an important change in reception conditions would return the algorithm back into the analogue gain adjustment in steps S200 and S300. Also disabling S400 and enabling S800 the analogue AGC loop could be dropped without departing from the herein described principle.

In further development the herein disclosed AGC system can be implemented into each branch of a multi-branch radio receiver, e.g. such as a diversity receiver. In this case, each receiving signal path or branch between one antenna 20 or more antennas and the equalizer 25 comprises the at least two separate AGC loops which operate independently of one another. Such an application of the AGC system and method is in particular useful for spatial diversity reception.

Moreover, in still another further development, the receiver comprises at least two parallel receiving signal paths, where the respective at least two analogue amplifiers in each receiving signal branch may be controlled by one single, i.e. common, amplification gain

control signal or factor, respectively, based on measurement of the analogue signal in each branch or path.

Fig. 4 shows an embodiment of such multi-branch receiver architecture as a further development, where two basically identical receiving signal branches or paths, as illustrated in fig. 1, are arranged in parallel. The receiving signal branches and share parts of the first analog AGC loop. That is to say, the first automatic gain control AGC1 is a common entity located in the analogue portion and the SPI RF control 27 controls amplification of both receiving signal paths. The other elements of the two branches remain separate and keep operating independently, i.e. the operation is in principle the same as described in connection with Figs. 1 to 3.

Accordingly, hardware (HW) complexity can be reduced regarding not only the number of HW pins, but also by reducing the digital RF control interface and FW or SW complexity. For instance, only two sets of three wire-buses, i.e. six control lines altogether are required. Thus, the novel AGC architecture allows simplification of the HW RF-Bbi interface of a HSDPA system, where by means of a single common three wire bus may be used to control the two radios.

In preferred embodiments the present disclosure is implemented in a mobile station. As mentioned above particularly wireless devices comprising zero-IF receivers benefit from efficient DC offset compensation. Especially battery powered devices benefit from reduced power losses by DC offset compensation. Thus battery life cycles and user's mobility are not unnecessarily shortened.

Possible applications for the present principle are in receivers for wireless communication systems, including wireless local loops, wireless LAN applications, and cellular systems such as 3G UMTS, i.e. Wideband Code Division Multiple Access (WCDMA) both UMTS Terrestrial Radio Access Time Division Duplex (UTRATDD) and UMTS Terrestrial Radio Access Frequency Division Duplex (UTRAFDD), Time Division-Synchronous Code Division Multiple Access (TDSCDMA), CDMA2000, Orthogonal Frequency Division Multiple Access (OFDMA)

systems. These receivers are common in mobile stations being capable of operating in cellular communication networks.

5 It shall be appreciated, that examples and embodiments of the present disclosure discussed above shall only aid in understanding and using the above description and many variations will be apparent to those skilled in the art that can be applied without departing from the scope of this disclosure as defined in the appended claims.

10 While the disclosure has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the disclosure is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the disclosure, from a study of the drawings and the appended claims. In the claims, the word
15 "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single means or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these
20 measured cannot be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS

1. Automatic Gain Control system for a radio receiver having at least one receiving signal path with an analogue and a digital portion, the Automatic Gain Control system comprising:
- 5 at least two Automatic Gain Control loops,
 wherein at least one first Automatic Gain Control loop is configured to control the gain of at least one signal amplifier located in the analogue portion of the receiver and has a first cycle time (t_1),
 wherein at least one second Automatic Gain Control loop is
10 configured to control signal amplification of at least one signal processing unit in the digital portion of the receiver and has a second cycle time (t_2); and
 wherein the second cycle time (t_2) is shorter than the first cycle time (t_1).
- 15 2. System according to claim 1,
 wherein the radio receiver is a multi-branch receiver having at least two parallel receiving signal paths, and
 wherein each receiving signal path comprises at least one first Automatic Gain Control loop and at least one second Automatic Gain
20 Control loop.
3. System according to claim 2,
 wherein in each receiving signal path the at least one first Automatic Gain Control loop is set by means of the same gain control signal.
- 25 4. System according to claim 1,
 wherein the system is located in a receiving signal path of a mobile communication device or a mobile station.
5. System according to claim 4,
 wherein the mobile communication device or station comprises a
30 receiver for at least one of a wireless communication systems, wireless local loops, wireless LAN applications, and/or cellular systems in accordance with at least one of the following communication standards

UMTS, WCDMA, UTRATDD, UTRAFDD, TDSCDMA, CDMA2000, and OFDMA.

5 6. System according to claim 4,
 wherein the mobile communication device or station is a device
capable for High Speed Downlink Packet Access.

 7. Method for Automatic Gain Control (AGC) in a radio receiver
having at least one receiving signal path with an analogue and a digital
portion, the method comprising

10 - at least one first amplifying step, in which an analogue
receiving signal is amplified in the analogue portion,

 - digitizing the amplified analogue receiving signal into a
digitized receiving signal;

 - at least one second amplifying step, in which the digitized
receiving signal is amplified in the digital portion,

15 - controlling a first gain for said first amplifying step based on a
first cycle time (t_1), and

 - controlling a second gain for said second amplifying step based
on a second cycle time (t_2),

20 wherein the second cycle time (t_2) is shorter than first cycle time
(t_1).

 8. Method according to claim 7,
 wherein the method comprises processing of several receiving
signals in a multi-branch receiver having at least two parallel receiving
signal paths, and

25 wherein the step of controlling the first gain comprises
determining one common gain control value in each branch.

 9. Method according to claim 7,
 wherein the second cycle time is by orders of magnitude shorter
than the first cycle time.

30 10. Method according to claim 7,
 wherein the method further comprises controlling the first gain
independently of the first cycle time (t_1) based on determining if there
is a predetermined change in receiving conditions.

11. Computer program comprising program instructions, which, when performed on a programmable processor, cause the processor to perform the steps of a method in accordance with one of the claims 7 to 10.

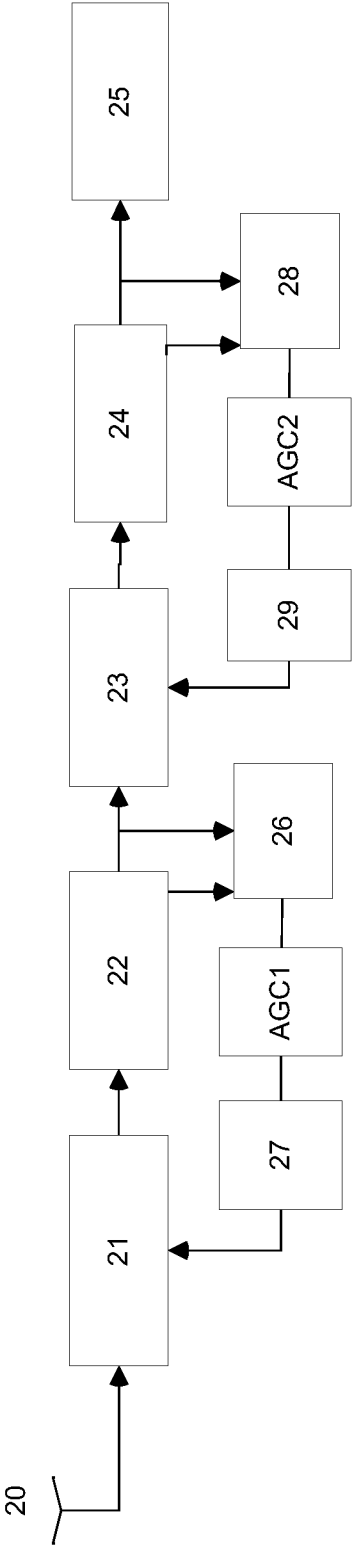


FIG. 1

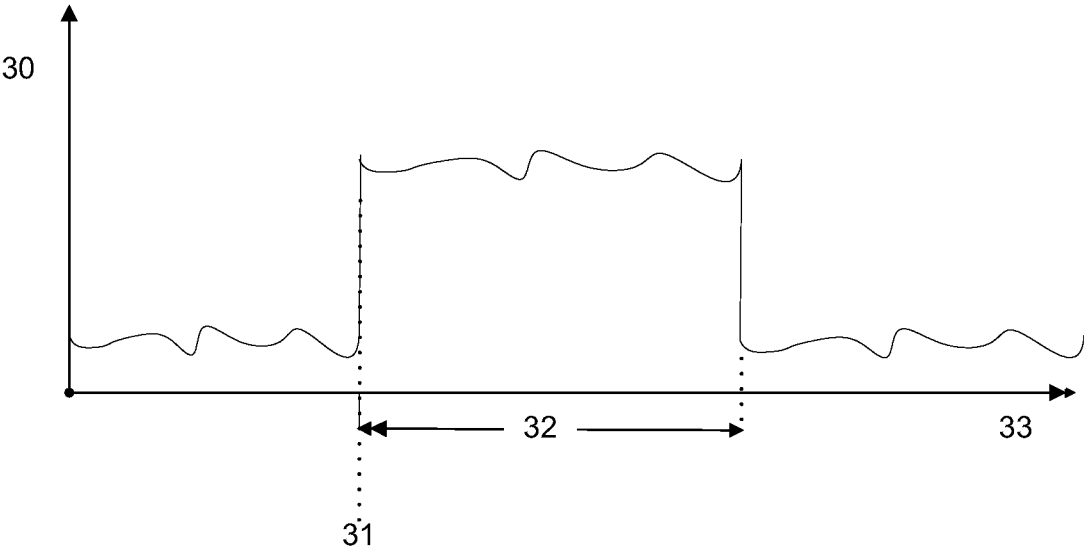


FIG. 2

3/4

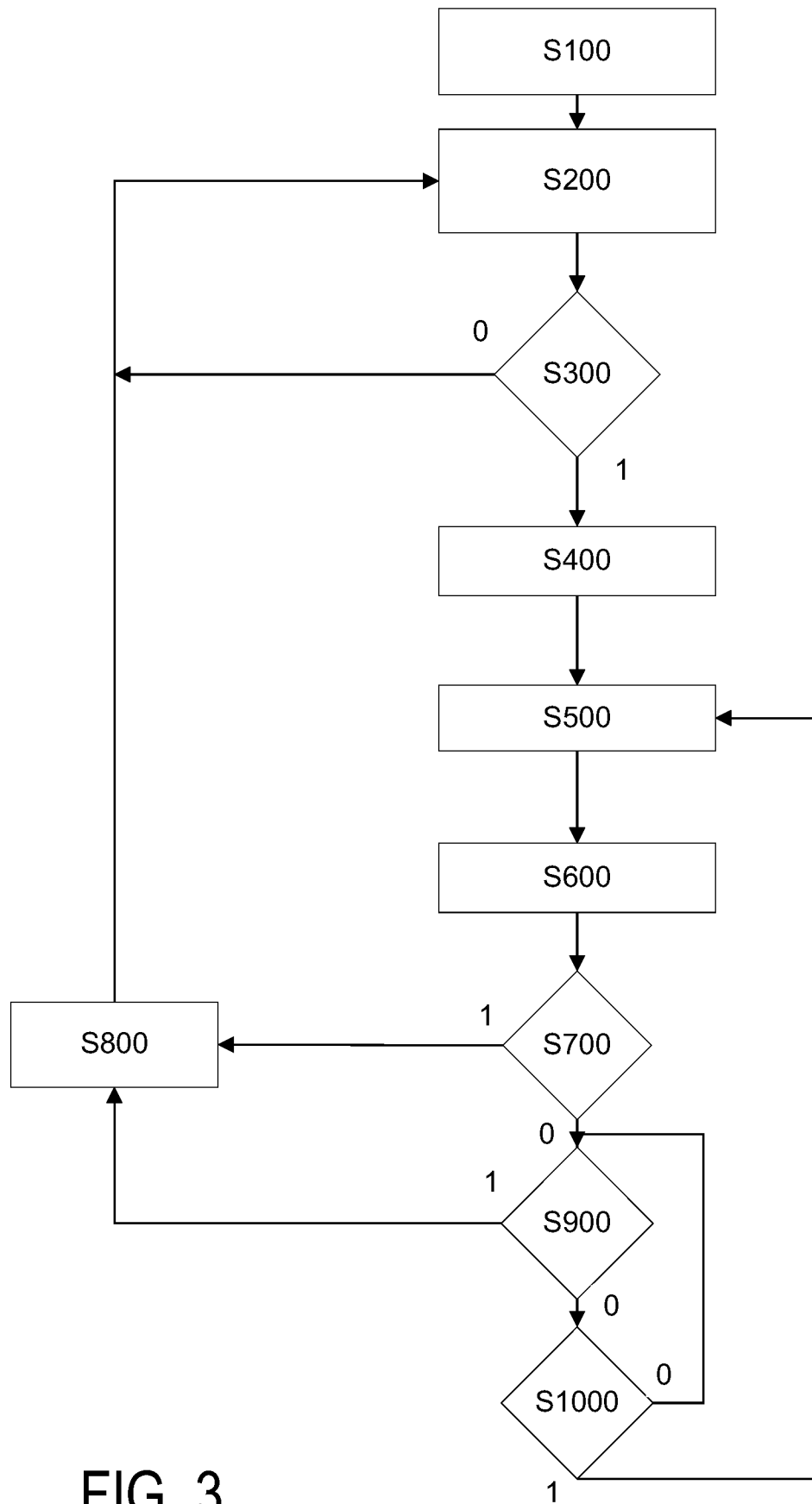


FIG. 3

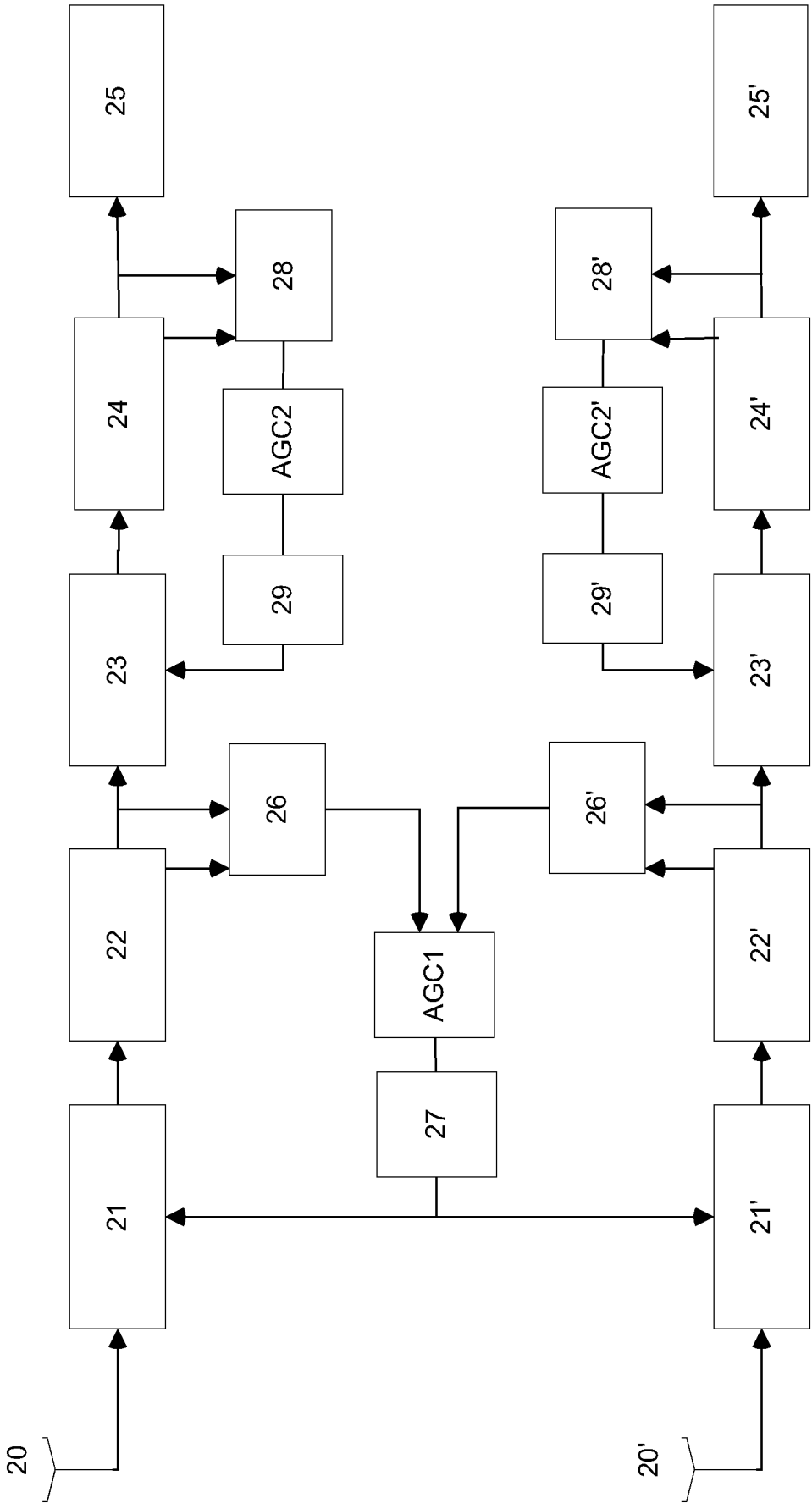


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/064671

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03G3/20 H03G3/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03G H04B H04W H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 216 353 A (SILICON SYSTEMS INC [US]) 4 October 1989 (1989-10-04) abstract page 7, paragraph 2 - page 10, paragraph 1; figure 1	1-11
X	LANE F ET AL: "A SINGLE CHIP DEMODULATOR FOR 64/256 QAM" 19961101, vol. 42, no. 4, 1 November 1996 (1996-11-01), pages 1003-1010, XP011008334 the whole document	1,7
A	EP 1 531 565 A (FUJITSU LTD [JP]) 18 May 2005 (2005-05-18) paragraph [0106] - paragraph [0111]; figure 2	2,8

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search

27 January 2010

Date of mailing of the international search report

04/02/2010

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Blaas, Dirk-Lütjen

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/064671

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/151264 A1 (MONTJOJO JUAN [US] ET AL) 5 August 2004 (2004-08-05) abstract paragraph [0018]; figures 2,4 -----	1-2,7-8
A	US 2008/273636 A1 (ZHU MINGRUI [US] ET AL) 6 November 2008 (2008-11-06) paragraph [0028] - paragraph [0042]; figures 1,3 -----	1-11
A	US 7 088 975 B1 (GOMEZ RAMON A [US] ET AL) 8 August 2006 (2006-08-08) abstract -----	1-2,7-8

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2009/064671

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
GB 2216353	A	04-10-1989	JP 1309418 A	13-12-1989
			JP 2909509 B2	23-06-1999
			US 4870370 A	26-09-1989
EP 1531565	A	18-05-2005	WO 2004006476 A1	15-01-2004
			JP 3924300 B2	06-06-2007
US 2004151264	A1	05-08-2004	AT 368978 T	15-08-2007
			BR PI0407127 A	10-01-2006
			CA 2514884 A1	19-08-2004
			DE 602004007887 T2	17-04-2008
			EP 1588517 A1	26-10-2005
			JP 2006517770 T	27-07-2006
			KR 20050096967 A	06-10-2005
			MX PA05008215 A	04-11-2005
			WO 2004071005 A1	19-08-2004
US 2008273636	A1	06-11-2008	WO 2008137837 A1	13-11-2008
US 7088975	B1	08-08-2006	NONE	