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(54) Error correction in a digital video recorder capable of high speed reproduction

(57) While recording and reproducing in a digital VTR, sync-block unit data is separated into an independent decodable code (IDC) and a dependent decodable code (DDC) to which respective inner parities are added and then recorded, and the independent decodable code (IDC) only is error-corrected during variable tape-speed reproduction. The IDC code contains the minimum information required to faithfully reproduce the original image whilst the DDC code contains the remaining information required to add detail to the image and during high-speed reproduction the IDC code only is used to form the image.

An embodiment of the error-correcting encoding apparatus is shown in fig. 2.

FIG. 2

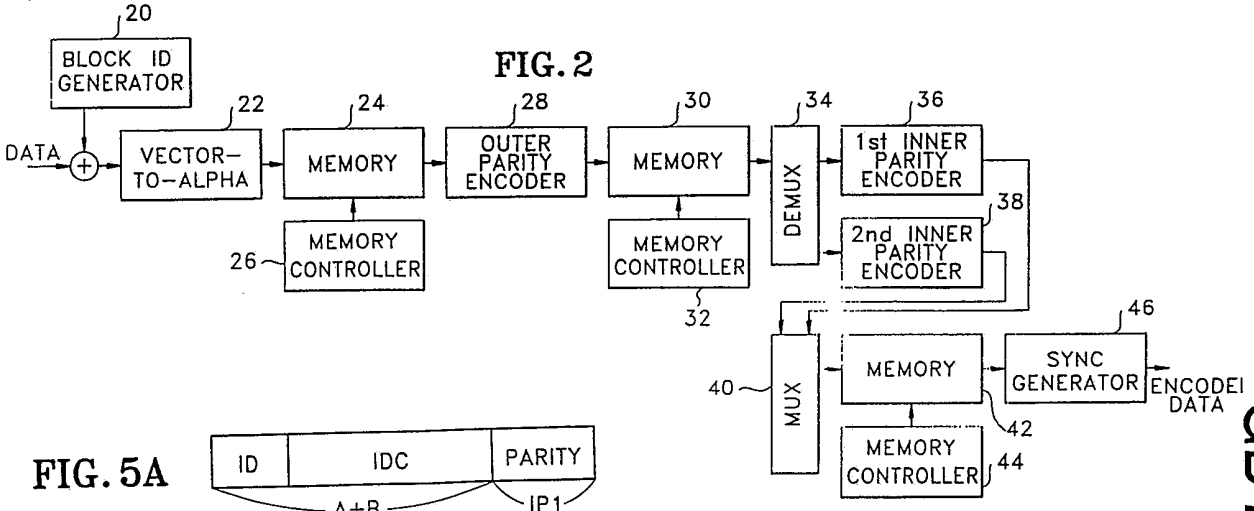

FIG. 5A

FIG. 5B

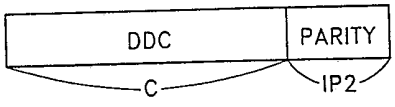

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FIG. 1

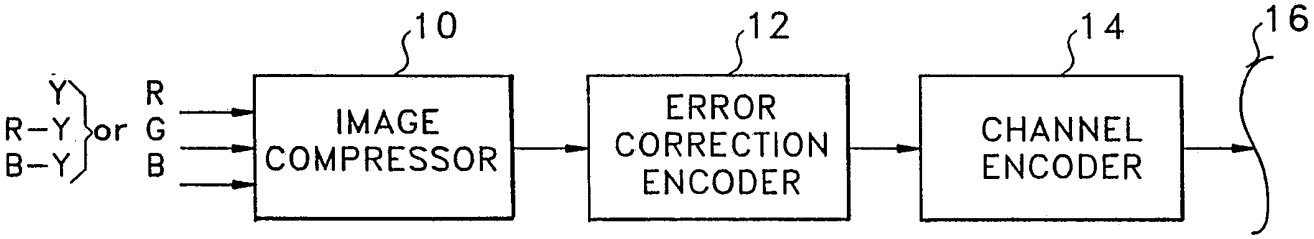

10
12
14
16
Y
R-Y
B-Y
or
R
G
B
IMAGE COMPRESSOR
ERROR CORRECTION ENCODER
CHANNEL ENCODER

FIG. 2

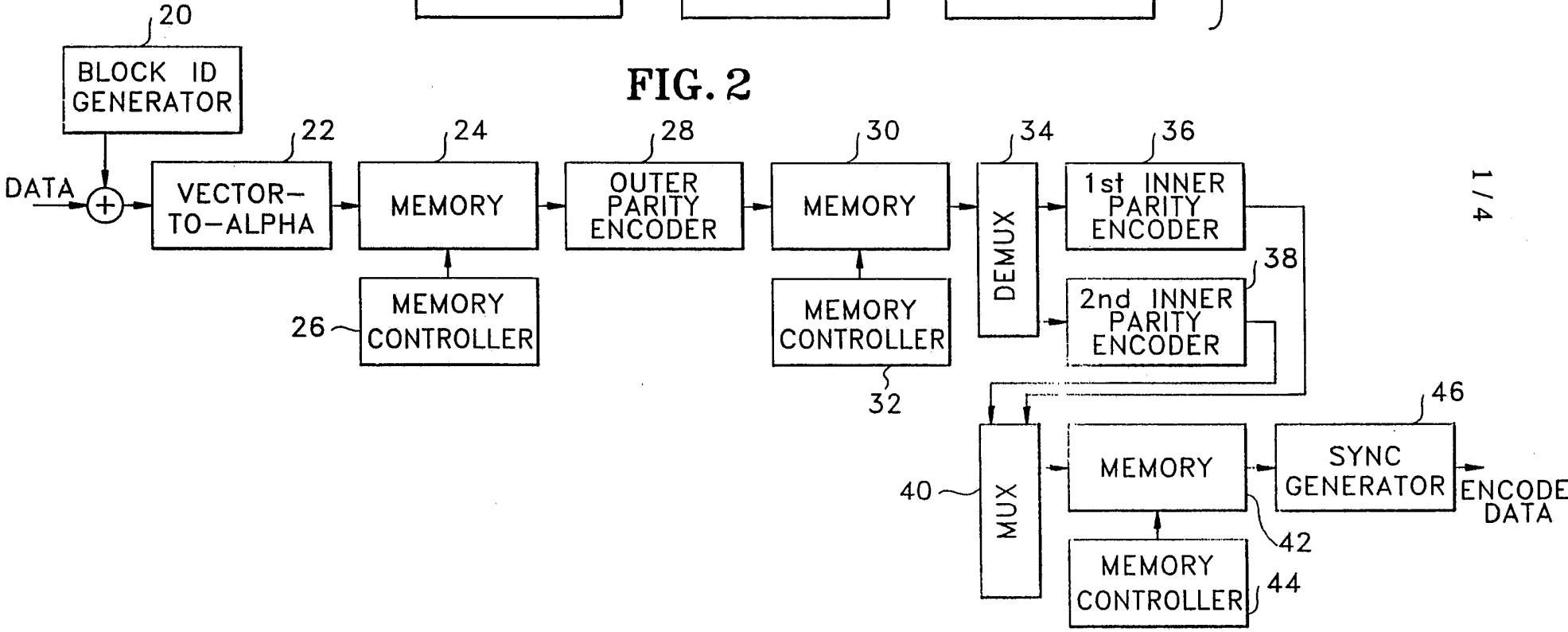

20
BLOCK ID GENERATOR
DATA
22
VECTOR-TO-ALPHA
24
MEMORY
26
MEMORY CONTROLLER
28
OUTER PARITY ENCODER
30
MEMORY
32
MEMORY CONTROLLER
34
DEMUX
36
1st INNER PARITY ENCODER
38
2nd INNER PARITY ENCODER
40
MUX
46
MEMORY
42
SYNC GENERATOR
ENCODE DATA
MEMORY CONTROLLER
44

FIG. 3

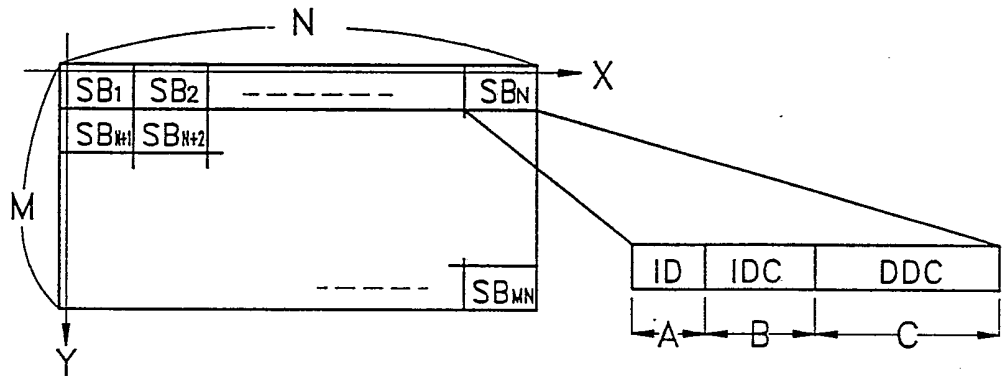

N
X
M
Y
SB1
SB2
SBN
SBN+1
SBN+2
SBMN
ID
IDC
DDC
A
B
C

FIG. 4

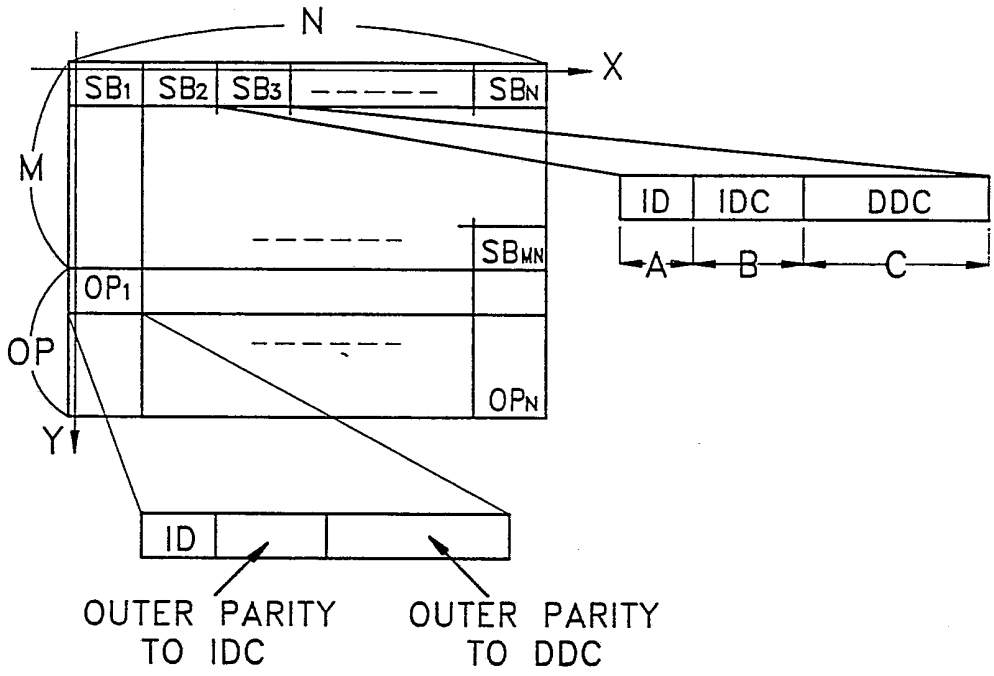

N
X
M
OP
Y
SB1
SB2
SB3
SBN
SBMN
OP1
OPN
ID
IDC
DDC
A
B
C
ID
OUTER PARITY TO IDC
OUTER PARITY TO DDC

FIG. 5A

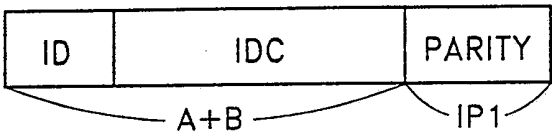


FIG. 5B

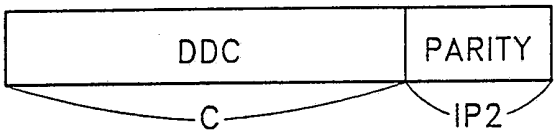


FIG. 6

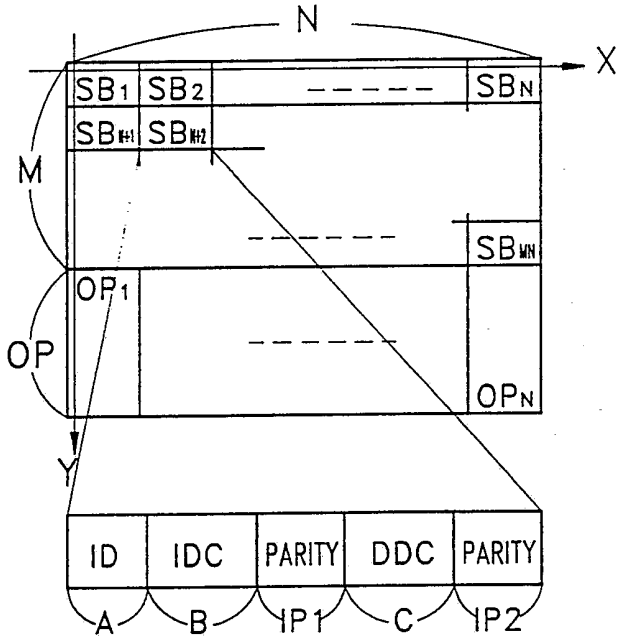


FIG. 7

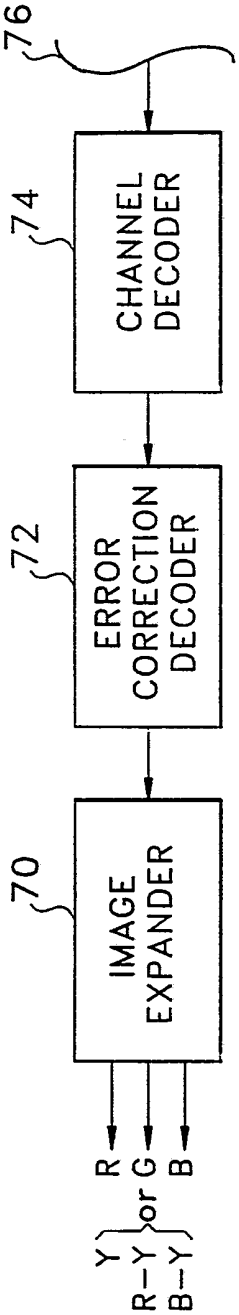
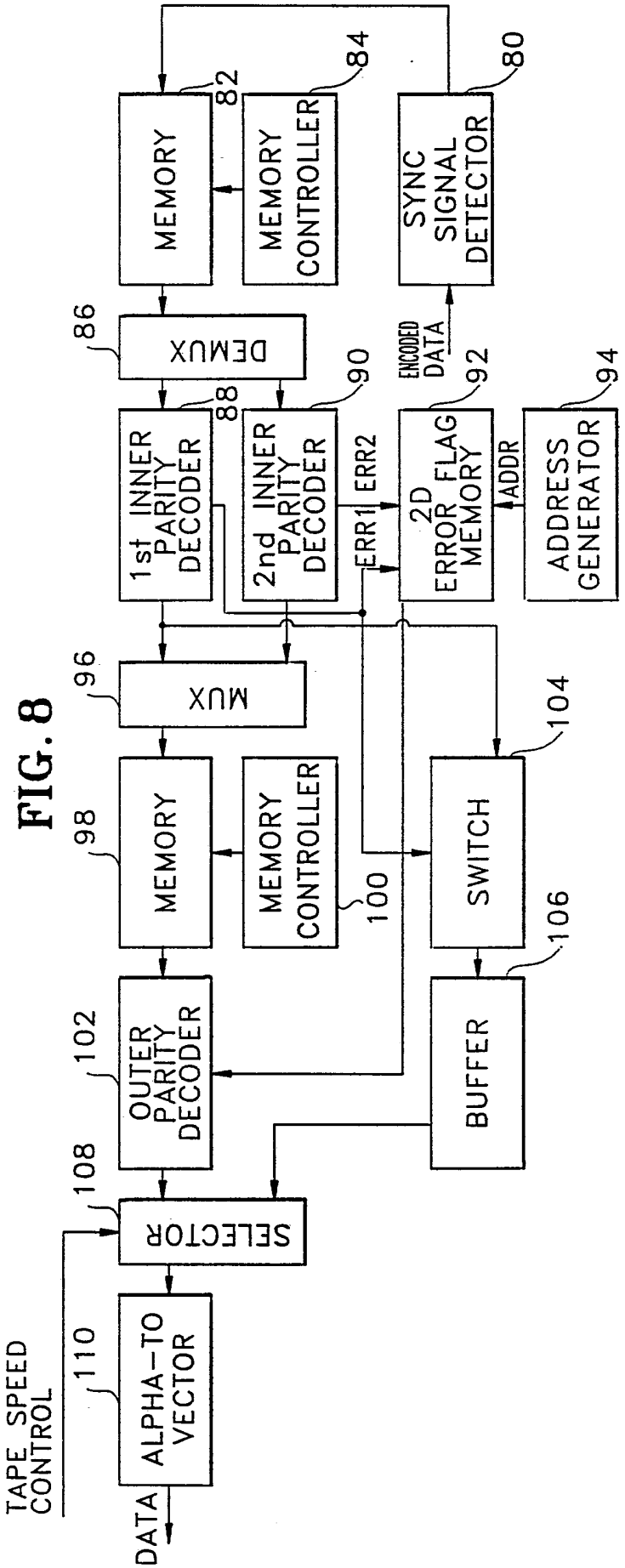

76
74
CHANNEL DECODER
72
ERROR CORRECTION DECODER
70
IMAGE EXPANDER
R
G
B
or
Y
R-Y
B-Y

FIG. 8


MEMORY
82
MEMORY CONTROLLER
84
SYNC SIGNAL DETECTOR
80
DEMUX
86
ENCODED DATA
92
1st INNER PARITY DECODER
88
2nd INNER PARITY DECODER
90
ERR1
ERR2
2D ERROR FLAG MEMORY
ADDR
ADDRESS GENERATOR
94
MUX
96
MEMORY
98
MEMORY CONTROLLER
100
SWITCH
104
OUTER PARITY DECODER
102
BUFFER
106
SELECTOR
108
TAPE SPEED CONTROL
ALPHA-TO VECTOR
110
DATA

ERROR CORRECTION IN DIGITAL RECORDING

The present invention relates to error correction in digital reording, and particularly although not exclusively to an error correcting method and apparatus of a digital video tape recorder (VTR).

A digital VTR records and/or reproduces image information as a digital signal, which has advantages over a conventional analog magnetic recording/reproducing apparatus, such as increased signal-to-noise ratio, increased resolution, easy editing, etc. Such a digital VTR typically converts an analog signal of a frame image into a digital signal, and stores the converted signal in a frame memory. The data stored in the frame memory is partitioned into unit blocks, and then compressed by a discrete cosine transform (hereinafter referred to as "DCT") operation and a Huffman variable-length coding. Each compressed unit block is added by an error correction code (inner parity), and then reorganized in another frame memory according to its original position. An outer parity block having another error correction code (outer parity) is added to each unit block in the vertical direction of the reorganized frame memory. The unit block and outer parity block are added with sync signal and block address, and then sequentially recorded on tracks of a tape. During reproduction, the unit block and outer parity block are reproduced from a pick-up signal generated by a head scanning the track, and the reproduced unit blocks or outer parity blocks are recorded in the frame memory in accordance with each block address. After that, error correction by the outer and inner parities, inverse Huffman variable coding, and inverse DCT are performed with respect to the unit blocks recorded in the frame memory. The digital signal having been subjected to

the inverse DCT is analog-converted, so that the analog signal representing the original image becomes reproduced.

The unit block is converted into an energy function having DC and AC coefficients by the DCT. A characteristic of the DCT is in that almost all energy of a signal converges on the low-frequency portion. In the Huffman variable-length coding, the coefficients of the frequency function are variable length-coded. To execute a variable tape-speed reproduction, the recording has to be carried out by compressing the bit amount of each unit block to be constant. When each block is compressed to have a constant bit amount, simple and complex portions in the original picture are compressed to the same bit amount, so that reproducibility of the complex portion degrades as compared with that of the simple portion during reproduction. Accordingly, to provide overall uniform reproducibility in the picture during normal reproduction, the relative complexity of a frame is calculated, and the bit amount of each unit block is adjusted. That is, fewer bits are allocated to the simple portions, and more bits are allocated to the complex portions.

U.K. Patent application 92 16119.9 (priority claim based on Korean patent application No. 92-4227) filed by this applicant discloses a method wherein recording is carried out by separating a unit block into an independent decodable code (hereinafter simply referred to as "IDC") having almost all information needed for reproducing the original image and a dependent decodable code (hereinafter simply referred to as "DDC") having the remaining information. In this method, the original image is reproduced by utilizing both IDC and DDC during normal reproduction, and IDC only during variable tape-speed reproduction, which makes the variable tape-speed reproduction simple and easy. Also, in spite of the occurrence of mismatched

sync blocks due to traversing the heads on several tracks during variable tape-speed reproduction, an image which is almost the same as the original image can be reproduced, provided that the IDC is detected, which is one portion of the unit block. Therefore, it is preferable that IDC and DDC are recorded by separate way of error correction encoding, to enhance reproduction rate of the recorded data during reproduction.

Preferred embodiments of the present invention aim to provide an error correcting encoding method suitable for a method of recording unit blocks truncated into an independent decodable code and a dependent decodable code.

It is another aim to provide an error correcting decoding method capable of facilitating a variable tape-speed reproduction.

It is yet another aim to provide an apparatus suitable for the error correcting encoding method.

It is still another aim to provide an apparatus suitable for the error correcting decoding method.

According to one aspect of the present invention, there is provided an error correcting encoding method in a digital video recorder or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code to record it in sync-block unit, and said recorded data is reproduced in accordance with the inverse order of said recording step,

said error correcting encoding method comprising a step of adding respective first and second inner parities to a block identification signal and said independent decodable code, and said dependent decodable code within one sync block.

According to another aspect of the present invention, there is provided an error correcting decoding method in a digital video reproducer or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code to which first and second inner parities are added to record it in sync-block unit, and said recorded data is reproduced in accordance with the inverse order of said recording step,

said error correcting decoding method comprising the steps of:

decoding said independent and dependent decodable codes by said first and second inner parities during normal reproduction; and

decoding only said independent decodable code by said first inner parity during variable tape-speed reproduction.

According to a further aspect of the present invention, there is provided an error correcting encoding apparatus in a digital video recorder or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code to record it in

sync-block unit by adding a block identification signal, and said recorded data is reproduced in accordance with the inverse order of said recording step,

said error correcting encoding apparatus comprising:

a demultiplexer for inputting said image data of block unit to which said block identification signal is added, and separating said image data into said block identification signal and said independent decodable code, and said dependent decodable code to thereby output them;

a first inner parity encoder for adding a first inner parity to said block identification signal and said independent decodable code from said demultiplexer;

a second inner parity encoder for adding a second inner parity to said dependent decodable code from said demultiplexer; and

a multiplexer for inputting said block identification signal and independent decodable code to which said first inner parity is added, and said dependent decodable code to which said second inner parity is added, and outputting the result of their combination.

According to another aspect of the present invention, there is provided an error correcting decoding apparatus in a digital video reproducer or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code, a block identification signal and independent decodable code, and dependent code are

recorded in sync-block unit by adding respective first and second inner parities, and said recorded data is reproduced in accordance with the inverse order of said recording step, said error correcting decoding apparatus comprising:

a demultiplexer for inputting said sync block, and separating said sync block into a first group consisting of said block identification signal, said independent decodable code and said first inner parity, and a second group consisting of said dependent decodable code and said second inner parity to thereby output them;

a first inner parity decoder for decoding said block identification signal and said independent decodable code by said first inner parity of said first group from said demultiplexer;

a second inner parity decoder for decoding said dependent decodable code by said second inner parity of said second group from said demultiplexer; and

a multiplexer for inputting said block identification signal and said independent decodable code from said first inner parity decoder, and said dependent decodable code from said second inner parity decoder, and outputting the result of their combination.

An error correcting decoding apparatus as above may further comprise:

a buffer for inputting said block identification signal and said independent decodable code from said first inner parity decoder; and

a selector for selectively outputting the outputs from said multiplexer and said buffer.

Said buffer may be a queue-type buffer.

The invention extends to a video recorder and/or reproducer arranged to operate in accordance with a method, or provided with an error correcting apparatus, according to any of the preceding aspects of the invention. Such a video recorder and/or reproducer is preferably a video tape recorder and/or reproducer.

In a digital VTR, embodiments of an error correcting method and apparatus according to the present invention may carry out recording by adding first and second parities to respective IDC having almost all image data needed and DDC having the remaining of the data in the individual unit block, thereby enhancing the maintainability of the data.

Further, by error-correcting only the IDC to be utilized during the variable tape-speed reproduction, embodiments of error correcting encoding and decoding apparatus according to the present invention may minimize the loss of effective data due to the mismatch of sync blocks which occurs due to the traversing of the heads on several tracks during variable tape-speed reproduction, and carry out error correction simply.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram showing a construction of a recording system in a digital VTR;

Figure 2 is a block diagram showing the detailed construction of one example of an error correction encoder according to the present invention;

Figure 3 shows the formation of data written in a first memory of Figure 2, and its read/write state;

Figure 4 shows the formation of data written in a second memory of Figure 2, and its read/write state;

Figures 5A and 5B show formations of an independent decodable code data and a dependent decodable code data, respectively, to which an inner parity is added by an inner parity encoder of Figure 2;

Figure 6 shows the formation of data written in a third memory of Figure 2, and its read/write state;

Figure 7 is a block diagram showing a construction of a reproducing system in a digital VTR; and

Figure 8 is a block diagram showing the detailed construction of an example of an error correction decoder according to the present invention.

In Figure 1, the data compression of a chroma signal (RGB signal, or luma signal and color difference signals) input to a recording system is carried out through an image compressor 10, an error correcting code is added in an

error correction encoder 12, and the color difference signals between tracks are alternated in a channel encoder 14, thereby recording the processed signal on a tape 16.

Figure 2 shows the construction of the example of an error correction encoder according to the present invention.

In Figure 2, reference numeral 20 designates a block ID generator for supplying a block identification (ID) signal for each unit block (sync block); 22 is a vector-to-alpha converter for converting the input data into involutions of an α value which is the root of a primitive polynomial expression of a Reed-Solomon (RS) code; 24 and 26 are a first memory and a first memory controller, respectively, which re-arrange and output the data for encoding an outer parity of the RS code having passed through vector-to-alpha converter 22; 28 is an outer parity encoder for adding an outer parity to the sync block in the column direction output from first memory 24; 30 and 32 are a second memory and a second memory controller which re-arrange the data for encoding an inner parity of the sync block having passed through outer parity encoder 28; 34 is a demultiplexer which separates a sync block from second memory 30 into a block ID signal, an IDC and a DDC; 36 and 38 are first and second inner parity encoders which add the respective inner parities to the block ID signal and IDC, and DDC; 40 is a multiplexer for combining the outputs from first and second inner parity encoders 36 and 38; 42 and 44 are a third memory and a third memory controller which re-arrange and output the sync block recorded on tape 16; and 46 is a sync generator which adds a sync code for each sync block.

The operation of the apparatus illustrated in Figure 2 will be described in detail.

The sync block output from image compressor 10 shown in Figure 1 is composed of the IDC and DDC. The IDC is data for variable tape-speed reproduction, which, e.g. includes a DC component and several low-frequency components in DCT, or is the result of a first vector quantization in a vector quantization method. The DDC is that portion other than the above-described portion. The input sync blocks are added by an ID signal which defines each sync block from block ID generator 20, and supplied to first memory 24 by being converted into involutions of α which is the root of a primitive polynomial expression of an RS code by vector-to-alpha converter 22.

Hereinbelow, the operation of the first memory will be described with reference to Figure 3.

As shown in Figure 3, the sync blocks input to first memory 24 are written in the X-direction, read out in bit units in the Y-direction, and then supplied to outer parity encoder 28, under the control of first memory controller 26.

The operations of outer parity encoder 28, second memory 30, and second memory controller 32 will be described with reference to Figure 4.

As illustrated in Figure 4, outer parity encoder 28 performs outer parity encoding with respect to an M-bit which has been read out under the control of first memory controller 26, and adds outer parity (OP) numbers, thereby

supplying the combined result to second memory 30. The data input to second memory 30 is written in the Y-direction under the control of second memory controller 32, read out in sync-block units in the X-direction, and separated into a "block ID signal and IDC" and a "DDC" by demultiplexer 34, thereby being supplied to first inner parity encoder 36 and second inner parity encoder 38.

The operations of inner parity encoders 36 and 38 will be described with reference to Figures 5A and 5B.

First inner parity encoder 36 performs inner parity encoding of "the block ID signal (A) and IDC data (B)" or "the outer parity with respect to the ID and IDC data", thereby adding first inner parity number IP1, as shown in Figure 5A. Second inner parity encoder 38 performs inner parity encoding of "the DDC data (C)" or "the outer parity with respect to the DDC data", thereby adding a second inner parity number IP2, as shown in Figure 5B. The outputs of the inner parity encoders are alternately selected by multiplexer 40, and supplied to third memory 42.

The operations of third memory 42 and third memory controller 44 will be described with reference to Figure 6.

The outputs from first and second inner parity encoders 36 and 38 are multiplexed by multiplexer 40, and supplied to third memory 42. Under the control of third memory controller 24, the data written in third memory 42 is read out in the X-direction in sync-block units as shown in Figure 7, and then supplied to sync generator 46. Sync generator 46 adds a sync code to each sync block, thereby supplying the result to channel encoder 14 of Figure 1.

Figure 7 illustrates the construction of a reproducing system in a digital VTR.

In Figure 7, the signal recorded on a tape 76 is channel-decoded via a channel decoder 74, and error compensation or correction is carried out by inner or outer parity via an error correction decoder 72. Then, the original signal (RGB, or luma signal and color difference signals) is demodulated by an image expander 70.

Figure 8 illustrates the example of a decoder for error-correcting codes according to the present invention.

In Figure 8, reference numeral 80 designates a sync signal detector; 82 and 84 are a fourth memory and a fourth memory controller, respectively, which re-arrange and output data to separate the sync block into a first group consisting of the block ID signal, IDC and the first inner parity, and a second group consisting of DDC and the second inner parity to which the inner parities are added; 86 is a demultiplexer which separates the data from fourth memory 82 into "the first group and the second group" or "the outer parity with respect to the ID and IDC data and the outer parity with respect to the DDC data"; 88 and 90 are inner parity decoders; 92 is a two-dimensional error flag memory; 94 is an address generator for generating a display address to two-dimensional flag memory 92 by the error signal from inner parity decoders 88 and 90; 96 is a multiplexer for selectively outputting the block ID signal, IDC and DDC data decoded with the inner parities; 98 and 100 are a fifth memory and a fifth memory controller, respectively, which combine the block ID signal, IDC and DDC data decoded by inner parities and re-arrange them to be output; 102 is an outer parity decoder; 104 is a switch

controlled to barricade the data transferring path by an error signal ERR1 from the first inner parity decoder 88; 106 is a buffer; 108 is a selector which selectively outputs the outputs from outer parity decoder 102 and buffer 106 in accordance with an externally supplied signal which indicates the variable tape-speed reproduction; and 110 is an alpha-to-vector converter for vector-converting the data which has been converted into the form of involutions of α.

In operation of the apparatus shown in Figure 8, sync signal detector 80 detects a sync code included in the input binary data column, and supplies it to fourth memory 82 by segmenting into sync-block units. As shown in Figure 6, fourth memory 82 is written by the input sync block-unit data under the control of fourth memory controller 84, reads out in the X-direction, and supplies the sync block-unit data to demultiplexer 86. Demultiplexer 86 alternately selects the first group and the second group among the input sync block-unit data, and supplies them to first inner parity decoder 88 and second inner parity decoder 90, respectively.

First and second inner parity decoders 88 and 90 carry out error correction to "the first group and the second group" or "the outer parity with respect to the ID and IDC data and the outer parity with respect to the DDC data", and according to their respective inner parities, supply them to multiplexer 96. Multiplexer 96 alternately selects the outputs from first and second inner parity decoders 88 and 90, and supplies them to fifth memory 98.

As shown in Figure 4, under the control of fifth memory controller 100, fifth memory 98 writes the "block ID signal and IDC and DDC" or "the

outer parity with respect to the ID and DDC and the outer parity with respect to the DDC" decoded by inner parities in multiplexer 96 in the X-direction, and reads out in sync-block units in the Y-direction, thereby supplying them to outer parity decoder 102.

When an error exceeds the limitation of error correction by inner parities, inner parity decoders 88 and 90 generate error signals ERR1 and ERR2 and supply them to two-dimensional error flag memory 92. Two-dimensional memory 92 writes the position of a sync block where an error occurs with reference to error signals ERR1 and ERR2 and an address ADDR in address generator 94. Outer parity decoder 102 carries out the error correction to the sync block where the uncorrectable inner parity error occurs, referring to two-dimensional error flag memory 92, and supplies them to a selector 108. The output of selector 108 is supplied to alpha-to-vector converter 110, and output by being converted into the original vector form from involutions of α which is the root of a primitive polynomial expression of an RS code.

On the other hand, in variable tape-speed reproduction, selector 108 is controlled to select buffer 106 by a variable tape-speed reproduction signal, thereby outputting only the "block ID signal and IDC" output from first inner parity decoder 88 via a path formed by switch 104, buffer 106, selector 108, and alpha-to-vector converter 110. Switch 104 is controlled to output toward buffer 106 only when the data supplied from first inner parity decoder 88 by error signal ERR1 has no defects. At this time, since the data from switch 104 is not the data which has successive block ID signals, a queue-type buffer is required. The error correcting path corresponding to the normal reproduction and the variable tape-speed reproduction operations is selected

by controlling selector 108 in accordance with a tape-speed control signal which indicates variable tape-speed reproduction.

It will be apparent that many modifications and variations could be effected easily by one skilled in the art without departing from the spirit or scope of the novel concepts of the present invention.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel

combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS:

1. An error correcting encoding method in a digital video recorder or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code to record it in sync-block unit, and said recorded data is reproduced in accordance with the inverse order of said recording step,

said error correcting encoding method comprising a step of adding respective first and second inner parities to a block identification signal and said independent decodable code, and said dependent decodable code within one sync block.

2. An error correcting decoding method in a digital video reproducer or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code to which first and second inner parities are added to record it in sync-block unit, and said recorded data is reproduced in accordance with the inverse order of said recording step,

said error correcting decoding method comprising the steps of:

decoding said independent and dependent decodable codes by said first and second inner parities during normal reproduction; and

decoding only said independent decodable code by said first inner parity during variable tape-speed reproduction.

3. An error correcting encoding apparatus in a digital video recorder or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code to record it in sync-block unit by adding a block identification signal, and said recorded data is reproduced in accordance with the inverse order of said recording step,

said error correcting encoding apparatus comprising:

a demultiplexer for inputting said image data of block unit to which said block identification signal is added, and separating said image data into said block identification signal and said independent decodable code, and said dependent decodable code to thereby output them;

a first inner parity encoder for adding a first inner parity to said block identification signal and said independent decodable code from said demultiplexer;

a second inner parity encoder for adding a second inner parity to said dependent decodable code from said demultiplexer; and

a multiplexer for inputting said block identification signal and independent decodable code to which said first inner parity is added, and said dependent decodable code to which said second inner parity is added, and outputting the result of their combination.

4. An error correcting decoding apparatus in a digital video reproducer or recorder/reproducer, wherein image data of one picture is partitioned into blocks and code-converted in block units, the result is separated into an independent decodable code and a dependent decodable code, a block identification signal and independent decodable code, and dependent code are recorded in sync-block unit by adding respective first and second inner parities, and said recorded data is reproduced in accordance with the inverse order of said recording step, said error correcting decoding apparatus comprising:

a demultiplexer for inputting said sync block, and separating said sync block into a first group consisting of said block identification signal, said independent decodable code and said first inner parity, and a second group consisting of said dependent decodable code and said second inner parity to thereby output them;

a first inner parity decoder for decoding said block identification signal and said independent decodable code by said first inner parity of said first group from said demultiplexer;

a second inner parity decoder for decoding said dependent decodable code by said second inner parity of said second group from said demultiplexer; and

a multiplexer for inputting said block identification signal and said independent decodable code from said first inner parity decoder, and said dependent decodable code from said second inner parity decoder, and outputting the result of their combination.

5. An error correcting decoding apparatus as claimed in claim 4, further comprising:

a buffer for inputting said block identification signal and said independent decodable code from said first inner parity decoder; and

a selector for selectively outputting the outputs from said multiplexer and said buffer.

6. An error correcting decoding apparatus as claimed in claim 5, wherein said buffer is a queue-type buffer.

7. An error correcting method in a digital video recorder and/or reproducer, the method being substantially as hereinbefore described with reference to the accompanying drawings.

8. An error correcting apparatus in a digital video recorder and/or reproducer, the apparatus being substantially as hereinbefore described with reference to Figure 2 and/or 8 of the accompanying drawings.

9. A video recorder and/or reproducer arranged to operate in accordance with a method, or provided with an error correcting apparatus, according to any of the preceding claims.

10. A video recorder and/or reproducer according to claim 9, being a video tape recorder and/or reproducer.

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Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition L) G5R (RB33,RHX); H4P (PEP); H4F (FDC,FBC,FRT,FRW)

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Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

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Documents considered relevant following a search in respect of claims ALL

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	0367264 A2 (SANYO) - see whole document	1

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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