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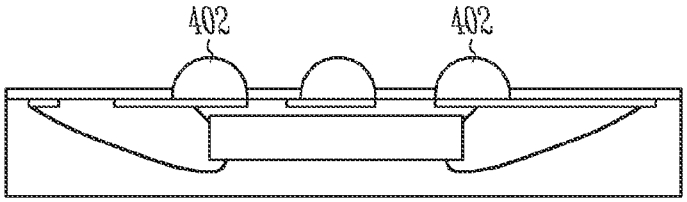

Fig. 4B

(57) Abstract: An integrated circuit assembly comprises an integrated circuit die, and a routable metal layer comprising metal traces linking a plurality of wire bond pads to a plurality of external connection pads such that the metal traces are routable under the die area. An electrically nonconductive adhesive layer couples the integrated circuit die to the routable metal layer, and a plurality of wire bonds link circuitry on the integrated circuit die to the wire bond pads in the routable metal layer. An overfill material encapsulates at least the integrated circuit die and the plurality of wire bonds, and a plurality of solder balls are formed on the plurality of external connection pads.

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WIRE-BONDED INTEGRATED CIRCUIT PACKAGE WITHOUT PACKAGE SUBSTRATE AND INCLUDING METAL TRACES LINKING TO EXTERNAL CONNECTION PADS ROUTED UNDER INTEGRATED CIRCUIT DIE

Claim of Priority

Benefit of priority is hereby claimed to U.S. Patent Application Serial Number 12/399,200, filed March 6, 2009, and entitled "Routable Array Metal Integrated Circuit Package", which is incorporated herein by reference its entirety.

Field of the Invention

The invention relates generally to integrated circuit packaging, and more specifically to a routable array metal integrated circuit package.

Background

Most electronic or computerized devices have electronic circuits that include one or more integrated circuits, often called "chips". These integrated circuits are usually relatively large or complex circuits such as computer processors, memory arrays, or other such devices. The actual circuits in the integrated circuit are typically formed using semiconductor devices formed on a substrate, such as doped silicon transistors, resistors, and capacitors formed on a silicon substrate.

The combination of a substrate and circuitry formed on the substrate is often referred to as a "die", and usually has circuitry that is so small that it is impossible to see the individual electronic components or circuit traces with the naked eye. Due to the small size of the circuit elements formed on the substrate, the die is also relatively fragile and can be easily damaged by scratching. Some circuits that operate at high power, such as high performance processors or controllers, also produce more heat than the integrated circuit die can dissipate, and so are not usable without some means of dissipating generated heat.

For these and other reasons, almost all integrated circuit dice are provided to the manufacturers of devices such as computers or cell phones in packages that are designed to protect the integrated circuit while making it easy to connect to other circuitry. Integrated circuit packages typically include pins, solder balls, or other electrical conductors that are coupled via small lead wires to various parts of

the die's electrical circuits, enabling easy and reliable electrical connection from the package's exterior to the die's circuitry. These packages provide a variety functions not related to electrical connection, including carrying heat away from the die to the exterior of the circuit package and perhaps to an external heat sink, and protecting the relatively fragile die from environmental factors such as abrasion, moisture, and shock.

But, packaging an integrated circuit die has several challenges itself. Although a typical integrated circuit die is too small to form connections to without specialized equipment, it is still desirable to keep the size of the packaged die small so that it can be easily integrated into compact or portable electronic devices. The cost of the package is a significant concern, as complex packages that provide good heat management, good protection of the die, and easy connectivity to external circuitry can be a significant part of the cost of a packaged integrated circuit.

It is therefore desired to package integrated circuit dice in a manner that addresses such commercial needs.

Summary

One example embodiment of the invention comprises an integrated circuit assembly including an integrated circuit die, and a routable metal layer comprising metal traces linking a plurality of wire bond pads to a plurality of external connection pads such that the metal traces are routable under the die area. An electrically nonconductive adhesive layer couples the integrated circuit die to the routable metal layer, and a plurality of wire bonds link circuitry on the integrated circuit die to the wire bond pads in the routable metal layer. An overfill material encapsulates the integrated circuit die, the plurality of wire bonds, and one side of the package's external connection pads. A plurality of solder balls are formed on the plurality of external connection pads.

Brief Description of the Figures

Figures 1a-1g show an example integrated circuit assembly fabricated using a sacrificial metal base substrate carrier, consistent with a prior art example.

Figure 2a shows a side view of an integrated circuit assembly having a

routable metal layer, consistent with some embodiments of the invention.

Figure 2b is a bottom view of the integrated circuit assembly having a routable metal layer of Figure 2a, consistent with an example embodiment of the invention.

Figures 3a-3f illustrate an example method of forming an integrated circuit assembly having a routable metal layer using a sacrificial base layer and localized solder stop, consistent with an example embodiment of the invention.

Figures 4a-4b illustrate an alternate method of forming an integrated circuit assembly having a routable metal layer using a sacrificial base layer using a full solder mask, consistent with an example embodiment of the invention.

Figure 5 is a top view of a series of integrated circuit assemblies formed on a sacrificial metal strip base layer, consistent with an example embodiment of the invention.

Detailed Description

In the following detailed description of example embodiments of the invention, reference is made to specific example embodiments of the invention by way of drawings and illustrations. These examples are described in sufficient detail to enable those skilled in the art to practice the invention, and serve to illustrate how the invention may be applied to various purposes or embodiments. Other embodiments of the invention exist and are within the scope of the invention, and logical, mechanical, electrical, and other changes may be made without departing from the subject or scope of the present invention.

Features or limitations of various embodiments of the invention described herein, however essential to the example embodiments in which they are incorporated, do not limit other embodiments of the invention or the invention as a whole, and any reference to the invention, its elements, operation, and application do not limit the invention as a whole but serve only to define these example embodiments. The following detailed description does not, therefore, limit the scope of the invention, which is defined only by the appended claims.

The invention disclosed herein comprises in one example embodiment an integrated circuit assembly comprising an integrated circuit die, and a routable metal layer comprising metal traces linking a plurality of wire bond pads to a

plurality of external connection pads such that the metal traces are routable under the die area. An electrically nonconductive adhesive layer couples the integrated circuit die to the routable metal layer, and a plurality of wire bonds link circuitry on the integrated circuit die to the wire bond pads in the routable metal layer. An overfill material encapsulates at least the integrated circuit die and the plurality of wire bonds, and one side of the package's external connection pads. In a further example, a plurality of solder balls are formed on the plurality of external connection pads.

Packaging for integrated circuits is typically designed to protect a relatively fragile integrated circuit die from its environment, to provide reliable electrical connection between the die and external circuitry, and in many cases to carry heat away from the die. Designing the packaging takes into consideration not only physical constraints such as these, but also the cost and complexity of the packaging process and the equipment required to package the dice.

One solution to packaging a die is illustrated in Figures 1a-1g, which show a sacrificial metal base strip packaging process. This example process starts by using a metal base strip onto which a package is formed, and from which the completed package is eventually separated.

In Figure 1a, a copper base strip 101 has a plating resist pattern applied to the surface of the copper base strip, as shown at 102. The bottom side of the copper base strip also has an unpatterned, solid layer of plating resist coating to prevent any plating metal deposition onto the bottom surface. The resist pattern on the top side allows a plating step shown in Figure 1b to deposit plating material in the patterned resist openings to form wire-bond metal pads 103 and die attach pad 104. In various embodiments, the plating material is one or more metal layers, such as gold, palladium, nickel, and copper. Palladium and gold work well for surfaces of metal layers to which wires will later be bonded, while metals such as nickel or copper are often used for the body of a plating step due to their high conductivity and relatively low cost. Gold is also resistant to oxidation, and so is often used for external plating of metal layers to prevent oxidation of the underlying solderable metal.

Once the metal plating process is completed, the resist material 102 applied in Figure 1a is removed in Figure 1c, leaving only the metal pads 103 and

104 formed in Figure 1b on the copper strip 101. Here, region 104 forms a base for attachment of the integrated circuit die, as shown in Figure 1d. The die 105 is attached to the metal plating region 104, such as by use of an epoxy or other adhesive.

The various circuits on the integrated circuit die are then connected to metal pads 103 formed during the plating process by using fine wire in what is known as a wirebond process. As shown in Figure 1e, the wires 106 connect various electrical contact points on the integrated circuit die to the metal pads 103, such that the metal pads 103 can be eventually coupled to electrical connections external to the completed package to couple the integrated circuit to external circuitry.

After the die is coupled via the wirebond wires to the metal pads formed in the plating process, the assembly is covered with an over-mold material as shown at 107 in Figure 1f to encapsulate and protect the die and the wiring and metal pads. This over-mold material is an electrically nonconductive material, such as epoxy or another suitable material.

The encapsulated assembly is then processed to remove the sacrificial metal base strip 101 from the assembly, resulting in the die assembly shown in Figure 1g. The copper base strip in this example is removed from the die assembly by a chemical etch that removes copper efficiently but does not attach to or react with the exposed metal used in the plated metal pads 103 and 104. The metal pads 103 and 104 in the assembly shown in Figure 1g can then be coupled to the next level board assembly using solder or conductive adhesive compound, or through other means. The metal pad 104 that supports the die is the same metal that is used to form the pads 103, but no metal pad formed in the plating process of Figure 1b is connected to any other metal pad. The bond wires shown at 106 of Figure 1e couple the die's circuits to the metal pads 103, enabling connection to external circuitry. Because the bond wires cannot cross one another without risking electrically coupling one wire to the other due to accidental contact, this packaging system does not provide the ability to cross or route wires to different pads.

One example embodiment of the invention addresses some problems with the assembly of Figure 1 by providing a sacrificial metal base strip packaging

process that includes a routable layer that is formed by pattern plating. This provides improved flexibility in routing circuit traces to facilitate external connections Figures 2a and 2b show a pattern-plated sacrificial metal strip die package including a Ball Grid Array (BGA) format, consistent with an example embodiment of the invention. Other package formats without solder balls are also commonly used. In Figure 2a, the die package is inverted from the example die package shown in Figure 1g, and includes a routable metal layer in place of the large pad 104 onto which the die is mounted in Figure 1.

Here, a routable metal layer of conductive traces 204 is formed on the sacrificial metal layer, including in the area in which the die is mounted. The traces are coupled to the die via wire bond connections to metal wirebond pads 203, which are coupled via the metal layer conductive traces 204 to package pads 201. Solder balls 202 are here formed on package pads 201 in openings in solder mask layer 206, for connection to external circuitry. To prevent the die, which is typically silicon material, from electrically shorting to the package pad metal 201 and metal traces 204, an electrically non-conductive die-attach adhesive material 205, such as epoxy compound, is used for die-attach. This provides a compact, efficient package, with enhanced flexibility in configuration due to the routable metal traces in the metal layer.

A bottom view of the example package of Figure 2a is shown in Figure 2b. Here, conductive traces 204 are shown to link various solder balls 202 to various metal wirebond pads 203, such that a wirebond connection from the die to the wirebond pad 203 is electrically coupled via conductive traces 204 to the solder balls 202. Some solder balls, such as power and ground connections, may be connected to multiple pads on the routable metal layer so that multiple power and ground connections can be made between the various circuits on the die and the external power source. An example is shown in Figure 2b at pads 207, which are coupled to one another and to a single solder ball via metal traces on the routable metal layer.

Figures 3a-3f illustrate a method of forming a die package having a routable metal layer using a sacrificial metal strip integrated circuit packaging process, consistent with an example embodiment of the invention. In Figure 3a, the sacrificial metal strip is a copper metal base 301, and a routable or patterned

metal circuit layer 302 is formed on the strip, such as by using a photo-definable plating resist material and photo-mask as described in greater detail with respect to the example of Figure 1. The metal layer here has one or more layers of metal in a metal-stack, where different types of metal may be used in different layers to provide different properties.

For example, the metal routable layer 302, which comprises wirebonding pad features 203, package pad features 201, and routing trace features 204 as illustrated in figures 2a and 2b, includes in one embodiment a wire-bondable metal on the top surface, such as palladium, silver, or gold. A diffusion barrier metal layer such as nickel is immediately below the wire-bondable metal layer, and a conductive metal such as copper is next. Below that a solder diffusion barrier metal such as nickel is formed, and the bottom layer is an oxidation prevention metal such as silver, gold, or palladium. In alternate embodiments, more layers, other layers, or only select layers from the above example are included in the routable metal layer 302.

The die is attached to the routable metal layer in Figure 3b via an electrically nonconductive epoxy layer 303, or via another nonconductive adhesive material. The die is therefore not directly electrically connected to any routable metal traces routed under the die, but is instead coupled to the routable metal layer via bond wires 304. The bond wires 304 are attached to various pads 305, which are coupled via the routable metal layer to external circuit connections.

The assembly is then encased as shown in Figure 3c with an overmold material 306, which protects the die and the bond wires from abrasion, moisture, and other environmental factors. The sacrificial metal strip copper base is then removed as shown in Figure 3d (shown upside-down), such as by chemical etching. This leaves the routable metal layer and the die-attach epoxy exposed from the overmold applied in Figure 3c. The sacrificial metal strip is in some examples a long or continuous metal strip that is cut into individual die packages near the end of the packaging process, such as by sawing the metal strip or the die package, as shown in Figure 5.

Solder balls are applied to the exposed solder ball regions 309 of the routable metal layer as shown in Figure 3d. In Figure 3e, solder stop 307 is applied at various points to constrain solder from flowing onto metal traces 204

during solder ball attachment to the pad areas as shown at 308 in Figure 3f.

Figures 4a and 4b present an alternate method of applying solder balls, using a full solder mask layer instead of solder stop as employed in Figures 3e and 3f. In Figure 4a, a permanent solder mask 401 is applied to the entire bottom side of the integrated circuit package except for the area over the package metal pads that will receive solder balls, as shown at 402 in Figure 4b. This solder mask layer can be of a photo-definable or non-photo-definable characteristic, in ink or dry-film form, and can be applied using screening or lamination process in various embodiments.

As previously discussed in the example presented in Figure 3, a series of integrated circuit assemblies can be formed on a long or continuous sacrificial metal strip base layer, such as is shown in Figure 5. The individual integrated circuit packages 501 are then separated from one another, such as by sawing, in the final stages of integrated circuit package production.

The routable metal layer integrated circuit assembly technology described herein therefore provides a variety of advantages over prior art integrated circuit mounting technologies such as the example illustrated in Figure 1, including providing the advantage of full layer routing capability. A typical BGA package uses an organic substrate for routing. Eliminating an organic substrate in the routable metal layer integrated circuit examples illustrated in Figures 2-4 makes these examples significantly less expensive than prior technologies, and substantially reduces the height of the finished integrated circuit assembly which allows for thinner devices such as cell phones, personal digital assistant devices, global positioning systems, and other portable or handheld electronic devices.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that achieve the same purpose, structure, or function may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the example embodiments of the invention described herein. It is intended that this invention be limited only by the claims, and the full scope of equivalents thereof.

Claims

1. An integrated circuit assembly, comprising:

an integrated circuit die;

a routable metal layer comprising metal traces linking a plurality of wire bond pads to a plurality of external connection pads such that the metal traces are routable under the die area;

an electrically nonconductive adhesive layer coupling the integrated circuit die to the routable metal layer; and

a plurality of wire bonds linking circuitry on the integrated circuit die to the wire bond pads in the routable metal layer.

2. The integrated circuit assembly of claim 1, further comprising a sacrificial metal strip upon which the routable metal layer is formed, such that the strip is removable from the rest of the integrated circuit assembly.

3. The integrated circuit assembly of claim 1, further comprising an overfill material encapsulating at least the integrated circuit die and the plurality of wire bonds.

4. The integrated circuit assembly of claim 3, wherein the overfill further fills at least some gaps between metal traces in the routable metal layer.

5. The integrated circuit assembly of claim 1, wherein a plurality of solder balls are formed on the plurality of external connection pads.

6. The integrated circuit assembly of claim 5, wherein at least one of solder stop or a solder mask are used to place the solder balls.

7. The integrated circuit assembly of claim 1, wherein the routable metal layer comprises a plurality of traces routed in the area in which the die is adhesively attached to the routable metal layer.

8. The integrated circuit assembly of claim 7, wherein the electrically nonconductive adhesive layer material fills gaps between two or more traces routed in the routable metal layer in the area in which the die is adhesively attached to the routable metal layer.

9. The integrated circuit assembly of claim 1, wherein the routable metal layer comprises one or more layers of metal comprising at least one of gold, silver, palladium, nickel, and copper.

10. A method of forming an integrated circuit assembly, comprising:

forming a routable metal layer on a sacrificial base layer;

attaching an integrated circuit die to the routable metal layer using an electrically nonconductive adhesive;

attaching wire bond wires coupling circuitry on the die to the routable metal layer;

encapsulating at least the die and the wire bond wires in an electrically nonconductive protective overfill material; and

removing the sacrificial base layer from the rest of the integrated circuit assembly.

11. The method of claim 10, wherein the sacrificial base layer comprises a metal layer that is chemically removed from the integrated circuit assembly.

12. The method of claim 10, further comprising filling at least some gaps between metal traces in the routable metal layer with the electrically nonconductive protective overfill material.

13. The method of claim 10, wherein the routable metal layer further comprises a plurality of external connection pads, the method further comprising forming a plurality of solder balls on the plurality of external connection pads.

14. The method of claim 13, further comprising applying at least one of solder stop or a solder mask near the external connection pads to constrain the location of

the formed solder balls.

15. The method of claim 13, further comprising mounting the integrated circuit assembly to a circuit board via the plurality of solder balls.

16. The method of claim 10, wherein the routable metal layer comprises a plurality of traces routed in the area in which the die is adhesively attached to the routable metal layer.

17. The method of claim 16, further comprising filling gaps between two or more traces routed in the routable metal layer in the area in which the die is adhesively attached to the routable metal layer with the electrically nonconductive adhesive used to attach the die to the routable metal layer.

18. An integrated circuit assembly, comprising:

an integrated circuit die;

a routable metal layer comprising metal traces linking a plurality of wire bond pads to a plurality of external connection pads such that the metal traces are routable under the die area;

an electrically nonconductive adhesive layer coupling the integrated circuit die to the routable metal layer;

a plurality of wire bonds linking circuitry on the integrated circuit die to the wire bond pads in the routable metal layer;

an overfill material encapsulating at least the integrated circuit die and the plurality of wire bonds; and

a plurality of solder balls formed on the plurality of external connection pads.

19. The integrated circuit assembly of claim 18, wherein the plurality of solder balls electrically couple the integrated circuit assembly to a printed circuit board.

20. The integrated circuit assembly of claim 19, wherein the integrated circuit assembly attached to the printed circuit board is encapsulated with an electrically

nonconductive overfill material.

21. The integrated circuit assembly of claim 18, wherein the integrated circuit assembly is further encased in at least one of a protective polymer, ceramic, or metal case.

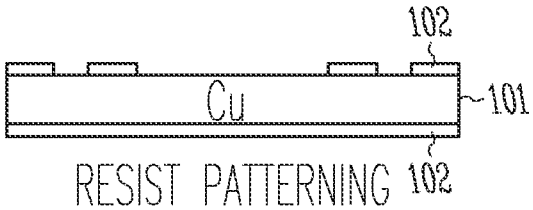


Fig. 1A

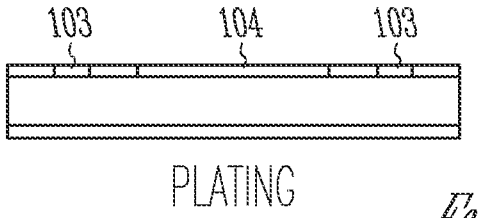


Fig. 1B

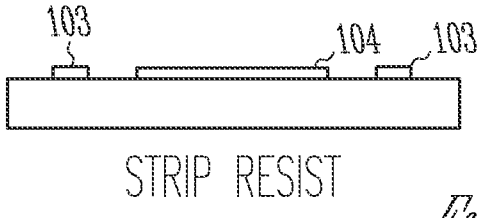


Fig. 1C

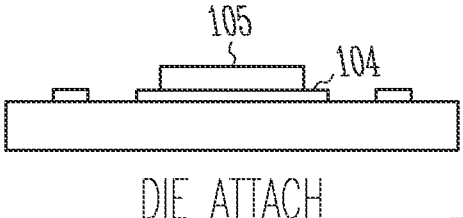
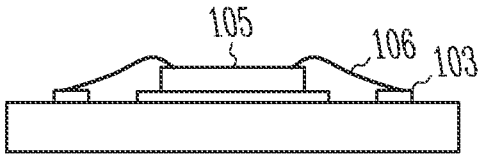
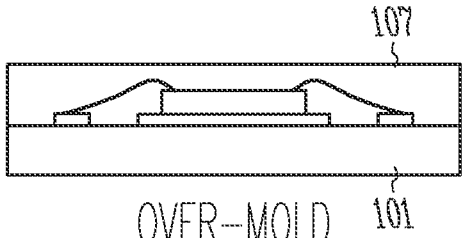


Fig. 1D



WIREBOND

Fig. 1E



OVER-MOLD

Fig. 1F

Cu ETCH

Fig. 1G

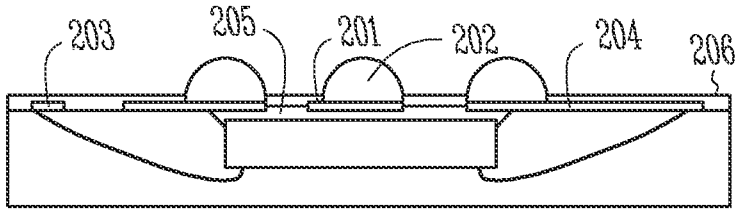


Fig. 2A

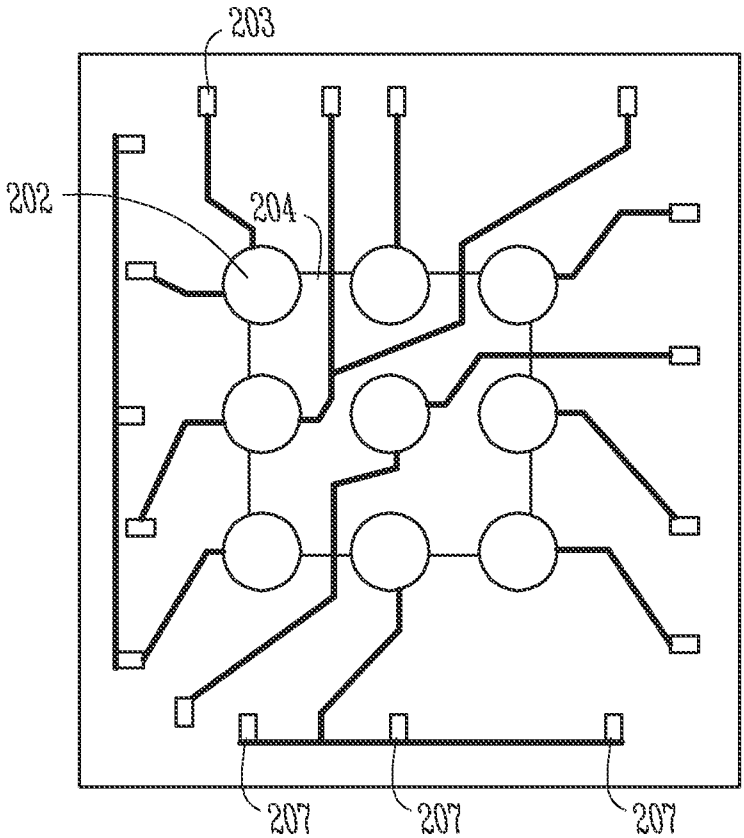


Fig. 2B

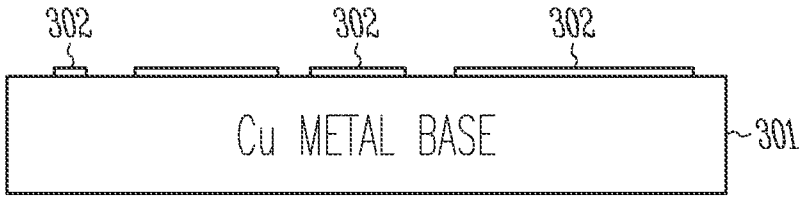


Fig. 3A

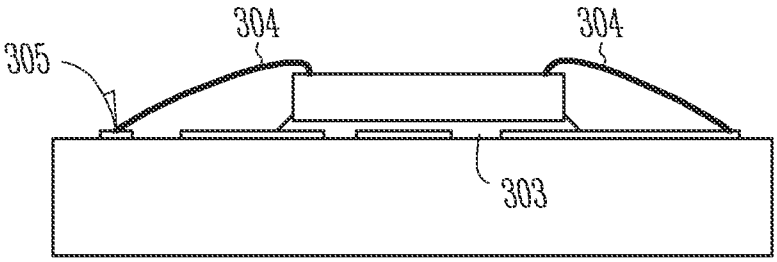


Fig. 3B

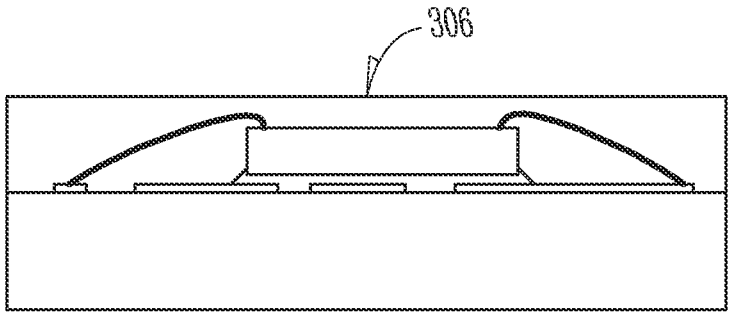


Fig. 3C

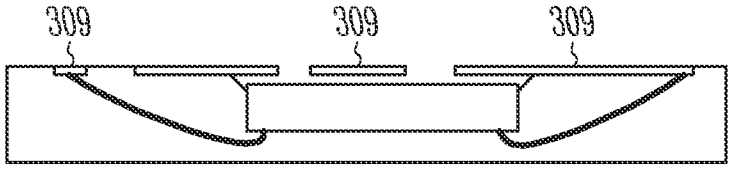


Fig. 3D

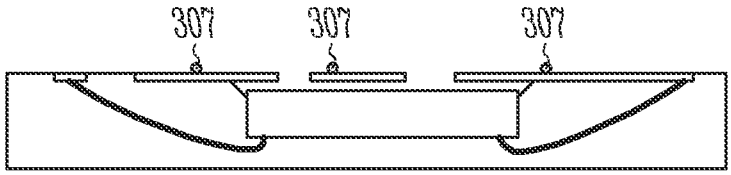


Fig. 3E

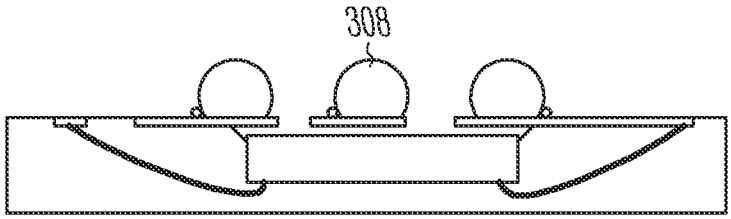


Fig. 3F

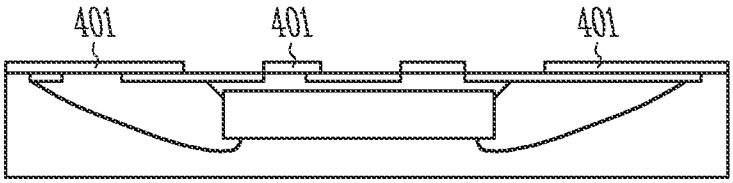


Fig. 4A

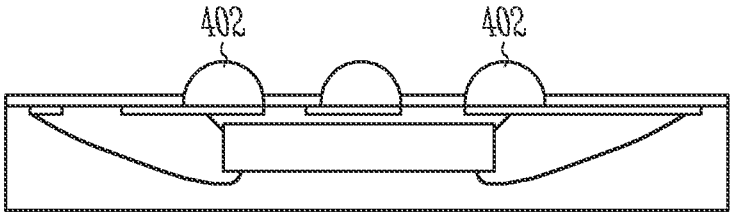


Fig. 4B

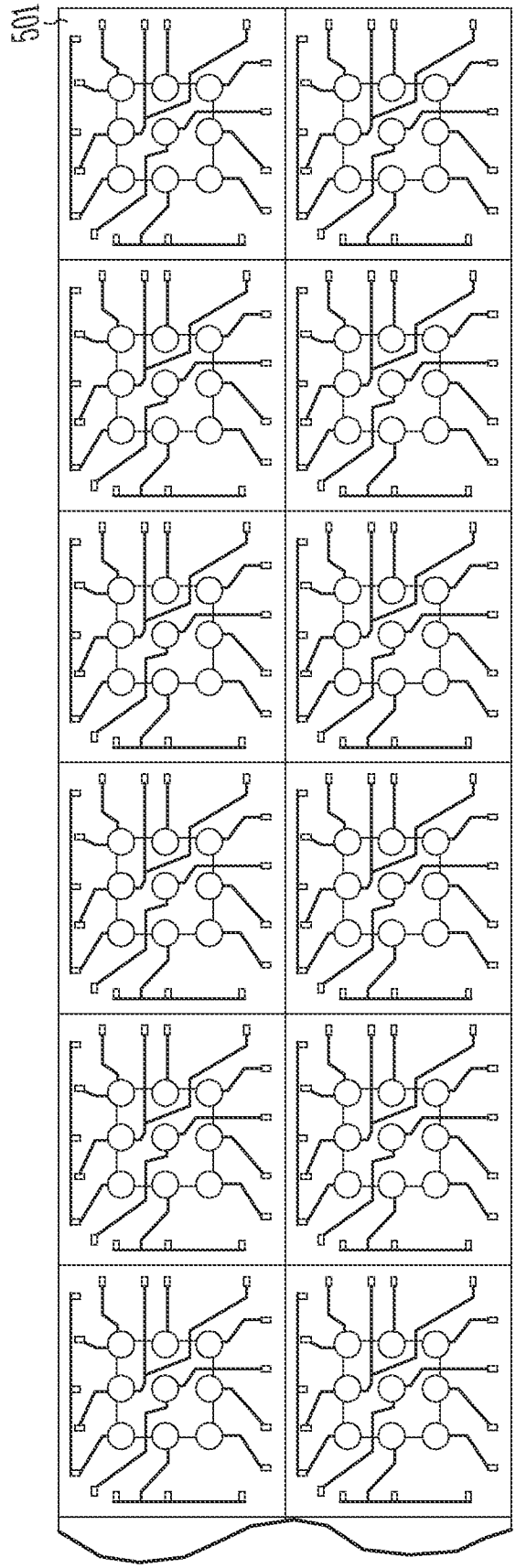


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/026394

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/68 H01L21/60 H01L21/48 H01L21/56 H01L23/31
H01L23/552 H01L23/08
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 830 800 A (LIN TING-HAO [TW]) 3 November 1998 (1998-11-03) figure 1 column 2, lines 3-47	1-21
X	US 7 245 023 B1 (LIN CHARLES W C [SG]) 17 July 2007 (2007-07-17) figure 17 column 15, lines 25-27 column 16, lines 17-21 column 20, line 43 - column 24, line 3 column 45, lines 35-37, 59-62	1,3,4, 7-9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 April 2010	07/05/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Crampin, Nicola

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/026394

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5830800 A	03-11-1998	NONE	
US 7245023 B1	17-07-2007	NONE	