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(71) Applicant: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: **HUI, Angela, T.**; 362 Pilgrim Loop, Fremont, CA 94539 (US). **LI, Wenmei**; 880 E. Fremont Avenue, #425, Sunnyvale, CA 94087 (US). **TU, Amy, C.**; 3761 Jasmine Circle, San Jose, CA 95135 (US).

(74) Agent: **COLLOPY, Daniel, R.**; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

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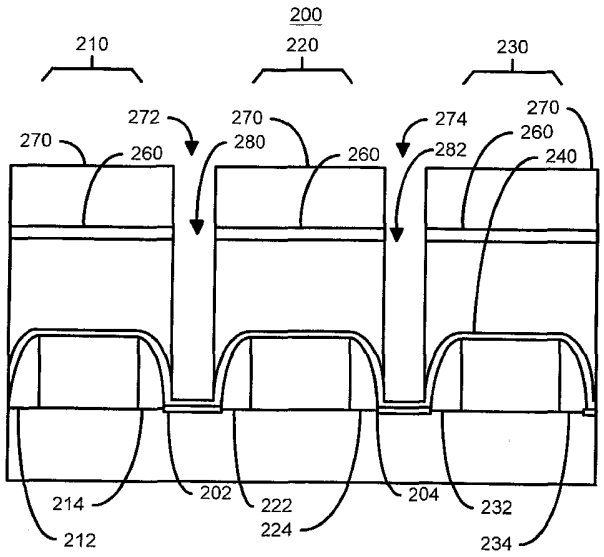
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR REDUCING CONTACT DEFECTS IN SEMICONDUCTOR CELLS



(57) Abstract: A method and system for providing at least One contact in a semiconductor device is described. The semiconductor device includes a substrate (201), an etch stop layer (240), an interlayer dielectric (250) on the etch stop layer (240), an anti-reflective coating (ARC) layer (260) on the interlayer dielectric (250), and at least one feature below the etch stop layer (240). A resist mask having an aperture and residing on the ARC layer (260) is provided. The aperture is above an exposed portion of the ARC layer (260). The method and system include etching the exposed ARC layer (260) and the underlying interlayer dielectric (250) without etching through the etch stop layer (240), thereby providing a portion of at least one contact hole. The method and system also include removing the resist mask in situ, removing a portion of the etch stop layer (240) exposed in the portion of the contact hole, and filling the contact hole with a conductive material.

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METHOD FOR REDUCING CONTACT DEFECTS IN SEMICONDUCTOR CELLS

TECHNICAL FIELD

The present invention relates to semiconductor devices, and more particularly to a method and system for providing contacts having connections for nonvolatile memory cells using polysilicon.

BACKGROUND ART

Conventional semiconductor devices, such as conventional nonvolatile memory devices, typically include gate stacks, sources and drains. Generally, a source is positioned at one edge of the gate stack, while the drain is at the opposing end of the gate stack. Field insulating regions generally run perpendicular to the gate stacks and are typically used to electrically isolate different devices. The field insulating regions are typically composed of oxide. The gate stacks, sources and drains are insulated using an interlayer dielectric that is typically composed of HDP, TEOS or BPTEOS. An etch stop layer, typically SiN or SiON, lies below the interlayer dielectric.

In order for the conventional semiconductor device to function, electrical contact is made to portions of the conventional semiconductor device, such as the drains and gate stack. In order to form the contacts, a CoSi layer is formed on the component, such as the drain, to reduce the electrical resistance to the contact. An antireflective coating ("ARC") layer is provided above the interlayer dielectric. The ARC layer is typically composed of SiN or SiON. A photoresist mask is provided above the ARC layer. The photoresist mask includes apertures above the regions of the interlayer dielectric which are to be etched to form contact holes. Typically, portions of the ARC layer, the interlayer dielectric and etch stop layer are removed in a single etch to form contact holes, exposing the underlying CoSi layer. The photoresist mask is then stripped. Typically, the photoresist mask is stripped using an ashing procedure. A wet cleaning is also typically performed to remove remnants of the etch of the interlayer dielectric, such as polymers within the contact hole. A conductive layer, such as a W plug, is deposited to fill the contact holes. The conductive layer can then be polished, typically using a chemical mechanical polish ("CMP") process. Thus a portion of the conductive layer outside of the contact holes is removed and a smooth surface provided.

One of ordinary skill in the art will readily recognize that the conventional method for forming contacts in a semiconductor device results in defects. For example, the etch of the ARC layer, interlayer dielectric and etch stop layer typically leaves a polymer residue within the contact hole. In order to remove this polymer, a wet clean is used to remove the polymers arising from the contact hole formation. Moreover, ashing is typically used to remove the resist. These multiple complicated ashing and wet cleaning processes typically result in defects, such as the presence of particles due to the additional handling of the semiconductor device. In addition, the layer W plug CMP process normally scratches the ARC layer on top of the dielectric material, thereby forming massive defects in the form of scratches. These scratches make it difficult to distinguish true particle defects from the scratches. Typically a long polishing step is necessary to remove the top ARC layer in order to preclude scratch formation.

Accordingly, what is needed is a system and method for providing a semiconductor device having

contacts with fewer defects. The present invention addresses such a need.

DISCLOSURE OF INVENTION

The present invention provides a method and system for providing at least one contact in a semiconductor device. The semiconductor device includes a substrate, an etch stop layer, an interlayer dielectric on the etch stop layer, an anti-reflective coating (ARC) layer on the interlayer dielectric, and at least one feature below the etch stop layer. A resist mask having at least one aperture and residing on the ARC layer is provided. The at least one aperture is above an exposed portion of the ARC layer. The method and system comprise etching the exposed portion of the ARC layer and the interlayer dielectric below the exposed portion of the ARC layer without etching through the etch stop layer to provide a portion of at least one contact hole. The method and system also comprise removing the resist mask in situ, removing a portion of the etch stop layer exposed in the portion of the at least one contact hole to provide the at least one contact hole in situ, and filling the at least one contact hole with a conductive material.

According to the system and method disclosed herein, the present invention performs a portion of the fabrication of the contact holes using an in-situ resist strip to provide a more effective post etch polymer removal, which simplifies the post contact cleaning cycle by eliminating additional ashing and wet cleaning processes and reduces the chance of introducing defect particles.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 is a high-level flow chart of one embodiment of a method in accordance with the present invention for providing contacts with reduced defects.

Figure 2 is a more detailed flow chart of one embodiment of a method in accordance with the present invention for providing contact with reduced defects.

Figures 3A-3E depict one embodiment of a semiconductor device in accordance with the present invention during fabrication.

MODE(S) FOR CARRYING OUT THE INVENTION

The present invention relates to an improvement in semiconductor devices. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments. Thus, the present invention is not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features described herein.

The present invention provides a method and system for providing at least one contact in a semiconductor device. The semiconductor device includes a substrate, an etch stop layer, an interlayer dielectric on the etch stop layer, an anti-reflective coating (ARC) layer on the interlayer dielectric, and at least one feature below the etch stop layer. A resist mask having at least one aperture and residing on the ARC layer is provided. The at least one aperture is above an exposed portion of the ARC layer. The method and system comprise etching the exposed portion of the ARC layer and the interlayer dielectric below the exposed portion of the ARC layer without etching through the etch stop layer to provide a portion of at least one contact hole. The method and system also comprise removing the resist mask in situ, removing a portion of the etch stop layer exposed in the portion of the at least one contact hole to provide the at least one contact hole in situ, and filling the at least

one contact hole with a conductive material.

The present invention will be described in terms of methods including particular steps. Furthermore, for clarity, some steps are omitted. One of ordinary skill in the art will, therefore, readily recognize that this method and system will operate effectively for other methods having different and/or additional steps. The present invention is also described in conjunction with a particular semiconductor device having certain components. However, one of ordinary skill in the art will readily recognize that the present invention is consistent with a semiconductor device having other and/or different components.

To more particularly illustrate the method and system in accordance with the present invention, refer now to Figure 1, depicting one embodiment of a method 100 in accordance with the present invention for providing contacts with reduced defects. The method 100 preferably commences after a mask has been provided on the semiconductor device. The semiconductor device includes an etch stop layer, an interlayer dielectric layer on the etch stop layer and an antireflective coating (ARC) layer on the interlayer dielectric. The ARC layer and etch stop layer may include SiN and/or SiON. The interlayer dielectric is preferably HDP, TEOS or BPTEOS. The semiconductor device also has feature(s) under the etch stop layer. For example, the semiconductor might have gate stacks and junctions such as source and drain junctions beneath the etch stop layer. Moreover, features such as the source and/or drain junctions may have a salicide layer, such as CoSi, in order to reduce their contact resistance. The resist mask preferably lies on top of the ARC layer. The resist mask is patterned with apertures that lie above the regions of the semiconductor device where the contacts are to be located.

The ARC layer and interlayer dielectric exposed by the apertures in the resist mask are removed in an etch step, via step 102. The etching performed in step 102 does not etch through the etch stop layer under the interlayer dielectric. In a preferred embodiment, the chemistry used for the etch in step 102 includes C_4F_8, C_4F_6, C_5F_8, C_2F_6 which etch the dielectric material and have a high selectivity to stop on the underlying nitride film (etch-stop layer).

The resist mask is removed in situ, via step 104. Because the resist mask is removed in situ, the resist mask is removed in a controlled environment, preferably in a vacuum chamber under low pressure and controlled gases introduced into the chamber. Thus, the resist mask is removed in the same chamber as the etch is performed without opening the chamber. Instead, the etch chemistry is simply changed to an O_2 based process. Thus, one chamber is used for multiple etch processes by changing the chemistry to allow various films to be etched. The etch chemistry used in step 104 is preferably O_2 based. In some embodiments, a small amount of forming gas such as N_2/H_2, or H_2, N_2 may be added. The range of pressures used generally varies depending upon the equipment used. For example, the pressure could vary from 30 mT to a range between 1-10 T.

The ARC layer and the portion of the etch stop layer at the base of the contact holes are removed in situ, via step 106. Thus, the contact holes are formed, and the feature(s) to which contact is to be made are exposed. In one embodiment, a CoSi layer on a source and/or drain junction is exposed in step 106. Because the ARC layer and etch stop layer are removed in situ, the ARC layer and etch stop layer are removed in a controlled environment, preferably in a vacuum chamber under low pressure and controlled gases introduced into the chamber. Also in a preferred embodiment, the ARC and etch stop layer are removed in the same chamber as the resist is removed in step 104. Thus, the same chamber is used without removing the semiconductor devices from the chamber. Instead, the etch chemistry is changed. Both the ARC and etch stop layers are preferably a nitride

type of material. For example, the ARC and etch stop layer might be either Si_3N_4, SiON or the combination. The ARC layer might also be SiRN (Si rich nitride). Thus, the etch chemistry preferably includes CHF_3, CF_4, CH_2F_2, or CH_3F. The pressure ranges vary, for example from from 20 mT to 500 mT, depending on the equipment used.

The contact holes are filled with a conductive material, such as W, via step 108. As a result, electrical contact can be made to the features of the semiconductor device. In addition, a CMP step may be performed to polish the W plug, via step 110. The CMP process should be controlled to avoid and/or reduce the introduction of scratches into the interlay dielectric.

Because the removal of the resist mask and etching of the ARC and etch stop layers are carried out in situ, fabrication of the contacts is simplified. A conventional resist ashing typically used to remove the resist mask can be avoided. In addition, the process of removing the resist mask in situ is cleaner and may obviate the need to perform a wet cleaning. Thus, defects introduced in formation of the contact hole can be reduced or avoided. In addition, because the ARC layer is removed in situ, the CMP used to planarize the material filling the contact holes is simplified. Because the ARC layer is removed, scratching of the ARC layer during the CMP is not an issue.

Figure 2 is a more detailed flow chart of one embodiment of a method 150 in accordance with the present invention for providing contact with reduced defects. Figures 3A-3D depict one embodiment of a semiconductor device 200 in accordance with the present invention during fabrication using the method 150. The method 150 preferably commences after an etch stop layer, an interlayer dielectric layer on the etch stop layer and an antireflective coating (ARC) layer on the interlayer dielectric have been provided. The ARC layer and etch stop layer may include SiN and/or SiON. The interlayer dielectric is preferably HDP, TEOS or BPTEOS. The semiconductor device also has feature(s) under the etch stop layer. For example, the semiconductor might have gate stacks and junctions such as source and drain junctions beneath the etch stop layer. Moreover, features such as the source and/or drain junctions may have a salicide layer, such as CoSi, in order to reduce their contact resistance.

A resist mask having apertures over the regions in which the contact holes are to be formed is provided, via step 152. The resist mask preferably lies on top of the ARC layer. Figure 3A depicts the semiconductor device 200 including gate stacks 210, 220 and 230 formed on a substrate 201. Spacers 212 and 214, 222 and 224, and 232 and 234 are at the edges of the gate stacks 210, 220 and 230, respectively. CoSi layers 204 and 206 have been formed between the gate stacks 210 and 220 and gate stacks 220 and 230 on junctions (not explicitly shown). An etch stop layer 240 is formed on the gate stacks 210, 220 and 230 and on the CoSi layers 202 and 204. The semiconductor device 200 also includes an interlayer dielectric 250 and an ARC layer 260. A resist mask 270 having apertures 272 and 274 is also shown. The apertures 272 and 274 are above the CoSi layers 202 and 204. Thus, in the semiconductor device 200, contact is to be made to the features below the CoSi layers 202 and 204.

The ARC layer 260 and interlayer dielectric 250 exposed by the apertures 272 and 274 in the resist mask 270 are removed in an etch step, via step 154. The etching performed in step 154 does not etch through the etch stop layer 240 under the interlayer dielectric 250. Figure 3B depicts the semiconductor device 200 after step 154 is performed. A portion of contact holes 280 and 282 has been formed beneath the apertures 272 and 274. However, at least a portion of the etch stop layer 240 remains at the base of the contact holes 280 and 282.

The resist mask 270 is removed and the contact holes 280 and 282 cleaned in situ, via step 156. Because the resist mask 270 is removed in situ, the resist mask 270 is removed in a controlled environment, preferably in a vacuum chamber under low pressure and controlled gases introduced into the chamber. Figure 3C depicts the semiconductor device 200 after removal of the resist mask 270. Because the resist mask 270 is removed and the contact holes 280 and 282 are cleaned in situ, any polymers in the contact holes 280' and 282' have been substantially eliminated. Thus, the surfaces of the contact holes 280' and 282' are substantially clean.

The ARC layer 260 and the portion of the etch stop layer 240 at the base of the contact holes 280 and 282 are removed in situ, via step 158. Figure 3D depicts the semiconductor device 200 after removal of the etch stop layer 240 at the base of the contact holes 280'' and 282''. Thus, the contact holes 280'' and 282'' have been formed, and the CoSi layers 202 and 204 to which contact is to be made are exposed. Because the ARC layer 260 and the portion of the etch stop layer 240 are removed in situ, the ARC layer 260 and the portion of the etch stop layer 240 are removed in a controlled environment, preferably in a vacuum chamber under low pressure and controlled gases introduced into the chamber. The contact holes 280'' and 282'' are filled with a conductive material and the contact material planarized, via step 160. As a result, electrical contact can be made to the features of the semiconductor device 200. Figure 3E depicts the semiconductor device 200 after formation of the contacts 290 and 292 are completed by filling the contact holes 280'' and 282'' and removing the excess conductive material, for example in a CMP step.

Because the removal of the resist mask 270 and etching of the ARC and etch stop layers 260 and 240 are carried out in situ, fabrication of the contacts is simplified. A conventional resist ashing typically used to remove the resist mask 270 can be avoided. In addition, the process of removing the resist mask 270 in situ is cleaner and may obviate the need to perform a wet cleaning. Thus, defects introduced in formation of the contact holes 280'' and 282'' can be reduced or avoided. In addition, because the ARC layer 260 is removed in situ, the CMP used to planarize the material filling the contact holes 280'' and 282'' is simplified. Because the ARC layer 260 is removed, scratching of the ARC layer 260 during the CMP is prevented.

A method and system has been disclosed for providing contacts in a semiconductor device. Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

INDUSTRIAL APPLICABILITY

One of ordinary skill in the art will readily recognize that the conventional method for forming contacts in a semiconductor device results in defects. For example, the etch of the ARC layer, interlayer dielectric and etch stop layer typically leaves a polymer residue within the contact hole. In order to remove this polymer, a wet clean is used to remove the polymers arising from the contact hole formation. Moreover, ashing is typically used to remove the resist. These multiple complicated ashing and wet cleaning processes typically result in defects, such as the presence of particles due to the additional handling of the semiconductor device. In addition, the layer W plug CMP process normally scratches the ARC layer on top of dielectric material, thereby forming massive defects in the form of scratches. These scratches make it difficult to distinguish true particle defects from the scratches. Typically a long polishing step is necessary to remove the top ARC layer in order to preclude

scratch formation.

Accordingly, what is needed is a system and method for providing a semiconductor device having contacts with fewer defects. The present invention addresses such a need.

CLAIMS

1. A method for providing at least one contact in a semiconductor including a substrate (201), an etch stop layer (240), an interlayer dielectric (250) on the etch stop layer (240), an anti-reflective coating (ARC) layer (260) on the interlayer dielectric (250), and at least one feature below the etch stop layer (240), a resist mask having at least one aperture therein residing on the ARC layer (260), the least one aperture being above an exposed portion of the ARC layer (260), the method comprising the steps of:

(a) etching (102) the exposed portion of the ARC layer (260) and the interlayer dielectric (250) below the exposed portion of the ARC layer (260) without etching through the etch stop layer (240) to provide a portion of at least one contact hole;

(b) removing the resist mask in situ (104);

(c) removing a portion of the etch stop layer (240) exposed in the portion of the at least one contact hole to provide the at least one contact hole in situ; and

(d) filling the at least one contact hole with a conductive material (108).

2. The method of claim 1 wherein the resist mask removing step (b) (104) further includes the step of:

(b1) cleaning the portion of the contact hole in situ.

3. The method of claim 1 wherein the etch stop layer (240) includes SiN and/or SiON.

4. The method of claim 1 wherein the ARC layer (260) includes SiN and/or SiON or SiRN (Si rich nitride).

5. The method of claim 1 further comprising the step of:

(e) planarizng the conductive material without scratching a surface of the interlayer dielectric (250).

6. The method of claim 1 further comprising the step of:

(e) removing a portion of the ARC layer (260) in situ before the at least one contact hole is filled.

7. A semiconductor device including a substrate (201), an etch stop layer (240), an interlayer dielectric (250) on the etch stop layer (240), an anti-reflective coating (ARC) layer (260) on the interlayer dielectric (250), and at least one feature below the etch stop layer (240), the method comprising the steps of:

a plurality of contacts, the plurality of contacts being provided by providing a resist mask having at least one aperture therein, the least one aperture being above an exposed portion of the ARC layer (260), etching the exposed portion of the ARC layer (260) and the interlayer dielectric (250) below the exposed portion of the ARC layer (260) without etching through the etch stop layer (240) to provide a portion of at least one contact hole, removing the resist mask in situ, removing a portion of the etch stop layer (240) exposed in the portion of the at least one contact hole to provide the at least one contact hole in situ, and filling the at least one contact hole with a conductive material.

8. The semiconductor device of claim 7 wherein the etch stop layer (240) includes SiN and/or SiON or SiRN (Si rich nitride).

9. The semiconductor device of claim 7 wherein the ARC layer (260) includes SiN and/or SiON.

10. The semiconductor device of claim 7 wherein the conductive layer is planarized without scratching a remaining portion of the ARC layer (260).

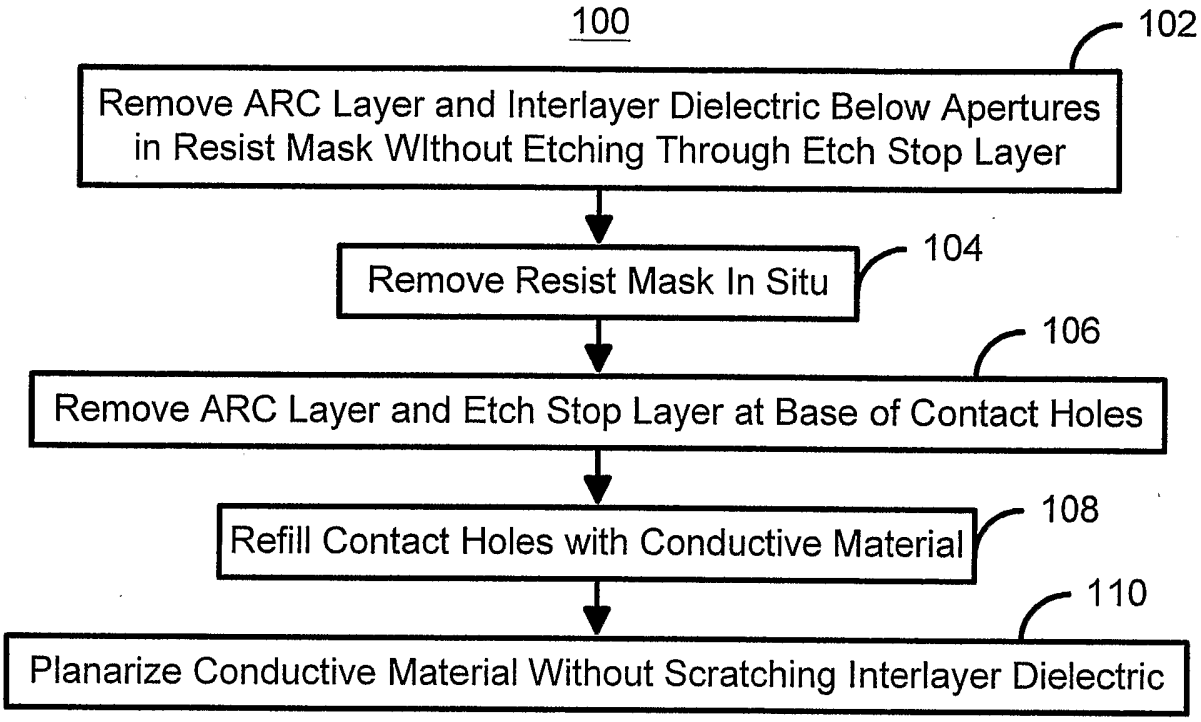

Figure 1

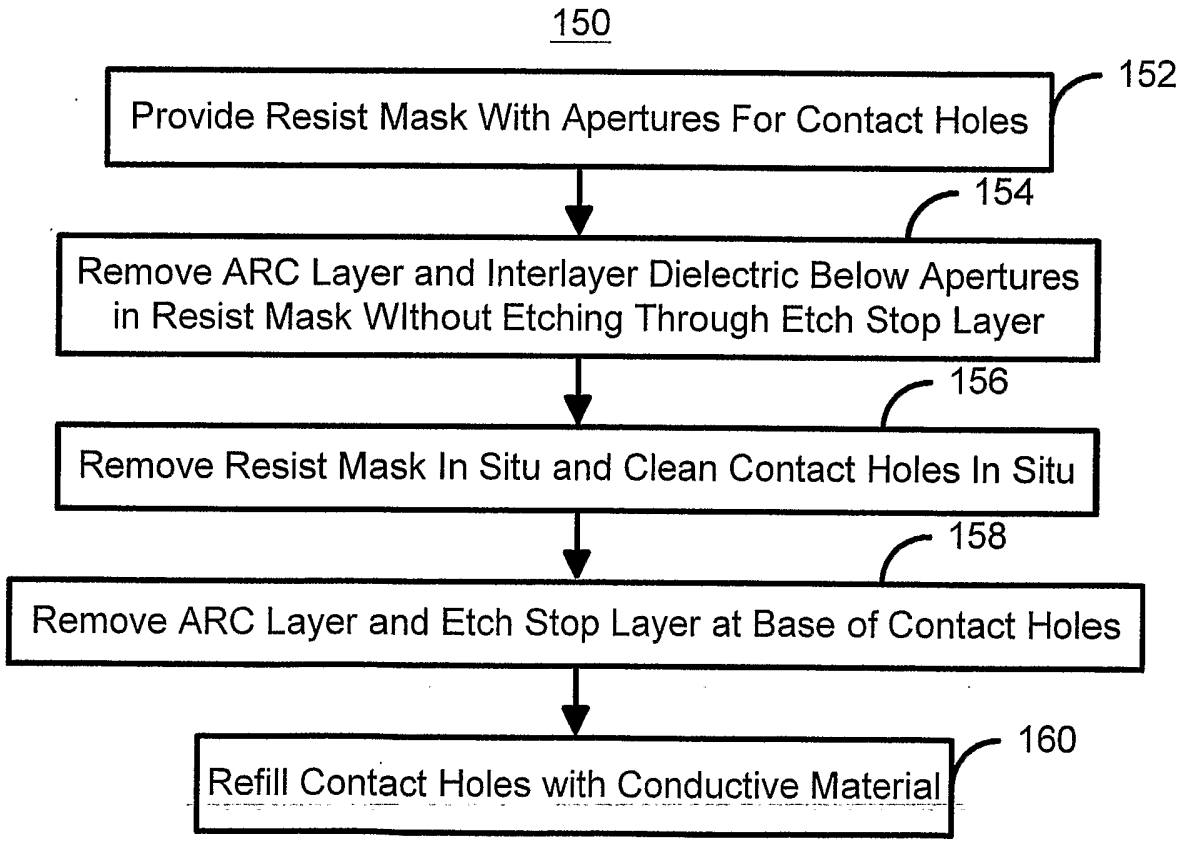

Figure 2

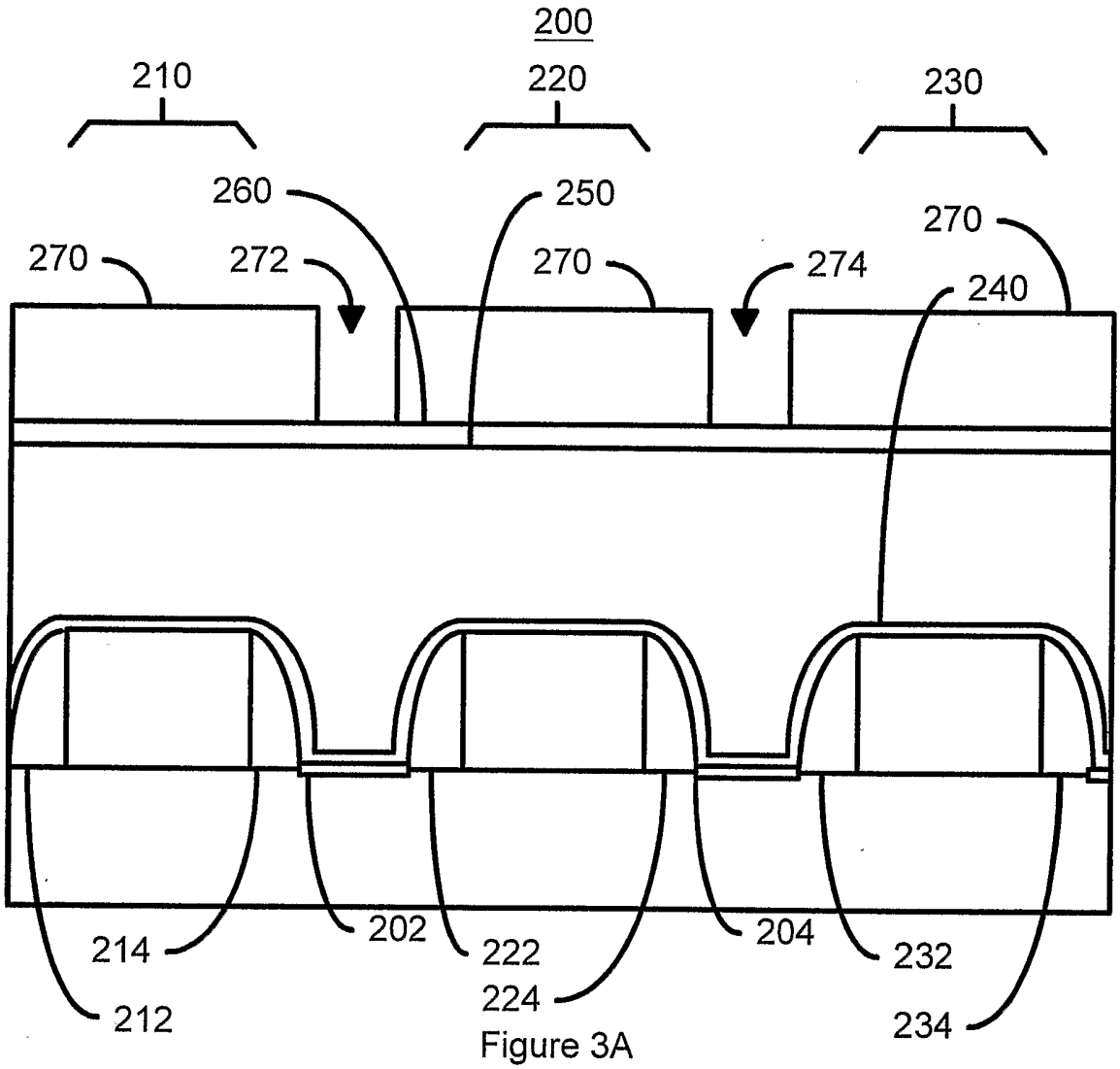
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Figure 3A

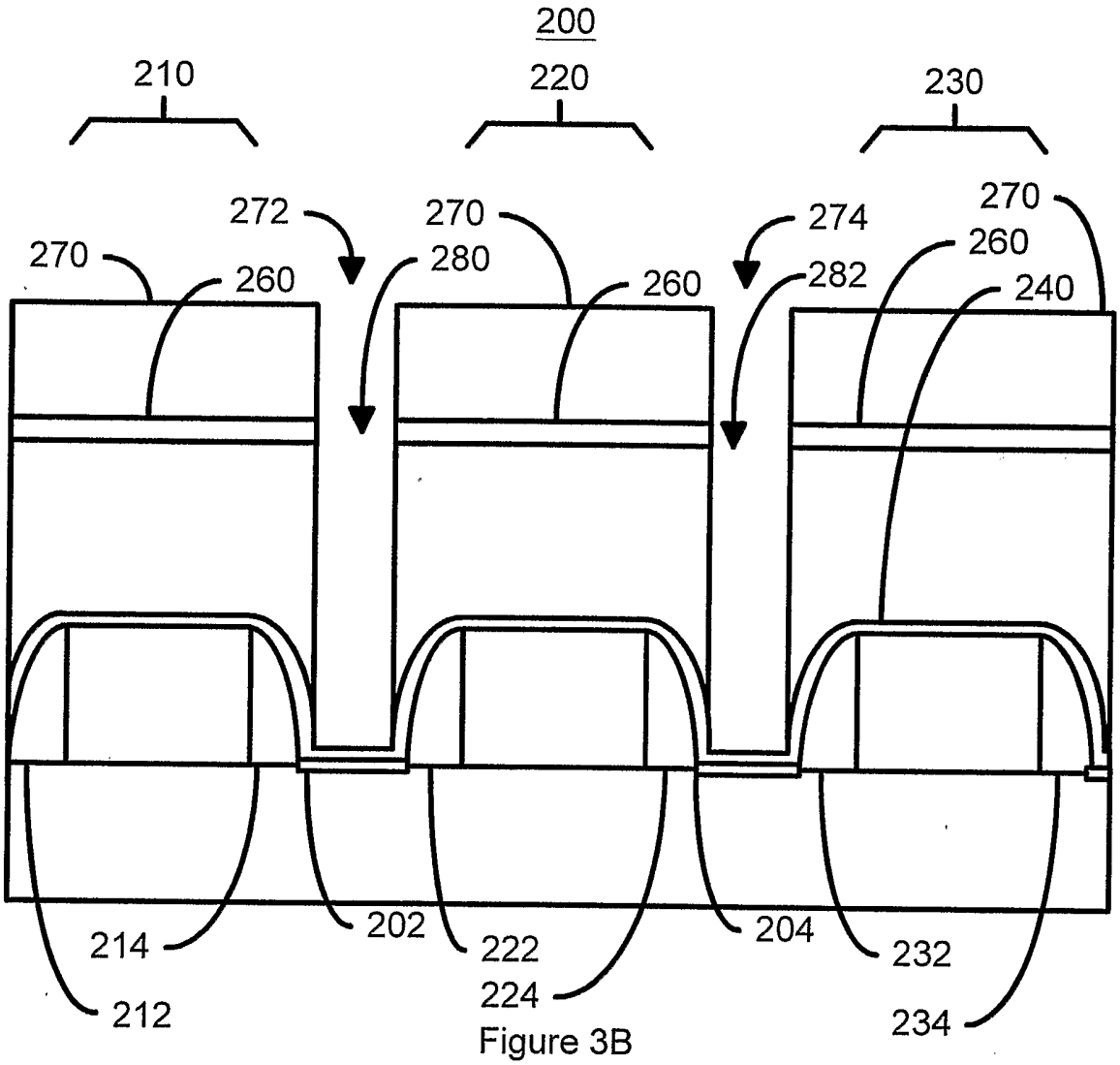
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Figure 3B

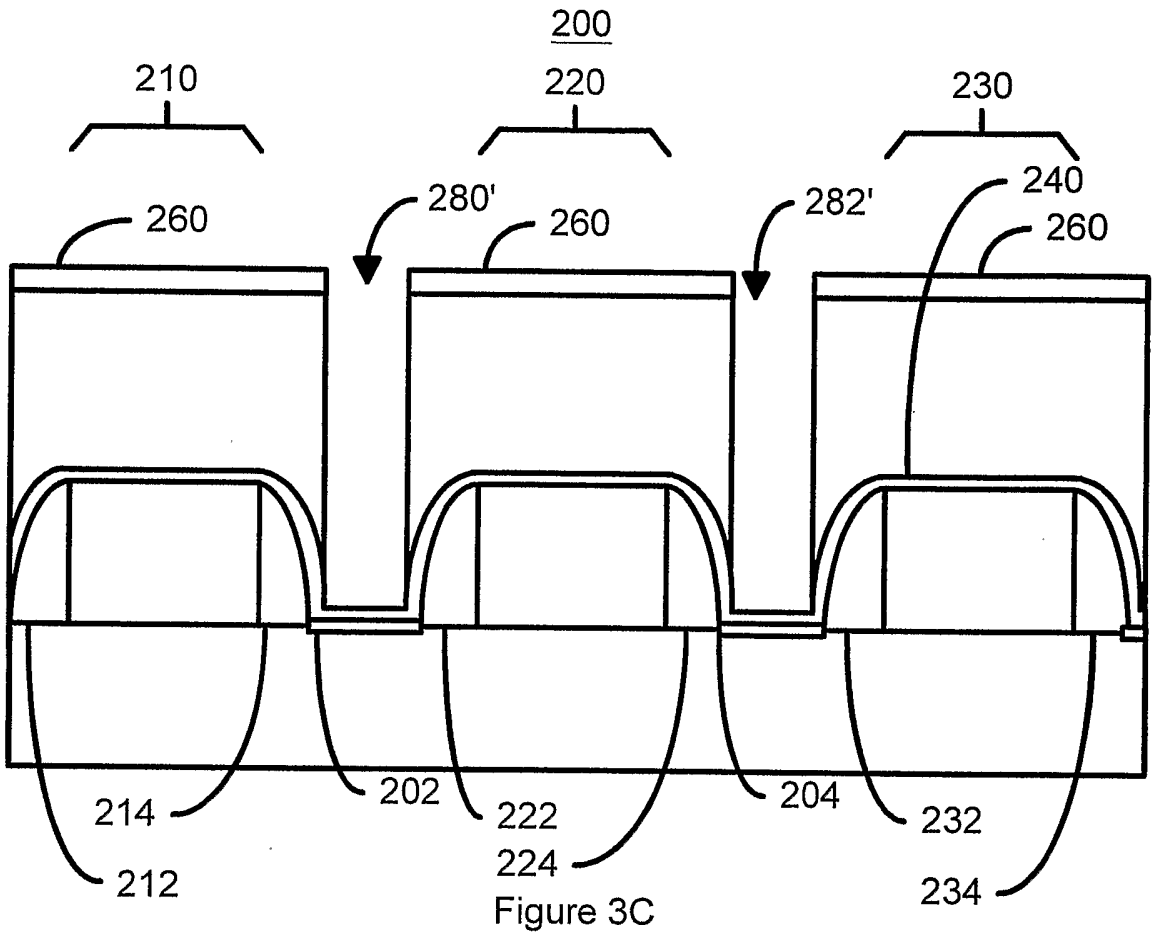
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Figure 3C

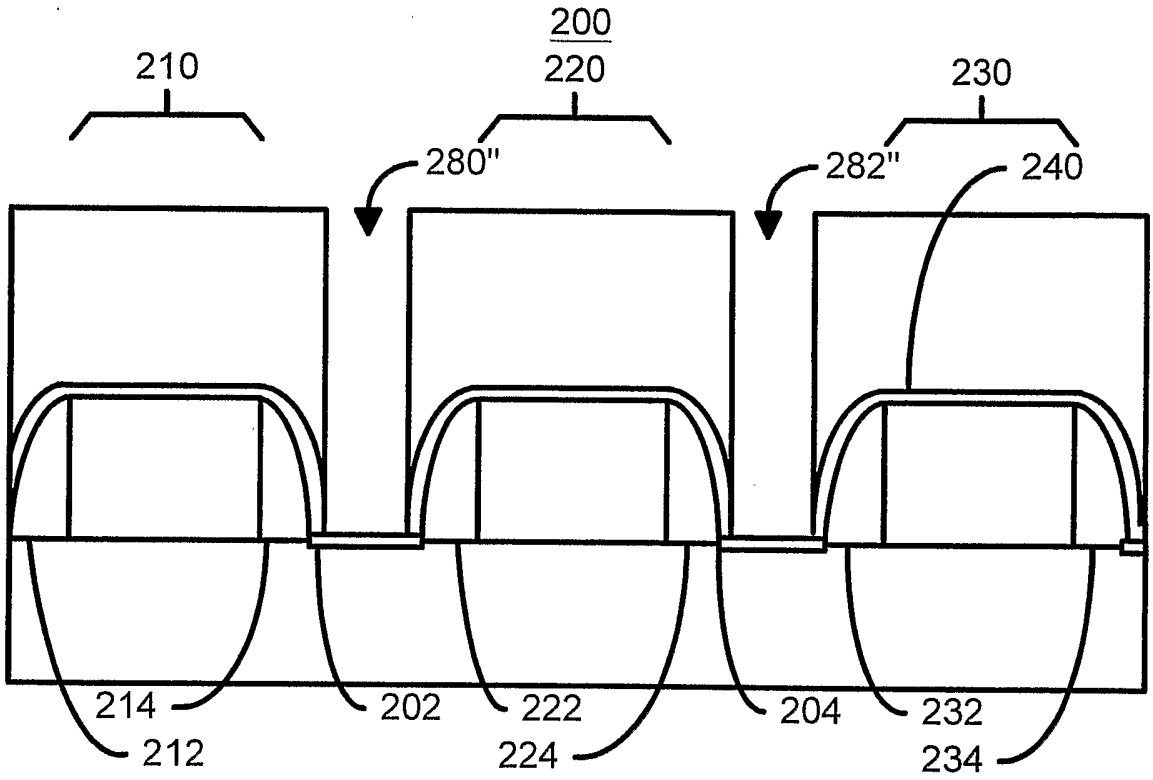

Figure 3D

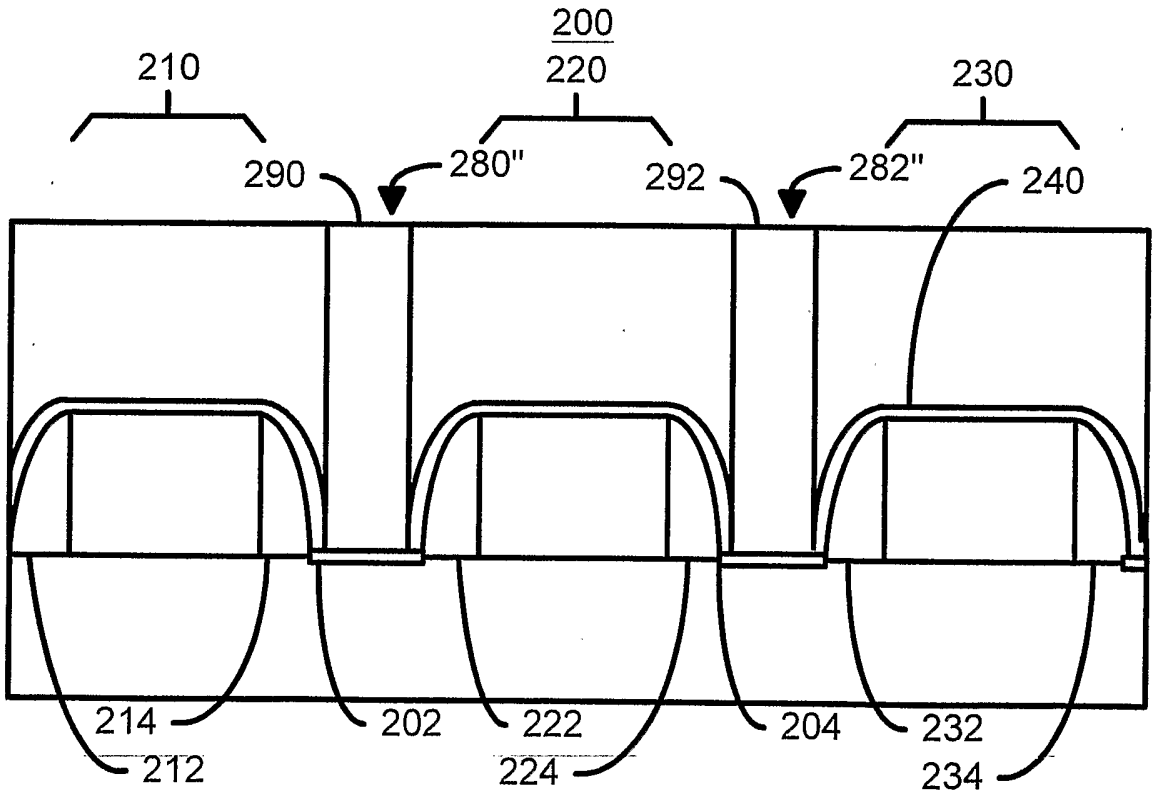

Figure 3E

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/29985

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/008226 A1 (DING JIAN ET AL) 19 July 2001 (2001-07-19) paragraphs '0007!,'0044!,'0053!,'0066!	1-10
X	US 6 358 842 B1 (CHOOI SIMON ET AL) 19 March 2002 (2002-03-19) the whole document	1-10
A	US 6 372 638 B1 (RODRIGUEZ ROBERT ARTHUR ET AL) 16 April 2002 (2002-04-16) column 4, line 1-5	1-10
A	US 6 235 640 B1 (FECHER MATHIAS ET AL) 22 May 2001 (2001-05-22) column 5, line 20-26	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
10 February 2004	18/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Ploner, G

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

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