

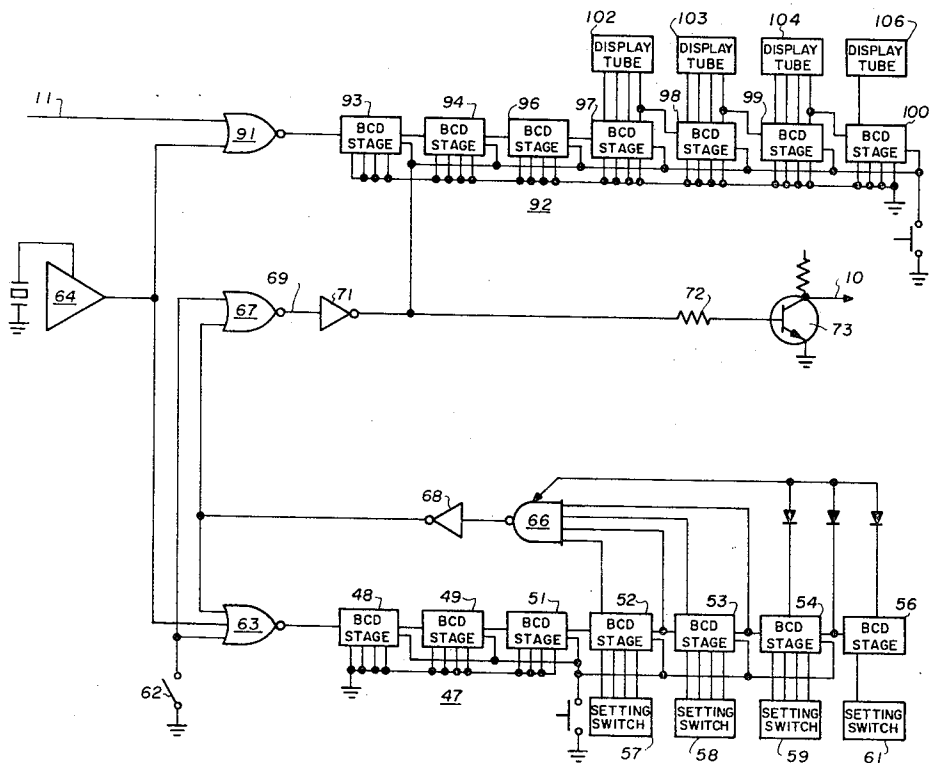
[54] **PULSE RESPONSIVE COUNTING CIRCUITS**
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[51] Int. Cl. H04q 1/32
[58] Field of Search 340/168, 309.4

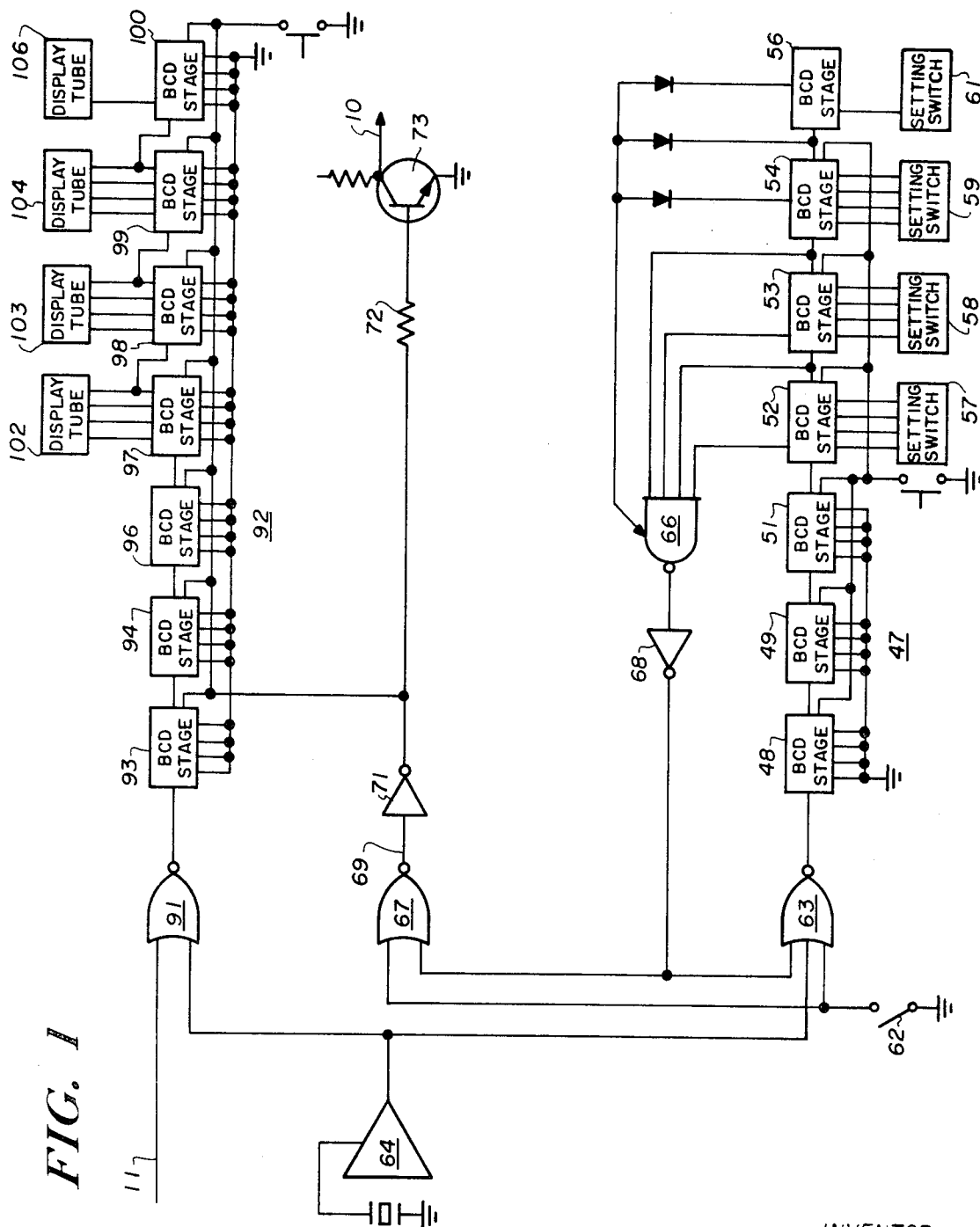
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[57] **ABSTRACT**
A system in which timing information is remotely set into a projectile to be fired. The system is configured to connect a time setting device, which contains (1) a plurality of setting switches, and (2) a plurality of read-out devices to an integrated circuit in the projectile by a minimum number of wires. The system functions to allow (1) hand setting of the timing information and (2) an error check, both at a remote location. The error check is provided as a visual read-out of data sent back from the integrated circuit after the timing information has been set.

9 Claims, 3 Drawing Figures





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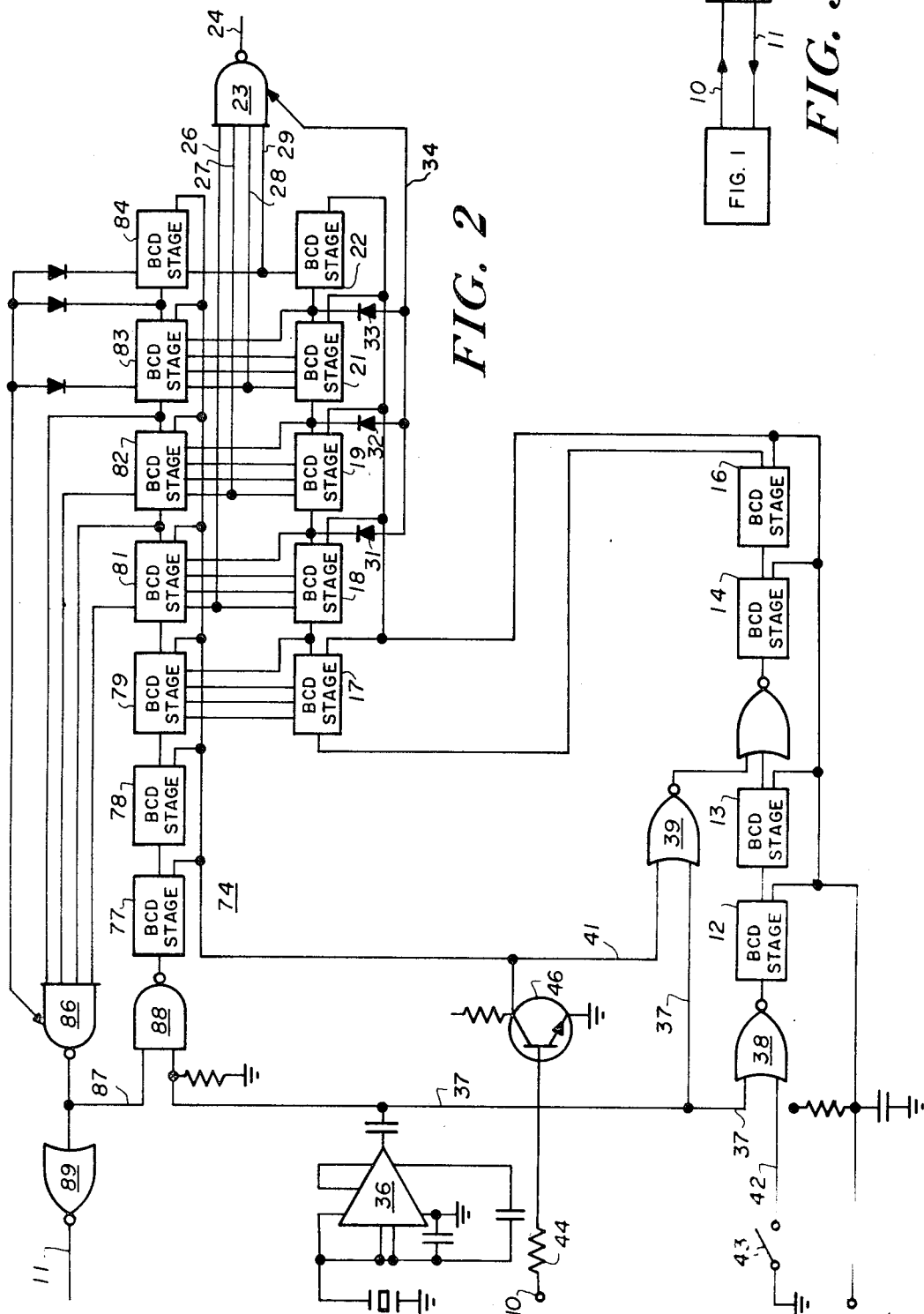


FIG. 2

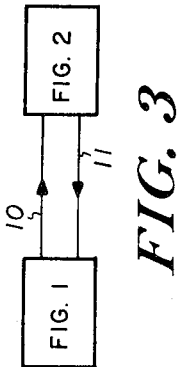


FIG. 3

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PULSE RESPONSIVE COUNTING CIRCUITS

GOVERNMENT INTEREST

The invention described herein may be manufactured, used and licensed by or for the Government for Governmental purposes without the payment to me of any royalties thereon.

FIELD OF THE INVENTION

This invention relates to preset timing devices and particularly to a preset timing device for military applications.

BACKGROUND OF THE INVENTION

Various ordnance devices require detonation at a fixed time after the occurrence of a physical event. The fixed time varies from situation to situation so that the ordnance device must be designed so that the fixed time can be set in the field immediately before use thereof.

Most ordnance devices with preset timing capability employ mechanical timers which are integral to the ordnance device. Personnel in the field must physically rotate dials with the aid of hand tools to set a desired time therein. These mechanical timers are not only expensive because they must withstand severe environmental conditions but also at times require personnel in the field to expose themselves to undue dangers in physically hand setting the timers which are located in the projectiles.

The mechanical preset timers are also expensive in operation because their cost is not spread over a number of uses but rather the entire setting mechanism is destroyed when the ordnance device is detonated.

Many systems exist which could be used for presetting information electronically and remotely into an ordnance device. These systems, however, require a large number of wires connecting the setting equipment and the ordnance device. The existing preset systems also lack error verification checks so that the person setting the information into the ordnance device cannot be sure that he has in fact preset the proper timing information.

Therefore, it is an object of this invention to provide an improved system for presetting timing information into ordnance devices.

It is another object of this invention to provide a system for remotely presetting timing information into an ordnance device enabling the person setting the information to protect himself from undue risk.

It is still another object of this invention to provide a system for remotely presetting timing information into an ordnance device in which a minimum number of wires connect the setting equipment and the ordnance device.

It is a further object of this invention to provide a system for remotely setting timing information into an ordnance device in which an economically significant portion of the equipment is not destroyed when the ordnance device is detonated.

It is still a further object of this invention to provide a system for remotely setting timing information into an ordnance device which confirms at the remote location that the proper information has been in fact set therein before the device is detonated.

BRIEF DESCRIPTION OF THE INVENTION

With these and other objects in view the present invention contemplates a system in which a first counting circuit located in an ordnance device generates an actuation signal when it has reached a first predetermined count. A second predetermined count is initially set into the first counting circuit from a remote location. A pulse generator in the ordnance device is rendered effective by a predetermined event to cause the first counting circuit to count from the second predetermined count to the first predetermined count thereby providing the actuation signal a predetermined time interval after the predetermined event.

The second predetermined count is initially set into the first counting circuit by a second counting circuit located at the remote location which generates a counting signal while the second counting circuit is advancing. A third predetermined count is initially set in the second counting circuit. The second counting circuit is then advanced from the third predetermined count to a fourth predetermined count.

The counting signal is sent to an integrated circuit located in the ordnance device and having the first counting circuit thereon to enable the first counting circuit to count during the presence of the counting signal thereby entering the second predetermined count therein.

The integrated circuit also contains a third counting circuit to which the second predetermined count is transferred at the termination of the counting signal. The third counting circuit is then counted down to provide a display signal at the remote location for verifying that the proper second predetermined count has been entered into the first counting circuit.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of remote setting circuitry forming a part of this invention and located at a remote location;

FIG. 2 is a schematic diagram of circuitry on an integrated circuit chip forming another part of this invention and located in an ordnance device; and

FIG. 3 is a block diagram showing how the circuitry of FIGS. 1 and 2 are interconnected in accordance with the teachings of this invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring first to FIG. 3, we see how a remote setting circuit (FIG. 1) is interconnected to a time delay generating circuit (FIG. 2) by a pair of wires 10 and 11. The wire 10 transfers setting information from the remote setting circuit (FIG. 1) to the time delay generating circuit (FIG. 2). The wire 11 transmits error checking information from the time delay generating circuit (FIG. 2) to the remote setting circuitry (FIG. 1) to insure that proper setting information has been received and stored in the time delay generating circuit (FIG. 2).

In operation the time delay generating circuit (FIG. 2) is manufactured on an integrated circuit chip and installed in an ordnance device to be detonated. The remote setting circuitry (FIG. 1) is mounted in a console to be connected to the time delay generating circuitry (FIG. 2) in the field for presetting a time delay

into the time delay generating circuitry (FIG. 2). Since the preset information is set under battlefield conditions, it is desirable to allow the person setting the information into the time delay generating circuitry (FIG. 2) maximum flexibility in positioning with respect thereto. After the time delay information is set into the circuitry of FIG. 2 and verification is made that proper information has in fact been inserted, the wires 10 and 11 may be disconnected leaving the remote setting circuitry in a safe area when the ordnance device is detonated.

Looking now at FIG. 2, we see a first counter circuit comprised on nine conventional binary coded decimal counting stages 12 through 14, 16 through 19, 21 and 22. A gate 23 senses the state of the four most significant stages 18, 19, 21 and 22 of the counter circuit to provide an actuation signal on an output lead 24 thereof when these stages 18, 19, 21 and 22 have reached a predetermined count.

In this example, the gate 23 provides an actuation signal on the lead 24 when the four stages 18, 19, 21 and 22 provide a signal on the outputs thereof indicating the number 9991. Therefore, two output leads of the stages 18, 19, and 21 must be sensed to determine the presence of 9's thereat while only one output lead of the stage 22 is sensed to detect when the stage 22 has reached the number 1. Since the gate 23 has only five inputs thereto, one lead from the stages 18, 19, 21, and 22 is fed directly into the gate 23 by leads 26 through 29. One lead from each of the stages 18, 19 and 21 is applied through diodes 31, 32 and 33 to the fifth input of the gate 23 by a lead 34 thereby expanding the number of useful inputs to the gate 23.

The stage of the counting circuit including the binary coded decimal stages 12 through 14, 16 through 19, 21 and 22 is controlled by a fixed frequency oscillator 36 which can be connected to advance the stages by one of two paths. The output from the oscillator 36 is applied by a lead 37 to steering gates 39 and 38. The steering gate 39 connects the oscillator 36 to advance the binary coded decimal stages 14, 16 through 19, 21 and 22 at a first rate when actuated by a signal on lead 41. The steering gate 38 connects the oscillator 36 to advance the stages 12 through 14, 16 through 19, 21 and 22 when actuated by a signal on lead 42. The stages 14, 16 through 19, 21 and 22 will advance at one hundredth the rate when actuated by the 38 than they will when actuated by the gate 39. This is because the fixed rate of the oscillator 36 will be divided by one hundred by the stages 12 and 13 before being applied to the stage 14. The gate 39 will enable the oscillator 36 to advance the stages 14, 16 through 19, 21 and 22 during a presetting interval to count to a preset number. This number initially preset therein will determine how long it will take the stages 18, 19, 21 and 22 to reach the count detected by the gate 23 thereafter.

After the initial number is set into the counter, the oscillator 36 is disengaged therefrom until a switch contact 43 is energized enabling the oscillator 36 to advance the counter starting with the stage 12. It should be clear that by connecting the oscillator 36 to the stage 14 during the setting interval 12 and to the stage 12 during the actual time delay interval, the presetting operation can be accomplished in one hundredth the time necessary for maximum countdown of the counter circuit.

In accordance with this invention, the first counter circuit is preset in response to a signal applied on the lead 10 through a resistor 44 and transistor 46 to the lead 41. The time during which the signal is present on the lead 10 determines how many counts the oscillator 36 will advance the stages 14, 16 through 19, 21 and 22 to their initial condition.

Referring now to FIG. 1, we see the circuitry for generating the signal on the lead 10. This circuitry includes a second counter circuit 47 which includes seven binary coded decimal counter stages 48, 49, 51 through 54 and 56. In operation, an initial count is set into the stages 52 through 54 and 56 by thumb wheel switches 57 through 59 and 61. A start switch 62 enables a gate 63 to pass pulses from an oscillator 64 to advance the second counting circuit 47 until a predetermined count is detected by a gate 66. A gate 67 driven by the switch 62 and the gate 66 through an inverter 68 provides a signal on a lead 69 during the interval starting when the switch 62 closes and ending when the gate 66 detects the second predetermined count in the counter circuit 47. Therefore, the signal on the lead 69 is at one level while the counter 47 is not advancing and at a second level during the interval when the counter 47 is advancing. An inverter 71 inverts the signal on the lead 69 and provides it to a resistor 72 to operate a transistor 73 for providing the counting signal on the collector thereof to the lead 10.

Therefore, it is seen that the time during which the oscillator 36 (see FIG. 2) advances the first counting circuit including the stages 14, 16 through 19, 21 and 22 at the faster rate is determined by the count set into the second counting circuit 47 by the switches 57 through 59 and 61. The time that the gate 23 will provide an actuation signal on the lead 24 after closure of the switch contact 43 is determined by the number set into the first counting circuit. Therefore, the numbers set into the second counting circuit 47 by the switches 57 through 59 and 61 will determine the time delay between the closure of the switch contact 43 and the generation of an actuation signal on the lead 24. This is done with only one wire connecting the second counting circuit 47 to the first counting circuit including the stages 12 through 14, 16 through 19, 21 and 22.

To verify that the proper delay timing information has been set into the first counting circuit a third counting circuit 74 (see FIG. 2) is employed to receive the count stored in the stages 17 through 19, 21 and 22 when the signal on the lead 10 returns to its initial state. To this end the output of the collector of transistor 46 is applied by a lead 76 to each stage 77 through 79 and 81 through 84 of the counter 74. When the signal on the lead 76 returns to its initial state thereby indicating that the counter 47 (see FIG. 1) has stopped counting the information in the stages 17 through 19 and 21 and 22 are applied to the stages 79 and 81 through 84 by nondestructive read-out. This means that the count in the stages 17 through 19, 21 and 22 is not disturbed but is also now in the stages 79 and 81 through 84.

A gate 86 senses the output of the stages 81 through 84 to provide a first signal on an output lead 87 when a count is present in the stages 81 through 84 and a second signal when any other count is present therein. When the signal from the stages 18, 19, 21 and 22 are transferred to the stages 81 through 84 the signal on the lead 87 enables a gate 88 to pass the signal from the

oscillator 36 to advance counter 74. The gate 86 also applies its output signal through an inverting gate 89 to the lead 11. The counter 74 will advance until the predetermined count sensed by the gate 86 is present at the output of the stages 81 through 84. The output of the gate 86 then reverts to its initial condition disabling the gate 88 from passing signals from the oscillator 36 and also returning the signal on the lead 11 back to its initial condition. It should be understood that the gate 86 will normally present a first signal on the output thereof until the count from the stages 17 through 19, 21 and 22 are transferred to the stages 79 and 81 to 84. If a different count is initially in the stages 81 through 84, the oscillator 36 will be enabled until the counter 74 is driven to the predetermined count.

It should be further understood that the time interval of the gate signal provided on the lead 11 will be the complement on the signal which was originally provided on the lead 10 by the counting circuit 47. Since the signal on the lead 10 enabled a seven-stage counter to count to a number and the signal on the lead 11 is generated by allowing a counter to count from that number to a fixed number, the time between the beginning of the signal on the lead 10 and the end of the signal on the signal on the lead 10 and the end of the signal on the lead 11 will be constant no matter what initial information is set into the first counting circuit stages 14, 16 through 19, 21 and 22.

The gate signal on the lead 11 is passed to a gate circuit 91 (see FIG. 1) which enables the oscillator 64 thereof to advance the counter circuit 92 during the presence of the gating signal on the lead 11. The counter 92 has seven stages 93, 94 and 96 through 99 and 101. The number to which the counter circuit 92 will count during the interval determined by the signal on the lead 11 will be the same number which was initially entered into the second counting circuit 47 by the switches 57 through 59 and 61 if all the circuits are operating properly. Therefore, four display tubes 102 through 104 and 106 are attached to the stages 97, 98, 99 and 101 to read out the count therein. If the setting operation has been successfully performed the count read-out visually will be the same count which appears on the setting switches 57 through 59 and 61. Since the setting switches and the read-out display tubes are in the same console, they may be arranged side by side for easy verification of proper setting information.

Since it is necessary for the number to be actually set into the counter including the stages 12 through 14, 16 through 19, proper read-out in the display tubes 102, 103, 104 and 106, a correspondence between the setting switches 57, 58, 59 and 61 and the display tube 102, 103, 104 and 106 can give the operator a reasonable assurance that the proper timing information has been set.

It should be understood that while this invention has been disclosed with respect to a particular embodiment thereof numerous others will become obvious to those of ordinary skill in the art in light thereof.

What is claimed is:

1. In combination:

a first counting circuit for generating an actuation signal when said first counting circuit has reached a first predetermined count;
means for setting a second count in said first counting circuit which includes;

a second counting circuit for generating a counting signal while said second counting circuit is advancing;

means for initially setting a third count in said second counting circuit;

means for advancing said second counting circuit from said third count to a fourth predetermined count;

means for applying said counting signal to said first counting circuit;

a pulse generating circuit for causing said first counting circuit to count; and

means responsive to a predetermined event for rendering said pulse generating circuit effective to cause said first counting circuit to count thereby enabling said first counting circuit to reach said first predetermined count and generate said actuation signal.

2. The combination as defined in claim 1 also including:

means responsive to said second counting circuit reaching said fourth predetermined count for displaying information indicating that the count in said first counting circuit has in fact reached said second count.

3. The combination as defined in claim 1 in which said counting signal renders said first counting circuit responsive to said pulse generating circuit to count to said second count.

4. The combination as defined in claim 3 in which said predetermined event renders said first counting circuit effective to count at a first rate and said counting signal renders said first counting circuit responsive to said pulse generating circuit to count at a second rate, said second rate being greater than said first rate.

5. The combination as defined in claim 3 also including:

means responsive to said second counting circuit reaching said fourth predetermined count for displaying information indicating that the count in said first counting circuit has in fact reached said second count.

6. The combination as defined in claim 5 in which said displaying means includes:

a third counting circuit;

a fourth counting circuit;

means responsive to said second counting circuit reaching said fourth predetermined count for setting said third counting circuit to said count in said first counting circuit;

means responsive to said setting of said third counting circuit for advancing said third counting circuit to a fifth predetermined count; and

means for advancing said fourth counting circuit while said third counting circuit is advanced.

7. The combination as defined in claim 6 in which said predetermined event renders said first counting circuit effective to count at a first rate and said counting signal renders said first counting circuit responsive to said pulse generating circuit to count at a second rate, said second rate being greater than said first rate.

8. The combination as defined in claim 6 in which said displaying means is driven by said fourth counting circuit.

9. The combination as defined in claim 8 in which said predetermined event renders said first counting

circuit responsive to said pulse generating circuit to count at a second rate, said second rate being greater than said first rate.

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