Abstract: A fabricating method of a printed circuit board (PCB) with a cavity and a structure of the PCB fabricated by the method are provided. The method includes a first step of forming a base circuit board provided with an internal circuit layer having cavity patterns on a surface of a substrate, a second step of forming a laser stopper layer on upper portions of the cavity circuit patterns, a third step of forming at least one external circuit layer on the base circuit board, and a fourth step of forming a cavity region by removing the external circuit layer on an upper portion of the laser stopper layer. Accordingly, in a fabricating method of a multi-layered PCB with a cavity, a laser stopper layer is formed on upper surfaces of cavity circuit patterns, so that it is possible to rapidly and precisely form the cavity, to precisely control the depth of the cavity and to have no influence on a circuit previously formed in the interior of the cavity.
Description

Title of Invention: PCB WITH CAVITY AND FABRICATING METHOD THEREOF

Technical Field

1. The present invention relates to a fabricating method of a printed circuit board (PCB) with a cavity formed in one region thereof and a structure of the PCB fabricated by the method.

Background Art

2. A printed circuit board (PCB) is formed by printing a circuit line pattern, formed of a conductive material, such as copper, onto an electrical insulating substrate. The PCB is in a state just before electronic components are mounted thereon. That is, the PCB refers to a circuit board that positions various kinds of electronic components and fixedly prints circuit lines (line patterns) connecting the electronic components onto a flat plate so as to densely mount the electronic components on the flat plate. PCBs are generally classified into a single-layer PCB and a build-up board, i.e., a multi-layer PCB, obtained by forming a PCB with multiple layers.

3. Recently, system integration technologies have been required so as to meet the requirement of a light, thin, and small electronic product, and techniques for fabricating an embedded PCB and a cavity PCB have come into the spotlight as countermeasure techniques. The embedded PCB is advantageous in that components mounted on a surface are completely embedded in the PCB during the PCB process so as to have a high degree of freedom in designing lines around the embedded components. However, the embedded PCB is disadvantageous in that it is difficult to have compatibility between the embedded components and PCB raw materials and to perform re-operation for a defective component and that there is a limitation in performing a component test.

4. The cavity PCB is disadvantageous in that components are not completely embedded in the PCB but mounted in cavities, thereby having a low degree of freedom. The cavity PCB is advantageous in that it is very effective to perform the re-operation for the defective component and the component test, which are problems of the embedded PCB.

5. The cavity PCB has been frequently applied in techniques to which a low temperature co-fried ceramic (LTCC)-based mold process is applied. However, the cavity PCB is hardly applied in layer-by-layer techniques. The reason is that it is difficult to perform machining of an exact cavity region and that a cavity internal circuit may be damaged in a process such as plating, imaging or etching during the PCB process.
FIGS. 1 and 2 are conceptual views schematically illustrating a cavity forming process in a cavity PCB according to the related art.

As illustrated in these figures, it is very difficult to form a cavity in which an electronic device chip will be mounted in a PCB with a structure in which a multiple insulating layers 1, 2, 3, 4 and 5 are stacked and a plurality of circuit patterns 1a, 1b, 2a, 4a and 6 are formed between the respective insulating layers.

That is, as illustrated in FIG. 1, a method of selectively machining the position of the cavity C using a milling bit M is frequently used in the PCB, in which the stacking has been performed in the state of a finished product. In the method, the machining accuracy should be controlled in the range of ±5μm, but is practically controlled in the range from about 50 to 100μm. Therefore, it is practically very difficult to perform the machining of the cavity. Since the difference in machining accuracy is very serious, product reliability is deteriorated in mass production.

Alternatively, as illustrated in FIG. 2, a method may be applied, in which a cavity is selectively formed by precisely punching a position of the cavity using a punching device in the state of a finished product. However, in the method, a C-stage substrate material is punched by a punching blade, and therefore, the outer wall of the cavity is inevitably damaged. The damage of the outer wall of the cavity induces cathode anode filament (CAF) shot (phenomenon that glass filament in prefreg becomes open due to punching, and hence an electrical short circuit is caused between vias in the interior of the PCB) due to moisture absorption, delamination, and damage of the bottom surface of the cavity. Therefore, cost increases due to manufacturing cost of the punching jig P, and the range in designing the cavity is narrowed.

Disclosure of Invention

Technical Problem

The present invention is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a fabricating method of a multi-layered printed circuit board (PCB) with a cavity and a structure of the PCB fabricated by the method, in which a laser stopper layer is formed on upper surfaces of cavity circuit patterns, so that it is possible to rapidly and precisely form the cavity, to precisely control the depth of the cavity and to have no influence on a circuit previously formed in the interior of the cavity.

Another object of the present invention is to provide a fabricating method of a multi-layered PCB with a cavity and a structure of the PCB fabricated by the method, in which a cavity insulating layer is used by machining the cavity using a prefreg with no flow so that a metal pattern layer is formed and fixed on an upper portion of an empty space, so that it is possible to precisely control the depth of the cavity and to have no
influence on a circuit previously formed in the interior of the cavity.

**Solution to Problem**

[12] In accordance with an aspect of the present invention, there is provided a fabricating method of a printed circuit board (PCB) with a cavity, the method including: a first step of forming a base circuit board provided with an internal circuit layer having cavity circuit patterns on a surface of a substrate; a second step of forming a laser stopper layer on upper portions of the cavity circuit patterns; a third step of forming at least one external circuit layer on the base circuit board; and a fourth step of forming a cavity region by removing the external circuit layer on an upper portion of the laser stopper layer.

[13] In accordance with another aspect of the present invention, there is provided a fabricating method of a PCB with a cavity, the method including: a first step of forming a base circuit board provided with internal circuit patterns having cavity circuit patterns on a surface of a substrate; a second step of forming a cavity circuit layer having an opening region at upper portions of the cavity circuit patterns on the base circuit board; and a third step of removing a cover metal layer corresponding to the cavity region in the cavity circuit layer.

**Advantageous Effects of Invention**

[14] According to embodiments of the present invention, in a fabricating method of a multi-layered printed circuit board (PCB) with a cavity, a laser stopper layer is formed on upper surfaces of cavity circuit patterns, so that it is possible to rapidly and precisely form the cavity, to precisely control the depth of the cavity and to have no influence on a circuit previously formed in the interior of the cavity.

[15] Particularly, the fabricating method is performed not by selecting a separate prefreg but by using a general-purpose insulating material to increase processing efficiency, and the laser stopper layer is used in the fabricating method. Thus, it is possible to ensure various shapes of the cavity circuit patterns subjected to the surface treatment and a wide range in designing the cavity.

[16] Further, in a fabricating method of a multi-layered PCB with a cavity, a cavity insulating layer is used by machining the cavity using a prefreg with no flow so that a metal pattern layer is formed and fixed on an upper portion of an empty space, so that it is possible to precisely control the depth of the cavity and to have no influence on a circuit previously formed in the interior of the cavity.

**Brief Description of Drawings**

[17] FIGS. 1 and 2 are conceptual views illustrating a fabricating method of a printed circuit board (PCB) according to the related art.

[18] FIGS. 3 to 6 illustrate a flowchart and sectional views of a fabricating method of a
PCB with a cavity according to an embodiment of the present invention.

FIG. 7 is a sectional view conceptually illustrating a structure of a PCB according to an embodiment of the present invention.

FIGS. 8 and 9 illustrate sectional views of a fabricating method of a PCB with a cavity according to another embodiment of the present invention.

**Best Mode for Carrying out the Invention**

The present invention provides a fabricating method of a printed circuit board with a cavity, in which a multi-layered PCB is formed using a laser stopper and a cavity region is then machined, so that it is possible to increase a degree of freedom in machining the cavity and to protect a circuit in the cavity.

To this end, a base circuit board provided with an internal circuit layer including cavity circuit patterns is formed on a surface of a substrate, and a laser stopper layer is formed on upper portions of the cavity circuit patterns. Then, at least one external circuit layer is formed on the base circuit board, and a cavity region is formed by removing the external circuit layer on an upper portion of the laser stopper layer.

**Mode for the Invention**

Reference will now be made in detail to exemplary embodiments of the present invention, examples of which are illustrated in the accompanying figures, wherein like reference numerals refer to the like elements throughout. The exemplary embodiments are described below in order to explain the present invention by referring to the figures. Although the terms "first", "second", and the like may be used herein to describe various components, these components should not be limited by these terms. These terms are only used to distinguish one component from another component.

1. First embodiment

FIGS. 3 and 4 illustrate a flowchart and sectional views of a fabricating method of a PCB with a cavity according to a first embodiment of the present invention.

The method according to the first embodiment of the present invention includes a first step of forming a base circuit board provided with an internal circuit layer including cavity circuit patterns on a surface of a substrate, a second step of forming a laser stopper layer on upper portions of the cavity circuit patterns, a third step of forming at least one external circuit layer on the base circuit board, and a fourth step of forming a cavity region by removing the external circuit layer on an upper portion of the laser stopper layer.

Detailed examples of the respective steps will be described with reference to the accompanying drawings.

(1) Process of forming internal circuit layer (cavity circuit patterns)

In the first step, as illustrated in FIG. 4, a via hole for electrical conduction between
layers is machined in a copper compound layer (CCL) in which copper foils 110 are formed on both surfaces of an insulating layer 120, respectively (S1), and internal circuit patterns 111 are implemented by patterning the copper foil 110 (S2). In this case, the internal circuit patterns 111 include cavity circuit patterns 112 disposed at a lower portion of a cavity region C having a cavity in which a chip will be mounted later (the structure in which the internal circuit patterns including the cavity circuit patterns are formed on the insulating layer is defined as a 'base circuit board').

[30] Subsequently, a photo solder resist (PSR) 130 is printed in the cavity region C (S3), and the PSR 130 in the cavity region C is exposed, thereby forming a structure in which solder resist patterns 131 are formed between the cavity circuit patterns 112 (S4). The cavity region C may be formed in circuit processing of the outside of the cavity circuit patterns 112, i.e., laser stopper stepped portions T that are metal patterns exposed to edge portions of the cavity region. The stepped portions are end portions at which a laser stopper layer is stacked in the cavity region C. Then, a portion of the stepped portion is exposed in the cavity region.

[31] Subsequently, there is added a process of forming a surface treatment layer 113 by performing oxidation treatment with respect to surfaces of the cavity circuit patterns 112. In addition to the oxidation treatment, the surface treatment layer 113 may be formed by performing plating with respect to a single layer or multiple layers using any one of Cu, Ni, Pd, Au, Sn, Ag and Co, or a binary or ternary alloy thereof.

[32] (2) Process of forming laser stopper layer

[33] In S5, the laser stopper stepped portions T are formed the edge portions of the cavity region C. In S6, a heat-resistance laser stopper layer 140 with a weak adhesion.

[34] The laser stopper layer 140 is a layer that serves as a stopper to automatically stop laser when the cavity region C is machined using a laser drill later. As described above, the laser stopper layer 140 may be formed of a heat resistance material with a weak adhesion. Particularly, the laser stopper layer 140 may be formed in a tape shape to facilitate attachment/detachment for convenience of processing. For example, the laser stopper layer 140 is preferably formed as an insulating layer formed using any one of epoxy, phenolic resin, prefrg, polyimide and ABF. More preferably, the laser stopper layer 140 may be formed in a tape shape using the aforementioned material.

[35] (3) Process of stacking external circuit layer

[36] After S5, metal circuit patterns are formed by stacking at least one insulating layer 150 and at least one metal circuit layer 160 on an upper or lower portion of the base circuit board and then patterning them (S7).

[37] When assuming that the structure shown in S8 is referred to as A, a stacking process of insulating and metal layers and a circuit forming process are generally performed on the substrate A in a subsequent process. That is, a general build-up process may be
performed to form via holes H1 and H2 electrically conducted with the internal circuit patterns and other circuit patterns. The substrate subjected to processing of the via hole and the like is referred to as A'.

Subsequently, a plurality of insulating layers and metal circuit layers are formed on the substrate A' (reference numeral B), and circuit patterns are formed using the metal circuit layers. Then, processes such as a via-hole machining process and a surface treatment process are performed, thereby forming a multi-layered PCB with a structure shown in S9.

(4) Process of forming cavity region

Subsequent processes will be described with reference to FIGS. 5 and 6.

A cavity machining process is performed as a process performed after the structure of the multi-layered PCB is formed. In the cavity machining process, a position of the cavity to be machined is aligned using a laser drill L, and the machining is started in a vertical direction of the laser stopper stepped portion T. Then, if the laser drill L reaches the laser stopper layer 140, the laser machining is automatically stopped (S10). Subsequently, the insulating layer and metal layers at the machined portion are removed, and the laser stopper layer 140 is finally removed, thereby completing the cavity machining (S11).

The aforementioned process can rapidly and precisely implement the formation of the cavity through the laser machining based on the laser stopper layer, and can precisely control the depth of the cavity. The aforementioned process has no influence on a circuit previously formed in the interior of the cavity. The aforementioned process can be performed not by selecting a separate prefreg but by using a general-purpose insulating material to increase processing efficiency according to characteristics of the cavity machining such as alkali etching. The laser stopper layer can be used in the aforementioned process. Thus, it is possible to ensure various shapes of the cavity circuit patterns subjected to the surface treatment and a wide range in designing the cavity.

Hereinafter, a structure of a PCB fabricated by the aforementioned method will be described.

FIG. 7 illustrates a structure of a PCB according to an embodiment of the present invention, in which the laser stopper layer in S11 is removed.

The PCB according to the embodiment of the present invention is provided with a base circuit board including an internal circuit layer 111 electrically connected to embedded circuit patterns. The internal circuit layer 111 has a structure including cavity circuit patterns 112 formed at a lower portion of a cavity region. The PCB is provided with a cavity region C to which the cavity circuit patterns 112 are exposed on a surface of the base circuit board, and the cavity region C provides a space in which
an electronic device chip will be mounted later.

As described in the fabricating method, solder resist patterns 113 are formed between the cavity circuit patterns 112 so as to protect the circuit patterns, and a surface treatment layer 113 may be further formed on surfaces of the cavity circuit patterns 112. Particularly, the PCB according to the present invention has a structure in which at least one circuit pattern P is exposed to a sidewall surface of at least one insulating layer that constitutes the cavity region C.

In the PCB, metal stepped portions T are exposed to lower edge portions of the cavity region C, and the surface treatment layer 113 may be implemented as an oxidation layer by performing oxidation treatment with respect to the exposed surfaces of the cavity circuit patterns or a plating layer of a single- or multi-layered structure, formed using any one of Cu, Ni, Pd, Au, Sn, Ag and Co, or a binary or ternary alloy thereof.

2. Second embodiment

This embodiment provides a fabricating method of a PCB with a cavity, which can effectively implement the cavity using an insulating layer with no flow and a cover metal layer formed on the insulating layer, and a reliable structure of the PCB fabricated by the aforementioned method.

FIGS. 8 and 9 illustrate sectional views of a fabricating method of a PCB with a cavity according to a second embodiment of the present invention.

The method according to the second embodiment of the present invention includes a first step of forming a base circuit board provided with internal circuit patterns including cavity circuit patterns on a surface of a substrate, a second step of forming a cavity circuit layer in which one region on upper portions of the cavity circuit patterns is empty on the internal circuit patterns, and a third step of removing a cover metal layer corresponding to a cavity region of the cavity circuit layer.

(1) Process of implementing internal circuit pattern

Specifically, a via hole H for electrical conduction between layers is machined in a copper compound layer (CCL) in which copper foils 210 are formed on both surfaces of an insulating layer 220, respectively (Q1), internal circuit patterns 211 are then implemented by patterning the copper foils 210 (Q12). The internal circuit patterns 211 include cavity circuit patterns 212 to be exposed to a lower surface of a cavity later.

Subsequently, solder resist patterns 231 are as protection patterns by coating a photo solder resist 230 on the cavity circuit patterns 212 (Q13 and Q14), and a plating layer is formed by performing surface treatment with respect to surfaces of the cavity circuit patterns, on which the solder resist patterns 231 are not formed. To this end, a plating mask layer 240 is formed in a region in which the plating layer will not formed, and a surface treatment layer 213 is formed through plating. The surface treatment layer 213
may be implemented as a single layer or multiple layers by using any one of Cu, Ni, Pd, Au, Sn, Ag and Co, or a binary or ternary alloy thereof. Subsequently, the plating mask layer 240 is removed (Q15 to Q17).

(2) Process of forming cavity circuit layer

Subsequently, a process in Q2 is performed.

In Q2, an insulating layer 250 with one opened region is stacked so that an empty space is formed on upper portions of the cavity circuit patterns 212, and a metal thin film 260 is stacked to cover the upper portions (the insulating layer with the one opened region is referred to as a 'cavity insulating layer').

Subsequently, in Q3, a cover metal layer C1 and other circuit patterns 261 are formed by patterning the metal thin film 260, and a process is then performed in which a second cover metal layer C2 and other circuit patterns 272 are formed by coating an insulating layer 270 with an opening in a region corresponding to the cavity circuit patterns on an upper portion of the cover metal layer CI, coating a metal thin film 271 on an upper portion of the insulating layer 270 and then patterning them. The aforementioned process may be repeatedly performed several times, and the height of a cavity to be formed later may be increased as the aforementioned process is repeated. Preferably, the cavity insulating layers 250 and 270 which form the opened spaces on the upper portions of the cavity circuit patterns preferably have no flow. This is because a prefreg used for the cavity insulating layer is not flowed into the cavity region in a subsequent process of stacking the cavity insulating layer in the state that its central region is opened so that an empty space is formed on the upper portions of the cavity circuit patterns 231 and then performing heat compression with respect to the cavity insulating layer. A process of stacking insulating and metal layers 252 and 261 may be performed on a surface opposite to the surface on which the cavity insulating layer and the metal thin film are formed.

Cover metal layers continuously formed in the stacking process may be formed longer than an opening region P1 or P2 of each of the insulating layers. Preferably, the region of an end of the cover metal layer, which comes in contact with an upper surface of the opening region, is formed in the range from 25 to 100/M so that the cover metal layer does not collapse down to the opening region in the continuous process. This is because the contact region easily collapses in the case of 25/M or less and a degree of freedom in design is degraded in the case of 100/M or more. Therefore, the region of each of both the ends of the cover metal layer, which comes in contact with the upper surface of the opening region, is preferably formed in the range from 50 to 200/M.

Subsequently, as shown in Q3, a cavity C can be implemented through a process of removing the cover metal layers C1 and C2. The process of removing the cover metal
layers may be performed using alkali etching for removing a cover metal layer formed of Cu. This is because the etching has no influence on the plating layer subjected to the surface treatment on surfaces of other circuit patterns.

[61] A structure of a PCB with a cavity according to an embodiment of the present invention, fabricated by the aforementioned method is as follows (see the figure in Q3).

[62] The PCB according to the embodiment of the present invention is provided with a cavity C to which cavity circuit patterns 212 are exposed on a surface of a substrate including outer circuit patterns 271 electrically connected to a plurality of embedded circuit patterns. The embedded circuit pattern includes patterns 261 on each insulating layer. Particularly, one or more circuit patterns Y1 and Y2 are exposed to a sidewall surface of at least one insulating layer that constitutes the cavity C, and the same circuit patterns are also exposed to the opposite sidewall surface of the insulating layer.

[63] A surface treatment layer 213 of a single- or multi-layered structure, formed using any one of Cu, Ni, Pd, Au, Sn, Ag and Co, or a binary or ternary alloy thereof is formed on surfaces of the cavity circuit patterns. A solder resist pattern layer 231 may be formed in one region of the cavity circuit patterns.

[64] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.
Claims

[Claim 1] A fabricating method of a printed circuit board (PCB) with a cavity, the method comprising:
- a first step of forming a base circuit board provided with an internal circuit layer having cavity circuit patterns on a surface of a substrate;
- a second step of forming a laser stopper layer on upper portions of the cavity circuit patterns;
- a third step of forming at least one external circuit layer on the base circuit board; and
- a fourth step of forming a cavity region by removing the external circuit layer on an upper portion of the laser stopper layer.

[Claim 2] The method of claim 1, wherein the first step comprises the steps of:
- al) forming internal circuit layers electrically conducted with each other on both surfaces of a first insulating layer, respectively; and
- a2) forming at least one solder resist pattern between the cavity circuit patterns in the internal circuit layer.

[Claim 3] The method of claim 2, wherein the step a2) comprises the steps of:
- forming the solder resist pattern to expose the cavity circuit patterns; and
- performing surface treatment with respect to the exposed cavity circuit patterns.

[Claim 4] The method of claim 2, wherein the third step is a step implemented through a process of sequentially forming at least one insulating layer and at least one metal layer on the base circuit pattern and forming via holes electrically conducted with the internal circuit patterns and other circuit patterns.

[Claim 5] The method of claim 1, wherein the fourth step comprises the steps of:
- bl) machining the insulating and metal layers on the upper portions of the cavity circuit patterns using a laser drill until the laser stopper layer is exposed;
- b2) forming the cavity region by removing the machined insulating and metal layers; and
- b3) removing the laser stopper layer.

[Claim 6] A PCB comprising:
- a base circuit board having internal circuit patterns electrically connected to embedded circuit patterns;
- a cavity region in which cavity circuit patterns are exposed on a surface
of the base circuit board; and
solder resist patterns formed between the cavity circuit patterns,
wherein at least one circuit pattern is exposed to a sidewall surface of the at least one insulating layer that constitutes the cavity region.

[Claim 7] The PCB of claim 6, further comprising a surface treatment layer formed on surfaces of the cavity circuit patterns.

[Claim 8] The PCB of claim 6 or 7, wherein a metal stepped portion is exposed to a surface of a lower edge portion in the cavity region.

[Claim 9] The PCB of claim 7, wherein the surface treatment layer is formed by performing oxidation treatment with respect to the exposed surfaces of the cavity circuit patterns.

[Claim 10] The PCB of claim 7, wherein the surface treatment layer is a plating layer of a single- or multi-layered structure, formed on the surfaces of the cavity circuit patterns by using any one of Cu, Ni, Pd, Au, Sn, Ag and Co, or a binary or ternary alloy thereof.

[Claim 11] A PCB comprising:
a cavity region formed in a depth direction of a base circuit board to implement a chip mounting region; and
a structure in which a metal stepped portion is exposed to a surface of a lower edge portion in the cavity region.

[Claim 12] The PCB of claim 11, wherein the base circuit board comprises internal circuit patterns electrically connected to embedded circuit patterns, and cavity circuit patterns are exposed to a surface of the base circuit board on a lower surface of the cavity region.

[Claim 13] The PCB of claim 12, further comprising solder resist patterns formed between the cavity circuit patterns.

[Claim 14] The PCB of claim 13, wherein at least one circuit pattern is exposed to a sidewall surface of at least one insulating layer that constitutes the cavity region.

[Claim 15] The PCB of claim 14, further comprising a surface treatment layer formed on surfaces of the cavity circuit patterns.

[Claim 16] A fabricating method of a PCB with a cavity, the method comprising:
a first step of forming a base circuit board provided with internal circuit patterns having cavity circuit patterns on a surface of a substrate;
a second step of forming a cavity circuit layer having an opening region at upper portions of the cavity circuit patterns on the base circuit board; and
a third step of removing a cover metal layer corresponding to the cavity
region in the cavity circuit layer.

[Claim 17] The method of claim 16, wherein the first step comprises the steps of:
al) forming outer circuit patterns electrically conducted with each other on both surfaces of a first insulating layer, respectively;
a2) forming at least one solder resist pattern between the cavity circuit patterns in the outer circuit patterns;
a3) forming a plating mask layer in a region except the cavity circuit patterns and forming a surface treatment layer through plating; and
a4) removing the plating mask layer.

[Claim 18] The method of claim 16, wherein the second step comprises the steps of:
b1) stacking a cavity insulating layer having an opening region on upper portions of the outer circuit patterns; and
b2) forming and patterning a method thin film to cover a front surface of the cavity insulating layer,
wherein the steps b1) and b2) are repeatedly performed one or more times, and the patterning in the step b2) implements circuit patterns in a region except the upper cover metal layer corresponding to the cavity circuit patterns.

[Claim 19] The method of claim 18, wherein the third step is implemented as a step of removing at least one cover metal layer formed on the upper portions of the cavity circuit patterns through alkali etching.

[Claim 20] A PCB comprising a cavity region in which cavity circuit patterns are exposed to a surface of a substrate having outer circuit patterns electrically connected to embedded circuit patterns,
wherein at least one circuit pattern is exposed to a sidewall surface of at least one insulating layer that constitutes the cavity region.

[Claim 21] The PCB of claim 20, wherein a solder resist pattern layer is formed in one region of the cavity circuit patterns.
[Fig. 3]

1. Form internal circuit layer (cavity circuit patterns)
2. Form laser stopper (LST) layer
3. Stack external circuit layer
4. Perform cavity machining (laser drilling)
5. Remove insulating layer, metal layer and LST layer