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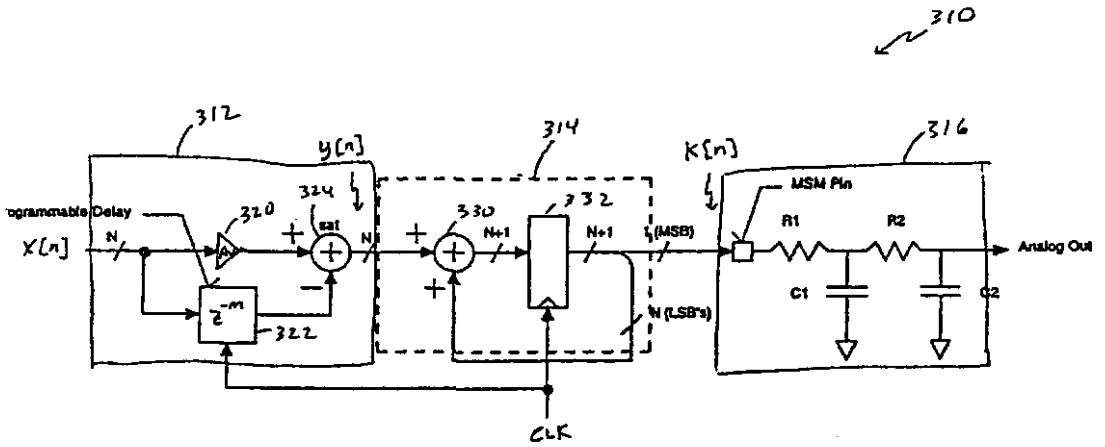
(54) Title: DIGITAL-TO-ANALOG INTERFACE CIRCUIT HAVING ADJUSTABLE TIME RESPONSE



(57) Abstract: An interface circuit for converting a digital signal to an analog signal. The interface circuit includes a time response adjustment circuit, a modulator, and a filter. The time response adjustment circuit receives the digital signal and generates an adjusted signal. The modulator couples to the time response adjustment circuit, receives the adjusted signal, and generates a modulator signal. The filter couples to the modulator, receives the modulator signal, and generates the analog signal. The analog signal has a time response that is modified by the time response adjustment circuit. In an embodiment, the time response adjustment circuit includes a gain element, a delay element, and a summer. The gain element receives and scales the digital signal by a scaling factor. The delay element receives and delays the digital signal by a time delay. The summer couples to the gain element and the delay element, sums the scaled signal from the gain element and the delayed signal from the delay element to generate the adjusted signal.

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DIGITAL-TO-ANALOG INTERFACE CIRCUIT HAVING ADJUSTABLE TIME RESPONSE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. Application Serial No. unknown, entitled "TRANSMITTER ARCHITECTURES FOR COMMUNICATIONS SYSTEMS," filed on the same day herewith, and incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates to electronics circuits, and more particularly to an interface circuit that provides an analog signal having an adjustable time response.

A digital-to-analog interface circuit is commonly used in many electronics circuits to provide an analog signal that drives an analog circuit element. The interface circuit typically employs a pulse width modulator (PWM) or a pulse density modulator (PDM) that receives a digital signal from a digital circuit and generates a corresponding intermediate signal that is filtered to provide the analog signal. The PWM or PDM act as an interface between the digital and analog circuits.

A conventional PWM or PDM receives a digital signal comprising a sequence of N-bit digital values and for each value generates a corresponding waveform. Each waveform has a predetermined period and includes a number of high ("1") and low ("0") values, as determined by the input digital value. For example, for a 9-bit PWM or PDM, the input digital value can range from 0 through 511 and each waveform has a period of 512 clock cycles and includes 0 to 511 high values. An input digital value of 128, for example, corresponds to a waveform having 128 high values and 384 low values. For a PWM, the high values are grouped together at the start of each waveform and for a PDM the high values are somewhat randomly spread across the waveform. For ease of implementation, some PDMs spread the high values in a pseudo-random

manner, and not uniformly. The waveforms are digital in nature and are filtered to generate the analog signal.

One common application for the interface circuit is in control loops. For example, for a receiver or a transmitter in a communications system, the interface circuit can be used for a carrier tracking loop, a bit timing loop, an automatic gain control (AGC) loop, a bias control loop, a power control loop, a DC offset adjustment loop, and others. For each of these loops, a loop control circuit generates a digital control signal that is provided to a PWM or PDM within the interface circuit associated with that loop. The PWM or PDM generates a sequence of waveforms based on the values in the digital control signal. The waveforms are filtered to generate the analog control signal that is used to drive the controlled element (e.g., a voltage-controlled oscillator, a variable gain amplifier, a summing element, and so on).

The analog control signals generated in conjunction with the PWMs or PDMs are typically required to meet various specifications. Typical specifications include a response time (i.e., the settling time) for a step input and ripple amplitude on the control signal. Fast response time and small amounts of ripple are desirable (or required) for many applications. The fast response time allows for a wide bandwidth control loop and a quick response to rapid changes in the input condition. The ripples on the control signal correspond to noise, and small amounts of ripple are generally required for better performance. However, fast response time and small amounts of ripple are conflicting design considerations. Optimizing for fast response time often results in larger ripple amplitude on the control signal.

As can be seen, an interface circuit having adjustable time response (i.e., to provide a faster response time) while maintaining small ripple amplitude is highly desirable.

SUMMARY OF THE INVENTION

The invention provides a digital-to-analog interface circuit that generates an analog signal having an adjustable time response and introduces minimum additional ripple, if any, on the analog signal. The interface circuit

includes a time response adjustment circuit that receives the digital signal, modifies (or adjusts) the digital signal to obtain the desired time response characteristics (i.e., faster response time), and provides the adjusted signal to a subsequent circuit that converts the adjusted signal into the analog signal. For example, to provide a faster response time, the time response adjustment circuit can add overdrive pulses corresponding to changes in the digital signal. The overdrive pulses provide additional drive for the subsequent filter which, in turn, speeds up the filter response.

A specific embodiment of the invention provides an interface circuit for converting a digital signal to an analog signal. The interface circuit includes a time response adjustment circuit, a modulator, and a filter. The time response adjustment circuit receives the digital signal and generates an adjusted signal. The modulator couples to the time response adjustment circuit, receives the adjusted signal, and generates a modulator signal. The filter couples to the modulator, receives the modulator signal, and generates the analog signal. The analog signal has a time response that is modified by the time response adjustment circuit. In an embodiment, the time response adjustment circuit includes a gain element, a delay element, and a summer. The gain element receives and scales the digital signal by a scaling factor. The delay element receives and delays the digital signal by a time delay. The summer couples to the gain element and the delay element. The summer subtracts the delayed signal from the scaled (or gained) signal to generate the adjusted signal.

Another specific embodiment of the invention provides a method for modifying a time response of an analog signal. The method includes: (1) receiving a digital signal; (2) generating an adjusted signal based on the digital signal and changes in the digital signal; (3) generating a modulator signal based on the adjusted signal; and (4) filtering the modulator signal to obtain the analog signal. The analog signal has a time response that is modified based on, for example, changes in magnitude of the digital signal. The modifications manifest in the adjusted signal and may include, for example, overdrive pulses corresponding to changes in the digital signal.

The invention can be used in various applications including, for example, control loops of a receiver or a transmitter.

The foregoing, together with other aspects of this invention, will become more apparent when referring to the following specification, claims, and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a block diagram of an embodiment of a transceiver for a communications system.

Figs. 2A and 2B show block diagrams of a portion of a conventional control loop and a portion of a control loop that includes an interface circuit of the invention, respectively.

Fig. 3A shows a diagram of a specific embodiment of an interface circuit of the invention.

Figs. 3B and 3C show diagrams of two specific embodiments of the time response adjustment circuit.

Figs. 4A and 4B show plots of step responses of a conventional interface circuit and an interface circuit that employs a time response adjustment circuit of the invention, respectively.

Fig. 5 shows a diagram of a specific embodiment of a time response adjustment circuit of the invention.

Fig. 6 shows a diagram of a specific embodiment of a first order sigma-delta modulator.

Fig. 7 shows a diagram of a specific embodiment of an interface circuit of the invention.

Figs. 8A and 8B show plots of the step responses for a case when the overdrive pulse is not clipped and a case when the overdrive pulse is clipped.

Figs. 8C and 8D show plots of the peak-to-peak ripple amplitude for all possible input digital values for two specific interface circuit implementations.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The interface circuit of the invention can be used for various applications to generate analog signals that control or interface to analog circuits. For example, the interface circuit can be used to generate analog control signals that are used in various control loops. The interface circuit can also be used to generate reference voltages, shaped waveforms, and other signals.

Fig. 1 shows a block diagram of an embodiment of a transceiver 100 for a communications system. The receiver and transmitter shown in Fig. 1 can be used for various applications, including cellular phone, HDTV, cable televisions, and others.

Within the received path, the transmitted signal (i.e., from a base station) is received by an antenna 112, routed through a duplexer 114, attenuated by a variable attenuator 116, and provided to a parallel combination of a low noise amplifier 118 and a switch 120. Depending on the required gain, the signal is either amplified by amplifier 118 or bypassed through switch 120. The signal from the output of amplifier 118 is then filtered by a filter 122 and provided to a second parallel combination of a low noise amplifier 124 and a switch 126. Again, depending on the required gain, the signal is either amplified by amplifier 124 or bypassed through switch 126. The signal from the output of amplifier 124 is then provided to a mixer 128 that downconverts the signal to an intermediate frequency (IF) using a local oscillator (LO) from a phase lock loop (PLL) circuit 130. The local oscillator is phase locked to a reference clock from a voltage-controlled-temperature-compensated crystal oscillator (VCTCXO) 132.

The IF signal from mixer 128 is filtered by a bandpass filter 134, amplified by a variable gain amplifier (VGA) 136, and provided to mixers 140a and 140b. Mixers 140a and 140b downconvert the IF signal with an in-phase sinusoidal from a phase shifter 142 and a quadrature sinusoid from a receiver IF phase lock loop (Rx IF PLL) 144, respectively. The baseband signal from each of mixers 140a and 140b is filtered by a lowpass filter 146, DC offset adjusted by a summer 148, and sampled by an analog-to-digital converter (ADC) 150. The

digital samples from ADCs 150a and 150b are provided to a signal processor 160 that processes the samples to generate the output data and the required control signals.

Within the transmit path, the transmit data samples from signal processor 160 are provided to digital-to-analog converters (DACs) 162a and 162b that generate the analog baseband signals corresponding to the data samples. The analog signals from each of DACs 162a and 162b is filtered by a filter 164 and provided to a mixer 166. Mixers 166a and 166b upconvert the filtered baseband signals to IF with the in-phase sinusoidal from a phase shifter 168 and a quadrature sinusoidal from a transmitter IF phase lock loop (Tx IF PLL) 170, respectively. The in-phase signal from mixer 166a and the quadrature signal from mixer 166b are summed by a summer 172. The resultant IF signal is amplified by a variable gain amplifier (VGA) 174, filtered by a filter 176, and upconverted by a mixer 178 with a second local oscillator signal from PLL 130. The radio frequency (RF) signal from mixer 178 is amplified by a driver 180 and further buffered by a power amplifier (PA) 182 that drives antenna 112 via duplexer 114.

Fig. 1 also shows various control loops within transceiver 100. For example, in the receive signal path, one or more gain control loops set the gains of attenuator 116 and VGA 136 (and can select between a bypass or a LNA path), a bias control loop sets the bias current of amplifiers 118 and 124, a frequency tracking loop sets the frequency of VCTCXO 132, and a DC offset loop attempts to null out the DC offset in the filtered signals from filters 146. In a specific implementation, filters 146 are active filters that provide high DC gain and can potentially generate large DC offsets in the filtered signals. The DC offsets loop removes the DC offset generated by filters 146 so that the offset compensated signals are within the input range of ADCs 150a and 150b. In the transmit signal path, a gain control loop sets the gain of VGA 174. Other transceiver implementations may include greater, fewer, or different control loops than that shown in Fig. 1.

As an example, consider the AGC loop that sets the gain of VGA 136 within the receive signal path to maintain the signal level for improved

signal-to-noise (SNR) performance. If the received signal is too high, the AGC loop reduces the VGA gain. Alternatively, if the received signal is too low, the AGC loop increased the VGA gain. The AGC loop adjusts the "desired" signal level (i.e., not the jammer signal level) such that it is approximately constant at the input of the ADCs. Otherwise, too high of a signal level would cause clipping by the ADCs and too low of a signal level would increase the noise level, both of which would result in reduction of SNR.

The control sections of the control loops are typically implemented within digital circuits (i.e., within signal processor 160). The digital control signals from the loop control circuits are then provided to interface circuits that generate the corresponding analog control signals used to drive the various elements shown in Fig. 1. Loop control theory and implementation of the loop control circuits are known in the art and not described herein.

Each transceiver design imposes a particular set of requirements on the performance of the interface circuits. These requirements typically include the response time and the amount of ripple on each of the control signals. For example, the bandwidth of the interface circuit generally needs to be much wider (i.e., three to ten times wider) than the closed loop bandwidth of the control loop. This is needed so that the interface circuit does not add excessive phase to the control loop and distort the loop response. Moreover, the ripples in the control signal behave as noise that degrades the performance of the control loop. The ripples need to be reduced to a predetermined amplitude that is defined by the requirement of the particular loop.

Fig. 2A shows a block diagram of a portion of a conventional control loop. A loop control circuit 210 generates a digital signal that is provided to an interface circuit 220. Within interface circuit 220, a pulse width modulator (PWM) or a "conventional" PDM 222 receives the digital signal and generates a sequence of waveforms corresponding to the values in the digital signal. A lowpass filter 224 receives and filters the waveforms to provide an analog control signal. Loop control circuit 210 in Fig. 2A can be the loop control circuit for any of the loops shown in Fig. 1 and described above.

Interface circuit 220 exhibits several disadvantages associated with conventional PWMs and PDMs. For each digital value in the digital signal, the PWM generates a particular waveform corresponding to that digital value. For a N-bit PWM, 2^N clock cycles are required to represent a N-bit value, resulting in PWM waveforms having a period of 2^N clock cycles. The number of high ("1") and low ("0") values for each waveform is determined by the input digital value. The high values from the PWM are typically grouped together. For example, a digital value of 128 corresponds to a PWM waveform that is high for the first 128 out of 512 clock cycles. This implementation results in an analog signal having a periodicity corresponding to the period of the PWM waveform, or a periodicity of 2^N clock cycles.

An important characteristic of pulse width and pulse density modulators is that the minimal amount of ripple occurs when the high values are uniformly spaced within the waveform. This is because the capacitor in the filter coupled to the modulator output would then have the same amount of time to charge and discharge each set of high and low values. When the high values are uniformly spaced, the overall minimum in the resulting voltage occurs just before the transition from low to high and the overall maximum occurs just before the high to low transition, resulting in a minimum amount of ripple at steady state. When the high values are not uniformly spaced, the capacitor would have asymmetric charge and discharge times, resulting in an increased steady state ripple amplitude.

Fig. 2B shows a block diagram of a portion of a control loop that includes an interface circuit of the invention. A loop control circuit 230 generates a digital signal that is provided to an interface circuit 240. Within interface circuit 240, a time response adjustment circuit 242 receives the digital signal and generates an "adjusted" signal having an adjusted time response, as will be described below. A sigma-delta modulator 244 receives the adjusted signal and generates a modulator signal that comprises a sequence of waveforms corresponding to the values in the adjusted signal. A lowpass filter 246 receives and filters the waveforms to provide an analog signal.

To reduce cost and minimize the number of components required to implement the interface circuit, some elements of the interface circuit are implemented in digital hardware (i.e., within signal processor 160) and some are implemented using analog components. Since the circuit elements to be controlled are typically analog in nature, the analog components provide the required signal conditioning to generate an analog signal from a digital signal. In an implementation, time response adjustment circuit 242 and sigma-delta modulator 244 are integrated within a digital IC that also provides other functionality required by the system.

Fig. 3A shows a diagram of a specific embodiment of an interface circuit 310 of the invention. Interface circuit 310 includes a time response adjustment circuit 312, a first order sigma-delta modulator 314, and a second order lowpass filter 316. The digital signal is provided to time response adjustment circuit 312 that generates an adjusted signal. In an embodiment, the adjusted signal includes modifications to the digital signal that provide a faster or modified response time.

Within time response adjustment circuit 312, the digital signal x[n] is provided to a gain element 320 and a delay element 322. Gain element 320 scales the digital signal by a scaling factor (Av) that can be fixed or programmable. In a specific embodiment, the scaling factor is two. Delay element 322 delays the digital signal by a time period that can also be fixed or programmable. The scaling factor and the amount of delay are dependent on the requirements of the particular application in which interface circuit is used. The scaled signal from gain element 320 and the delayed signal from delay element 322 are provided to a summer 324 that subtracts the delayed signal from the scaled signal. In an embodiment, summer 324 is a saturation summer that limits the output to N-bit values, which fall within the input range of the subsequent sigma-delta modulator 314. The adjusted signal y[n] from summer 324 is provided to sigma-delta modulator 314.

Within sigma-delta modulator 314, the adjusted signal is provided to a summer 330 that adds the adjusted signal with the N least significant bits (LSBs) from a register 332. The (N+1)-bit output from summer 330 is provided

to and stored by register 332. The most significant bit (MSB) from register 332 comprises the modulator signal k[n] that is provided to filter 316. As shown in the embodiment in Fig. 3A, both delay element 322 and register 332 are clocked by the same clock signal (CLK).

Filter 316 filters the modulator signal from modulator 314 to generate the analog signal. In the embodiment shown in Fig. 3A, filter 316 is a second order lowpass filter comprising two resistors and two capacitors.

Fig. 3B shows a diagram of another specific embodiment of a time response adjustment circuit 342a. Interface circuit 342a includes a gain element 350, a delay element 352, and a summer 354 that correspond to gain element 320, delay element 322, and summer 324 of interface circuit 312 in Fig. 3A. Interface circuit 342a further includes a second gain element 356 having a gain of (Av-1) and coupled between the circuit input and delay element 352. Gain element 356 provides the proper gain such that the adjusted signal y[n] from summer 354 is equal to the digital signal x[n] after the delay period $M \bullet T_s$ provided by delay element 352.

Fig. 3C shows a diagram of yet another specific embodiment of a time response adjustment circuit 342b. Interface circuit 342b includes gain element 350, delay element 352, and summer 354 of Fig. 3B. Interface circuit 342b further includes a second summer 358 having an non-inverting input coupled to the output of gain element 350 and an inverting input coupled to the circuit input. Interface circuit 342b provides the same transfer function as that of Fig. 3B.

Time Response Adjustment Circuit

The waveforms from a PWM, PDM, or sigma-delta modulator are digital in nature and are filtered by an analog filter to provide the desired analog signal. Conventionally, the step response of the analog signal due to a step change in the digital signal is determined by the analog filter. A filter having a wide bandwidth provides a faster response time but results in larger ripple amplitude in the analog signal. Thus, the filter is typically set at the highest possible bandwidth that results in an acceptable ripple amplitude (i.e.,

meeting the ripple specification). The response time associated with this filter bandwidth then represents the fastest possible response time achievable by the interface circuit.

For some applications, such as control loops having wide loop bandwidths, the response time achieved with conventional interface circuits is not acceptable. For example, referring to Fig. 1, driver 180 in the transmit AGC loop is controlled by a digital signal having fast transition time. As driver 180 is switched between a low gain state and a high gain state, the gain in the signal path changes and needs to be compensated by adjusting the gain of VGA 174. If the Tx AGC control signal has a slow response time (i.e., because of the limitations imposed by the analog filter providing this control signal), then the response times of driver 180 and VGA 174 are not "matched". The mismatch results in a bump in the signal gain when the gain of driver 180 is switched.

Fig. 4A shows a plot of a step response of a conventional interface circuit. The digital signal transitions from a starting value to a final value at a time t_1. The output of the filter, in response, begins transitioning from the starting value (V_{start}) shortly after t_1 and asymtotically approaches (V_{final}). At a time t_3, the digital signal again changes and the filter then responds accordingly.

Fig. 5 shows a diagram of a specific embodiment of a time response adjustment circuit 512 of the invention. For a particular filter, the response time can be increased (or made faster) by temporarily overdriving the modulator with a signal (or a pulse) generated by the time response adjustment circuit. Within time response adjustment circuit 512, the digital signal is provided to a gain element 520 and a delay element 522. In the embodiment shown in Fig. 5, gain element 520 scales the digital signal x[n] by a scaling factor of two and delay element 522 delays the digital signal by M cycles of the clock signal (CLK). The scaling factor and the delay period can also be made programmable. The scaled signal from gain element 520 and the delayed signal from delay element 522 are provided to a saturation summer 524 that subtracts the delayed signal from the scaled signal. Summer 524 limits the adjusted signal y[n] to N-bit values.

In a specific embodiment, the digital signal x[n] is in unsigned binary (i.e., having a range of 0 to 512 for a 9-bit implementation). In another specific embodiment, the digital signal x[n] is in two's complement (i.e., having a range of -256 to 255 for a 9-bit implementation). The digital signal x[n] changes at a much slower rate than the clock signal (CLK) used to clock the delay element and the subsequent modulator. For example, for a 9-bit modulator the digital signal changes at 1/512 the rate of the clock signal, or slower.

Time response adjustment circuit 512 operates in the following manner. For a predetermined delay period of $M \bullet T_s$, where M is the number of clock cycles of delay and T_s is the period of the clock signal (CLK), the adjusted signal y[n] from time response adjustment circuit 512 is:

$$y[n] = 2x[n] - x[n-M], \text{ or} \quad \text{Eq (1)}$$

$$y[n] = x[n] + (x[n] - x[n-M]), \quad \text{Eq (2)}$$

where x[n-M] is the digital signal delayed by M clock periods. For a particular n, y[n] is greater than or equal to x[n]. In fact, y[n] is (x[n]-x[n-M]) greater than the current digital value of x[n] during this delay period. At the conclusion of the delay period, once the current digital value of x[n] is provided from delay element 522, the output from summer 524 becomes y[n] = x[n]. Response time adjust circuit 512 thus generates an "overdrive" pulse train p[n] having the same amplitude as the step change (i.e., $p[n] = \Delta x[n] = x[n] - x[n-M]$). Each overdrive pulse has a duration of $M \bullet T_s$ that is determined by the delay element.

The filter coupled to the time response adjustment circuit via the modulator responds to the difference between the current and the previous input value (i.e., y[n] - y[n-1]). Time response adjustment circuit 512 effectively doubles the filter drive during the delay period from (y[n] - y[n-1]) = (x[n] - x[n-1]) to (y[n] - y[n-1]) = 2•(x[n] - x[n-1]). This higher y[n] results in more drive to the filter, which speeds up the response time. At the conclusion of the delay

period, after $M \bullet T_s$ time, time response adjustment circuit 512 has no effect on the input digital value and y[n] becomes x[n].

Fig. 4B shows a plot of a step response of an interface circuit that employs time response adjustment circuit 512. Initially, the adjusted signal transitions from a starting value to a new value at time t_1. However, as shown in Fig. 4B, the modulator is overdriven by time response adjustment circuit 512 to an adjusted value corresponding to $(2V_{final} - V_{start})$, which is twice the change of the digital signal x[n-M]. The analog signal from the filter, shortly after t_1, begins transitioning from the starting value (V_{start}) toward $(2V_{final} - V_{start})$ and reaches V_{final} at a faster rate. As the analog signal approaches V_{final} at time t_4, the overdrive pulse is removed and the adjusted signal returns to a value corresponding to V_{final}. The filter then transitions to its final value V_{final}. As shown in Fig. 4B, the overdrive pulse has an amplitude equal to the change in input value ($\Delta V = V_{final} - V_{start}$) and a duration of $(t_4 - t_1)$.

For some changes in the input digital signal, the amplitude of the overdrive pulse is the same as the change in the digital signal (i.e., $p[n] = \Delta x[n] = x[n] - x[n-M]$), as shown in Fig. 4B. This result occurs when there is adequate headroom from the current digital value to provide an overdrive pulse having an amplitude of ($p[n] = \Delta x[n]$). Specifically, if ($x[n-M] + 2\Delta x[n]$) falls within the input range of the modulator, then the amplitude of the overdrive pulse is equal to the step change. For all changes in the digital signal that meet this condition, the amount of improvement in the response time is (theoretically) the same.

However, because of the saturation performed by summer 524 to maintain the adjusted signal y[n] within the valid input range of the subsequent circuit (e.g., the sigma-delta modulator), the amplitude of the overdrive pulse is less than $\Delta x[n]$ for some changes in the digital signal. This occurs when there is inadequate headroom from the current value of x[n] to provide an overdrive pulse having an amplitude of $\Delta x[n]$. The overdrive pulse is then clipped by an amount related to the available headroom. When the pulse amplitude is clipped, the response time is not as fast as when the pulse amplitude is not clipped. To further improve (i.e., speed up) the response time, the duration of the overdrive pulse can then be increased. In an embodiment, the duration of

the overdrive pulse is increased (from the nominal pulse duration of M) in accordance with the amount of clipping. For example, a pulse that is clipped by half (i.e., $p[n] = 0.5 \bullet \Delta x[n]$) would have a longer duration than that of a pulse that is clipped by a quarter (i.e., $p[n] = 0.75 \bullet \Delta x[n]$).

Figs. 8A and 8B show the effects of clipping on the step response in the analog signal. Fig. 8A shows a plot of the step response for a case when the overdrive pulse is not clipped and Fig. 8B shows a plot of the step response for a case when the overdrive pulse is clipped. For the specific implementation corresponding to Fig. 8A, when the overdrive pulse is not clipped, the duration of the overdrive pulse is 112 chipx8 or 11.4 μsec, and the step response time to 70% of final value is approximately 10 μsec. For the same implementation, when the overdrive pulse is clipped by 100 percent (i.e., no overdrive pulse is provided), the step response time to 70% of final value is approximately 24 μsec. As noted above, the step response time can be improved by increasing the duration of the overdrive pulse when clipping occurs.

As shown in Figs. 3 and 5, the response time can be controlled by adjusting the gain of the gain element or the delay of the delay element, or both. For a particular gain, if the delay is too short, a shorter overdrive pulse is generated and the time response adjustment circuit has less impact on the response time. When the delay is zero (M=0), the output of the time response adjustment circuit is simply x[n] and has no impact. To speed up the response time, the delay is increased as much as possible. However, if the delay is made too long, too much overdrive may cause the analog signal to overshoot the final value, which may be an undesirable result for many applications. The delay that results in the fastest possible response time without overshoot can be determine empirically, by simulation, or by calculation.

Similarly, for a particular delay period $M \bullet T_s$, if the gain of the gain element is small (i.e., close to one), a smaller overdrive pulse is generated and the time response adjustment circuit has less impact on the response time. When the gain is set to one, the time response adjustment circuit has no impact on the response time.

In an embodiment, the gain element and the delay element are both programmable. In another embodiment, the gain delay is adjusted based on the amount of change in the digital signal. For example, a higher gain or a longer delay, or both, is used for a large change and a lower gain or a shorter delay, or both, is used for a smaller change. In yet another embodiment, each change in the input digital signal can be associated with a set of programmed gain and delay values that results in the fastest response time without overshoot.

Figs. 3 and 5 show one embodiment of the time response adjustment circuit of the invention. The time response adjustment circuit can be implemented with digital circuit. The time response adjustment circuit can also be implemented with a memory element such as a random access memory (RAM) or a read only access memory (ROM). For a particular change in digital value, the memory element provides a sequence of values that provides the desired time response characteristics (i.e., the fastest response time without overshoot).

Although the time response adjustment mechanism of the invention has been described as being implemented using digital circuit, the invention can also be implemented in software or microcode that is executed by a processor (i.e., signal processor 160). Also, the time response adjustment mechanism has been described for a specific application in which an overdrive pulse is generated to obtain faster response time. The time response adjustment mechanism of the invention can be used for other applications, such as to "waveshape" the time response to achieve a particular waveform characteristic. Thus, the time response adjustment mechanism of the invention is intended to cover any and all modifications to the time response characteristics of the analog signal as generated by a conventional modulator and filter combination.

Sigma-Delta Modulator

The sigma-delta modulator provides a modulator signal k[n] comprising a sequence of high and low values (i.e., a sequence of output waveforms) corresponding to the adjusted signal y[n] at its input. The high

values are uniformly distributed in the output waveforms. This characteristic results in smaller ripple amplitude because the capacitor in the filter coupled to the modulator would have the same amount of time to charge and discharge each set of high and low values.

Fig. 6 shows a specific embodiment of a first order sigma-delta modulator 600. The N-bit adjusted signal y[n] is provided to a summer 612 that sums this signal with the N least significant bits (LSBs) from a register 614. The most significant bit (MSB) from adder 612 is provided to a first input of an exclusive-OR (XOR) gate 616 and the N LSBs from adder 612 are provided to and stored by register 614. A polarity control signal (Polarity) is provided to a second input of XOR gate 616. XOR gate 616 toggles the polarity of the MSB from summer 612 depending on the state of the polarity control signal (e.g., high=toggle and low=no toggle). The output from XOR gate 616 is provided to a register 618 that synchronizes the output with the clock signal (CLK). The output from register 618 comprises the modulator signal from sigma-delta modulator 600.

Sigma-delta modulator 600 uniformly distributes the spacing between the high values to provide improved steady state ripple performance over that of conventional PDMs. Analysis indicates that sigma-delta modulator 600, with nine bits of resolution (N=9), can reduce the worse case peak-to-peak ripple amplitude by a factor of approximately three.

Sigma-delta modulator 600, in addition to spreading the ripple energy uniformly in frequency by oversampling, also noise shapes the ripple energy by utilizing feedback. Through noise shaping, a large portion of the ripple energy is moved to higher frequencies and filtered by the subsequent filter, thereby resulting in less ripple in the unfiltered lower frequencies of interest. Noise shaping by sigma-delta modulator 600 is shown by the following expression:

$$K(z) = z^{-1}Y(z) + \left(1 - z^{-1}\right)E_Q(z) \ , \qquad \text{Eq (3)}$$

where Y(z), K(z), and $E_Q(z)$ are the z-transforms of the modulator input, the modulator output, and the quantization error, respectively. The modulator transfer function ($H_Y(z) = K(z)/Y(z)$) is given by:

$$H_Y(z) = z^{-1}, \quad \text{Eq (4)}$$

and the quantization error function ($H_E(z) = K(z)/E_Q(z)$) is given by:

$$H_E(z) = \left(1 - z^{-1}\right). \quad \text{Eq (5)}$$

Since z^{-1} becomes 1 at DC frequency and -1 at $f_{CLK}/2$, the quantization error function $H_E(z)$ provides zero gain (or infinite attenuation) at DC frequency, large attenuation at lower frequencies, and relative amplification at higher frequencies. The quantization noise is effectively moved from lower frequencies to higher frequencies where filtering is more easily achieved.

A single order sigma-delta modulator outputs a particular waveform for each valid input digital value. Each waveform has a particular ripple characteristic based on the placement of the high and low values in the waveform.

Figs. 8C and 8D show plots of the peak-to-peak ripple amplitude for all possible input digital values for two specific interface circuit implementations. As shown in Fig. 8C, the sigma-delta modulator has 9 bits of resolution. It can be noted that the ripple amplitude varies depending the input digital value, and is higher near the extreme values of 0 and 511. For input values of 5 through 508, the worse case ripple amplitude is 1.7 mV in Fig. 8C. The ripple amplitude can be reduced by providing additional filtering (i.e., lowering the bandwidth of the filter coupled to the sigma-delta modulator). For the same interface circuit implementation as for Fig. 8C, when the filter bandwidth is reduced by shifting the poles from p_1 = 9.33 kHz and p_2 = 54.34 kHz down to p_1 = 624 Hz and p_2 = 32.48 kHz, the worse case ripple amplitude decreases to 300 μV.

The ripple performance is a function of the type of modulator, the bandwidth of the lowpass filter, and also the speed of the modulator clock. It

can be shown that the amount of ripple in the analog signal from a second order RC-RC filter, for ripples of less than 100% of one LSB, follows the following relationship:

$$ripple\ as\ \%\ of\ step\ size \approx 480\% \bullet \left(\frac{2^N \bullet f_c}{f_{CLK}} \right)^2, \qquad \text{Eq (6)}$$

or equivalently,

$$ripple\ as\ \%\ of\ full\ scale \approx 480\% \bullet 2^N \left(\frac{f_c}{f_{CLK}} \right)^2, \qquad \text{Eq (7)}$$

where f_c is the corner frequency of the filter. From these relationships, it follows that speeding up the clock frequency (f_{CLK}) of the sigma-delta modulator results in a corresponding reduction in the amount of ripple. The improvement in ripple performance can then be traded for faster response time, by increasing the bandwidth of the analog filter.

Although the invention is described in conjunction with a first order sigma-delta modulator, higher order sigma-delta modulators (i.e., second or third order modulator) can also be used. Generally, higher order sigma-delta modulators push more in-band quantization noise to higher frequencies where filtering may be more easily performed. If the order of the sigma-delta modulator is higher than the order of the analog filter, the out-of-band quantization noise may not be adequately filtered and the analog signal may contain high amounts of out-of-band noise that may degrade the performance of the system. The order of the sigma-delta modulator is selected in light of the order of the analog filter used.

The time response adjustment circuit of the invention can provide improved performance when used in conjunction with a sigma-delta modulator. However, the time response adjustment circuit can also be used in combination with a PWM, a PDM, or an M-bit DAC.

Analog Filter

A single order lowpass filter is typically used to filter the modulator signal from the modulator. The single order filter can be implemented with a single resistor and a single capacitor. Although the single order filter results in a low component count, the response time and ripple performance is not satisfactory for some applications.

In conjunction with the invention, a second order or higher order filter can be used to provide faster response time or smaller amount of ripple, or both, on the analog signal. The improvement in performance with a second order lowpass filter over a single order lowpass filter is described below. In a specific embodiment, the second order filter is implemented as a RC-RC filter having two resistors and two capacitors, as shown in Fig. 3A. This implementation is only slightly more complex than the single order RC filter but provides much improved performance when used in combination with the time response adjustment circuit of the invention.

With a first order RC filter, over much of the range of operation (i.e., for frequencies higher than the frequency of the pole of the filter, $f_P = \frac{1}{RC}$), ripple is proportional to the cutoff frequency f_p of the RC filter. This results from the fact that the magnitude of the frequency response of the RC filter falls off as $1/f$ beyond the pole frequency. The ripple on the analog signal has a lowest fundamental frequency equal to the periodicity of the waveform, or $f_{ripple} = \frac{f_{CLK}}{2^N}$, where f_{CLK} is the frequency of the clock signal used to clock the modulator.

The general transfer function of a second order lowpass filter can be expressed as:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \qquad \text{Eq (8)}$$

where the poles are given by:

$$p_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}\,. \qquad \text{Eq (9)}$$

For a second order RC-RC lowpass filter shown in Fig. 3A, $\zeta > 1$, both poles p_1 and p_2 are real, and the transfer function reduces to:

$$H(s) = \frac{p_1 p_2}{(s - p_1)(s - p_2)}\,. \qquad \text{Eq (10)}$$

For a second order filter having two poles, the frequency response of the filter falls off as $1/f$ between the frequencies of the first and second poles, and as $1/f^2$ after the frequency of the second pole. By selecting the frequencies of the two poles to be lower than the ripple components (i.e., f_{p1} and $f_{p2} < f_{ripple}$), the ripple is attenuated by 40 dB/decade slope, which is faster than a slope of 20 dB/decade achieved with a first order filter. The improvement in ripple can then be traded for improvement in the response time of the filter. Stated differently, to meet a particular ripple requirement, the poles of the second order filter can be increased higher than that of the single order filter, thereby resulting in a faster response time without sacrificing ripple performance.

Referring to equation (8), the natural frequency ω_n controls the time scale of the second order filter. The desire for smaller ripple amplitude and faster response time poses conflicting requirements on this parameter. For a second order filter, a critically damped condition results in the fastest step response without overshoot. For a second order filter, the critically damped condition occurs for $\zeta = 1$ which results in the poles being located at the same position on the real axis (or $p_1 = p_2$).

In an application that requires fast response time for a specified ripple amplitude, the RC-RC filter can be designed to approach the critically damped condition (i.e., ζ as close to 1 as possible), and the natural frequency ω_n is increased as high as allowed by the specified ripple performance. Analysis indicates that by using a second order critically damped filter, the response time of the filter can be sped up by a factor of approximately ten over

that of a single order filter for a ripple amplitude specification of 30% of an LSB. The response time improvement is even greater for smaller specified ripple amplitude.

Further improvements in the response time may be achieved through the use of even higher order filters (e.g., third order, fourth order, or higher order).

Fig. 3A shows a filter implementation comprising only resistors and capacitors. Filters using other reactive components (e.g., inductors) can also be designed. For example, a second order filter can be designed using a single inductor and a single capacitor. LC filters provide additional flexibility since the damping ζ for these filters can take on all values, unlike RC filters that are limited to $\zeta > 1$. Thus, an LC filter can be designed to be under-damped (i.e., having $\zeta < 1$) to provide even faster response time with some overshoot. The filter can also be implemented as an active filter in the manner known in the art. The various filter implementations are within the scope of the invention.

Specific Implementation of an Interface Circuit

Fig. 7 shows a diagram of a specific embodiment of an interface circuit 710 of the invention that is used, for example, for the transmitter AGC loop for a CDMA cellular phone. Interface circuit 710 includes a time response adjustment circuit 712, a first order sigma-delta modulator 714, and a second order lowpass filter 716.

Within time response adjustment circuit 712, the digital signal x[n] is provided to a gain element 720 and a register 722. Gain element 720 scales the digital signal by a scaling factor of two to generate 2x[n]. Register 722 latches the digital signal x[n] after a period of delay as determined by the delay value on the bus (Delay_Val). Register 722 retains the old value until the new value is latched. A counter 726 is loaded with the delay value and provides an enable signal for register 722 after the delay period indicated by the delay value. The scaled signal from gain element 720 and the delayed signal from delay element 722 are provided to a summer 724 that subtracts the delayed signal

from the scaled signal. Summer 724 is a saturation summer that generates an adjusted signal y[n] having N bit values that fall within the input range of sigma-delta modulator 714. The adjusted signal is provided to sigma-delta modulator 714.

Sigma-delta modulator 714 is similar in implementation to the modulator shown in Fig. 6, with N=9. Lowpass filter 716 filters the modulator signal from modulator 714 to generate the analog signal. In the embodiment shown in Fig. 7, lowpass filter 716 is a second order RC-RC filter, similar to that shown in Fig. 3A.

Many cellular phones operate in more than one operating mode. For example, dual-band cellular phones are capable of operation in either digital mode or analog mode. The digital mode can be characterized by the transmission of a code division multiple access (CDMA) signal or a time division multiple access (TDMA) signal such as a Global System for Mobil Communication (GSM) signal. The analog mode can be characterized by the transmission of a frequency modulated (FM) signal or an amplitude modulated (AM) signal.

Often, the requirements for the digital mode and the analog mode are different. For example, fast response time is required in digital (e.g., CDMA) mode and lower ripple amplitude is required for analog (e.g., FM) mode. Consequently, the bandwidth of the analog filter is wider for digital mode in order to achieve faster response time and more narrow for analog mode in order to obtain lower ripple amplitude. Cellular phones that operate in both modes are required to meet the specifications of both modes, and the combined requirements can complicate the design of dual-mode phones.

As shown in Fig. 7, filter 716 includes an additional capacitor 748 coupled in series with a switch 750, the combination of which is coupled in parallel with a capacitor 746. In digital mode when wider bandwidth is required for faster response time, switch 750 is opened and capacitor 748 is not part of the RC-RC filter. In analog mode when a narrower bandwidth is required for smaller ripple amplitude, switch 750 is closed and capacitor 748 is coupled in parallel with capacitor 746 to provide more capacitance. In a specific

embodiment, the following values are selected for the resistors and capacitors: R1 = R2 = 1 KΩ, C1 = 10 nF, C2 = 5nF (for CDMA mode), and C3 = 120 nF (for FM mode). With this implementation, the same basic RC-RC filter (R1 = R2 = 1 KΩ, C1 = 10 nF, C2 = 5 nF) is used for both modes and the additional capacitor 748 (C3 = 120 nF) is switched in parallel with capacitor 746 for the analog mode. Switch 750 can be implemented with a bipolar transistor, a metal-oxide-semiconductor (MOS) gate, or other circuit elements.

Different time response characteristics can also be achieved, in part, by selecting the appropriate frequency for the modulator clock (f_{CLK}). In a specific implementation, f_{CLK} = 19.6608 MHz for CDMA mode and f_{CLK} = 19.68 MHz for FM mode, for a 9-bit modulator implementation. For an AGC control loop, the lowest fundamental frequency ($f_{CLK}/512$) is typically 38.4 KHz for both CDMA and FM modes. The poles of second order RC filters are selected such that these RC-RC filters provide adequate ripple attenuation to meet the ripple specifications. For FM mode, the ripple specifications are typically more difficult to meet, and the FM RC-RC filter is designed to provide more attenuation. Thus, the poles of the FM RC-RC filter are set at lower frequencies (e.g., p_1 = 624 Hz and p_2 = 32.48 kHz) so that the ripple fundamentals are at frequencies higher than p_1 and p_2, and are attenuated at 40 dB/decade. For CDMA mode, the constraints on ripple filtering are more relaxed, allowing p_1 and p_2 to be set at higher frequencies (e.g., p_1 = 9.33 kHz and p_2 = 54.34 kHz). The lowest fundamental located between p_1 and p_2 is attenuated at 20 dB/decade and the remaining ripple fundamentals at frequencies greater than p_1 and p_2 are attenuated at 40 dB/decade.

The foregoing description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. For example, the invention can also be used to provide shaped step response and other characteristics. Thus, the present invention is not intended to be

limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

1. An interface circuit comprising:

a time response adjustment circuit that receives a digital signal and generates an adjusted signal;

a modulator coupled to the time response adjustment circuit to receive the adjusted signal and generate a modulator signal; and

a filter coupled to the modulator to receive the modulator signal and generate an analog signal,

wherein the analog signal has a time response that is modified by the time response adjustment circuit.

2. The circuit of claim 1 wherein the time response adjustment circuit generates an overdrive pulse corresponding to a change in the digital signal.

3. The circuit of claim 2 wherein the overdrive pulse has an amplitude twice that of the change in the digital signal.

4. The circuit of claim 2 wherein the overdrive pulse has an amplitude determined by a magnitude of the change in the digital signal.

5. The circuit of claim 2 wherein the overdrive pulse has a time duration determined by a magnitude of the change in the digital signal.

6. The circuit of claim 2 wherein the overdrive pulse is clipped to within a input range of the modulator.

7. The circuit of claim 6 wherein a time duration of the clipped overdrive pulse is lengthened in accordance with an amount of clipping.

8. A circuit of claim 1 wherein the modulator is a sigma-delta modulator.

9. A circuit of claim 8 wherein the sigma-delta modulator is first order.

10. A circuit of claim 1 wherein the filter is a second order RC lowpass filter.

11. A control loop comprising the interface circuit of claim 1.

12. A receiver comprising the interface circuit of claim 1.

13. An interface circuit comprising:

a time response adjustment circuit that receives a digital signal and generates an adjusted signal, time response adjustment circuit including

a gain element that receives and scales the digital signal by a scaling factor,

a delay element that receives and delays the digital signal by a time delay, and

a summer coupled to the gain element and the delay element;

a modulator coupled to the time response adjustment circuit to receive the adjusted signal and generate a modulator signal; and

a filter coupled to the modulator to receive the modulator signal and generate an analog signal, wherein the analog signal has a time response that is modified by the time response adjustment circuit.

14. The circuit of claim 13 wherein the scaling factor is two.

15. The circuit of claim 13 wherein the time delay is determined by a value on a control signal.

16. The circuit of claim 13 wherein the time delay is determined, in part, based on a magnitude of a change in the digital signal.

17. The circuit of claim 13 wherein the scaling factor and the time delay are programmable.

18. A circuit of claim 13 further comprising:

an exclusive-OR gate that receives the modulator signal and a polarity signal and generates a modulator signal having a correct polarity,

wherein the filter receives the modulator signal having the correct polarity.

19. An method for modifying a time response of an analog signal comprising:

receiving a digital signal;

generating an adjusted signal based on the digital signal and changes in the digital signal;

generating a modulator signal based on the adjusted signal;

filtering the modulator signal to obtain an analog signal,

wherein the analog signal has a time response that is modified.

20. The method of claim 22 wherein the time response of the analog signal is modified by adjustment of a frequency of a clock signal used to clock the modulator.

21. The method of claim 22 wherein the time response of the analog signal is modified by adjustment of a bandwidth of the filter.

22. The method of claim 19 wherein the time response of the analog signal is modified based on changes in magnitude of the digital signal.

23. The method of claim 22 wherein the time response of the analog signal is further modified based on time delay and scaling factor of the time response adjustment circuit.

24. The method of claim 19 wherein the adjusted signal includes overdrive pulses corresponding to changes in the digital signal.

25. A receiver comprising:

a variable gain element;

a gain control loop that sets a gain of the variable gain element, the gain control loop including

a loop control circuit that generates a digital control signal,

a time response adjustment circuit coupled to the loop control signal to receive the digital control signal and generate an adjusted signal,

a modulator coupled to the time response adjustment circuit to receive the adjusted signal and generate a modulator signal,

a filter coupled to the modulator to receive the modulator signal and generate an analog control signal,

wherein the gain of the variable gain element is adjusted in accordance with the analog control signal.

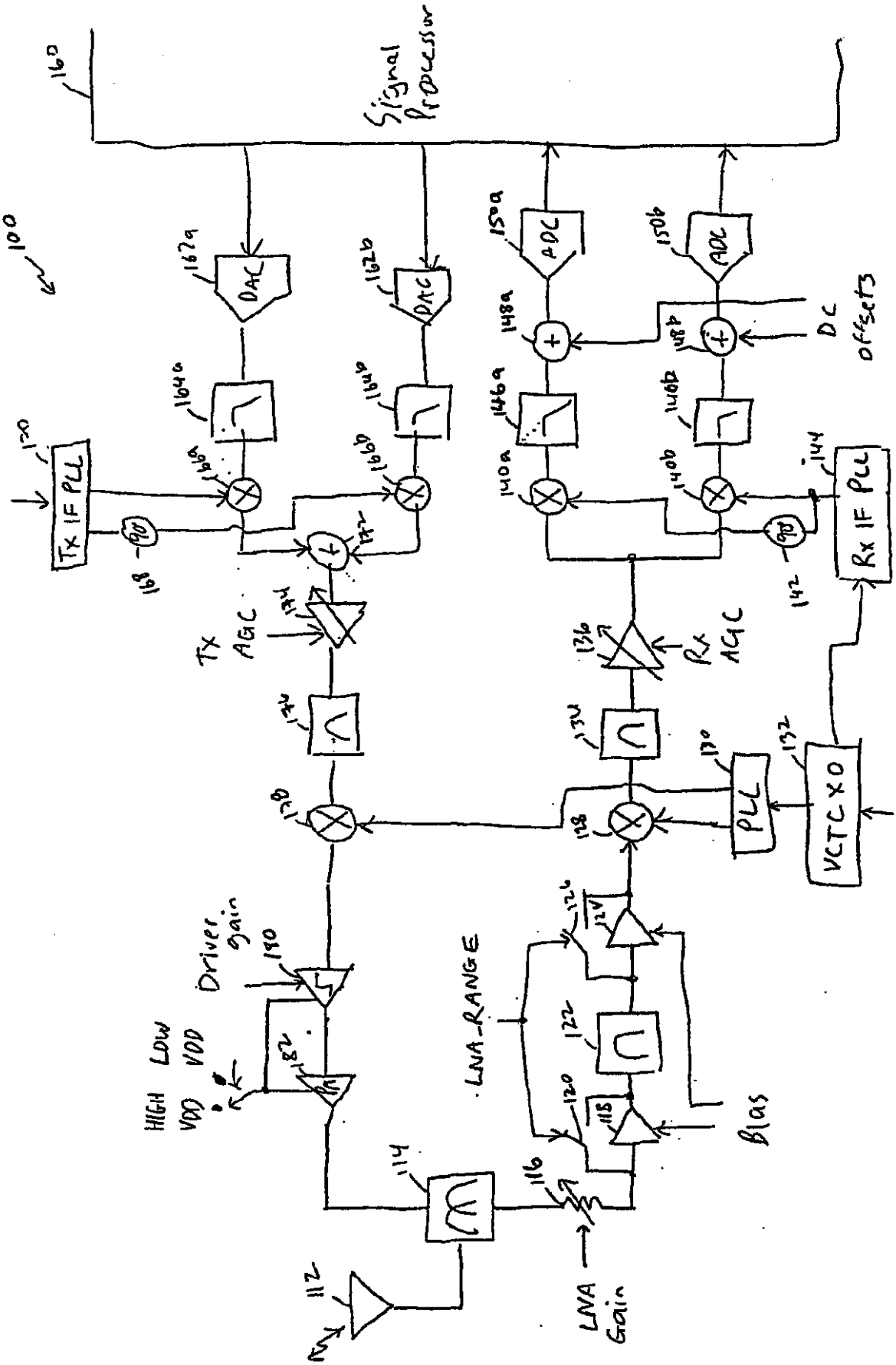
160
Signal Processor
100
162a
DAC
162b
DAC
150a
ADC
150b
ADC
148a
148b
DC offsets
164a
164b
146a
146b
140a
140b
130
TX IF PLL
168
144
Rx IF PLL
142
166
TX AGC
134
136
Rx AGC
138
132
PLL
VCTCXO
Freq. Track
190
Driver gain
HIGH VDD
LOW VDD
187
LNA_RANGE
176
174
122
120
118
Bias
114
116
112
LNA Gain

FIG. 1

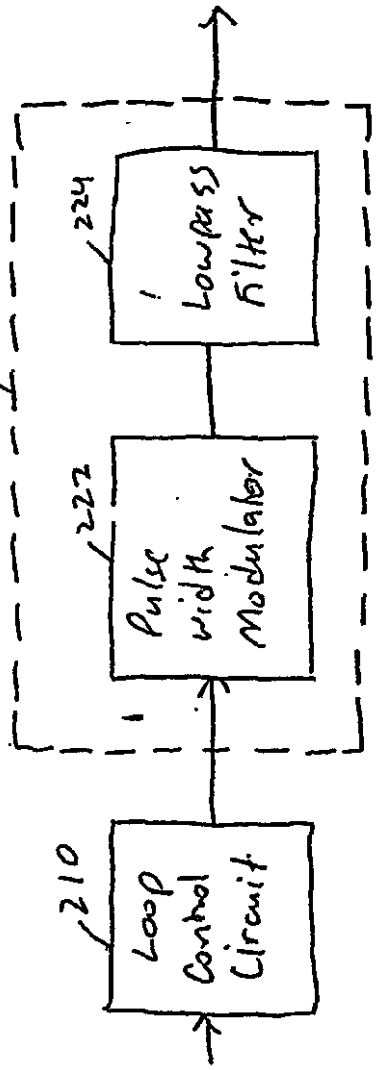
220
224
Lowpass Filter
222
Pulse width Modulator
210
Loop Control Circuit

FIG. 2A

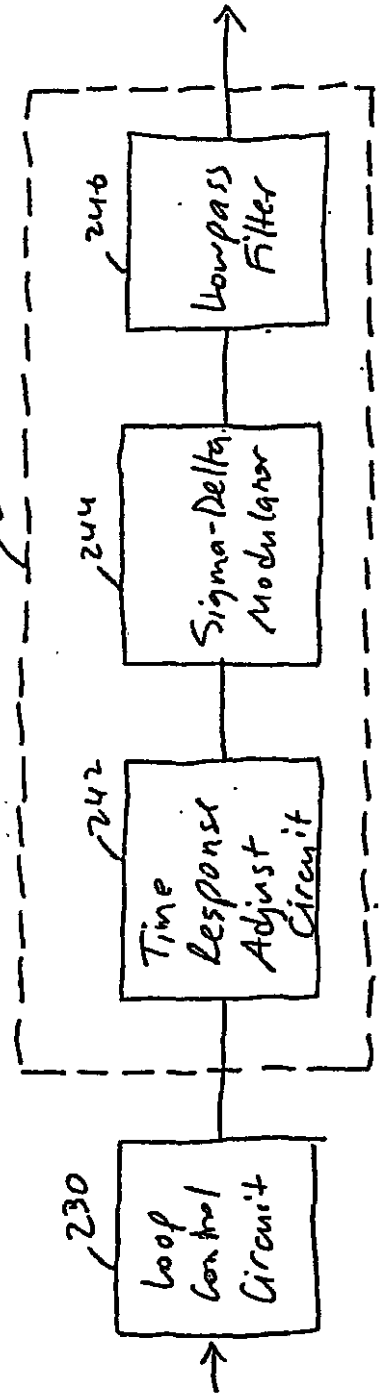
240
246
Lowpass Filter
244
Sigma-Delta Modulator
242
Time Response Adjust Circuit
230
Loop Control Circuit

FIG. 2B

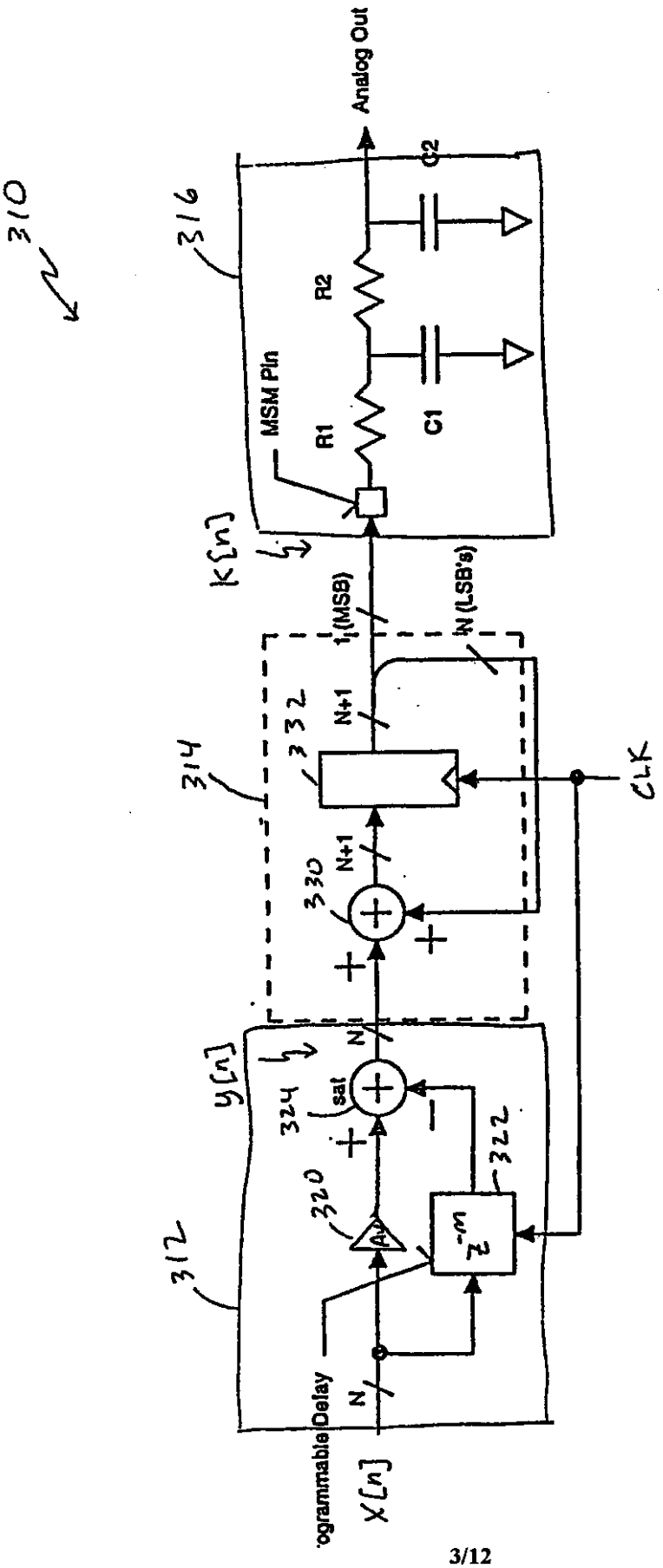
310
316
Analog Out
C2
R2
C1
R1
MSM Pin
K[n]
314
N+1
332
N (LSB's)
i_1(MSB)
CLK
330
N+1
y[n]
N
324
sat
322
320
312
Programmable Delay
N
X[n]

FIG. 3A

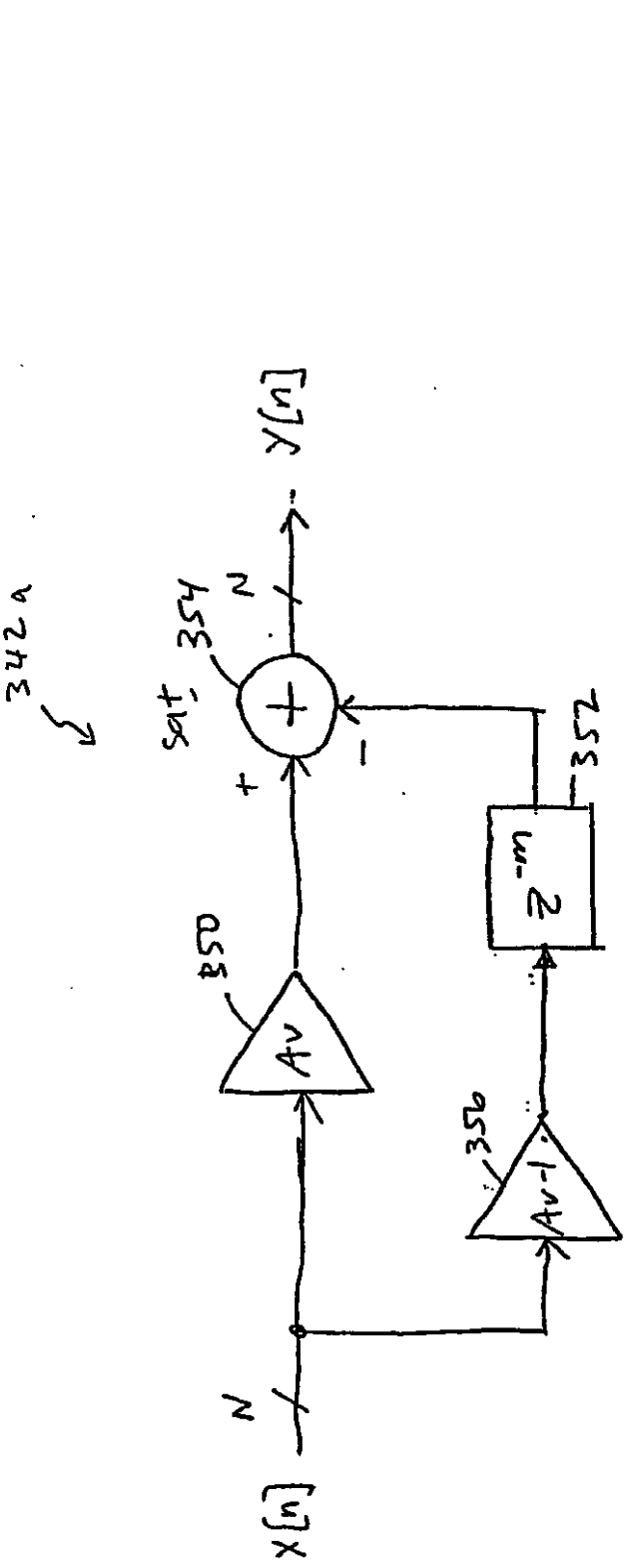
342a
Sat.
354
N
y[n]
+
-
352
z^{-m}
350
Av
356
Av-1
N
x[n]

FIG. 3B

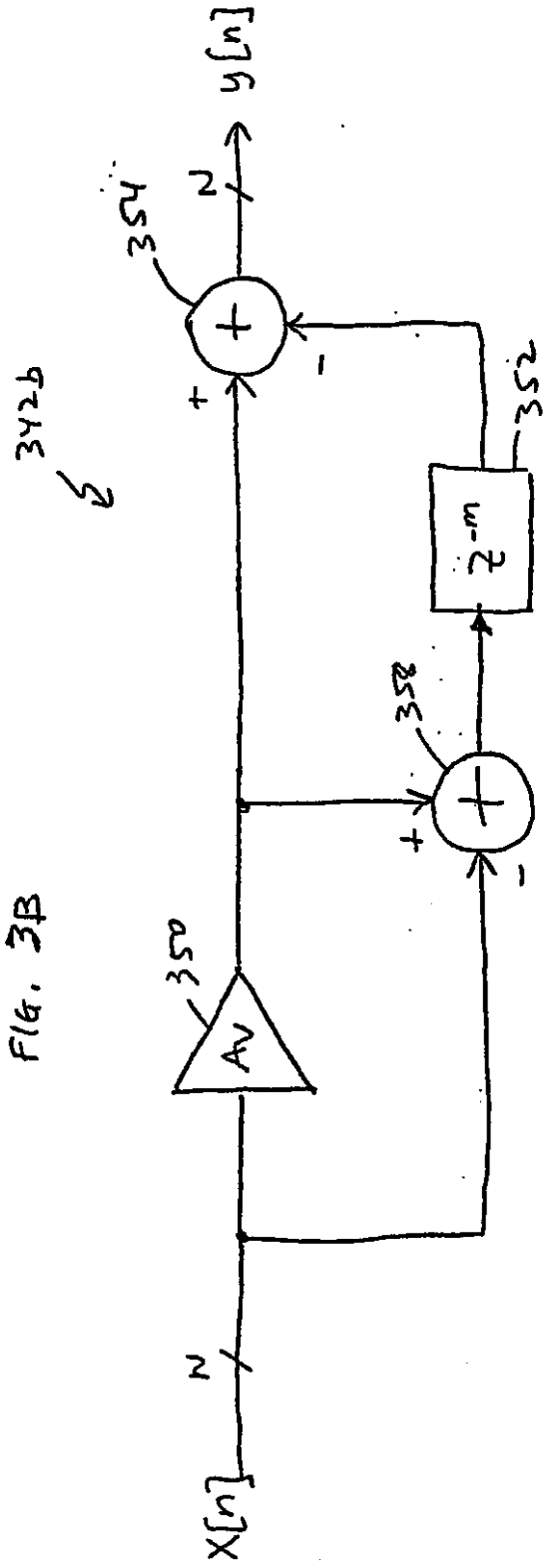
342b
354
N
y[n]
+
-
352
z^{-m}
358
+
-
350
Av
N
x[n]

FIG. 3C

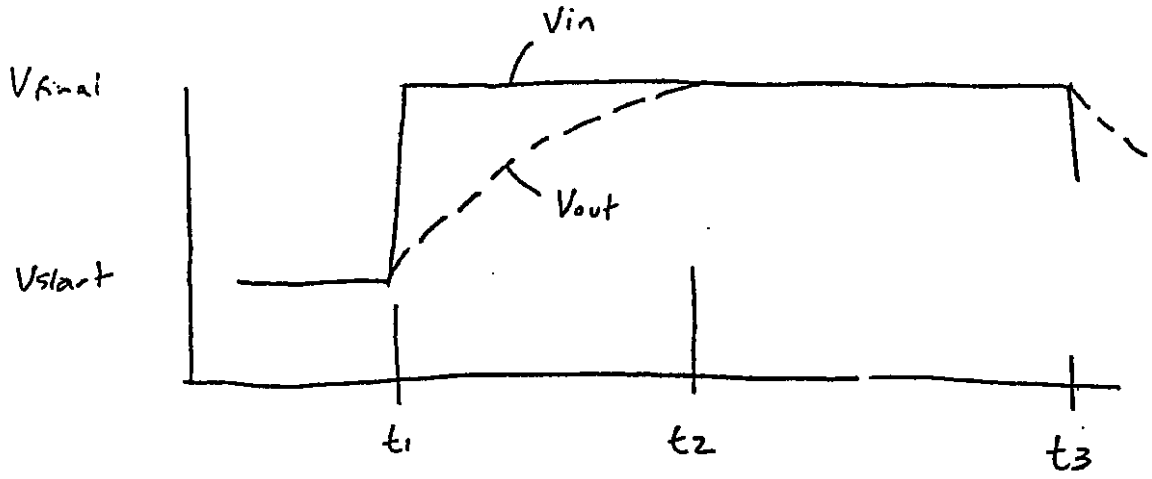
Vin
Vfinal
Vout
Vstart
t1
t2
t3

FIG. 4A

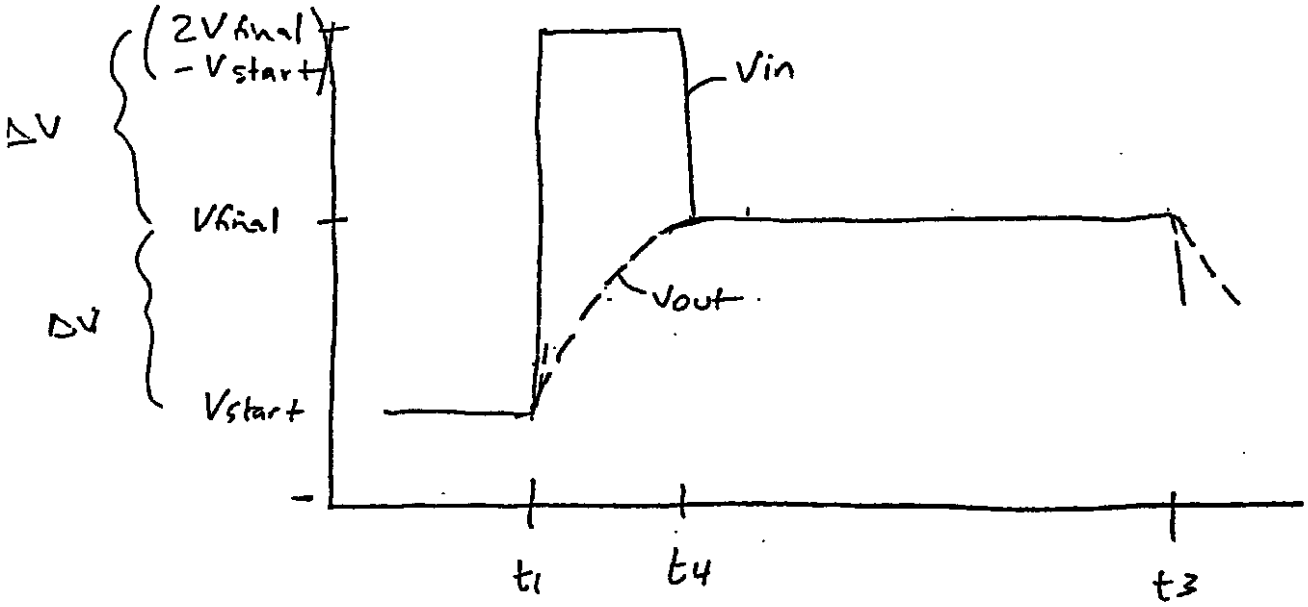
(2Vfinal
-Vstart)
ΔV
Vin
Vfinal
Vout
ΔV
Vstart
t1
t4
t3

FIG. 4B

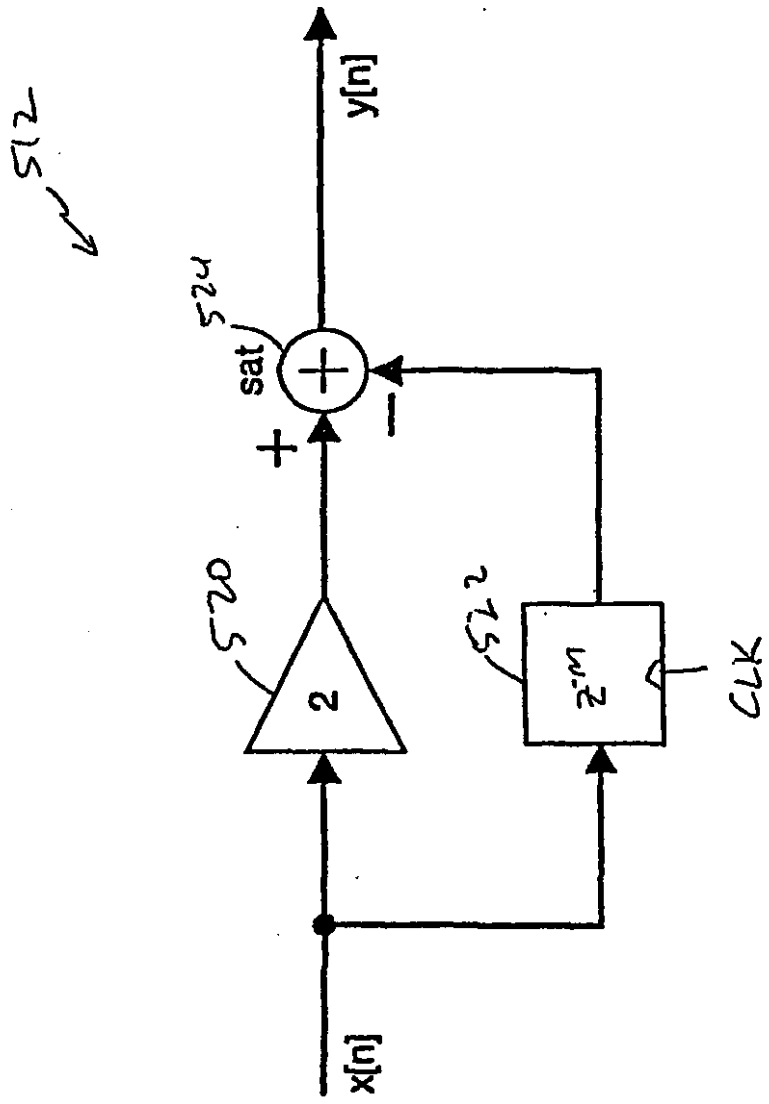

FIG. 5

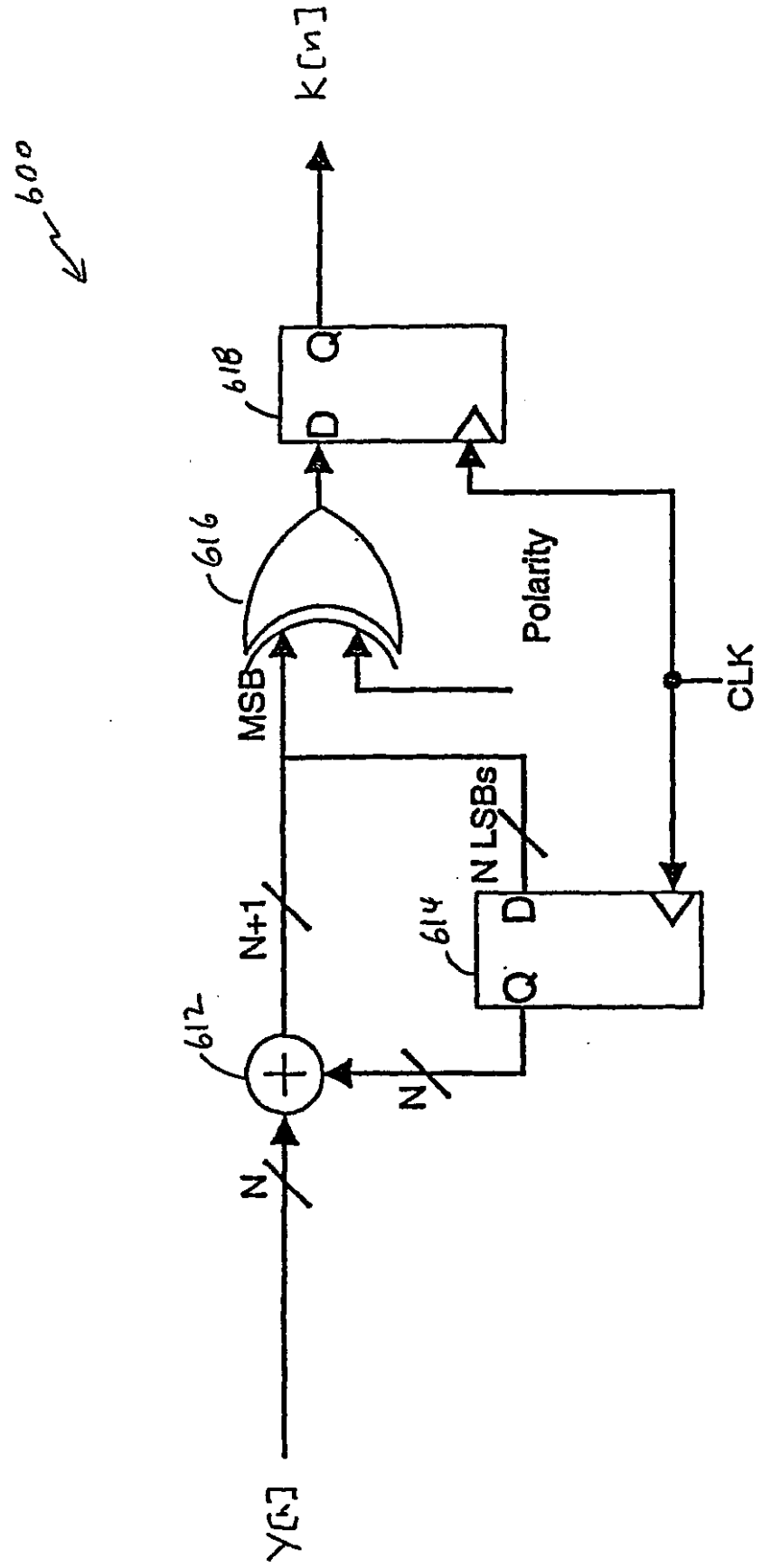

FIG. 6

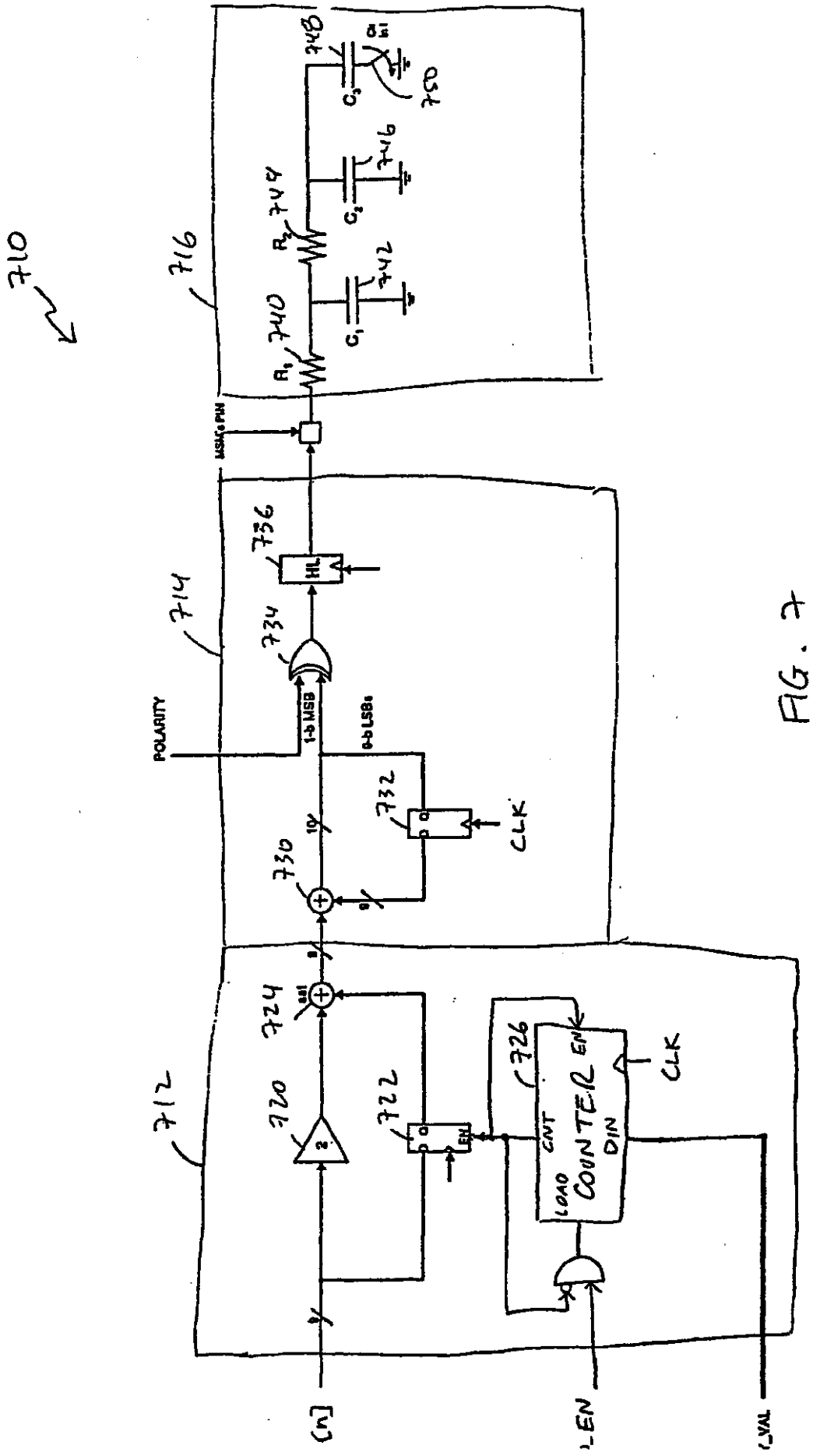
710
716
748
746
742
740
R2
R1
C2
C1
MSB to PWM
736
HL
734
714
POLARITY
1-b MSB
6-b LSBs
732
CLK
730
724
720
722
EN
726
CNT
LOAD
COUNTER
DIN
CLK
712
[n]
LEN
LVAL

FIG. 7

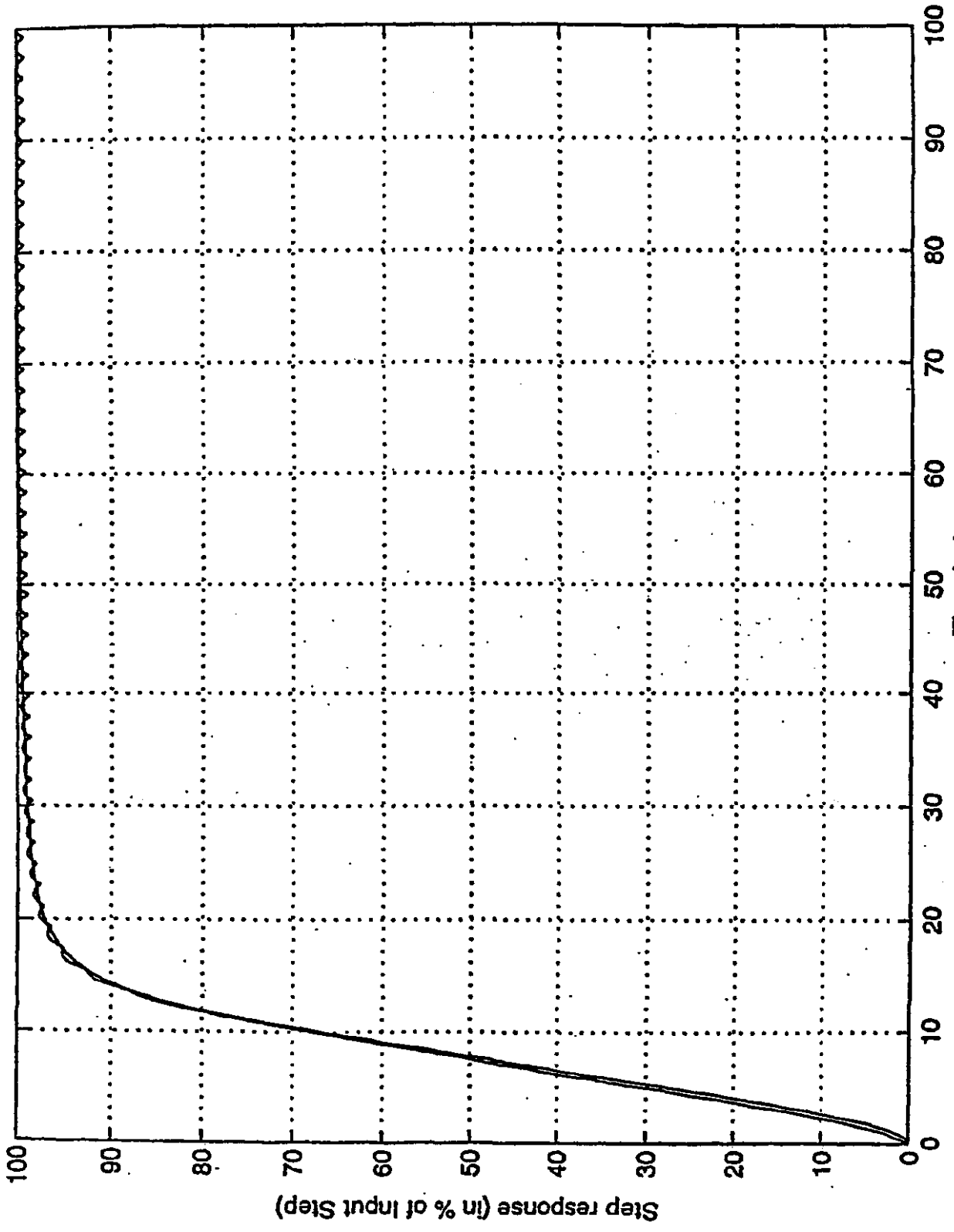
Step response (in % of input Step)
Time (us)
0
10
20
30
40
50
60
70
80
90
100

FIG. 6A

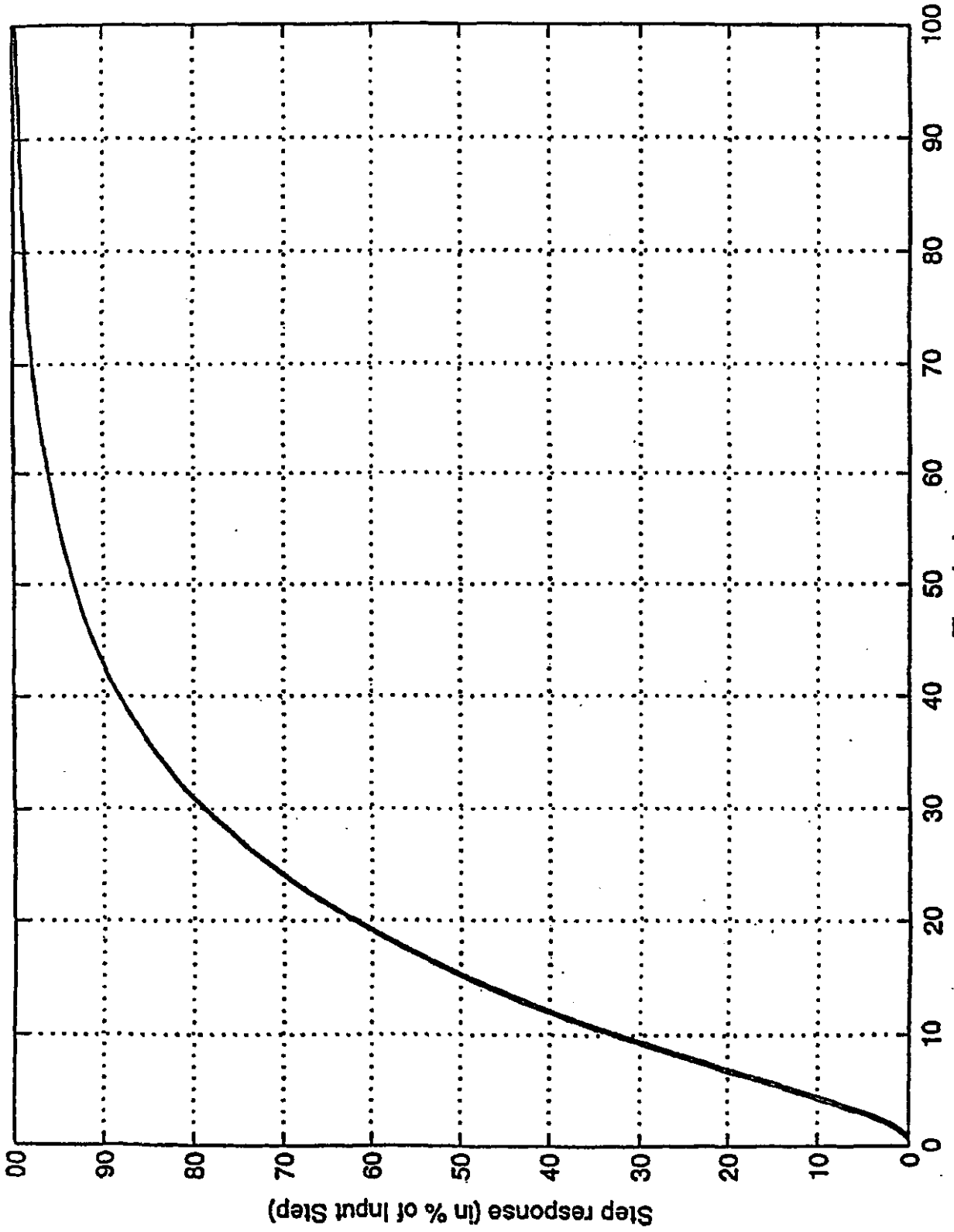
Step response (in % of Input Step)
0
10
20
30
40
50
60
70
80
90
100
Time (us)
0
10
20
30
40
50
60
70
80
90
100

FIG. 8B

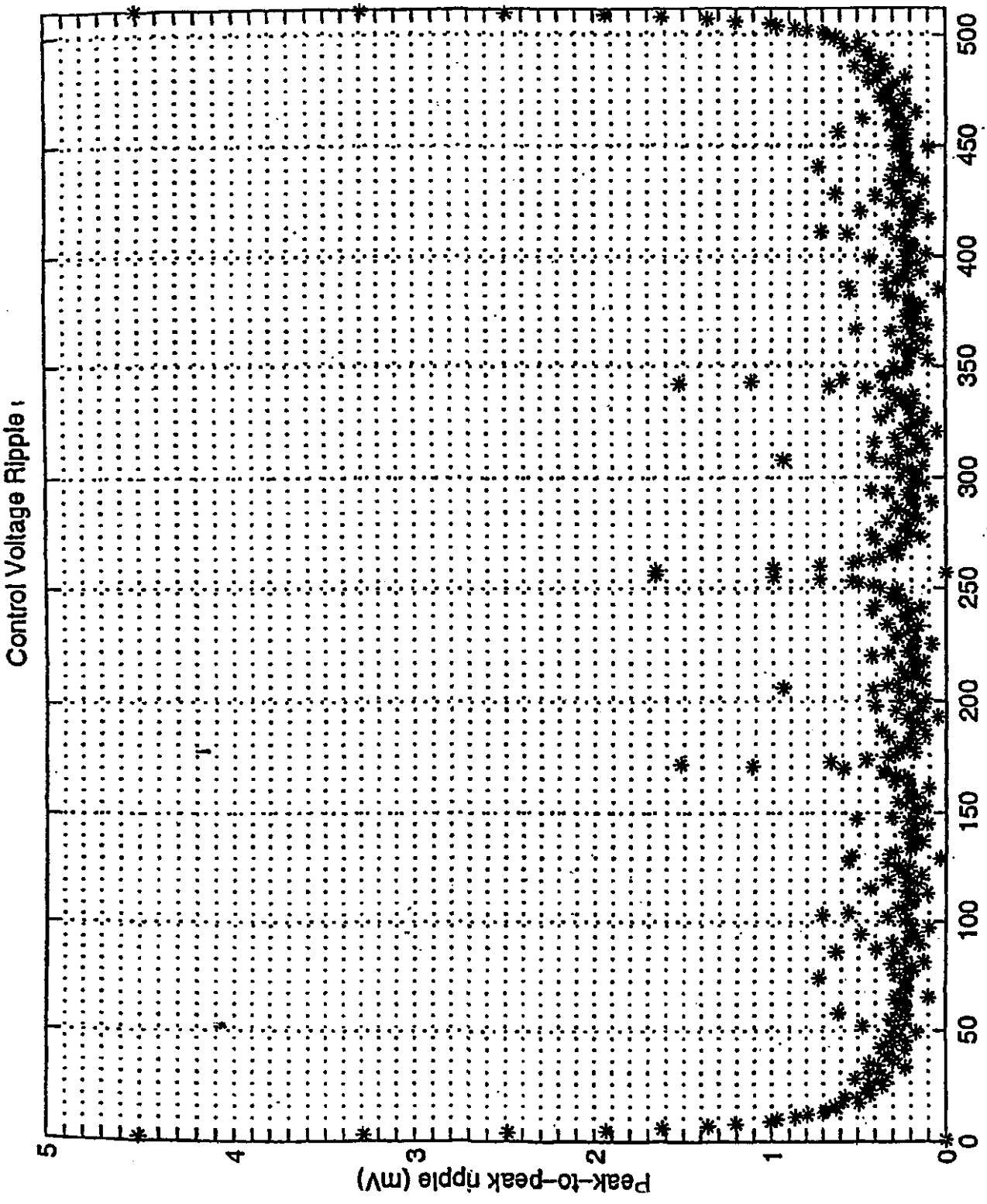
Control Voltage Ripple
Peak-to-peak ripple (mV)
Input Code
0
1
2
3
4
5
0
50
100
150
200
250
300
350
400
450
500

FIG. 8C

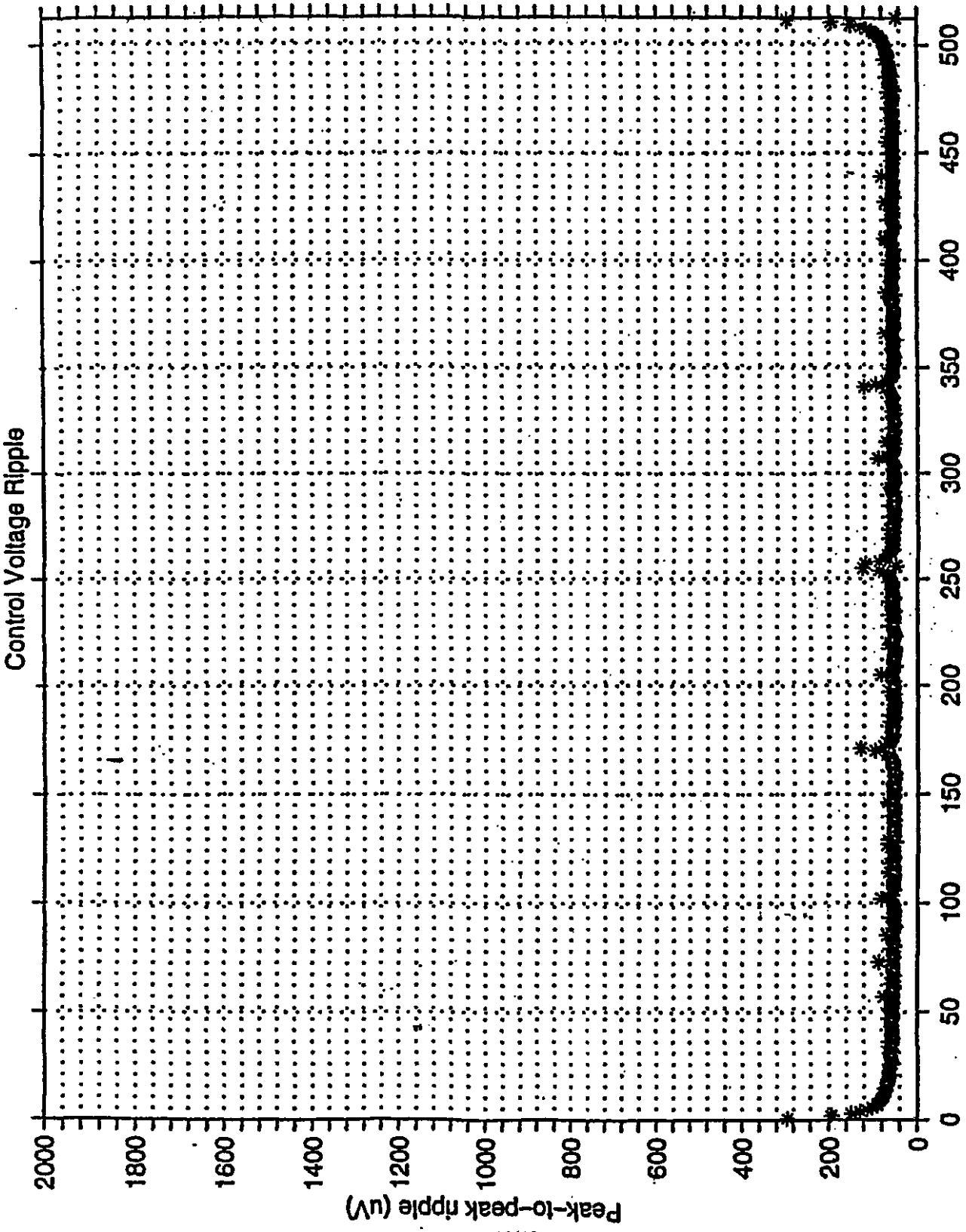
Control Voltage Ripple
Peak-to-peak ripple (uV)
Input Code
0
50
100
150
200
250
300
350
400
450
500
200
400
600
800
1000
1200
1400
1600
1800
2000

FIG. 8D

[19] 中华人民共和国国家知识产权局

[51] Int. Cl[7]
H03G 3/30

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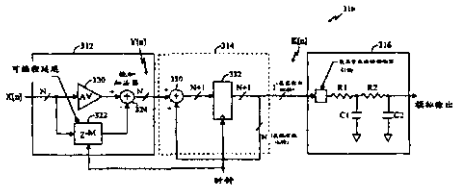
权利要求书 3 页 说明书 17 页 附图 12 页

[54] 发明名称 具有可调整的时间响应的数字－模拟接口电路

[57] 摘要

一种用于将数字信号转换成模拟信号的接口电路。 所述接口电路包括时间响应调整电路、调制器以及滤波器。 所述时间响应调整电路接收数字信号并产生经调整的信号。 所述调制器耦合至所述时间响应调整电路，接收所述经调整的信号并产生调制器信号。 所述滤波器耦合至所述调制器，接收所述调制器信号并产生模拟信号。 所述模拟信号具有由所述时间响应调整电路调整的时间响应。 在一个实施例中，所述时间响应调整电路包括放大元件、延迟元件以及加法器。 所述放大元件接收并以缩放因子缩放所述数字信号。 所述延迟元件接收并以时间延迟延迟所述数字信号。 所述加法器耦合至所述放大元件和所述延迟元件，将来自所述放大元件的经缩放的信号和来自所述延迟元件的经延迟的信号相加以产生经调整的信号。



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1．一种接口电路，其特征在于包括：

接收数字信号并产生经调整的信号的时间响应调整电路；

耦合至所述时间响应调整电路以接收所述经调整信号并产生调制器信号的调制器；以及

耦合至所述调制器以接收所述调制器信号并产生模拟信号的滤波器，

其中所述模拟信号具有经所述时间响应调整电路调整的时间响应。

2．如权利要求 1 所述的电路，其特征在于所述时间响应调整电路产生相应于数字信号中的变化的过度激励脉冲。

3．如权利要求 2 所述的电路，其特征在于所述过度激励脉冲具有所述数字信号中的变化 2 倍的幅度。

4．如权利要求 2 所述的电路，其特征在于所述过度激励脉冲具有由所述数字信号中的变化的幅度所确定的幅度。

5．如权利要求 2 所述的电路，其特征在于所述过度激励脉冲具有由所述数字信号中的变化的幅度所确定的持续时间。

6．如权利要求 2 所述的电路，其特征在于所述过度激励脉冲限幅于所述调制器的输入范围之内。

7．如权利要求 6 所述的电路，其特征在于根据限幅量而增长所述经限幅的过度激励脉冲的持续时间。

8．如权利要求 1 所述的电路，其特征在于所述调制器是Σ-Δ调制器。

9．如权利要求 8 所述的电路，其特征在于所述Σ-Δ调制器是一阶的。

10．如权利要求 1 所述的电路，其特征在于所述滤波器是二阶 RC 低通滤波器。

11．一种控制回路，其特征在于包括权利要求 1 的接口电路。

12．一种接收机，其特征在于包括权利要求 1 的接口电路。

13．一种接口电路，其特征在于包括：

接收数字信号并产生经调整信号的时间响应调整电路，所述时间响应调整电路包括

接收并以缩放因子缩放所述数字信号的放大元件；

接收并以时间延迟延迟所述数字信号的延迟元件；

耦合至所述放大元件和所述延迟元件的加法器；

耦合至所述时间响应调整电路以接收所述经调整信号并产生调制器信号的调制器；以及

耦合至所述调制器以接收所述调制器信号并产生模拟信号的滤波器，其中所述模拟信号具有经所述时间响应调整电路修改的时间响应。

14．如权利要求 13 所述的电路，其特征在于所述缩放因子是 2。

15．如权利要求 13 所述的电路，其特征在于所述时间延迟由控制信号上的值确定。

16．如权利要求 13 所述的电路，其特征在于部分地根据所述数字信号中的变化的幅度确定所述时间延迟。

17．如权利要求 13 所述的电路，其特征在于所述缩放因子和所述时间延迟是可编程的。

18．如权利要求 13 所述的电路，其特征在于进一步包括：

接收所述调制器信号以及极性信号并产生具有正确极性的调制器信号的“异或”门，

其中所述滤波器接收具有所述正确极性的调制器信号。

19．一种用于修改模拟信号的时间响应的方法，其特征在于包括：

接收数字信号；

根据所述数字信号以及所述数字信号中的变化产生经调整的信号；

根据所述经调整的信号产生调制器信号；

对所述调制器信号进行滤波以获得模拟信号，

其中所述模拟信号具有经修改的时间响应。

20．如权利要求 22 所述的电路，其特征在于由用于对所述调制器计时的时钟信号的频率的调整而修改所述模拟信号的时间响应。

21．如权利要求 22 所述的电路，其特征在于由所述滤波器的带宽的调整修改所述模拟信号的时间响应。

22．如权利要求 19 所述的电路，其特征在于根据所述数字信号的幅度中

的变化修改所述模拟信号的时间响应。

23. 如权利要求 22 所述的电路，其特征在于根据所述时间响应调整电路的时间延迟和缩放因子进一步修改所述模拟信号的时间响应。

24. 如权利要求 19 所述的电路，其特征在于所述经调整的信号包括相应于所述数字信号中的变化的过度激励脉冲。

25. 一种接收机，其特征在于包括：

可变增益元件；

设置所述可变增益元件的增益的增益控制回路，所述增益控制回路包括

产生数字控制信号的回路控制电路，

耦合至所述回路控制信号以接收所述数字控制信号并产生经调整的信号的时间响应调整电路，

耦合至所述时间响应调整电路以接收所述经调整信号并产生调制器信号的调制器，

耦合至所述调制器以接收所述调制器信号并产生模拟控制信号的滤波器，

其中根据所述模拟控制信号调整所述可变增益元件的增益。

具有可调整的时间响应的数字-模拟接口电路

相关申请对照

本申请与本申请同一天申请的美国专利申请序列号（未知）名为“TRANSMITTER ARCHITECTURE FOR COMMUNICATION SYSTEMS”的申请相关，并在此引用作为参考。

发明背景

本发明涉及电子电路，尤其涉及提供具有可调整的时间响应的模拟信号的接口电路。

数字-模拟接口电路通常用于许多电子电路中，以提供驱动模拟电路元件的模拟信号。所述接口电路典型地使用脉宽调制（PWM）或脉冲密度调制（PDM）接收来自数字电路的数字信号并产生对应的经滤波的中间信号来提供所述模拟信号。所述 PWM 或 PDM 充当所述数字和模拟电路间的接口。

常规的 PWM 或 PDM 接收包括 N 比特数字值序列的数字信号并对每个值产生对应的波形。每个波形具有预定的周期并且包括由所述输入数字值决定的若干高（“1”）和低（“0”）的值。例如，对于 9 比特 PWM 或 PDM，所述输入数字信号值可从 0 到 511 变动并且每个波形有 512 个时钟周期的周期并包括 0 至 511 个高值。例如，输入数字值 128 对应于具有 128 个高值以及 384 个低值的波形。对于 PWM，所述高值在每个波形的起始处集中在一起，而对于 PDM，所述高值有些随机地分散于所述波形之中。为了实现的简易性，一些 PDM 以伪随机方式而不是均匀地散布所述高值。所述波形本质上是数字的，并经滤波以产生所述模拟信号。

所述接口电路的一个普通应用是用于控制回路中。例如，对于通信系统中的接收机或发射机，所述接口电路可用于载波跟踪回路、比特定时回路、自动增益控制（AGC）回路、偏置控制回路、功率控制回路、直流（DC）偏移调整回路以及其它。对于这些回路的每一个，回路控制电路产生提供给与该

回路相关联的接口电路中的 PWM 或 PDM 的数字控制信号。所述 PWM 或 PDM 根据所述数字控制信号中的值产生波形序列。对所述波形滤波以产生用于驱动受控元件（如压控振荡器、可变增益放大器、加法元件等等）的模拟控制信号。

连同所述 PWM 或所述 PDM 所产生的所述模拟控制信号一般要求满足各种技术要求。典型的技术要求包括关于控制信号的阶跃输入的响应时间（即稳定时间）以及波纹振幅。对于许多应用快速响应时间和少量的波纹是想要的（或所要求的）。所述快速响应时间考虑到宽带宽控制回路并对输入条件中的急剧变化迅速响应。所述控制信号上的波纹对应于噪声，并且较好的性能一般要求少量的波纹。然而，快速响应时间和少量波纹是相冲突的设计考虑。优化快速响应时间常导致控制信号上的大幅度波纹。

如能看出的那样，具有可调整的时间响应（即提供较快速的响应时间）而保持小波纹幅度的接口电路是非常想要的。

发明概述

本发明提供了产生具有可调时间响应的模拟信号，并在模拟信号上引入最小的额外波纹（如果有的话）的数字-模拟接口电路。所述接口电路包括时间响应调整电路，该电路接收数字信号，修正（或调整）所述数字信号来获得想要的时间响应特性（即较快响应时间），并将所调整的信号提供给后面的电路将所调整的信号转换成模拟信号。例如，为了提供较快响应时间，所述时间响应调整电路能对应于所述数字信号中的改变而加入过度激励脉冲。所述过度激励脉冲为后面的滤波器提供额外的激励，该滤波器依次又加速了滤波响应。

本发明的一个详细实施例提供了用于将数字信号转换成模拟信号的接口电路。所述接口电路包括时间响应调整电路、调制器以及滤波器。所述时间响应调整电路接收数字信号并产生经调整的信号。所述调制器耦合至所述时间响应调整电路，接收所述调整信号并产生调制器信号。所述滤波器耦合至所述调制器，接收所述调制器信号并产生模拟信号。所述模拟信号具有由所述时间响应调整电路修正的时间响应。在一个实施例中，所述时间响应调整

电路包括放大元件、延迟元件以及加法器。所述放大元件接收并以缩放因子缩放所述数字信号。所述延迟元件接收并以时间延迟延迟所述数字信号。所述加法器耦合至所述放大元件和所述延迟元件。所述加法器从经缩放（或放大）的信号中减去所述经延迟的信号来产生经调整的信号。

本发明的另一详细实施例提供了用于修正模拟信号的时间响应的方法，该方法包括：（1）接收数字信号；（2）根据所述数字信号和所述数字信号中的变化产生经调整的信号；（3）根据所述调整信号产生调制器信号；以及（4）对所述调制器信号进行滤波以获得模拟信号。所述模拟信号具有例如根据所述数字信号的幅度的变化而修正的时间响应。所述修正表现在所述调整的信号中，并可包括例如与所述数字信号中的变化对应的过度激励脉冲。

本发明能用于各种应用，例如包括接收机或发射机的控制回路。

当参考下面的说明、权利要求和附图时，上述描述和本发明的其它方面将变得更清楚。

附图简述

图 1 示出了通信系统的收发机的实施例的框图。

图 2A 和 2B 分别示出了常规控制回路的一部分和包括本发明的接口电路的控制回路的一部分的框图。

图 3A 示出了本发明的接口电路的详细实施例的框图。

图 3B 和 3C 示出了时间响应调整电路的两个详细实施例的框图。

图 4A 和 4B 分别示出了常规接口电路和使用本发明的时间响应调整电路的接口电路的阶跃响应曲线。

图 5 示出了本发明的时间响应调整电路的详细实施例的图。

图 6 示出了一阶Σ-Δ（累积-增量）调制器的详细实施例的图。

图 7 示出了本发明的接口电路的详细实施例的图。

图 8A 和 8B 示出了对于不限幅所述过度激励脉冲的情况和限幅所述过度激励脉冲的情况的阶跃响应的曲线。

图 8C 和 8D 示出了两个详细接口电路实现的对于所有可能的输入数字值的峰一峰波纹幅度曲线。

详细实施例的说明

本发明的接口电路可用于各种应用来对模拟电路产生控制或接口的模拟信号。例如，可以使用所述接口电路来产生用于各种控制回路的模拟控制信号。所述接口电路还可用于产生参考电压、整形波形以及其它信号。

图 1 示出了通信系统的收发机 100 的实施例的框图。图 1 中示出的接收机和发射机可用于各种应用，包括蜂窝网电话机、HDTV、有线电视以及其它。

在接收通路中，经发送的信号（即来自基站）由天线 112 接收，通过双工器 114 传送，由可变衰减器 116 衰减并提供到并联组合的低噪声放大器 118 和开关 120。根据所要求的增益，所述信号或者由放大器 118 放大或者通过开关 120 旁路。然后，来自放大器 118 的输出的信号由滤波器 122 滤波并提供给第 2 个并联组合的低噪声放大器 124 和开关 126。同样地，根据所要求的增益，所述信号或者由放大器 124 放大或者通过开关 126 旁路。来自放大器 124 的输出的信号然后提供给混频器 128，使用来自锁相环（PLL）电路 130 的本地振荡器（LO）将所述信号下变频成中频（IF）。所述本地振荡器相位锁定到来自压控温度补偿晶体振荡器（VCTCXO）132 的参考时钟上。

来自混频器 128 的中频信号由带通滤波器 134 滤波，经可变增益放大器（VGA）136 放大并提供给混频器 140a 和 140b。混频器 140a 和 140b 用分别来自移相器 142 的同相正弦信号和来自接收机中频锁相环（Rx IF PLL）144 的正交正弦信号对所述中频信号进行下变频。来自每个混频器 140a 和 140b 的基带信号由低通滤波器 146 滤波，由加法器 148 进行直流偏移调整，并由模拟－数字转换器（ADC）150 进行采样。来自 ADC 150a 和 150b 的数字采样提供给信号处理器 160，处理所述采样产生输出数据和所要求的控制信号。

在发射通路中，来自信号处理器 160 的发送数据采样提供给数字-模拟转换器（DAC）162a 和 162b，产生对应于所述数据采样的模拟基带信号。来自 DAC 162a 和 162b 的每一个的模拟信号有滤波器 164 滤波并提供给混频器 166。混频器 166a 和 166b 用分别来自移相器 168 的同相正弦信号和来自发射机中频锁相环（Tx IF PLL）170 的正交正弦信号将所述滤波的基带信号上变频成中频信号。来自混频器 166a 的同相信号和来自混频器 166b 的正交信号由加法器 172 相加。所产生的中频信号由可变增益放大器（VGA）174 放大，经滤波

器 176 滤波并由混频器 178 用来自 PLL 130 的第 2 本地振荡器信号进行上变频。来自混频器 178 的射频（RF）信号由驱动器 180 放大并进一步由通过双工器 114 驱动天线 112 的功率放大器（PA）182 缓冲。

图 1 还示出了收发机 100 中的各种控制回路。例如，在所述接收信号通路中，一个或多个增益控制回路设置衰减器 116 和 VGA 136 的增益（并可在旁路或 LNA 通路间选择），偏置控制回路设置放大器 118 和 124 的偏置电流，频率跟踪回路设置 VCTCXO 132 的频率，以及直流偏移回路试图使来自滤波器 146 的滤波信号中的直流偏移归零。在一个详细实现中，滤波器 146 是有源滤波器，提供了高直流增益并能在经滤波的信号中潜在地产生较大的直流偏移。所述直流偏移回路除去滤波器 146 产生的直流偏移，使得经偏移补偿的信号处于 ADC 150a 和 150b 的输入范围之内。在所述发射信号通路中，增益控制回路设置 VGA 174 的增益。其它收发机的实现可以包括比图 1 中所示更多、更少或不同的控制回路。

举例来说，考虑 AGC 回路，它设置所述接收信号通路中的 VGA 136 的增益为改进的信噪比（SNR）性能维持所述的信号电平。如果所接收的信号太高，所述 AGC 回路降低 VGA 增益。另一方面，如果所接收的信号太低，所述 AGC 回路增加 VGA 增益。所述 AGC 回路调整“希望的”信号电平（即不是干扰信号电平）使其在所述 ADC 的输入端近似恒定。否则，太高的信号电平将造成 ADC 削波，而太低的信号电平将增加噪声电平，这两者都将导致 SNR 的降低。

所述控制回路的控制部分典型地实现于数字电路中（即在信号处理器 160 中）。来自所述回路控制电路的数字控制信号随后提供给接口电路，产生用于驱动图 1 中所示的各种元件的对应的模拟控制信号。回路控制理论和回路控制电路的实现在本领域中众所周知并在此不作描述。

每个收发机设计在所述接口电路的性能上加入了特定的一组要求。这些要求典型地包括对每个控制信号的响应时间和波纹量。例如，所述接口电路的带宽一般需要比所述控制回路的闭环带宽更宽（即 3 至 10 倍宽）。这是所需的，使得所述接口电路不把过量的相位加到所述控制回路而使回路响应失真。而且，所述控制信号中的波纹表现为噪声，从而降低所述控制回路的性能。所述波纹需要降低到由特定回路的要求定义的预定幅度。

图 2A 示出了常规控制回路的一部分的框图。回路控制电路 210 产生提供给接口电路 220 的数字信号。在接口电路 220 中，脉宽调制器（PWM）或“常规”PDM 222 接收所述数字信号并产生相应于所述数字信号中的值的波形序列。低通滤波器 224 接收并滤波所述波形，以提供模拟控制信号。图 2A 中的回路控制电路 210 可以是图 1 中所示的和上述的任何回路控制电路。

接口电路 220 显示出若干与常规 PWM 和 PDM 相关联的缺点。对于所述数字信号中的每一个数字值，所述 PWM 产生对应于该数字值的某一波形。对于 N 比特 PWM，要求 2^N 个时钟周期来表示 N 比特值，导致具有 2^N 个时钟周期的 PWM 波形。对于每个波形，高（“1”）和低（“0”）值的数量由所述输入数字信号确定。PWM 产生的高值典型地分组在一起。例如，数字值 128 对应于 512 个时钟周期中的最初 128 个时钟周期为高的 PWM 波形。该实现导致具有对应于所述 PWM 波形周期的周期性或具有 2^N 个时钟周期的周期性的模拟信号。

脉冲宽度和脉冲密度调制器的一个重要特性是当所述高值在所述波形中均匀隔开时出现最小量的波纹。这是由于耦合至调制器输出的滤波器中的电容器对每组高和低值进行充电和放电将具有相同的时间量。当所述高值均匀间隔时，在从低到高转换之前，产生的电压中的总最小值出现，而在从高到低转换之前，总最大值出现，导致在稳态中最小量的波纹。当所述高值不是均匀间隔时，所述电容器将具有不对称的充电放电时间，导致增加的稳态波纹幅度。

图 2B 示出了包括本发明的接口电路的控制回路的一部分的框图。回路控制电路 230 产生提供给接口电路 240 的数字信号。在接口电路 240 中，如下面将要描述的那样，时间响应调整电路 242 接收所述数字信号并产生具有经调整的时间响应的“经调整的”信号。Σ-Δ调制器 244 接收经调整的信号并产生包括对应于所述经调整的信号中的值的波形序列的调制器信号。低通滤波器 246 接收并滤波所述波形以提供模拟信号。

为了降低成本并使实现所述接口电路所需的元件数量最小，所述接口电路的一些元件以数字硬件实现（即在信号处理器 160 中）而一些元件使用模拟元件实现。由于要控制的电路元件实际上典型地是模拟的，所述模拟元件提供了所要求的调整信号，用于从数字信号产生模拟信号。在实现中，时间

响应调整电路 242 和Σ-Δ调制器 244 集成于提供系统所要求的其它功能的数字集成电路（IC）中。

图 3A 示出了本发明的接口电路 310 的详细实施例的框图。接口电路 310 包括时间响应调整电路 312、一阶Σ-Δ调制器 314 以及二阶低通滤波器 316。所述数字信号提供给时间响应调整电路 312，产生经调整的信号。在一个实施例中，所述经调整的信号包括对所述数字信号的修正，提供更快或修改的响应时间。

在时间响应调整电路 312 中，数字信号 x[n]提供给放大元件 320 和延迟元件 322。放大元件 320 以可以是固定的或可编程的缩放因子（Av）缩放所述数字信号。在详细实施例中，所述缩放因子是 2。延迟元件 322 以可以是固定的或可编程的时间间隔延迟所述数字信号。所述缩放因子和所述延迟量取决于在其中使用的接口电路的特定应用的要求。来自放大元件 320 的经缩放的信号和来自延迟元件 322 的经延迟的信号提供给加法器 324，该加法器从所述经缩放的信号中减去所述经延迟的信号。在一个实施例中，加法器是饱和加法器，将其输出限制到落在后面的Σ-Δ调制器 314 的输入范围内的 N 比特值。来自加法器 324 的经调整的信号 y[n]提供给Σ-Δ调制器 314。

在Σ-Δ调制器 314 中，所述经调整的信号提供给加法器 330，该加法器用来自寄存器 332 的 N 个最低有效比特（LSB）加到所述经调整的信号上。加法器 330 的（N+1）比特输出提供给寄存器 332 并由其存储。来自寄存器 332 的最高有效比特组成提供给滤波器 316 的调制器信号 k[n]。如图 3A 中的实施例中所示，延迟元件 322 和寄存器 332 用相同的时钟信号（CLK）计时。

滤波器 316 将来自调制器 314 的调制器信号滤波以产生模拟信号。在图 3A 中所示的实施例中，滤波器 316 是包括两个电阻器和两个电容器的二阶低通滤波器。

图 3B 示出了时间响应调整电路 342a 的另一详细实施例的框图。接口电路 342a 包括放大元件 350、延迟元件 352 以及加法器 354，它们对应于图 3A 中接口电路 312 的放大元件 320、延迟元件 322 以及加法器 324。接口电路 342a 进一步包括具有增益（Av-1）并耦合在电路输入和延迟元件 352 之间的第 2 放大元件 356。放大元件 356 提供适当的增益，使得来自加法器 354 的经调整

的信号 y[n]在延迟元件 352 提供的延迟间隔 $M \bullet T_s$ 之后等于所述数字信号 x[n]。

图 3C 示出了时间响应调整电路 342b 的又一详细实施例的框图。接口电路 342b 包括图 3B 的放大元件 350、延迟元件 352 以及加法器 354。接口电路 342b 进一步包括具有耦合至放大元件 350 的输出的非倒相输入和耦合至电路输入的倒相输入的第 2 加法器 358。接口电路 342b 提供与图 3B 相同的传递函数。

时间响应调整电路

来自 PWM、PDM 或Σ-Δ调制器的波形实际上是数字的，并由模拟滤波器滤波以提供所希望的模拟信号。通常地，由于数字信号中的阶跃变化造成的模拟信号的阶跃响应由模拟滤波器确定。具有宽带宽的滤波器提供较快响应时间但导致模拟信号中较大的波纹幅度。因此，所述滤波器典型地设置成最高可能的带宽并产生可接受的波纹幅度（即满足波纹规范）。然后与该滤波器带宽相关的响应时间代表了该接口电路可达到的最快可能的响应时间。

对于某些应用，如具有宽回路带宽的控制回路，常规接口电路达到的响应时间是不可接受的。例如，参考图 1，发送 AGC 回路中的驱动器 180 由具有快速过渡时间的数字信号控制。由于驱动器 180 在低增益状态和高增益状态间切换，在所述信号通路中的增益改变并且需要通过调整 VGA 174 的增益进行补偿。如果所述发射机 AGC 控制信号由低响应时间（即由于由提供该控制信号的模拟滤波器施加的限制），那么驱动器 180 和 VGA 174 的响应时间就不“匹配”。所述失配导致当切换驱动器 180 的增益时产生信号增益中的跳动。

图 4A 示出了常规接口电路的阶跃响应曲线。数字信号在时刻 t_1 从起始值过渡到终值。作为响应，滤波器的输出在 t_1 之后从所述起始值（$V_{起始}$）开始过渡并渐近地趋近（$V_{最终}$）。在时刻 t_3，所述数字信号再次改变而所述滤波器随即相应地响应。

图 5 示出了本发明的时间响应调整电路 512 的详细实施例的框图。对于特定的滤波器，通过用所述时间响应调整电路产生的信号（或脉冲）过度激

励所述调制器能够增加（或加快）所述响应时间。在时间响应调整电路 512 中，数字信号提供给放大元件 520 和延迟元件 522。在图 5 所示的实施例中，放大元件 520 以缩放因子 2 缩放所述数字信号 x[n]并且延迟元件 522 以时钟信号（CLK）的 M 个周期延迟所述数字信号。所述缩放因子和所述延迟时间间隔还能是可编程的。来自放大元件 520 的经缩放的信号和来自延迟元件 522 的经延迟的信号提供给饱和加法器 524，它从所述经缩放的信号中减去所述经延迟的信号。加法器 524 将经调整的信号 y[n]限制到 N 比特值。

在详细实施例中，所述数字信号 x[n]是无符号的二进制信号（即对于 9 比特实现有 0 至 512 范围的值）。自另一详细实施例中，所述数字信号 x[n]是二进制补码（即对于 9 比特实现有-256 至 255 范围的值）。所述数字信号 x[n]以比用于所述延迟元件和后面的调制器定时节拍的时钟信号（CLK）变化慢得多的速率变化。例如，对于 9 比特调制器，所述数字信号在时钟信号的速率的 1/512 或更低的速率变化。

时间响应调整电路 512 以下面的方式工作。对于预定的延迟时间间隔 $M \bullet T_s$，其中 M 是延迟的时钟周期的数量，T_s 是所述时钟信号（CLK）的周期，时间响应调整电路 512 的输出经调整的信号 y[n]是：

$y[n]=2x[n]-x[n-M]$ 方程（1），或者

$y[n]=x[n]+(x[n]-x[n-M])$ 方程（2）

其中 x[n-M]是经 M 个时钟周期延迟的数字信号。对于某一 n，y[n]大于或等于 x[n]。实际上，在该延迟时间间隔期间，y[n]比 x[n]的当前数字值大（x[n]-x[n-M]）。当所述延迟时间间隔完结时，一旦从延迟元件 522 提供了 x[n]的当前值，加法器 524 的输出变成 y[n]=x[n]。从而时间响应调整电路 512 产生与所述阶跃变化具有相同幅度的“过度激励”脉冲串 p[n]（即 $p[n]=\Delta x[n]=x[n]-x[n-M]$）。每个过度激励脉冲具有由所述延迟元件确定的 $M \bullet T_s$ 的持续时间。

经调制器耦合至所述时间响应调整电路的所述滤波器响应当前和先前输入值间的差异（即 y[n]-y[n-1]）。时间响应调整电路 512 在从(y[n]-y[n-1])=(x[n]-x[n-1])到(y[n]-y[n-1])=2•(x[n]-x[n-1])的延迟周期期间有效地使滤波器的激励加倍。该较高的 y[n]导致对所述滤波器较多的激励，加速所

述响应时间。在所述延迟周期终结时，即在 $M \bullet T_s$ 时间之后，时间响应调整电路 512 对所述输入数字值无影响并且 y[n]变成 x[n]。

图 4B 示出了使用时间响应调整电路 512 的接口电路的阶跃响应曲线。最初，在时刻 t_1 所述经调整的信号从起始值跃迁到新值。然而，如图 4B 中所示，所述调制器由时间响应调整电路 512 过度激励到对应于（$2V_{最终}-V_{起始}$）的到经调整的值，该值是所述数字信号 x[n-M]的变化的两倍。在 t_1 之后不久来自滤波器的模拟信号开始从所述起始值（$V_{起始}$）向（$2V_{最终}-V_{起始}$）过渡并以较快的速率到达 $V_{最终}$。当所述模拟信号在时刻 t_4 接近 $V_{最终}$ 时，所述过度激励脉冲被消除并且所述经调整的信号返回到对应于 $V_{最终}$ 的值。然后所述滤波器转换到其最终值 $V_{最终}$。如图 4B 中所示，所述过度激励脉冲具有等于输入值中的变化（$\Delta V=V_{最终}-V_{起始}$）的幅度并且具有（t_4-t_1）的持续时间。

如图 4B 中所示，对于所述输入数字信号中的某些变化，所述过度激励脉冲的幅度与所述数字信号中的变化相同（即 $p[n]=\Delta x[n]=x[n]-x[n-M]$）。当当前数字值有足够的峰值空间来提供具有幅度（$p[n]=\Delta x[n]$）的过度激励脉冲时该结果发生。特别地，如果（$x[n-M]+2\Delta x[n]$）落在所述调制器的输入范围内，那么所述过度激励脉冲的幅度等于所述阶跃变化。对于数字信号中满足该条件的所有变化，在响应时间方面的改进量是（理论上）相同的。

然而，由于加法器 524 进行的饱和操作以保持经调整的信号 y[n]处于后续电路（如Σ-Δ调制器）的有效输入范围之内，对于所述数字信号中的某些变化所述过度激励脉冲的幅度小于$\Delta x[n]$。当当前数字值 x[n]没有足够的峰值空间来提供具有幅度$\Delta x[n]$的过度激励脉冲时，这就发生。过度激励脉冲随后就受到可用峰值空间量的限幅。当所述脉冲幅度被限幅时，所述响应时间就没有当所述脉冲幅度不限幅时快。为了进一步提高（即加速）所述响应时间，可增加所述过度激励脉冲的持续时间。在一个实施例中，根据限幅的量增加所述过度激励脉冲的持续时间（从额定为 M 的脉冲持续时间）。例如，限幅一半的脉冲（即 $p[n]=0.5\bullet\Delta x[n]$）将比限幅四分之一的脉冲（即 $p[n]=0.75\bullet\Delta x[n]$）有更长的持续时间。

图 8A 和 8B 示出了模拟信号中在阶跃响应上限幅的影响。图 8A 示出了对于不限幅所述过度激励脉冲的情况的阶跃响应的曲线，而图 8B 示出了限幅所

述过度激励脉冲的情况的阶跃响应的曲线。对于对应于图 8A 的详细实现，当不限幅所述过度激励脉冲时，所述过度激励脉冲的持续时间是 112 码元×8 或 11.4 微秒，并且所述阶跃响应到最终值的 70%的时间大约是 10 微秒。对于相同的实现，当 100%限幅所述过度激励脉冲时（即不提供过度激励脉冲），所述阶跃响应到最终值的 70%的时间大约是 24 微秒。如上所述，当发生限幅时通过增加所述过度激励脉冲的持续时间可提高所述阶跃响应时间。

如图 3 和图 5 中所示，通过调整所述放大元件的增益或所述延迟元件的延迟或两者，可控制所述响应时间。对于某一的增益，如果所示延迟太短，产生较短的过度激励脉冲并且所述时间响应调整电路对所述响应时间有较少的影响。当所述延迟为 0（M=0），所述时间响应调整电路的输出仅是 x[n]并且无影响。为了加速响应时间，尽可能地增加所述延迟。然而，如果延迟太长，过多的过度激励脉冲可造成所述模拟信号超过所述最终值，这对于许多应用是不希望的结果。通过模拟或通过计算可实验地确定导致最快可能响应时间而不过冲的延迟。

类似地，对于某一特定延迟时间间隔 $M \bullet T_s$，如果所述放大元件的增益很小（即接近于 1），产生较小的过度激励脉冲并且所述时间响应调整电路对所述响应时间有较少的影响。当所述增益设置成 1 时，所述时间响应调整电路对所述响应时间无影响。

在一个实施例中，所述放大元件和所述延迟元件都是可编程的。在另一实施例中，根据所述数字信号中的变化量调整所述放大元件。例如，较高的增益或较长的延迟或两者，用于大变化，而较低的增益或较短的延迟或两者，用于较小的变化。在又一实施例中，所述输入信号中的每个变化可与一组编程的增益和延迟值相关，导致最快的响应时间而无过冲。

图 3 和图 5 示出了本发明的时间响应调整电路的一个实施例。所述时间响应调整电路可用数字电路实现。所述时间响应调整电路还可用诸如随机存取存储器（RAM）或只读存储器（ROM）的存储器元件实现。对于数字值中的某一特定改变，所述存储器元件提供值序列，该值序列提供所希望的时间响应特性（即最快的响应时间而无过冲）。

虽然以使用数字电路实现表述了本发明的时间响应的调整机构，但是本

发明还可以处理器（即信号处理器 160）执行的软件或微代码实现。而且，为具体应用描述了时间响应调整机构，在该具体应用中产生过度激励脉冲来获得较快响应时间。本发明的时间响应调整机构可用于其它应用，如“波形成形”所述时间响应来获得某一特定波形特性。从而，本发明的时间响应调整机构意味着覆盖任何及所有对由常规调制器和滤波器组合产生的模拟信号的时间响应特性的修改。

Σ-Δ调制器

所述Σ-Δ调制器提供调制器信号 k[n]，该信号包括对应于其输入处的经调整信号的高和低值序列（即输出波形序列）。所述高值均匀分布于输出波形之中。此特性导致较小的波纹幅度，因为耦合至所述调制器的滤波器中的电容器对每组高和低值进行充电和放电将具有相同的时间量。

图 6 示出了一阶Σ-Δ调制器 600 的详细实施例的图。所述 N 比特经调整的信号 y[n]提供给加法器 612，该加法器用来自寄存器 614 的 N 个最低有效比特（LSB）加该信号。来自加法器 612 的最高有效比特（MSB）提供给“异”（XOR）门 616 的第 1 输入，而来自加法器 612 的 N 个 LSB 提供给寄存器 614 并由其存储。极性控制信号（极性）提供给 XOR 门 616 的第 2 输入。XOR 门 616 根据所述极性控制信号的状态反转来自加法器 612 的 MSB 的极性（如高=反转，而低=不反转）。XOR 门 616 的输出提供给寄存器 618，使输出与所述时钟信号（CLK）同步。寄存器 618 的输出包括来自Σ-Δ调制器 600 的调制器信号。

Σ-Δ调制器 600 均匀地分布高值间的间隔，以提供超过常规 PDM 的改进稳态波纹性能。分析指出用 9 比特分辨率（N=9），Σ-Δ调制器 600 能以大约为 3 的因子降低峰-峰波纹幅度的较差情况。

Σ-Δ调制器 600 除了通过过采样在频率中均匀地扩展波纹能量之外，还通过利用反馈对所述波纹能量进行噪声成形。通过噪声成形，大部分波纹能量移到较高频率并由后续的滤波器滤除，从而导致在所关心的未滤除的较低频率中有较少的波纹。Σ-Δ调制器 600 的噪声成形由下面的表示式示出：

$$K(z)=z^{-1}Y(z)+(1-z^{-1})E_Q(z) \qquad \text{方程（3）}$$

其中 Y(z)、K(z)和 $E_Q(z)$分别是调制器输入、调制器输出以及量化误差的 z 变

换。所述调制器转移函数（$H_Y(z)=K(z)/Y(z)$）由下式给出：

$$H_Y(z)=z^{-1} \qquad \text{方程（4）}$$

并且所述量化误差函数（$H_E(z)=K(z)/E_Q(z)$）由下式给出：

$$H_E(z)=(1-z^{-1}) \qquad \text{方程（5）}$$

由于 z^{-1} 在直流频率变成 1 而在 $f_{CLK}/2$ 变成-1，所述量化误差函数 $H_E(z)$ 在直流频率提供 0 增益（或无限衰减），在较低频率提供大的衰减，而在较高频率提供相对的放大。量化噪声有效地从较低频率移到可容易地实现滤波的较高频率。

一阶Σ-Δ调制器对每个有效的输入数字值输出特定的波形。根据所述高值和低值在所述波形中的布局，每个波形有特定的波纹特性。

图 8C 和 8D 示出了两个详细接口电路实现的对于所有可能的输入数字值的峰一峰波纹幅度曲线。如图 8C 中所示，所述Σ-Δ调制器具有 9 比特的分辨率。注意到所述波纹幅度依赖于所述输入数字值变化，并且在极值 0 和 512 附近较高。在图 8C 中对于 5 至 508 的输入值，较差情况的波纹幅度是 1.7mV。通过提供额外的滤波（即减小耦合至所述Σ-Δ调制器的滤波器的带宽）可降低所述波纹的幅度。就图 8 而言，对于相同的接口电路实现，当通过将极点 p_1=9.33kHz 和 p_2=54.34kHz 下移至 p_1=624Hz 和 p_2=32.48kHz 降低所述滤波器的带宽时，所述较差情况的波纹幅度降低到 300μV。

所述波纹性能是调制器类型、所述低通滤波器的带宽以及所述调制器时钟的速率的函数。可示出，对于小于一个 LSB 的 100%的波纹，来自二阶 RC-RC 滤波器的模拟信号中的波纹量遵循下面的关系式：

$$\text{波纹占步长的百分数} \approx 480\% \bullet \left(\frac{2^N \bullet f_c}{f_{CLK}}\right)^2 \qquad \text{方程（6）}$$

或等价于，

$$\text{波纹占步长的百分数} \approx 480\% \bullet 2^N \left(\frac{f_c}{f_{CLK}}\right)^2 \qquad \text{方程（7）}$$

其中 f_c 是所述滤波器的转角点频率。从这些关系式可见加速所述Σ-Δ调制器的时钟频率（f_{CLK}）导致波纹量的对应减少。然后通过增加所述模拟滤波器的带宽，波纹性能方面的改进可用于换取较快的响应时间。

虽然结合一阶Σ-Δ调制器描述了本发明，但是也可使用较高阶的Σ-Δ调制器（即二或三阶调制器）。一般地，较高阶Σ-Δ调制器把更多的带内量化噪声推到能较容易地进行滤波的较高频率。如果所述Σ-Δ调制器的阶数高于所述模拟滤波器的阶数，就不能充分地滤除带外量化噪声并且所述模拟信号可能包含较高量的带外噪声，这可能降低系统的性能。根据所用的模拟滤波器的阶数选择所述Σ-Δ调制器的阶数。

当连同Σ-Δ调制器一起使用时，本发明的时间响应调整电路能提供改进的性能。然而，所述时间响应调整电路还可与 PWM、PDM 或 M 比特 DAC 组合使用。

模拟滤波器

一阶低通滤波器典型地用于对来自所述调制器的调制器信号进行滤波。可以用单个电阻器和单个电容器实现所述一阶滤波器。虽然一阶滤波器导致较低的元件计数，但是对于某些应用所述响应时间和波纹性能不令人满意。

结合本发明，可使用二阶或较高阶滤波器来提供对于模拟信号的较快响应时间或较小波纹量或两者。下面描述了二阶低通滤波器比一阶低通滤波器在性能方面的改进。在详细实施例中，如图 3A 所示，以具有 2 个电阻器和 2 个电容器的 RC-RC 滤波器实现所述二阶滤波器。该实现仅比所述一阶 RC 滤波器稍微复杂一点，但是当与本发明的时间响应调整电路组合使用时，提供改进得多的性能。

用一阶 RC 滤波器，在大部分工作范围上（即对于高于所述滤波器的极点的频率的频率，$f_p = \frac{1}{RC}$），波纹与所述 RC 滤波器的截止频率 f_p 成比例。这是由于所述 RC 滤波器的频率响应的幅度在极点频率之外以 1/f 衰减。所述模拟信号上的波纹具有等于波形的周期的最低基频或 $f_{波纹} = \frac{f_{CLK}}{2^N}$，其中 f_{CLK} 是用于对所述调制器时钟节拍的时钟信号的频率。

二阶低通滤波器的总转移函数可以如下表示：

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \text{方程（8）}$$

其中所述极点由下式给出：

$$p_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$$ 方程（9）

对于图 3A 中示出的二阶 RC-RC 低通滤波器，$\zeta>1$，两个极点 p_1 和 p_2 是实数，并且所述转移函数化为：

$$H(s) = \frac{p_1 p_2}{(s-p_1)(s-p_2)}$$ 方程（10）

对于具有两个极点的二阶滤波器，所述滤波器的频率响应在第 1 极点和第 2 极点的频率间以 1/f 衰减，并在所述第 2 极点的频率之后以 $1/f^2$ 衰减。通过选择两个极点的频率低于波纹分量（即 f_{p1} 和 $f_{p2}<f_{波纹}$），所述波纹以 40dB/10 倍频的斜率衰减，这比用一阶滤波器获得的 20dB/10 倍频的斜率快。然后波纹中的改进可以换取滤波器的响应时间中的改进。换句话说，为了满足特定的波纹要求，所述二阶滤波器的极点可以增加到比一阶滤波器的极点高，从而导致较快的响应时间而不牺牲波纹性能。

参考方程（8），自然频率 ω_n 控制所述二阶滤波器的标度。对于较小波纹幅度和较快响应时间的期望对该参数的要求互相矛盾。对于二阶滤波器，临界阻尼条件导致最快的阶跃响应而无过冲。对于二阶滤波器，邻界阻尼发生在 $\zeta=1$ 时，这将导致极点落在实轴上的同一位置（或 $p_1=p_2$）。

在对于规定的波纹幅度要求快响应时间的应用中，可以把所述 RC-RC 滤波器设计成接近所述临界阻尼条件（即 ζ 尽可能接近于 1），并且按所规定的波纹性能允许的那样尽可能高地增加所述自然频率 ω_n。分析指出，通过使用二阶临界阻尼滤波器，对于 LSB 的 30%的波纹幅度规范，可以以大约是一阶滤波器的 10 倍的因子加速所述滤波器的响应时间。对于较小规定的波纹幅度，响应时间的改进甚至更大。

通过对于更高阶滤波器（如 3 阶、4 阶或更高阶）的使用可以实现响应时间方面的进一步改进。

图 3A 示出了仅包括电阻器和电容器的滤波器实现。还可以设计使用其它电抗元件（如电感器）设计滤波器。例如，可以把二阶滤波器设计成使用单个电感器和单个电容器。由于不同于限制于 $\zeta>1$ 的 RC 滤波器，对于这些滤波器阻尼 ζ 可取所有的值，LC 滤波器提供提供额外的灵活性。从而，可把 LC 滤波器设计成欠阻尼的（即具有 $\zeta<1$）来提供带有一些过冲的更快的响应时间。还可以本领域中所知的方式以有源滤波器实现所述滤波器。各种滤波器实现

处于本发明的范围之中。

接口电路的详细实现

图 7 示出了用于例如 CDMA 蜂窝网电话机的发射机 AGC 回路的本发明的接口电路 710 的详细实施例的图。接口电路 710 包括时间响应调整电路 712，一阶Σ-Δ调制器以及二阶低通滤波器 716。

在时间响应调整电路 712 中，数字信号 x[n]提供给放大元件 720 和寄存器 722。放大元件 720 以缩放因子 2 缩放所述数字信号以产生 2x[n]。寄存器 722 以由总线上的延迟值（Delay_Val）确定的延迟时间间隔锁存所述数字信号 x[n]。寄存器 722 保留旧的值直到锁存新值为止。计数器 726 以所述延迟值输入并在所述延迟值指示的延迟时间间隔之后向寄存器 722 提供启动信号。来自放大元件 720 的经缩放的信号和来自延迟元件 722 的经延迟的信号提供给加法器 724，所述加法器 724 从所述经缩放的信号中减去所述经延迟的信号。加法器 724 是饱和加法器，产生具有落入Σ-Δ调制器 714 的输入范围之内的 N 比特值的经调整信号 y[n]。所述经调整的信号提供给Σ-Δ调制器 714。

Σ-Δ调制器 714 与图 6 中所示的调制器类似地实现，具有 N=9。低通滤波器 716 对来自调制器 714 的调制器信号进行滤波以产生模拟信号。在图 7 所示的实施例中，低通滤波器 716 是类似于图 3A 中所示的二阶 RC-RC 滤波器。

许多蜂窝网电话机以不止一个操作模式运行。例如，双频带蜂窝网电话机能在数字模式或模拟模式下运行。可由诸如全球数字移动电话系统（GSM）信号的码分多址（CDMA）信号或时分多址（CDMA）信号的传输来表征所述数字模式。可由调频（FM）信号或调幅（AM）信号表征所述模拟模式。

通常，对于数字模式和对于模拟模式的要求是不同的。例如，在数字（如 CDMA）模式中要求快响应时间，而对于模拟（如 FM）模式要求较低波纹幅度。因此，为了获得较快响应时间，对于数字模式模拟滤波器的带宽较宽，而为了获得较低波纹幅度，对于模拟模式模拟滤波器的带宽较窄。要求在两种模式下运行的蜂窝网电话机满足两种模式的规格，并且组合的要求可使双模电话机的设计复杂化。

如图 7 所示，滤波器 716 包括与开关 750 串联耦合的额外的电容器 748，

它们的组合与电容器 746 并联。在数字模式中，当对于较快的响应时间要求较宽的带宽时，开关 750 打开并且电容器 748 不是 RC-RC 滤波器的一部分。在模拟模式中，当对于较小波纹幅度要求较窄的带宽时，开关 750 闭合并且电容器 748 与电容器 746 并联耦合以提供更大电容量。在一特定实施例中，对所述电阻器和电容器选择下面的值：R1=R2=1KΩ、C1=10nF、C2=5nF（对于 CDMA 模式），以及 C3=120nF（对于 FM 模式）。用该实现，相同的基本 RC-RC 滤波器（R1=R2=1KΩ、C1=10nF、C2=5nF）用于两种模式并且对于模拟模式切换所述额外的电容器 750（C3=120nF）使之与电容器 746 并联。可以用双极性晶体管、金属氧化物半导体（MOS）门或其它电路元件实现开关 750。

部分地通过对调制器时钟选择适当的频率（f_{CLK}），还可获得不同的时间响应特性。在详细实施例中，用 9 比特的调制器实现时，对于 CDMA 模式 f_{CLK}=19.6608MHz，而对于 FM 模式 f_{CLK}=19.68MHz。对于 AGC 控制回路，对于 CDMA 和 FM 模式，最低基频（f_{CLK}/512）是典型的 38.4KHz。选择二阶 RC 滤波器的极点使得这些 RC-RC 滤波器提供足够的波纹衰减以满足波纹规范。对于 FM 模式，所述波纹规范一般很难满足，并且把 FM RC-RC 滤波器设计成提供更多衰减。从而，在较低频率设置 FM RC-RC 滤波器的极点（如 p_1=624Hz，p_2=32.84kHz）使得所述波纹基频在比 p_1 和 p_2 高的频率处，并以 40dB/10 倍频衰减。对于 CDMA 模式，波纹滤波上的限制较不严格，允许在较高的频率处设置 p_1 和 p_2（p_1=9.33kHz，p_2=54.34kHz）。位于 p_1 和 p_2 之间的最低基频以 20dB/10 倍频衰减，并且剩下的波纹频率成分在高于 p_1 和 p_2 的频率处以 40dB/10 倍频衰减。

给出了较佳实施例的上述说明，使本领域的任何普通技术人员能够制造或使用本发明。对于本领域的普通技术人员，这些实施例的各种修改是显而易见的，并且在此定义的一般原则可适用于其它实施例而不使用创造能力。例如，本发明还可用于提供整形的阶跃响应以及其它特性。因此，本发明不打算局限于在此示出的实施例，而是要使最宽泛的范围符合这里揭示的原理和新颖特点。

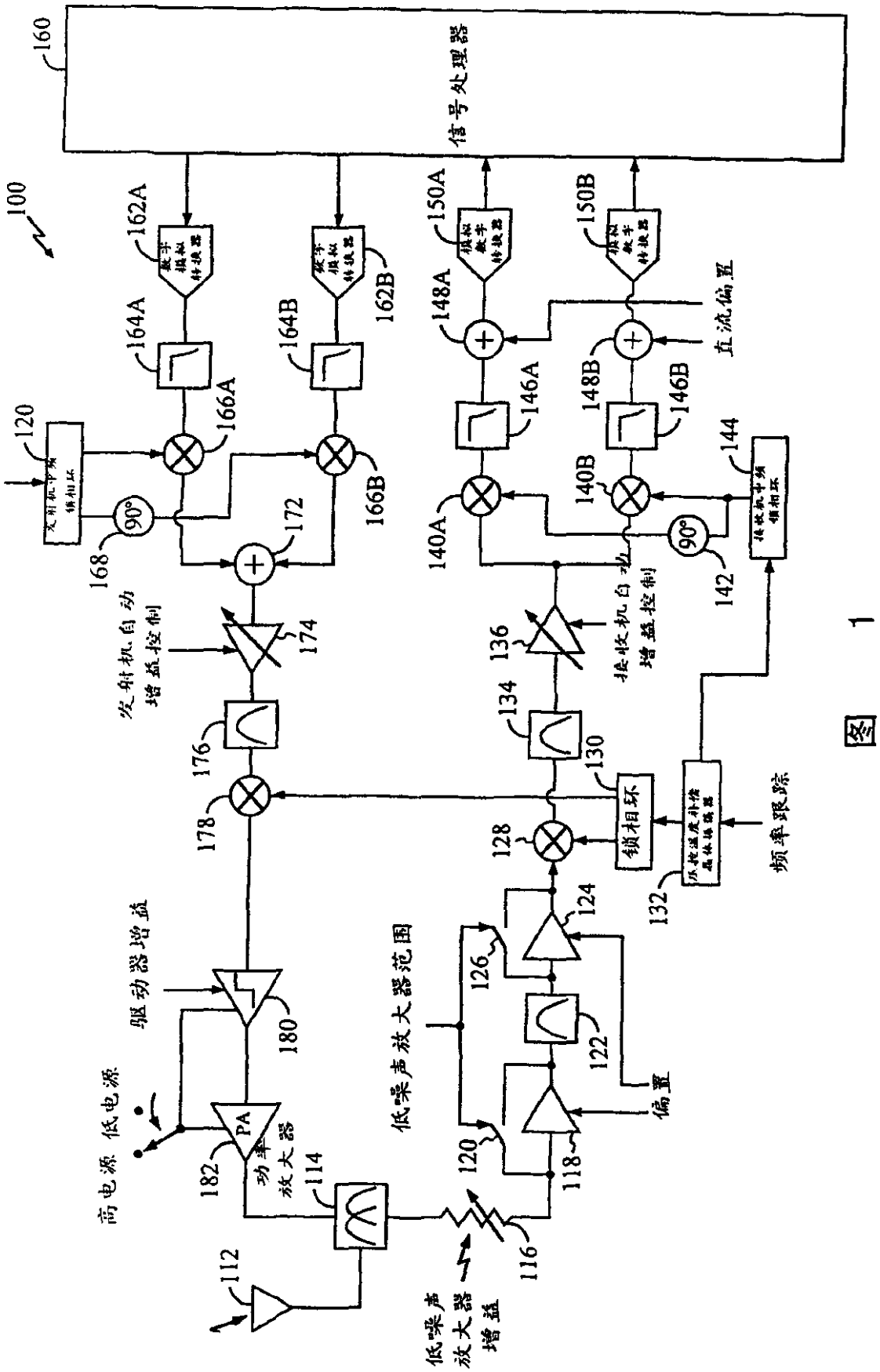
100
160
信号处理器
162A
162B
164A
164B
166A
166B
120
168
90°
172
174
发射机自动增益控制
176
178
180
驱动器增益
高电源
低电源
182
PA
功率放大器
114
112
低噪声放大器增益
116
118
120
122
偏置
124
126
低噪声放大器范围
128
130
锁相环
132
频率跟踪
134
136
接收机自动增益控制
140A
140B
142
144
146A
146B
148A
148B
150A
150B
直流偏置

图 1

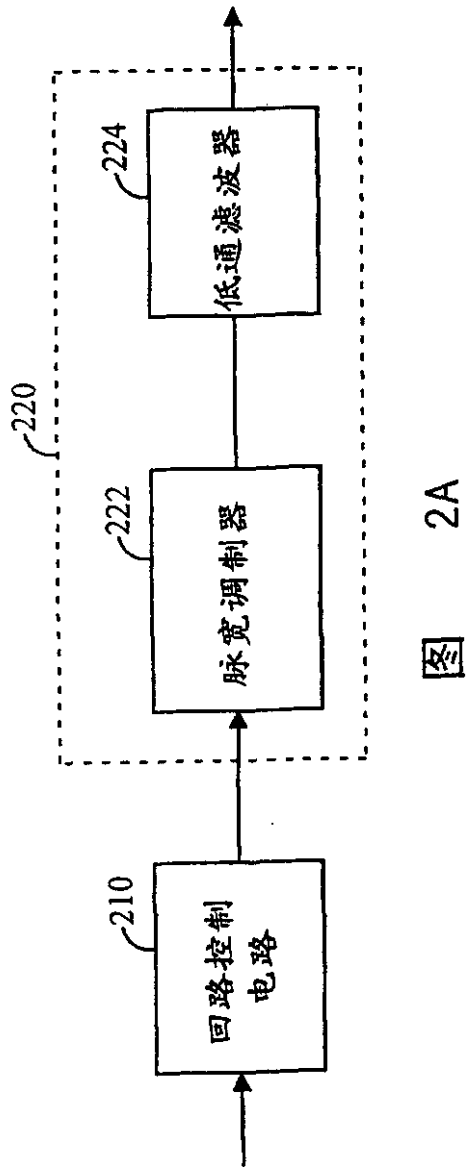
回路控制电路
210
脉宽调制器
222
低通滤波器
224
220

图 2A

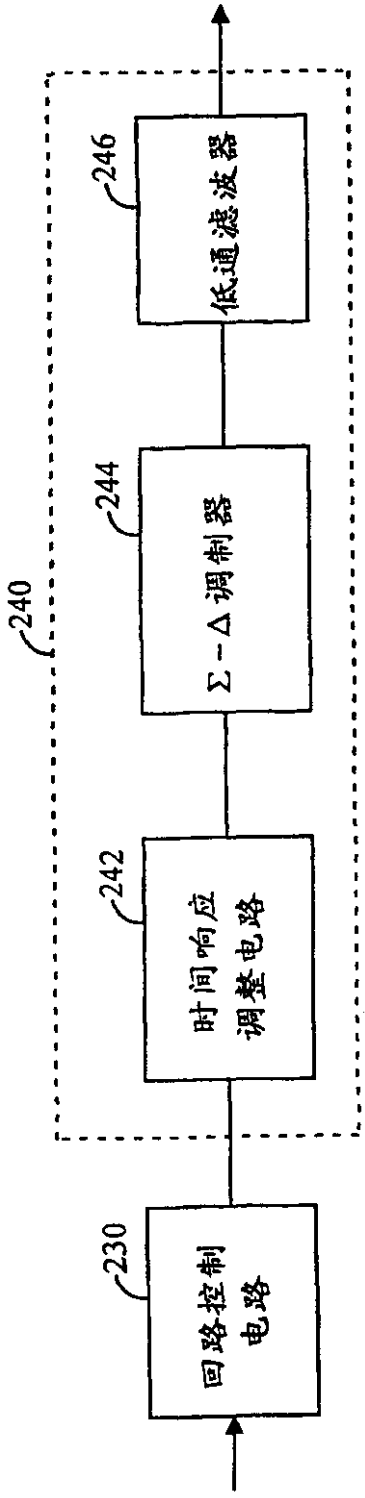
回路控制电路
230
时间响应调整电路
242
Σ-Δ调制器
244
低通滤波器
246
240

图 2B

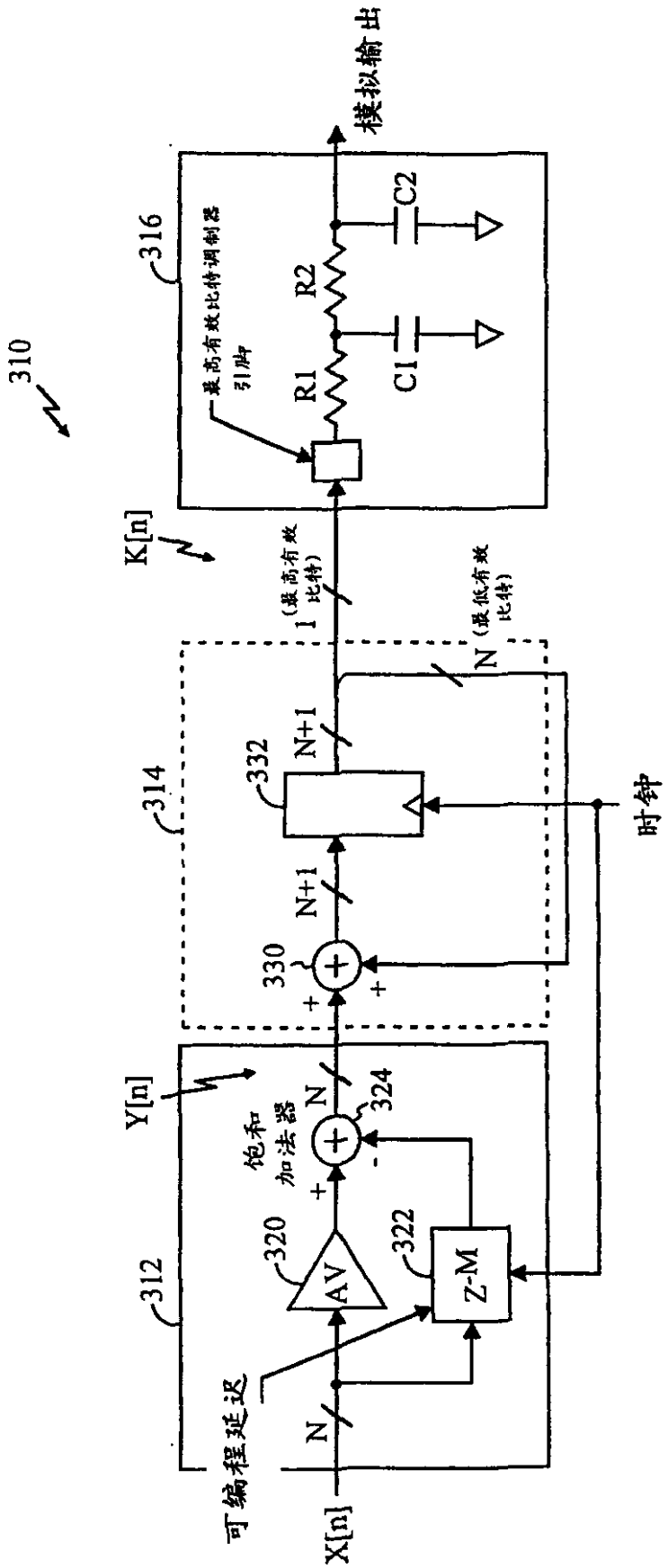
310
316
模拟输出
最高有效比特调制器引脚
R1
R2
C1
C2
K[n]
1 (最高有效比特)
N (最低有效比特)
314
332
N+1
330
时钟
Y[n]
饱和加法器
324
320
AV
322
Z-M
312
可编程延迟
X[n]

图 3A

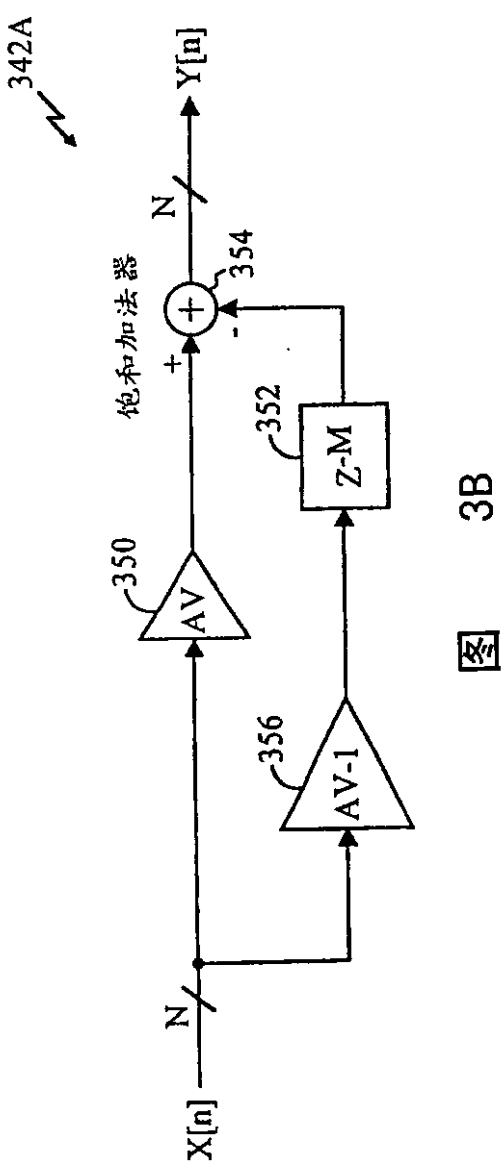
342A
Y[n]
N
饱和加法器
354
+
-
352
Z-M
350
AV
356
AV-1
N
X[n]

图 3B

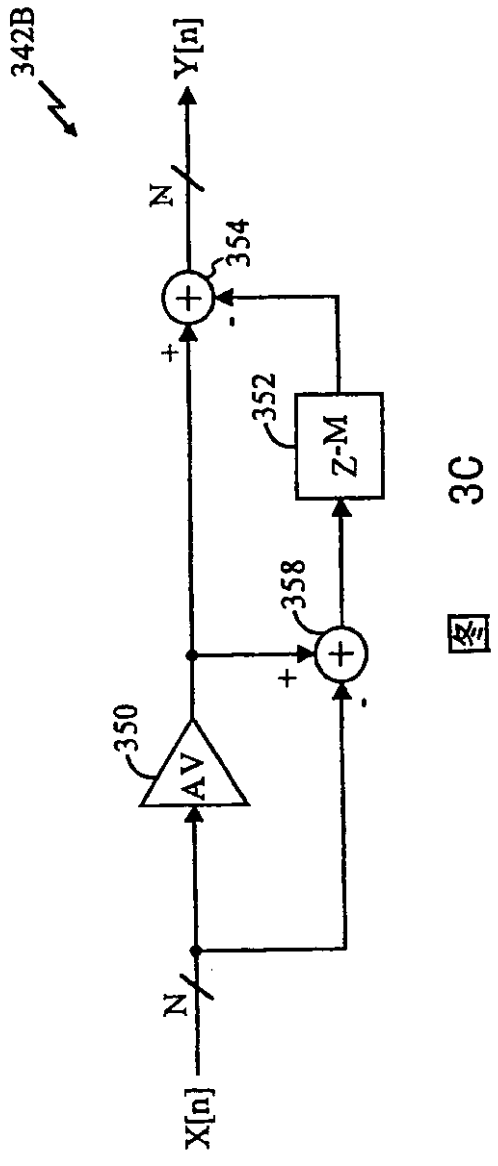
342B
Y[n]
N
354
+
-
352
Z-M
358
+
-
350
AV
N
X[n]

图 3C

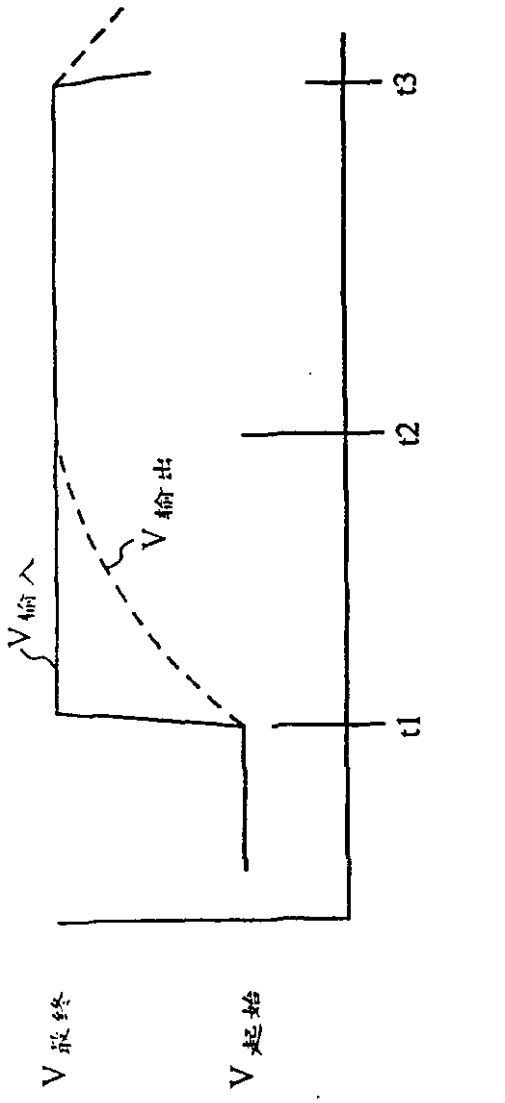

图 4A

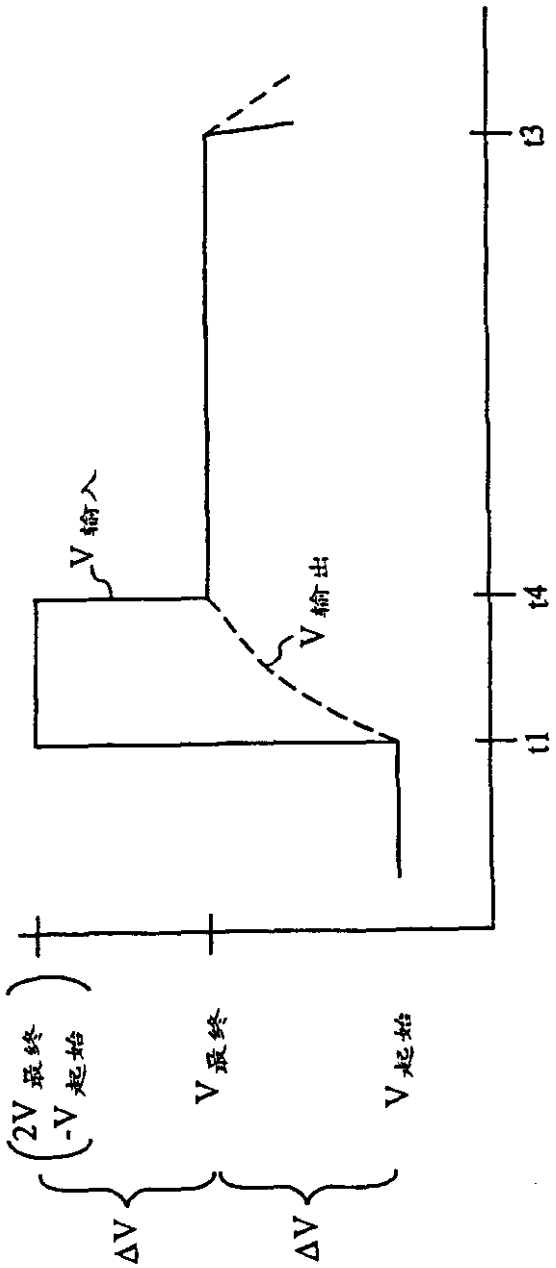

图 4B

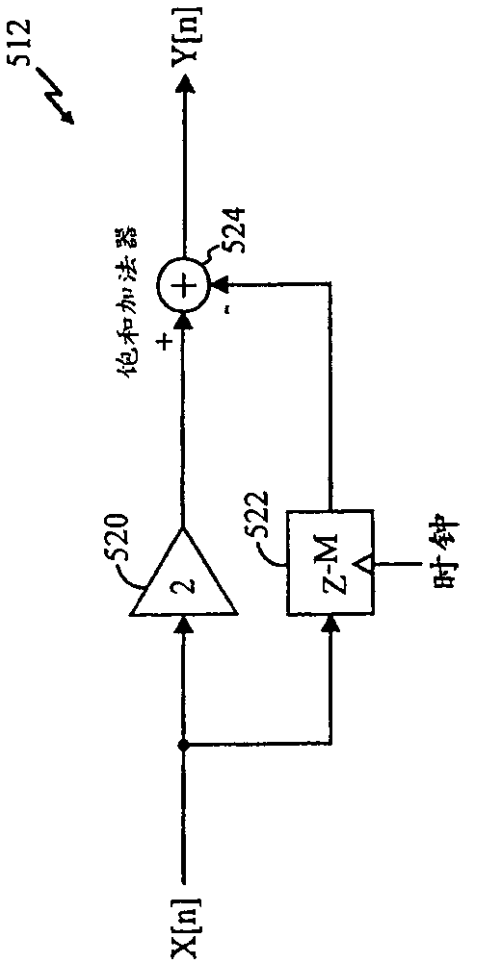

图 5

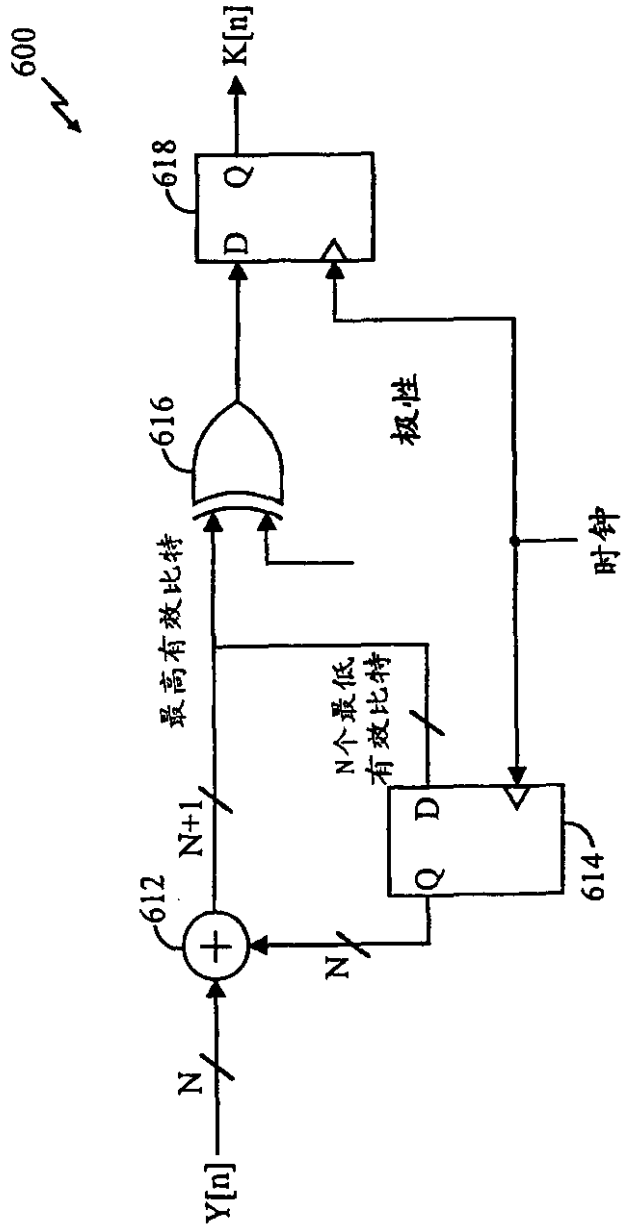

图 6

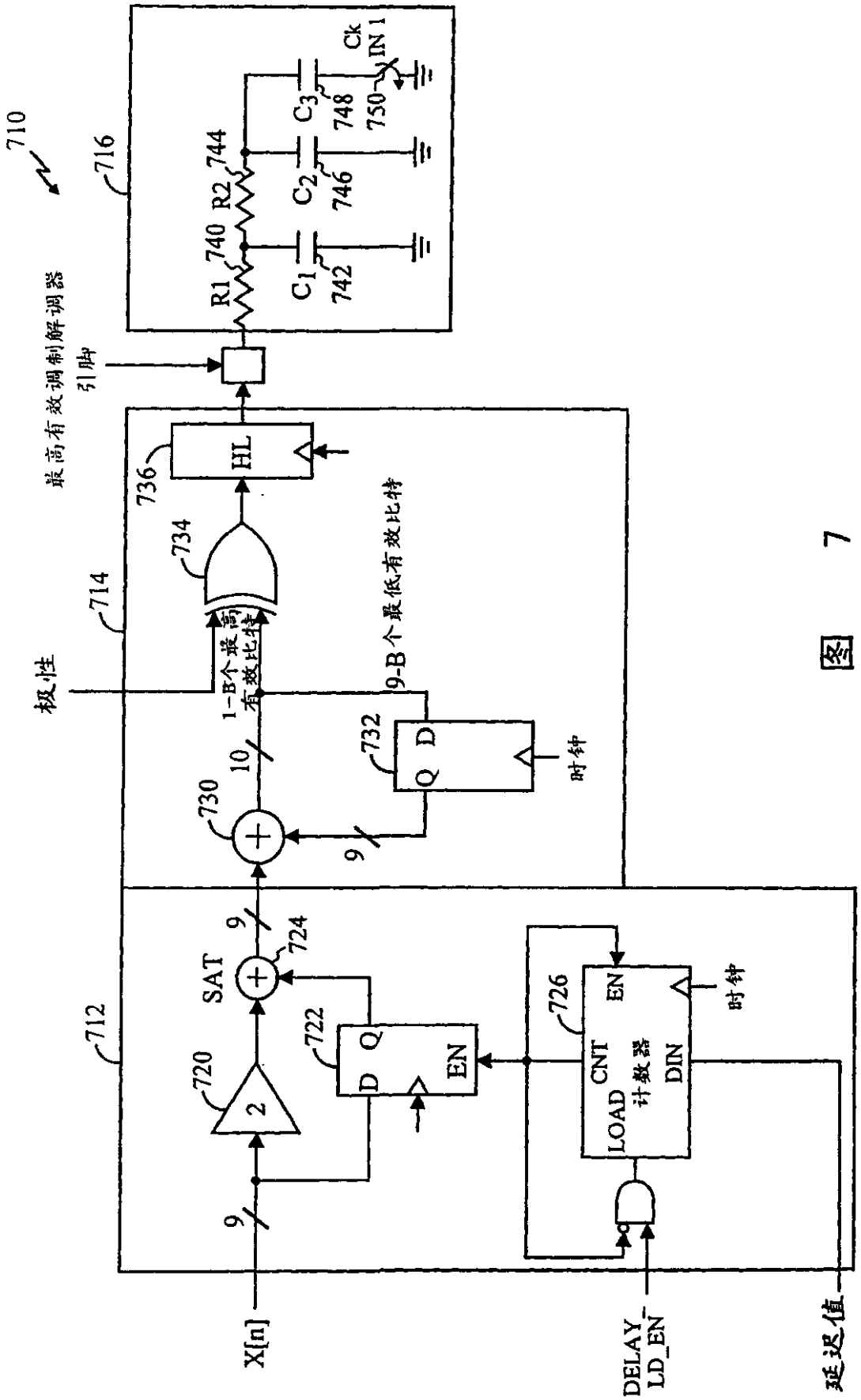
710
716
R1 740
R2 744
C1 742
C2 746
C3 748
750
Ck
IN 1
最高有效调制解调器引脚
714
HL
736
734
1-B个最高有效比特
9-B个最低有效比特
极性
732
D
Q
时钟
730
10
9
712
SAT
724
720
2
722
D
Q
EN
726
EN
CNT
LOAD
计数器
DIN
时钟
X[n]
DELAY_LD_EN
延迟值

图 7

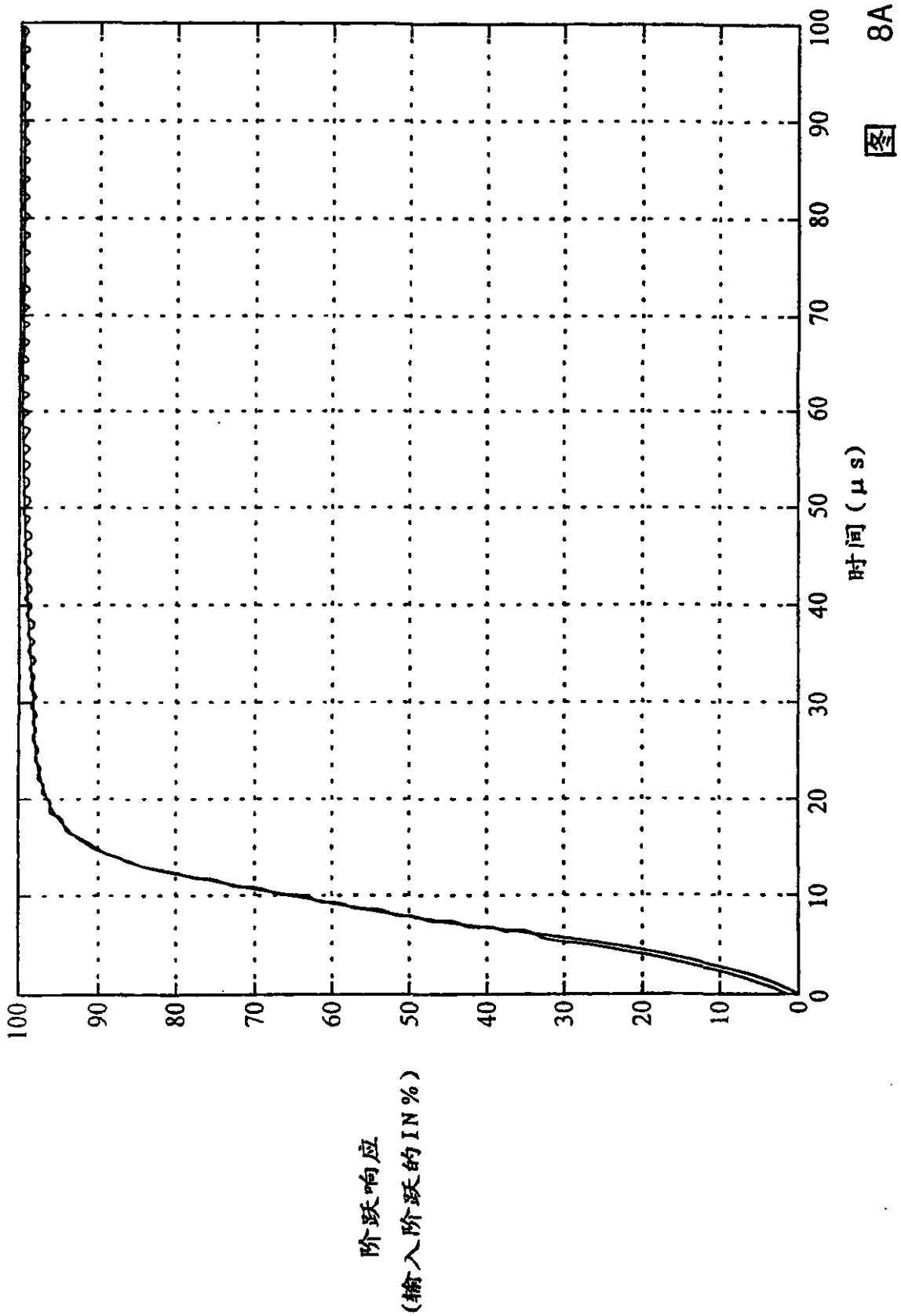

图 8A

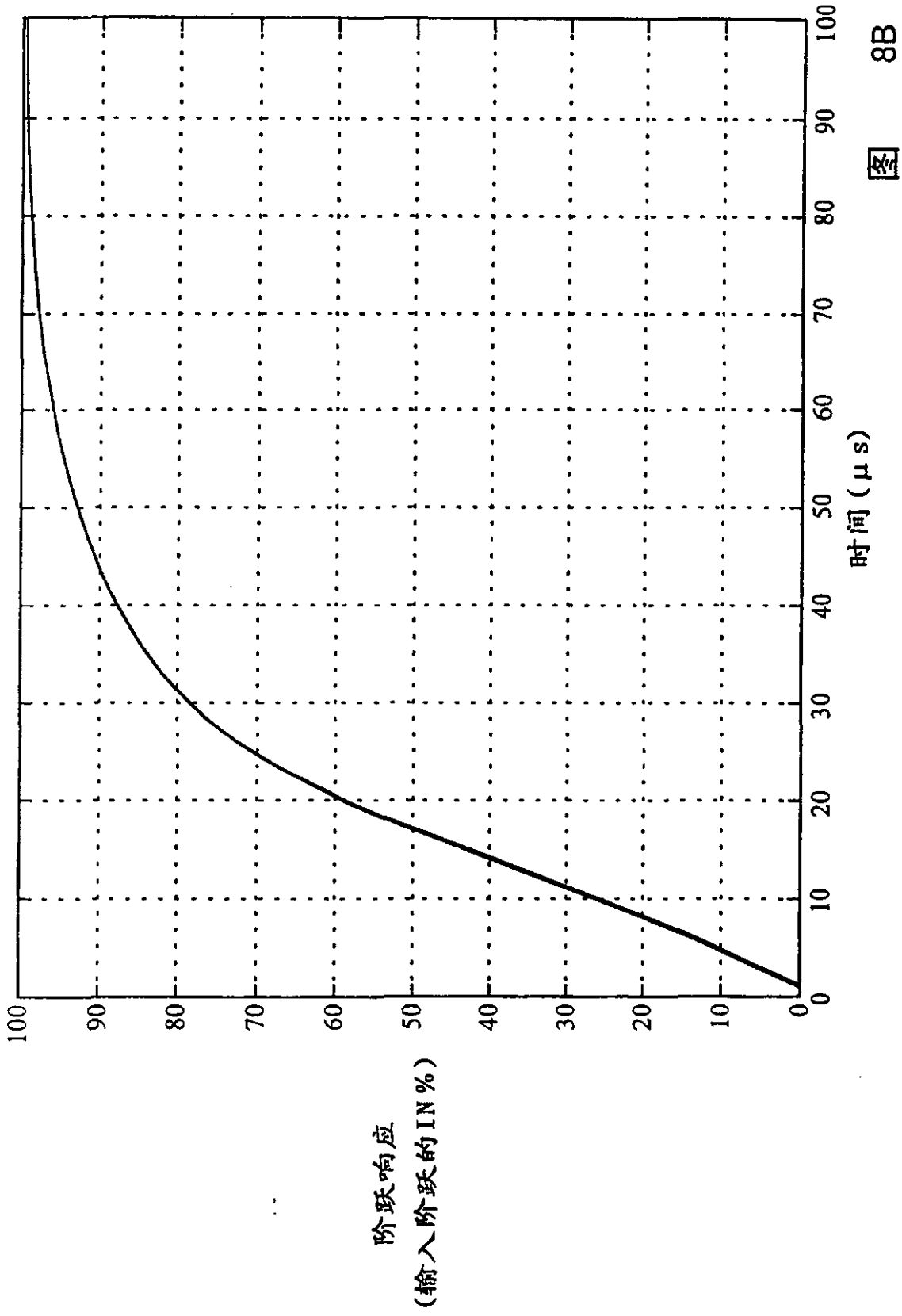

图 8B

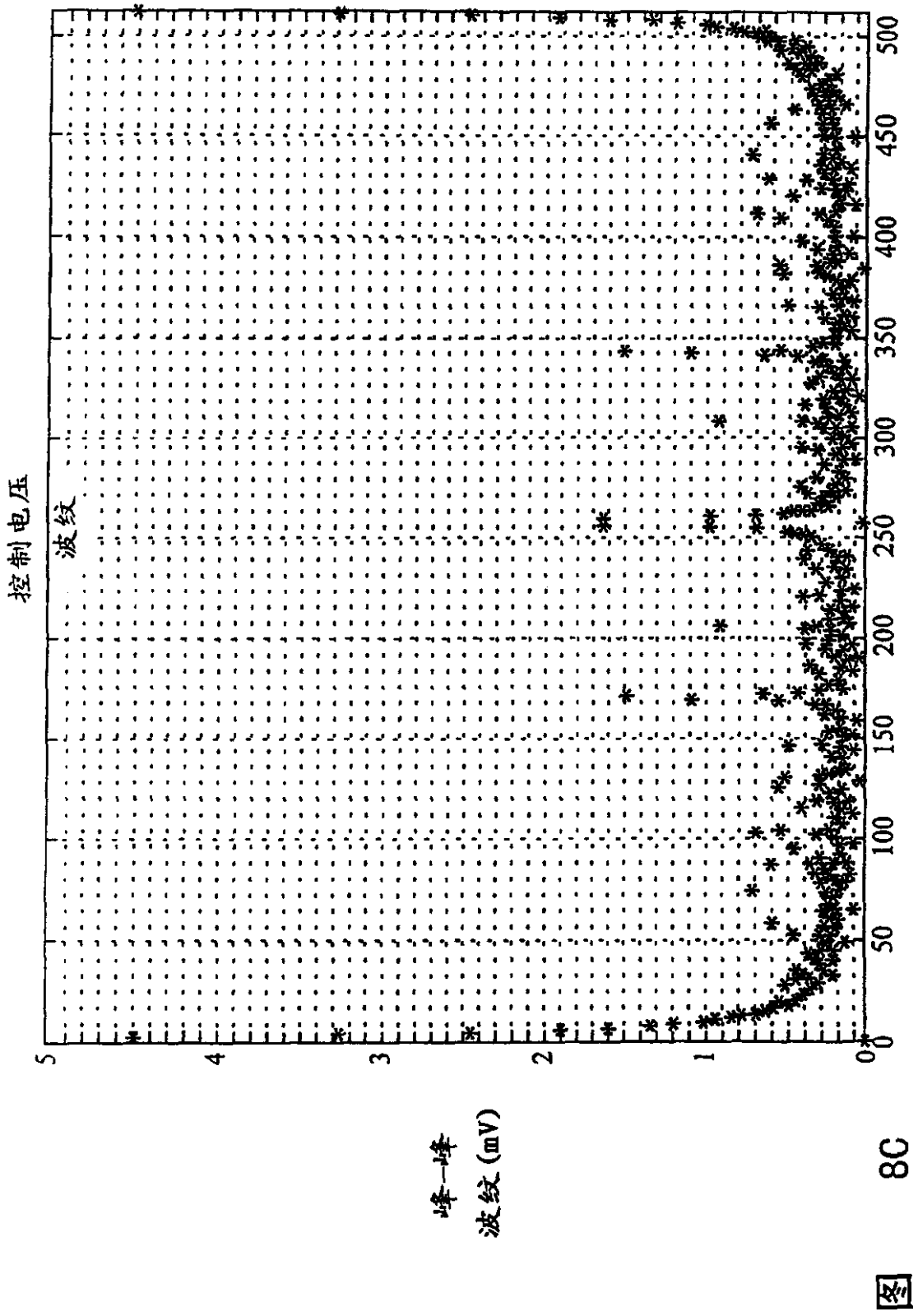
控制电压
波纹
输入编码
峰—峰
波纹(mV)
0
50
100
150
200
250
300
350
400
450
500
1
2
3
4
5

图 8C

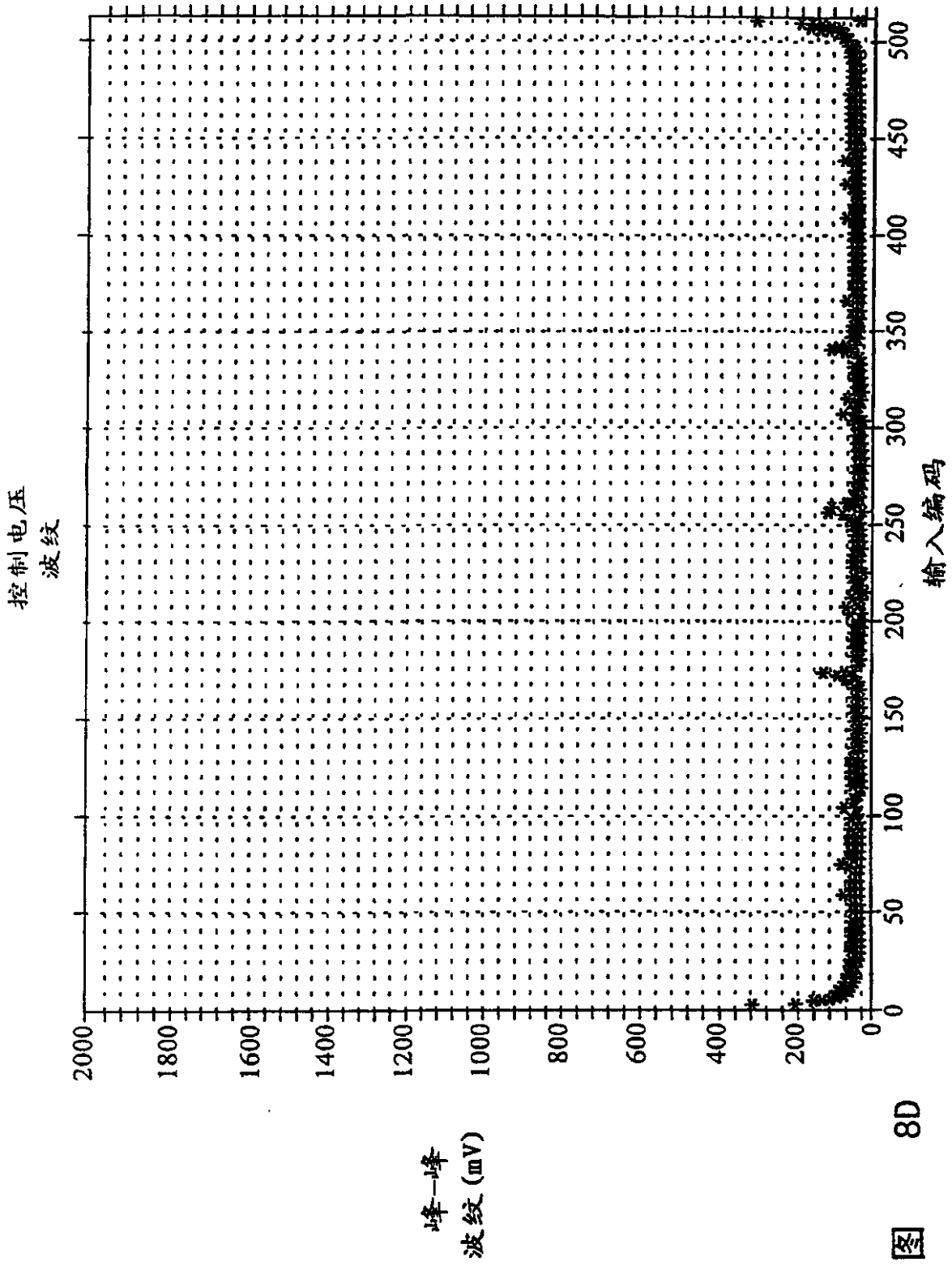
控制电压
波纹
峰—峰
波纹(mV)
输入编码
2000
1800
1600
1400
1200
1000
800
600
400
200
0
0
50
100
150
200
250
300
350
400
450
500

图 8D