

[54] **TURBINE ENGINE CYCLE COUNTER**
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235/92 CA, 235/92 R
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[58] **Field of Search**.....73/116; 235/92 FQ, 92 MT, 92
CA; 324/161

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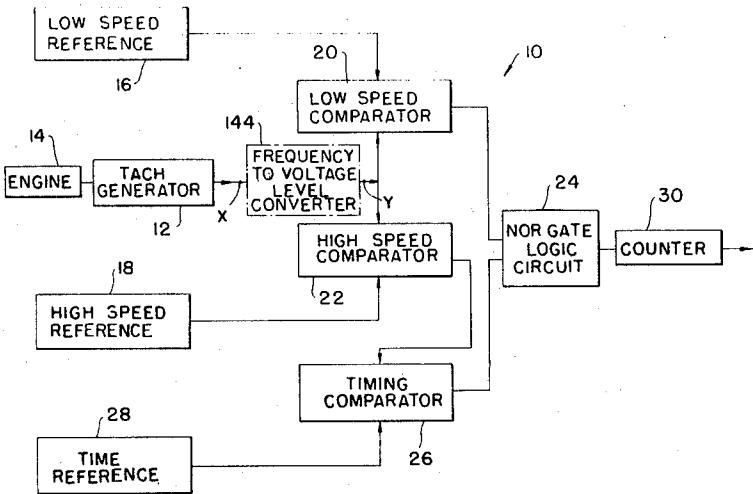
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[57] **ABSTRACT**

The number of times a turbine engine or the like is operated through a speed cycle consisting of passing upward through a predetermined selected low speed, passing upward through a predetermined selected high speed and returning downward through the high and low speeds after operating above the high speed for a predetermined selected time is counter by the structure disclosed in accordance with the method disclosed to provide an indication of engine maintenance requirements.

13 Claims, 3 Drawing Figures



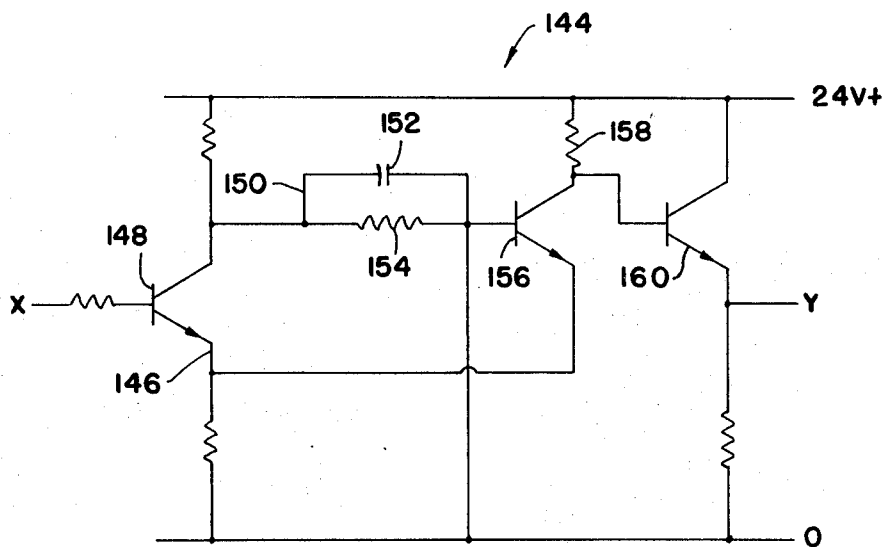
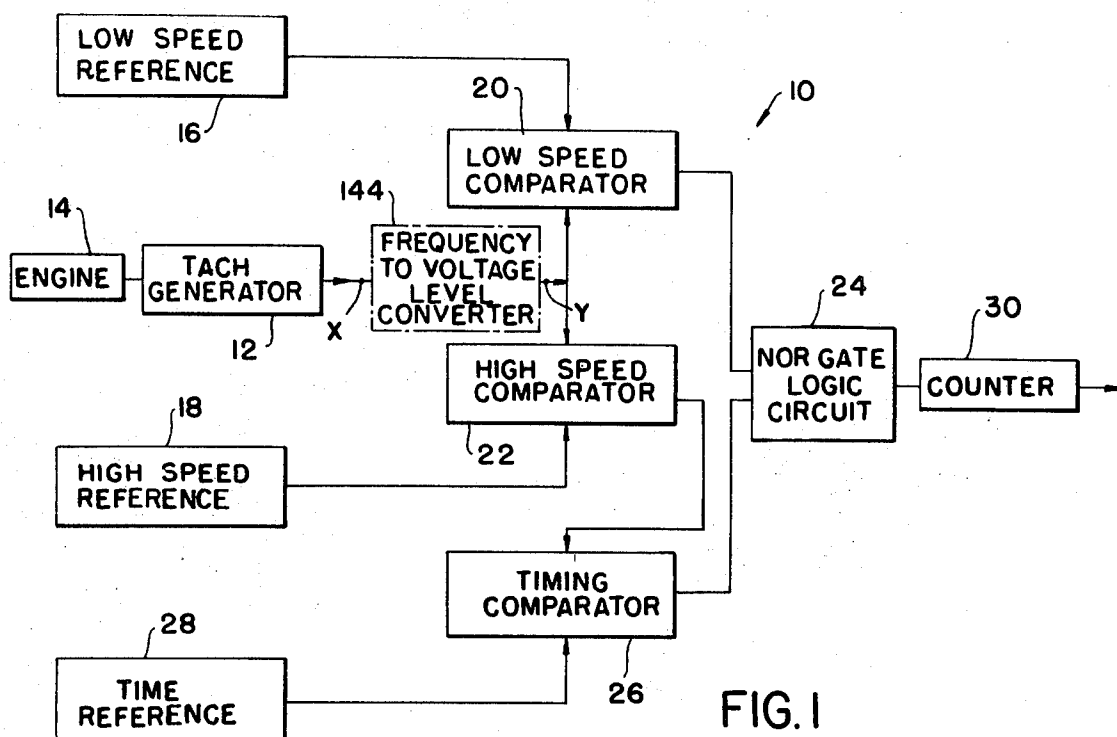


FIG. 3

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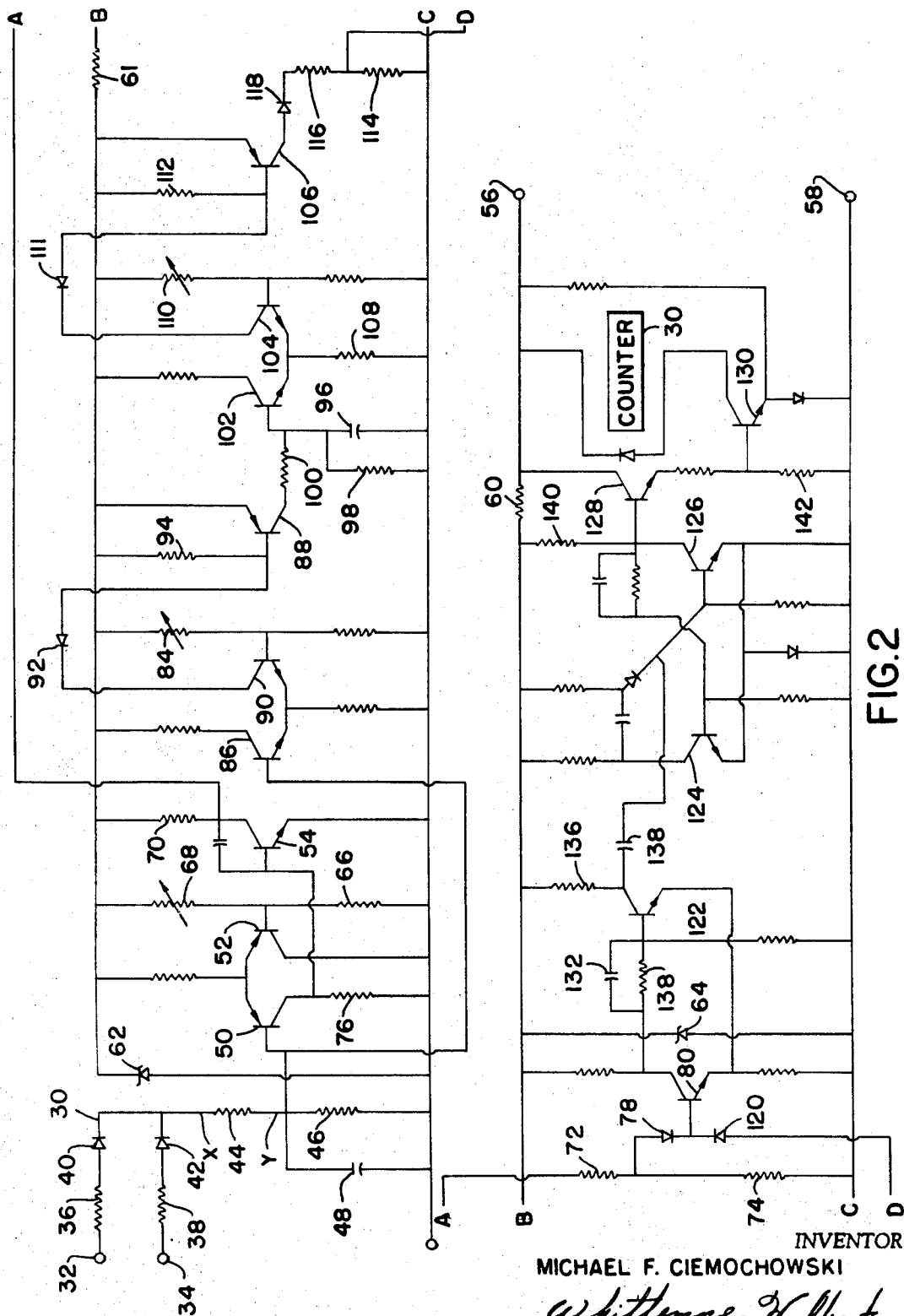


FIG. 2

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TURBINE ENGINE CYCLE COUNTER

This is a continuation of application Ser. No. 788,248, filed Dec. 31, 1968, now abandoned.

BACKGROUND OF THE INVENTION**1. Field of the Invention**

The invention relates to turbine engines and the like and refers more specifically to cycle counter structure for and a method of determining when maintenance is necessary on a turbine engine due to operational stresses caused by bringing the engine from a predetermined selected low speed to a predetermined selected high speed, maintaining the engine at or above the high speed for a predetermined selected time and subsequently bringing the engine back to the low speed or below a plurality of times.

2. Description of the Prior Art

In the past maintenance of engines, especially aircraft engines, both military and civilian, has been schedules primarily on the basis of the number of hours the engine has operated. Thus, for example, regulations may require checking of particular portions of an engine after every 100 hours of operation and may require complete removal and overhaul of the engine every 1,000 hours of operation. It has been found that such methods of scheduling engine maintenance is inadequate since engines are often overhauled before overhauling is necessary as discovered after the engines have been dismantled. Even more serious engine failures prior to standard maintenance times have been noted when maintenance is scheduled based only on hours of engine operation.

SUMMARY OF THE INVENTION

In accordance with the present invention, it has been determined that the number of times a turbine engine has been brought to a predetermined selected high speed from a predetermined selected low speed and returned to the low speed is a better indication of the need of engine maintenance than the total number of hours that the engine has been operated, particularly if the engine has been operated at the high speed for a time sufficient to bring the engine up to the normal operating temperature at the high speed.

It is high stresses at the high temperatures generated at high speed and the change from low stresses at lower temperatures to high stresses at high temperatures and back to the low stresses at low temperatures which apparently fatigue the turbine engine parts sufficiently to cause ultimate failure if the engine is not overhauled after a predetermined number of such cycles. The time of constant operation of an engine at a particular speed even though the speed may be a high speed is apparently not as damaging to an engine as repeated speed cycles of an engine operated for a lesser time.

Thus, engine maintenance should not be required as often for aircraft running on long schedules as it is on aircraft flying local flights. Transatlantic planes therefore need less maintenance than planes of commercial feeder lines.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a turbine engine cycle counter constructed in accordance with the invention.

FIG. 2 is a schematic diagram of the cycle counter illustrated in FIG. 1.

FIG. 3 is a schematic diagram of a frequency to voltage level transducer for use in a modified engine cycle counter, as illustrated in FIGS. 1 and 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

As shown best in FIG. 1, the cycle counter 10 includes a tachometer generator 12 for developing a voltage signal proportional to the speed of a turbine engine 14 or the like, a low speed reference signal circuit 16 for providing a selected voltage signal representing a predetermined low engine speed and a high speed reference signal circuit 18 for providing a selected voltage signal representing a predetermined high engine speed.

The cycle counter 10 further includes low speed and high speed comparators 20 and 22. The signals from the low speed reference signal circuit 16 and the tachometer generator 12 are compared in the low speed comparator 20 and an output signal is provided to the input of the logic circuit 24 when the voltage from the tachometer generator is greater than the voltage from the low speed reference signal circuit. Similarly, the signal from the high speed reference signal circuit 18 is compared with the signal from the tachometer generator in the high speed comparator 22 and an output signal is provided to the timing comparator 26 when the signal from the high speed reference signal circuit 18 is less than the signal from the tachometer generator.

The time reference signal circuit 28, illustrated in FIG. 1, provides an output signal to the timing comparator 26 a predetermined selected time after a signal is received by the timing comparator from the high speed comparator. On receipt of the signals from the high speed comparator 22 and the subsequent signal from the time reference signal circuit 28, the timing comparator 26 provides an output signal to the logic circuit 24.

In operation, considering the block diagram of FIG. 1, as the engine 14 goes from, for example, an idle speed to operating speed, a signal is first provided from the low speed comparator 20 to the logic circuit 24 but no output is provided from the logic circuit 24 at this time. As the engine passes through the predetermined high speed, an output signal is provided from the high speed comparator 22 to the timing comparator 26. If the engine remains at a speed above the predetermined high speed for the time determined by the time reference signal circuit 28, a signal output is provided from the timing comparator to the logic circuit 24. However, again no output is provided from the logic circuit 24 at this time.

When the engine speed is subsequently reduced, first the signal from the timing comparator 26 to the logic circuit 24 is lost, again without an output from the logic circuit 24. However, on the engine speed being reduced below that of the predetermined low speed, the signal to the logic circuit 24 from the low speed comparator 20 is also lost, at which time a single output pulse is provided from the logic circuit 24 to the cycle counter 30.

Thus, it will be seen that the structure illustrated in FIG. 1 will provide a count each time the engine is passed through a speed cycle, including passing through a predetermined low speed, subsequently

passing through a predetermined high speed and returning through the predetermined high speed and the predetermined low speed. The engine cycles are thus counted to determine the necessity of engine maintenance in a more exact manner than previously possible when such maintenance was based only on hours of engine running and not heat and varying speed stress cycles.

More specifically, the cycle counter 10, as shown in schematic form in FIG. 2, includes input pins 32 and 34 from the tachometer generator 12. The tachometer generator 12 is in the embodiment illustrated a two phase generator, one phase of which is connected to pin 32 of the cycle counter 10 and the other phase of which is connected to the pin 34 of the cycle counter 10.

The signals from the tachometer generator 12 are passed through resistors 36 and 38 and are rectified through diodes 40 and 42. The rectified signals are then passed through the voltage divider consisting of resistors 44 and 46. The capacitor 48 provides a filtering function so that the signal between the resistors 44 and 46 is substantially a steady direct current signal having a voltage proportional to the speed of the engine 14 as sensed by the tachometer generator 12.

The voltage signal proportional to engine speed is passed to the base of the transistor 50 which together with the transistor 52 and the transistor 54 and associated circuitry comprises the low speed comparator 20. In the circuit configuration shown in FIG. 2, the transistors 50, 52 and 54 are supplied with a direct current operating voltage of, for example, 24 volts through the input pins 56 and 58 of the cycle counter 10 and the dropping resistors 60 and 61. The operating voltage supplied through pins 56 and 58 for the semi-conductor components of the circuit 10 including the transistors 50, 52 and 54 is regulated by means of the Zener diodes 62 and 64.

The low speed reference signal circuit 16 includes the voltage divider consisting of resistor 66 and potentiometer 68. In the circuit configuration shown in FIG. 2, the transistor 52 is biased into a normally on or conducting condition with the speed of the engine 14 below a predetermined low speed which predetermined low speed may be selected by adjustment of the potentiometer 68. Initially with the engine 14 operating at a speed below the predetermined low speed, the transistors 50 and 54 are off or non-conducting so that no output signal is provided across the resistor 70 through the voltage divider, including resistors 72 and 74.

In operation, as the speed of the engine 14 increases and the voltage provided on the base of the transistor 50 across the resistor 46 increases, a voltage level is reached at which the transistor 50 is turned on and the transistor 52 is turned off. Turning on of the transistor 50 provides a bias signal to the transistor 54 across the resistor 76 in the circuit of the transistor 50 which causes the transistor 54 to turn on, developing a signal across the resistor 70 and through the voltage divider resistors 72 and 74. A low speed signal is thus provided across the resistor 74 through the blocking diode 78 onto the base of the transistor 80 of the logic circuit 24. However, nothing further happens in the logic circuit 24 at this time.

The high speed reference signal circuit 18, as shown in FIG. 2, includes the voltage divider, consisting of resistor 82 and potentiometer 84. The high speed comparator includes the transistors 86 and 88 which are normally on with the engine 14 operating at a speed below the predetermined high speed selected by adjustment of potentiometer 84 and the transistor 90 which is normally non-conducting at engine speeds below that necessary to generate an electrical voltage through the tachometer generator 12 greater than the high speed reference signal voltage.

When the signal from the tachometer generator applied to the base of the transistor 86 exceeds the high speed reference signal, the transistor 86 will stop conducting and the transistor 90 will conduct through the blocking diode 92 to create a voltage across the resistor 94. The voltage across the resistor 94 will cause the transistor 88 to stop conducting with the capacitor 96 substantially fully charged due to previous conduction of the transistor 88 through the resistors 98 and 100.

The capacitor 96 and resistor 98, along with transistors 102, 104 and 106 are included in the timing comparator 26 of FIG. 1. The time reference signal source 28 of FIG. 1 includes the voltage divider, comprising resistor 108 and potentiometer 110 in FIG. 2. Transistor 102 in the configuration illustrated is normally off, while transistor 88 is conducting, as is transistor 106. Transistor 104 is normally on at this time.

When transistor 88 turns off due to the speed of the engine generating a signal through the tachometer generator greater than the high speed reference signal, the transistor 102 remains off until capacitor 96 discharges through the resistor 98 sufficiently to lower the voltage on the base of the transistor 102 in accordance with the time constant of the capacitor 96 and resistor 98 to a point such that the bias on the transistor 104 set by the potentiometer 110 is no longer sufficient to maintain the transistor 104 in an on condition and transistor 102 in an off condition. At this time after the predetermined high speed has been exceeded, the transistor 102 will turn on and transistor 104 will turn off.

Turning off of the transistor 104 will remove the voltage drop across the resistor 112 in series with blocking diode 111, so that the transistor 106 will turn on to produce a voltage across the resistor 114 in series with the resistor 116 and the blocking diode 118 which is applied through the blocking diode 120 to the base of the transistor 80. Again, because of the configuration of the logic circuit 24, which includes the transistor 80, transistor 122, transistors 124, 126, 128 and 130, nothing further happens at this time in the operation of the cycle counter.

However, as the engine is subsequently lowered in speed to pass through the high speed reference signal voltage, the signal through the blocking diode 120 to the base of the transistor 80 is removed with no additional action in the logic circuit 24 which is now set to be triggered on removal of the signal on the blocking diode 78.

On subsequent lowering of the speed of the engine 14 below the low speed reference signal, the signal to the base of the transistor 80 through the blocking diode 78 will be removed at which time the transistor 80

changes state to produce a pulse of energy in the differentiating circuit, including the capacitor 132 and resistor 134 and cause conduction of the transistor 122 and an output signal across the resistor 136 through coupling capacitor 138 to cause the multivibrator including the transistors 124 and 126 and their associated circuitry to produce a voltage across the resistor 140. The amplifying transistor 128 is thus turned on to provide a signal across the resistor 142 closing the transistor switch 130 and providing an actuating pulse through the counter 30 in series with the switch 130 across the direct current operating voltage for the cycle counter 10.

Thus, it will be seen that the logic circuit 24 includes a one-shot multivibrator consisting of the transistor 80 and transistor 122 energized as a NOR gate and a multivibrator, including the transistors 124 and 126 for actuating the switching transistor 130 through the amplifier 128 to provide a count on the counter 30 each time the engine 14 passes back through a predetermined low speed after having attained a predetermined high speed for a predetermined time in accordance with the setting of the potentiometer 110.

It will be understood that the number of cycles between maintenance for any particular engine 14 will vary with the particular low and high speed settings as selected by the adjustment of the potentiometers 68 and 84 and with the time at which the engine is run above the high speed reference signal. That is to say, that if the engine is not run at a high speed for a sufficient length of time to cause the engine to heat up, the particular cycle is not generally considered to be sufficiently damaging to warrant counting in the cycle counter. Therefore, the time reference signal circuit and timing comparator have been provided in the cycle counter. If in a particular application it is determined that all cycles should be counted, the time reference potentiometer 10 can be set to a zero time effectively removing the time reference signal circuit and time comparator from the cycle counting circuit of FIGS. 1 and 2.

While one embodiment of the invention has been considered in detail, it will be understood that other embodiments and modifications are contemplated by the inventor. Thus, for example, the signal from the tachometer generator may be a signal having a frequency varying with respect to engine speed. If such is the case, it will be necessary to provide a frequency to voltage level converter 144 between the tachometer generator and the low and high speed comparators 20 and 22, as shown in FIG. 3 and as shown in phantom in the block diagram of FIG. 1.

The frequency to voltage converter illustrated in FIG. 3, comprises an overdriven amplifier circuit 146 including transistor 148, a differentiating circuit 150 including capacitor 152 and resistor 154 and transistor 156, all forming a one-shot multivibrator to produce output pulses having an amplitude across the resistor 158 proportional to engine speed, which pulses are amplified through the transistor 160 and subsequently passed to the base of the transistors 50 and 86 after being filtered to again provide a direct current signal, the voltage of which is proportional to engine speed.

It is the intention to include all such embodiments and modifications as are defined by the appended claims within the scope of the invention.

What I claim as my invention is:

1. Structure for counting the number of times an engine is passed through a speed cycle, comprising low speed sensing means operably connected to the engine for sensing the passing of the engine through a predetermined low speed, high speed sensing means operably connected to the engine for sensing the passing of the engine through a predetermined high speed, logic means operably connected to the high and low speed sensing means and responsive thereto for providing an output signal only each time the engine passing through one of the predetermined speeds after first passing from the one predetermined speed through the other predetermined speed is sensed and counter means connected to the logic means for counting the number of said output signals from the logic means.

2. Structure for counting the number of times an engine is passed through a speed cycle, comprising low speed sensing means operably connected to the engine for sensing the passing of the engine through a predetermined low speed, high speed sensing means operably connected to the engine for sensing the passing of the engine through a predetermined high speed, logic means operably connected to the high and low speed sensing means and responsive thereto for providing an output signal only each time the engine passing down through the predetermined low speed after first passing from the predetermined low speed through the predetermined high speed is sensed and counter means connected to the logic means for counting the number of said output signals from the logic means.

3. Structure as set forth in claim 2 and further including timing means operably connected to the high speed sensing means and means for providing an output signal to inhibit an output signal until the engine has remained at a speed above said predetermined high speed for a predetermined time.

4. Structure as set forth in claim 2 and further including a transducer positioned between the engine and at least one of the sensing means permitting sensing of a specific engine parameter as an indication of at least one of the predetermined engine speeds.

5. Structure for counting the number of times an engine is passed through a speed cycle, comprising low speed sensing means operably connected to the engine for sensing the passing of the engine through a predetermined low speed including means for providing a low speed reference signal, means for providing a signal proportional to engine speed and a low speed comparator for comparing the low speed reference signal and signal proportional to engine speed connected to the means for providing a low speed reference signal and the means for providing a signal proportional to engine speed for providing an output signal when the signal proportional to engine speed is above the low speed reference signal, high speed sensing means operably connected to the engine for sensing the passing of the engine through a predetermined high speed including means for providing a high speed reference signal and a high speed comparator for comparing the high speed reference signal and signal proportional to engine speed connected to the means for providing a high speed reference signal and the means for providing a signal proportional to engine speed for providing an output signal when the signal

proportional to engine speed is above the high speed reference signal and means operably connected to the high and low speed comparators for providing an output signal only each time the engine passes down through the predetermined low speed after first passing from the predetermined low speed through the predetermined high speed including a logic circuit having a one-shot multivibrator, a bi-stable multivibrator, a switch, an amplifier and a counter in series providing a single count on removal of the low speed comparator and the high speed comparator output signals from the one-shot multivibrator.

6. Structure as set forth in claim 5 and further including means for providing a time reference signal and a timing comparator connected to the means for providing a time reference signal and between the high speed comparator and the logic circuit for permitting signals to pass from the high speed comparator to the logic circuit only after the engine has operated above the predetermined high speed for a predetermined time.

7. Structure as set forth in claim 5 and further including a frequency to voltage transducer positioned between the means for providing a signal proportional to engine speed and the comparators.

8. Structure for counting the number of times an engine is passed through a speed cycle, comprising means for providing a low speed reference signal, means for providing a high speed reference signal, means for providing a signal proportional to engine speed, a low speed comparator connected to the means for providing a low speed reference signal and to the means for providing a signal proportional to engine speed for providing a low speed comparator output signal when the signal proportional to engine speed is greater than the low speed reference signal, a high speed comparator connected to the means for providing a high speed reference signal and to the means for providing a signal proportional to engine speed for providing a high speed comparator output signal when the signal proportional to engine speed is greater than the high speed reference signal, a logic circuit connected to the low speed and high speed comparators operable to provide a logic circuit output signal on receiving a first low speed comparator output signal from the low speed comparator, a high speed comparator output signal from the high speed comparator and a subsequent signal from the low speed comparator indicating passage of the engine speed back through the low speed reference, and a counter connected to the logic circuit for providing a

single count in response to each said logic circuit output signal.

9. Structure as set forth in claim 8 and further including means for developing a time reference signal and a timing comparator connected to the high speed comparator and the means for developing a time reference signal for permitting an output signal from the high speed comparator to the logic circuit only after an output signal from the high speed comparator has been present for a predetermined time.

10. Structure as set forth in claim 8 wherein the means for developing a signal proportional to engine speed includes a tachometer generator connected to the engine operable to rotate at a speed proportional to engine speed and a frequency to voltage level converter connected between the tachometer generator and the comparators.

11. The method of determining the number of times an engine is passed through a speed cycle comprising providing a low speed reference signal, providing a high speed reference signal, providing a signal proportional to engine speed, comparing the low speed reference signal to the signal proportional to engine speed and providing a low speed output signal only when the signal proportional to engine speed is greater than the low speed reference signal, comparing the high speed reference signal with the signal proportional to engine speed and providing a high speed output signal only when the signal proportional to engine speed is greater than the high speed reference signal, providing a logic output signal in response to the high and low speed output signals indicating an engine speed greater than the low speed reference signal followed by an engine speed greater than the high speed reference signal and a subsequent engine speed lower than the low speed reference signal and providing an indication of the number of said logic output signals provided.

12. The method as set forth in claim 11 and further providing a reference time signal and permitting a high speed output signal indicating the passing of the engine through a speed greater than the high speed reference signal only after the engine speed has been maintained higher than the high speed reference signal for a predetermined time.

13. The method as set forth in claim 11 wherein the signal proportional to engine speed is first developed as an alternating frequency proportional to engine speed and subsequently converted into a voltage level signal.

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