

Aug. 25, 1970

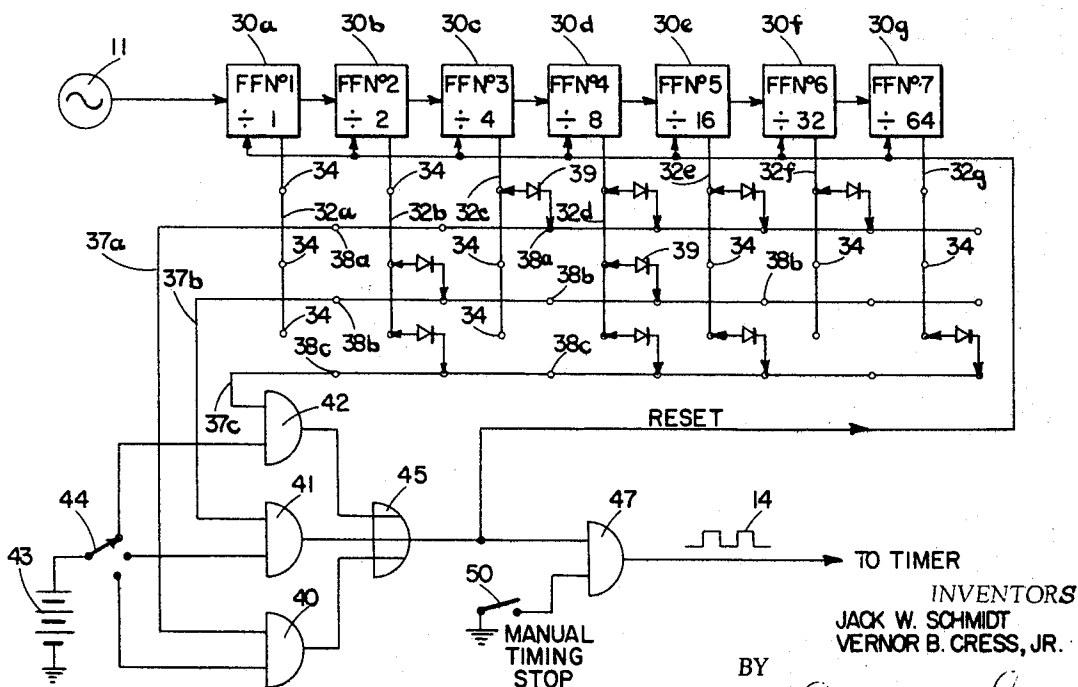
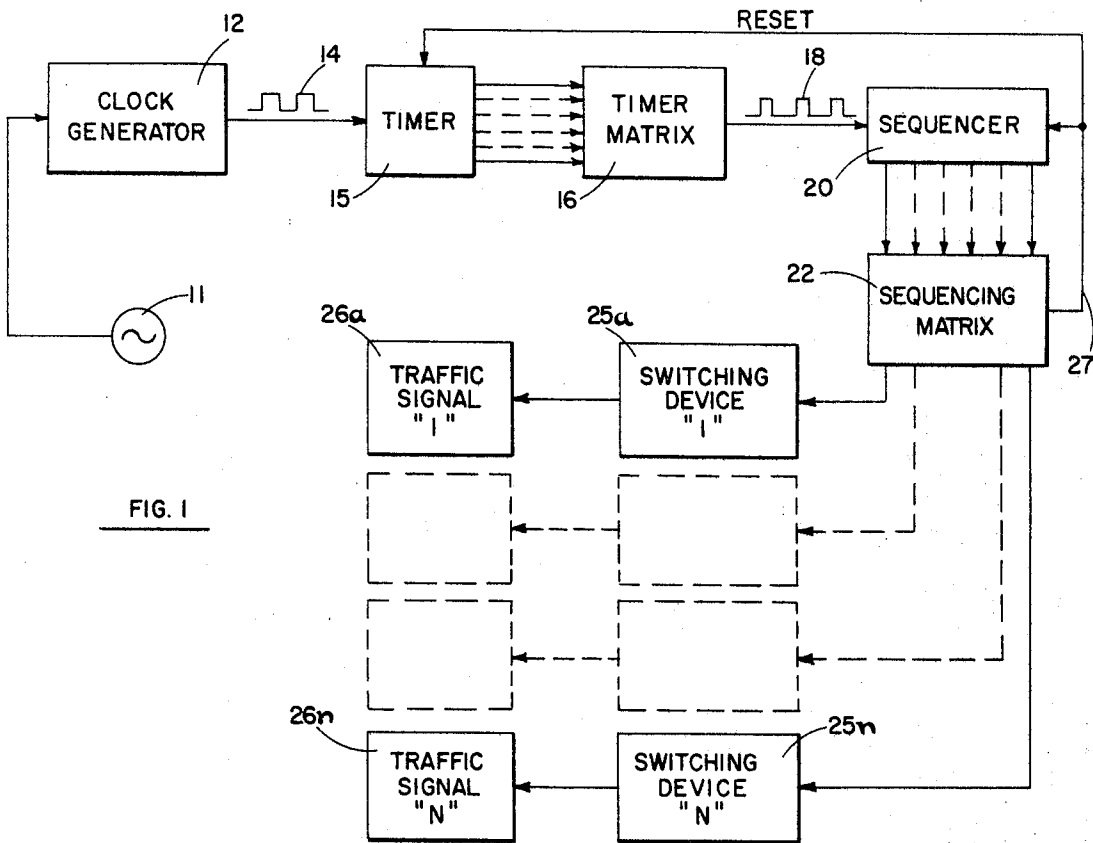
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3,525,980

FIXED TIMING TRAFFIC CONTROL SYSTEM

Filed Aug. 16, 1966

4 Sheets-Sheet 1



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FIXED TIMING TRAFFIC CONTROL SYSTEM

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4 Sheets-Sheet 2

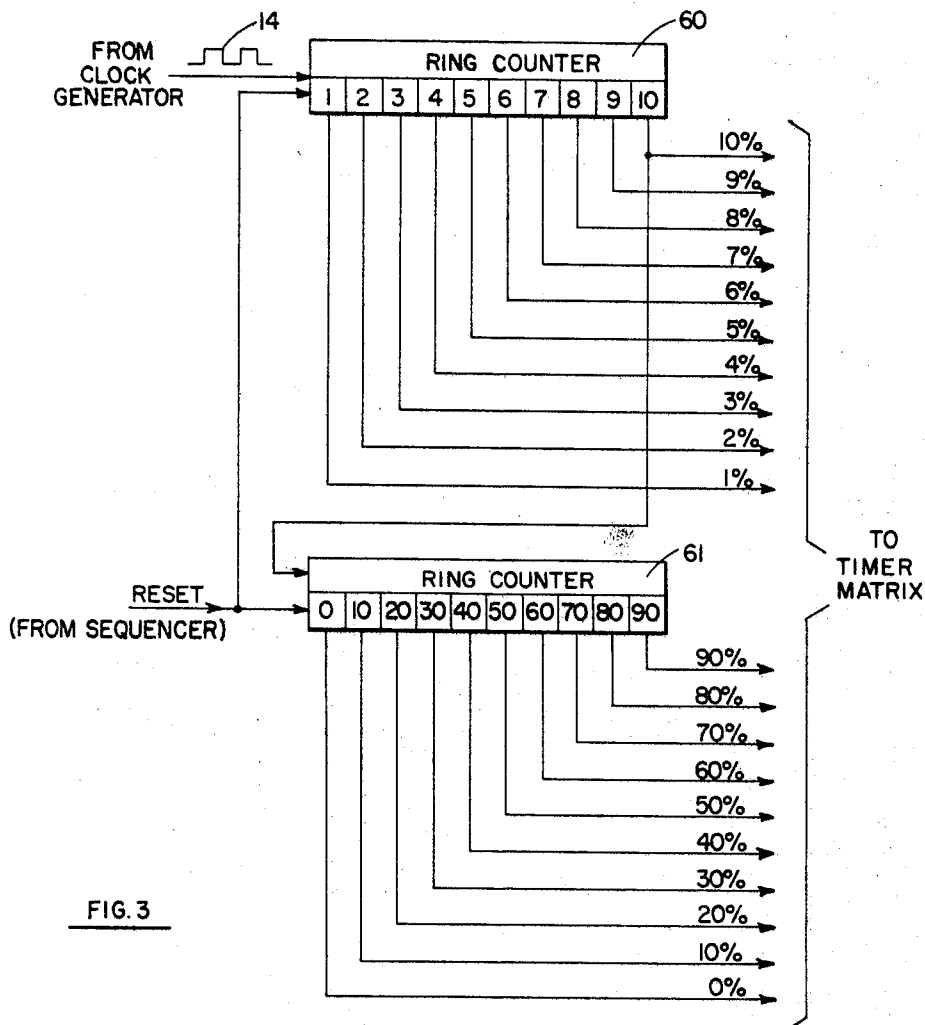


FIG. 3

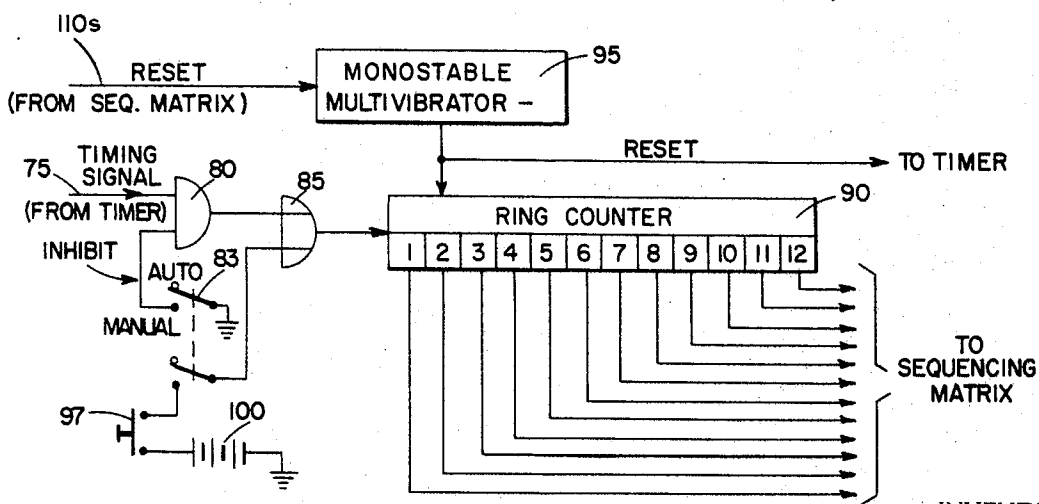


FIG. 5

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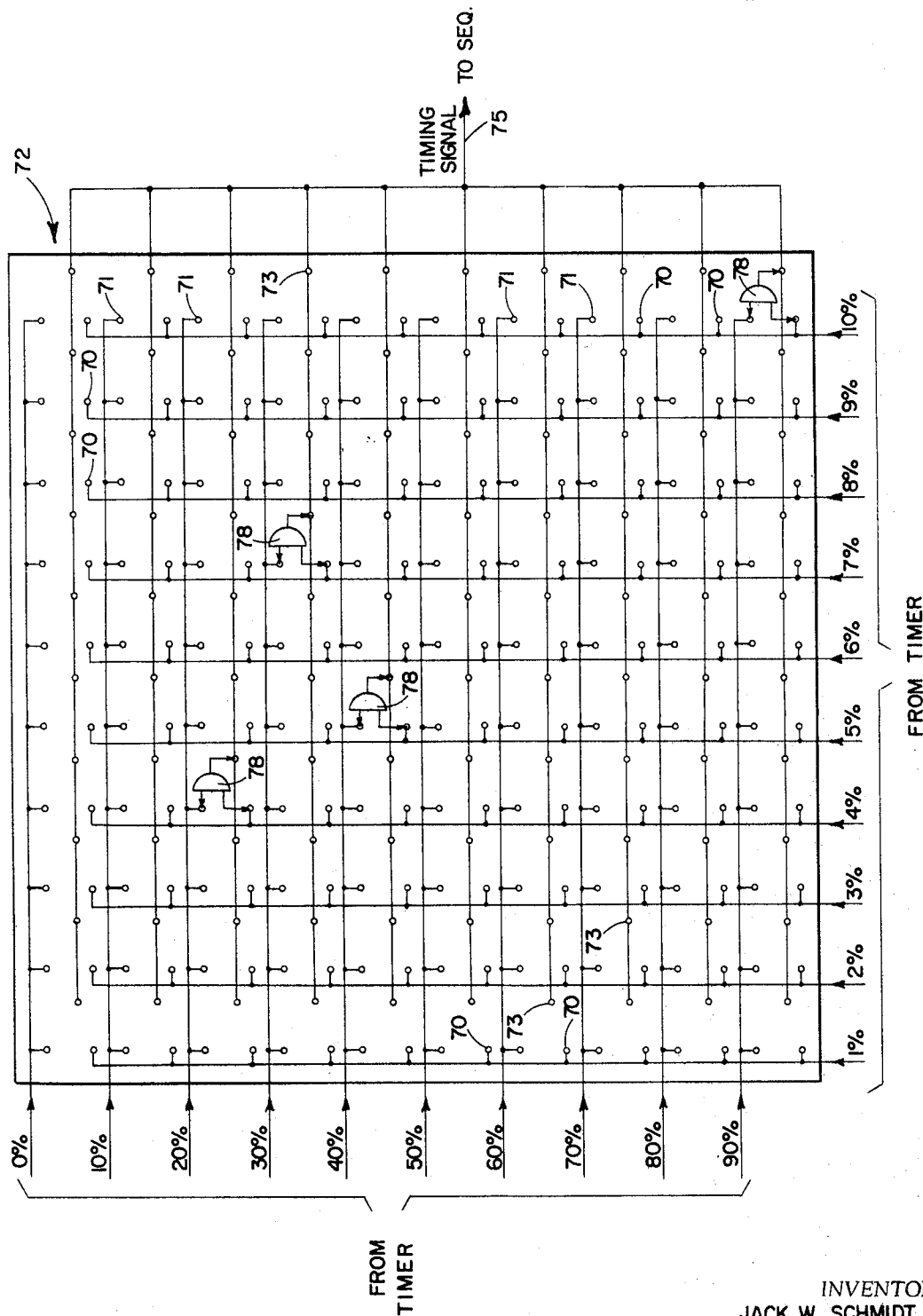
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FIXED TIMING TRAFFIC CONTROL SYSTEM

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4 Sheets-Sheet 3



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FIXED TIMING TRAFFIC CONTROL SYSTEM

Filed Aug. 16, 1966

4 Sheets-Sheet 4

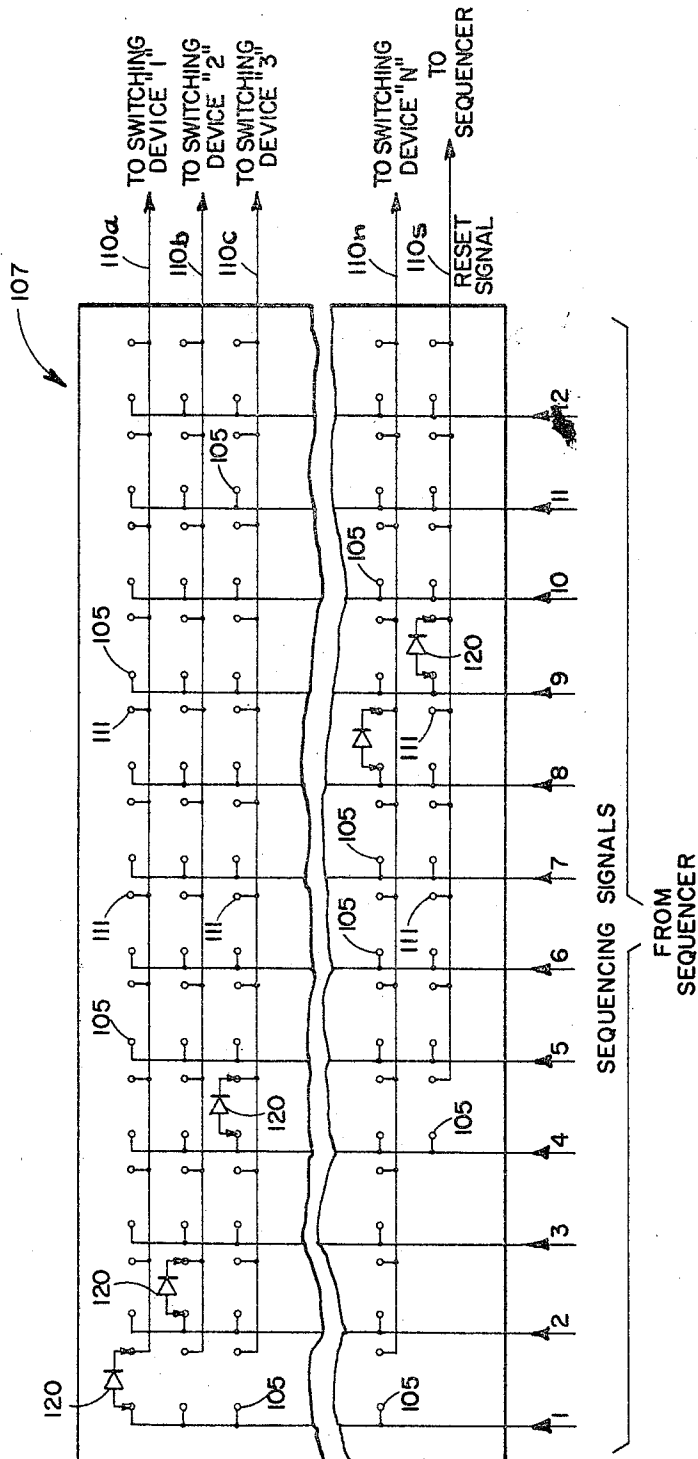


FIG. 6

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FIXED TIMING TRAFFIC CONTROL SYSTEM
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Int. Cl. G08g 1/07

U.S. Cl. 340—41

14 Claims

ABSTRACT OF THE DISCLOSURE

A clock generator is synchronized to the AC power line and has a selection matrix for generating timing pulses at any one of a number of timing rates. The output of the clock generator is utilized to drive a timer unit which includes a timer matrix which enables the selection of timing signals representing various percentages of a total timing cycle. The signals from the timer matrix are utilized to drive a sequencer unit as each timing interval is completed, a selection matrix being provided in the sequencer to enable the selection of any of the sequence signals to control particular traffic control switching operation.

This invention relates to a fixed timing traffic control system and more particularly to such a system utilizing digital techniques which lends itself to solid state circuitry.

Fixed timing traffic control systems of the prior art generally utilize electromechanical timers such as timing dials, which are rotatably driven by a motor mechanism and are arranged to actuate relay control circuits at appropriate positions in their rotation cycles. Such systems have several shortcomings. Firstly, they tend to be rather bulk and heavy, making their installation, handling and servicing somewhat more cumbersome than would be desired. Further, this type of unit generally consumes considerably more power and dissipates more heat than is the case with solid state control circuitry. Such systems of the prior art further do not lend themselves to modular construction, and their adaptability and versatility of operation is somewhat limited. Timing dial mechanizations also have the inherent shortcomings of analog timing which requires initial calibration with an accurate time-piece and fairly frequent recalibration to provide even moderately accurate timing. It also takes a fair amount of time and effort to set up a new timing and/or control program in such prior art devices.

The system of this invention provides a significant improvement over prior art traffic control systems in a digitally implemented mechanization utilizing solid state components which has a high degree of versatility of operation and which is adapted for relatively simple reprogramming of its timing operation and control functions in the field. With the utilization of solid state components in the digital implementation of the device of the invention, the bulk, weight and power consumption of the system is minimized. Further, the system units are designed so that they can readily be removed and replaced as necessary for servicing or modification of operation. Also, extremely accurate timing is obtained in the device of the invention by the synchronization of the digital timing units utilized with the AC power line.

The system of the invention utilizes a clock generator which is synchronized with the AC power line and which can be adjusted to generate timing pulses at any one of a number of timing rates. The clock generator is utilized to drive a timer unit in the form of a ring counter which generates a series of timing signals which are fed to a timer matrix. The timer matrix provides interconnecting

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means in the form of a patch panel which is set up so that timing signals can be preselected by appropriately connecting various portions of the matrix to an output line. The signals on the timer matrix output line are utilized to drive a sequencer, which may comprise a ring counter, to advance the sequence of operation as each timing signal appears. The sequencer outputs are connected to a sequencing matrix where patch interconnections can be made to cause any of the sequence signals to control any desired switching operation.

In this manner, high accuracy and great versatility of operation is made possible and the timing program and control can be rapidly and easily changed in the field as may be desired.

It is therefore an object of this invention to provide an improved fixed timing traffic controller.

It is a further object of this invention to provide a fixed timing traffic controller utilizing solid state circuitry and digital techniques which has great versatility of operation.

It is still another object of this invention to provide a traffic controller having more compact construction and lower power requirements than prior art systems.

It is still another object of this invention to provide an improved traffic control system which readily lends itself to modular construction.

It is a further object of this invention to provide a fixed timing traffic control system having greater reliability and accuracy than prior art systems.

It is still a further object of this invention to provide a fixed timing traffic control system which readily lends itself to the reprogramming of its timing operation and control in the field.

Other objects of this invention will become apparent from the following description taken in connection with the accompanying drawings, of which:

FIG. 1 is a block diagram illustrating the general features of the system of the invention,

FIG. 2 is a functional schematic drawing of a clock generator which may be used in a preferred embodiment of the device of the invention,

FIG. 3 is a functional schematic drawing of the timer unit of the preferred embodiment of the device of the invention,

FIG. 4 is a schematic drawing illustrating the timer matrix of the preferred embodiment of the device of the invention,

FIG. 5 is a functional schematic drawing of the sequencer of the preferred embodiment of the device of the invention, and

FIG. 6 is a schematic drawing of the sequencing matrix of the preferred embodiment of the device of the invention.

Referring now to FIG. 1, a block diagram of the system of the invention is shown. Synchronizing signals are fed from AC power source 11 to clock generator 12 to synchronize the timing operation of clock generator 12 at the power source frequency. Clock generator 12, as described more fully in connection with FIG. 2, frequency divides the output of the power source to produce timing pulses 14, which are accurately synchronized with such source. In view of the generally precision nature of the frequency regulation of most commercial power sources, pulses 14 provide highly accurate timing.

Pulses 14 which may, for example, be at a rate of one per second, are fed as clock pulses to timer 15. Timer 15, which may for example comprise a ring counter circuit, generates a series of successive timing signals in response to successive clock pulses 14, the first of such signals appearing one second after the initial starting time of the system, the second of such pulses appearing after two seconds, the third of such pulses after three seconds,

etc., in the case of clock pulses at the rate of one per second. Each of the successive timing outputs of timer 15 is fed to a separate "grid" of timer matrix 16. As to be explained fully in connection with FIG. 4, means are provided to connect any combination of timer matrix grid portions into the matrix output line so as to provide timing signals 18 to sequencer 20 at the preselected timing points.

Sequencer 20, which may comprise a ring counter, advances to a succeeding sequence each time a timing pulse 18 is received thereby. The various sequencing stages of sequencer 20 are separately fed to associated grids of sequencing matrix 22. Means are provided in sequencing matrix 22 to connect any of the sequencing matrix grid portions to a respective associated switching device 25a-25n. Each such switching device is thus responsive to the actuation of an associated sequence of sequencer 20. Sequencing matrix 22 can be readily set up in the field as may be desired to actuate any of the switching devices in response to any sequence. Each of switching devices 25a-25n controls a separate traffic signal 26a-26n or other traffic control function, as the case may be.

A reset signal is provided on line 27 from sequencing matrix 22 to both sequencer 20 and timer 15 to reset the timer and sequencing operation when any preselected sequence is reached, such sequence in effect establishing the completion of the timing cycle and effecting the start of a new timing cycle.

Let us now examine the various units comprising a preferred embodiment of the system of the invention. Referring to FIG. 2, a functional schematic drawing of the clock generator unit of the preferred embodiment of the invention is shown. Flip-flop units 30a-30g are connected in cascade to form a binary divider, each successive stage dividing the output of the prior stage by two. The output of each of the divider flip-flop stages 30a-30g is fed to an appropriate output line 32a-32g, respectively, each of which is connected to a group of contact points 34, to form the grids of a matrix. Lines 37a-37c each is connected to a separate group of associated contact points 38a-38c to form separate matrix grids running transversely to the aforementioned grids. Lines 37a-37c are each connected to a respective one of AND gates 40-42. Key members 39, which include diodes, may be used to interconnect any of contacts 34 with an adjoining one of contacts 38 to make for various pulse rate clock pulses on each of lines 37a-37c. In an operative embodiment of the device of the invention, key members 39 are in the form of plug-in units with the matrix in the form of a patch panel, but any other type of switching arrangement may be utilized if so desired.

The key members 39 as combined to connect various flip-flop outputs to any one of lines 37a-37c form a logical gating circuit. As shown in FIG. 2, if we assume that power source 11 is 60 cycle, then with the key members 39 connected as indicated, line 37a will have one second timing pulses, line 37b will have 1/2 second timing pulses, and line 37c will have 1.5 second timing pulses. Thus, it can be seen that the key members can be arranged to produce a great variety of different clock pulses on each of lines 37a-37c. Any one of the clock signals set up on lines 37a-37c can be selected for utilization by means of switch 44. Switch 44 operates to connect a positive potential from DC power source 43 to one of AND gates 40-42 to provide a keying signal for the selected gate. Thus, whichever one of the AND gates is connected by means of switch 44 to power source 43 will pass the clock signal fed thereto to OR gate 45. Switch 44 may be controlled remotely or may be set manually.

The clock signal is fed from OR gate 45 to AND gate 47. A switch 50 is connected in circuit with AND gate 47 to provide an inhibit signal thereto to stop the timing operation if so desired. Switch 50 may be manually controlled. The output of OR gate 45 is fed back to each of flip-flop stages 30a-30g as a reset signal therefor, so that

with the appearance of each clock pulse the divider stages are reset to institute a new dividing cycle.

Referring now to FIG. 3, the clock pulse output 14 of the clock generator is fed to ring counter 60 of the timer unit. Ring counter 60 operates to successively produce outputs at each of its stages 1-10 in response to clock pulses 14. An output remains at any stage of the ring counter until the counter is again driven by one of clock pulses 14 to move the output to a succeeding stage. Thus, for example, with clock pulses 14 spaced by one second, one second duration pulses will appear sequentially at output stages 1-10, with the signal appearing at stage "10" ten seconds after the arrival of the first clock pulse to actuate ring counter 60.

The output of the stage "10" of ring counter 60 is fed as an input signal to ring counter 61 which is identical in configuration to ring counter 60. Thus, with one second clock pulses 14, the output stages of ring counter 61 will successively be activated at ten-second timing intervals. The outputs of the stages of ring counters 60 and 61 are marked in "percent" in FIG. 3, this being indicative of the percentage of the maximum timing interval capability of the timer which they represent. Thus, for example, with one-second clock pulses 14 making for a maximum timing interval of 100 seconds, the output marked "50%" represent a 50-second timing interval, while the output stage marked "4%" represent a 4-second timing interval, etc. With other value clock pulses, these percentages would of course represent different absolute timing intervals.

A reset signal is provided from the sequencer, as to be explained further on in the specification, to reset both ring counters 60 and 61 at an appropriate timing sequence.

Referring now to FIG. 4, the "1%-10%" outputs of ring counter 60 are each fed to a separate series of contacts 70 forming separate grids of matrix panel 72. Similarly, the "0%-90%" outputs of ring counter 61 are fed to associated terminals 71 arranged to form grids of the matrix panel running transverse to the "1%-10%" grids. Terminals 73 which form output terminals are all connected together and to timing signal output line 75.

Contacts 70, 71 and 73 form patch terminals, adjoining ones of said terminals being interconnectable as may be desired, by means of key members 78. Such key members are shown in plug-in form to indicate that they are removable and can be placed in any portion of the patch panel as application requirements may dictate. Also, a various number of such key members may be utilized, depending on the number of timing sequences desired.

Each of key members 78 comprises an AND gate which when placed in any plug-in position in panel 72 provides a timing sequence which combines two selected outputs, one from ring counter 60 and the other from ring counter 61. Thus, any combination of the timing signals can be set up on the patch panel to provide a corresponding series of timing outputs on line 75. To illustrate this, with the key member 78 set up as indicated in FIG. 4, timing signals will be generated at the times corresponding to 24%, 37%, 45%, and 100% of the total timing interval. In the case of one-second clock pulses, these percentages would be 24 seconds, 37 seconds, 45 seconds, and 100 seconds after the commencement of the timing cycle.

Referring now to FIG. 5, the timing signal from the timer matrix is fed on line 75 to AND gate 80 in the sequencer. With switch 83 in the "auto" position, the timing signal is fed through AND gate 80 and OR gate 85 to ring counter 90. Ring counter 90 is similar in its general configuration to the ring counters 60 and 61, which have been described in connection with FIG. 3, and operates to sequentially produce an output at each of its stages in response to successive input signals fed thereto. Thus, initially, stage "1" of ring counter 90 is in the "on" state and with the arrival of the first timing signal on line 75, the output is shifted to stage "2"; with the second timing signal the output will be shifted to stage "3," and

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so on. Each counter stage output thus represents a predetermined timing interval. Ring counter 90 is reset to reinitiate its sequential count by means of a reset signal which originates in the sequencing matrix, as to be explained in connection with FIG. 6, such signal being fed to monostable multivibrator 95; the output of the multivibrator providing the required relatively sharp reset pulse.

If it is desired to manually advance the sequencer, switch 83 may be thrown to the "manual" position. Under such conditions a grounding "inhibit" signal is fed to AND gate 80, preventing the passage of any timing signals which may arrive on line 75 therethrough to OR gate 85. At the same time, the lower ganged portion of switch 83 provides a connection to OR gate 85 from manual sequence advance switch 97. When manual sequence advance switch 97 is actuated, a voltage is applied from power source 100 through OR gate 85 to ring counter 90 to provide an actuation pulse to advance the counter one step.

Referring now to FIG. 6, the sequencing signal outputs from the various stages of ring counter 90 are each fed to a separate set of contacts 105, each such set forming a grid of sequencing matrix panel 107. Each of output lines 110a-110n is connected to a separate set of terminals 111, forming grids of the matrix panel running transverse to the first mentioned grids. Each of output lines 110a-110n is fed to a separate respective switching device 25a-25n to provide a control for a separate function, as indicated in FIG. 1. A control line 110s is connected to one set of terminals 111 to carry a reset signal for use in resetting the sequencer and the timer.

Patch key members 120 are utilized to interconnect any of the sequencer outputs to any of the output control lines 110a-110n and 110s, as may be desired. Key members 120 comprises diodes to assure that there is only unidirectional signal coupling from the sequencing matrix to the various switching devices.

With patching key members 120 in the positions indicated in FIG. 6, switching device "1" is actuated at the start of the first timing sequence, switching device "2" at the start of the second timing sequence, switching device "3" at the start of the 4th timing sequence and switching device "N" at the start of the 8th switching sequence, the reset signal being generated at the start of the 9th timing sequence. In this manner, various control functions can be made to occur as the sequencer advances through its operation cycle, with a resetting of the sequencer and the timer being accomplished when all the switching operations have been completed, this in response to one of the sequencing signals.

It is to be noted that the matrices utilized for setting up both the timing and sequencing operations greatly facilitate and simplify the initial setting up and the changing of the program for the traffic controller. This arrangement as operated in conjunction with associated digital control also makes for great versatility of operation which can be implemented rapidly and simply.

The system of this invention thus provides a fixed timing traffic control system utilizing digital techniques which has the advantages of compactness, simplicity, reliability and accurate timing operation. Further, the system lends itself to modular construction and has great versatility in its programming capability by virtue of its matrix interconnection structure which facilitates the rapid set up of programming and control functions to suit the requirements at hand.

While the device of the invention has been described and illustrated in detail, it is to be clearly understood that this is intended by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of this invention being limited only by the terms of the following claims.

We claim:

1. A fixed timing traffic control system for controlling traffic signals comprising:

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a clock generator for generating clock pulses, timer means for generating a series of timing signals representing percentages of a total timing cycle, said timer means being driven by the clock pulse output of said clock generator,

timer matrix means having a plurality of input channels forming a grid, the timing signal outputs of said timer means each being fed to an associated one of said channels, each position on said grid representing a predetermined percentage of the total timing cycle, said timer matrix means including a common output line and means for interconnecting selected ones of said grid positions to said output line to provide predetermined combinations of said timing signal outputs on said output line, said timing signal outputs each representing timing functions which are a portion of the total timing cycle,

sequencer means responsively connected to said output line for generating a sequence advance signal in response to each successive timing signal output, said sequencer means having a plurality of output control lines, each of said output control lines corresponding to a separate timing sequence,

a plurality of switching means for controlling the operation of said traffic signals, and

means for selectively connecting any of said sequencer means output control lines to any of said switching means, each of said switching means operating in response to the signals on the control line connected thereto.

2. The system as recited in claim 1 and additionally including an AC power source, said clock generator being synchronized with the AC power source.

3. The system as recited in claim 1 wherein said means for selectively connecting said sequencer means output lines to said switching means comprises a patch panel having groups of contacts connected respectively to each of said control lines and said switching means, and key members for interconnecting preselected ones of said contacts.

4. The system as recited in claim 1 wherein said timer comprises ring counter means connected to provide output signals at timing intervals between one percent and one hundred percent of a predetermined maximum timing interval.

5. The system as recited in claim 1 wherein said sequencer means comprises a ring counter, each of said control lines being connected to a separate stage of said ring counter.

6. A fixed timing traffic control system for controlling traffic signals comprising:

an AC power source,

a clock generator for generating clock pulses, said clock generator being synchronized with said AC power source,

timer means for generating a series of timing signals representing percentages of a total timing cycle, said timer means being driven by the clock pulse output of said clock generator,

a timer matrix having a plurality of input channels forming a matrix grid, the timing signal outputs of said timer means each being fed to an associated one of said channels, each position on said grid representing a predetermined percentage of the total timing cycle, said timer matrix including a common output line and means for interconnecting selected ones of said grid positions to said output line to provide predetermined ones of said timing signal outputs on said output line, each of said timing signal outputs providing a timing function which is a portion of the total timing cycle,

sequencer means responsively connected to said output line for generating a sequence advance signal in response to each successive timing signal, said sequencer means having a plurality of output lines,

each of said sequencer means output lines corresponding to a separate sequence of operation,

a sequencing matrix having a plurality of input channels forming a grid, the output lines of said sequencer means each being connected to an associated one of said channels, said sequencing matrix including a plurality of output control lines and means for interconnecting selected ones of said sequencing matrix grid positions to selected ones of said output control lines, and

a plurality of switching means for controlling the operation of said traffic signals, each of said switching means being connected to receive one of said sequencing matrix output control lines and operating in response to the signals thereon.

7. The system as recited in claim 6 wherein said timer matrix and said sequencing matrix each comprises a patch panel, said interconnecting means comprising plug-in key members for said patch panels.

8. The system as recited in claim 6 wherein said timer comprises first and second ring counters, the stages of said counters respectively providing output signals at timing intervals between 1-9% and 10-100% of a predetermined maximum timing interval.

9. The system as recited in claim 8 wherein said timer matrix grids each are connected to receive an output from one of said timer ring counter stages.

10. The system as recited in claim 6 wherein said sequencer means comprises a ring counter, the outputs of the stages of said ring counter being connected to said sequencer means output lines.

11. The system as recited in claim 6 and further including means for interconnecting one of the output control lines of said sequencing matrix with said sequencer and said timer to provide a reset signal therefor.

12. A fixed timing traffic control system for controlling traffic signals comprising:

an AC power source,

a clock generator synchronized with said AC power source for generating clock pulses, said clock generator comprising a flip-flop divider and a matrix connected to receive the various outputs of said divider and key means for interconnecting said matrix to select various pulse rate clock pulses,

a timer for generating a series of timing signals, said timer being driven by the clock pulse output of said clock generator,

timer interconnecting means having a plurality of input channels, the timing signal outputs of said timer each being fed to an associated one of said channels, said timer interconnecting means including a common output line and means for interconnecting selected ones of said channels to said output line to provide predetermined ones of said timing signal outputs on said output line,

sequencer means responsively connected to said output line for generating a sequence advance signal in response to each successive timing signal, said sequencer means having a plurality of output control lines, each of said output control lines corresponding to a separate timing sequence,

a plurality of switching means for controlling the operation of said traffic signals, and

means for selectively connecting any of said sequencer means output control lines to any of said switching means, each of said switching means operating in response to the signals on the control line connected thereto.

13. A fixed timing traffic control system for controlling traffic signals comprising:

an AC power source,

a clock generator for generating clock pulses, said clock generator being synchronized with said AC power source,

a timer for generating a series of timing signals, said

timer being driven by the clock pulse output of said clock generator, said timer comprising first and second ring counters, the stages of said counters respectively providing output signals at timing intervals between 1-9% and 10-100% of a predetermined maximum timing interval,

a timer matrix having a plurality of input channels forming a matrix grid, the timing signal outputs of said timer each being fed to an associated one of said channels, said timer matrix including a common output line and means for interconnecting selected ones of said grid positions to said output line to provide predetermined ones of said timing signal outputs on said output line, said timer matrix channels each being connected to receive an output from one of said timer ring counter stages, the stages of one of said counters being connected to a first set of said timer matrix channels and the stages of the other of said counters being connected to a second set of said timer matrix channels running transverse to said first set, said interconnecting means comprising AND gate means for gating signals from preselected ones of said grid positions,

sequencer means responsively connected to said output line for generating a sequence advance signal in response to each successive timing signal, said sequencer means having a plurality of output lines, each of said sequencer means output lines corresponding to a separate sequence of operation,

a sequencing matrix having a plurality of input channels forming a grid, the output lines of said sequencer means each being connected to an associated one of said channels, said sequencing matrix including a plurality of output control lines and means for interconnecting selected ones of said sequencing matrix grid positions to selected ones of said output control lines, and

a plurality of switching means for controlling the operation of said traffic signals, each of said switching means being connected to receive one of said sequencing matrix output control lines and operating in response to the signals thereon.

14. A fixed timing traffic control system for controlling traffic signals comprising:

an AC power source,

a clock generator for generating clock pulses, said clock generator being synchronized with said AC power source and comprising a flip-flop divider, a matrix for receiving the outputs of the stages of said divider, said matrix having a common output line, and key means for selectively interconnecting said divider stages with said output line to provide various preselected pulse rate clock pulses on said line,

a timer for generating a series of timing signals, said timer driven by the clock pulse output of said clock generator,

a timer matrix having a plurality of input channels forming a matrix grid, the timing signal outputs of said timer each being fed to an associated one of said channels, said timer matrix including a common output line and means for interconnecting selected ones of said grid portions to said output line to provide predetermined ones of said timing signal outputs on said output line,

sequencer means responsively connected to said output line for generating a sequence advance signal in response to each successive timing signal, said sequencer means having a plurality of output lines, each of said sequencer means output lines corresponding to a separate sequence of operation,

a sequencing matrix having a plurality of input channels forming a grid, the output lines of said sequencer means each being connected to an associated one of said channels, said sequencing matrix including a plurality of output control lines and means for inter-

connecting selected ones of said sequencing matrix grid positions to selected ones of said output control lines, and
 a plurality of switching means for controlling the operation of said traffic signals, each of said switching means being connected to receive one of said sequencing matrix output control lines and operating in response to the signals thereon.

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U.S. Cl. X.R.

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