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- (71) **Applicant: BITMAIN TECHNOLOGIES INC.**
[CN/CN]; F2, Building 25, Courtyard 1, Baosheng South Road, Haidian District, Beijing 100192 (CN).
- (72) **Inventors: SUN, Guochen;** F2, Building 25, Courtyard 1, Baosheng South Road, Haidian District, Beijing 100192 (CN). **YANG, Cunyong;** F2, Building 25, Courtyard 1, Baosheng South Road, Haidian District, Beijing 100192 (CN). **ZHAN, Micree;** F2, Building 25, Courtyard 1, Baosheng South Road, Haidian District, Beijing 100192 (CN).
- (74) **Agent: LEADER PATENT & TRADEMARK FIRM;** 8F-6, Bldg. A, Winland International Center, No.32 Xizhimen North Street, Haidian District, Beijing 100082 (CN).
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(54) **Title:** COMPUTATIONAL SYSTEM AND CORRESPONDING ELECTRONIC APPARATUS

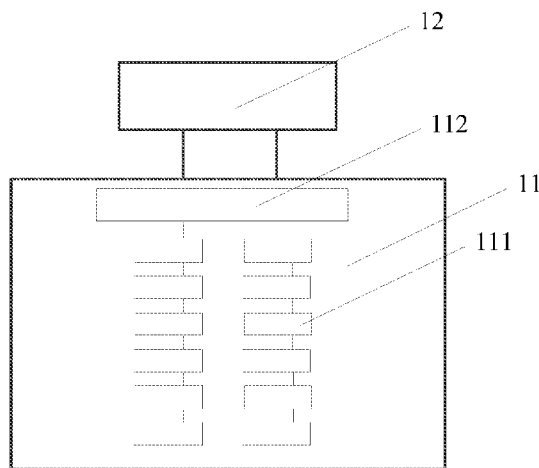


FIG. 1

(57) **Abstract:** Disclosed are a computational system and an electronic apparatus, the electronic apparatus comprising one or more forgoing computational systems. The computational system comprises a computing device and a control device. The control device comprises a data input-output interface connecting the control device to external devices and a control-device data-input component connecting the control device to the computing device. The computing device comprises a plurality of arithmetic units connected in series, each arithmetic unit comprising an arithmetic-unit data-input component, an arithmetic-unit data-output component, and a clock-signal-input interface. A first-stage arithmetic unit among the plurality of arithmetic units is connected to the control device. The arithmetic-unit data-input component of the first-stage arithmetic unit is connected to the arithmetic-unit data-output component of a second-stage arithmetic unit among the plurality of arithmetic units, and is configured to receive data processed by the second-stage



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OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
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COMPUTATIONAL SYSTEM AND CORRESPONDING ELECTRONIC APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the priority to Chinese Patent Application No. 201721617831.9, entitled “COMPUTATIONAL SYSTEM AND CORRESPONDING ELECTRONIC APPARATUS,” filed on November 28, 2017, the entire content of which is incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of electronic technology, in particular to a computational system and the corresponding electronic apparatus.

BACKGROUND

[0003] With the development of electronic technology, a variety of technical fields, such as artificial intelligence and security computing, have emerged. These technical fields may involve resource consuming computational tasks. In order to improve the speed and capacity of data processing, it may be necessary to control and operate multiple computational integrated circuit chips simultaneously. Further, with the rapid development of the computational integrated circuit chips, it may be necessary to develop dedicated computational systems to parallel process multiple computing tasks and improve computation speed.

SUMMARY

[0004] The present disclosure provides a computational system and the corresponding electronic apparatus.

[0005] In one aspect of the present disclosure, a computational system is provided. The present disclosure provides a computational system. The computational system comprises a computing device and a control device. The control device comprises a data input-output interface connecting the control device to external devices and a control-device data-input component connecting the control device to the computing device. The computing device comprises a plurality of arithmetic units connected in series, each arithmetic unit comprising an arithmetic-unit data-input component, an arithmetic-unit data-output component, and a clock-signal-input interface. A first-stage arithmetic unit among the plurality of arithmetic units is connected to the control device. The arithmetic-unit data-input component of the first-stage arithmetic unit is connected to the arithmetic-unit data-output component of a second-stage arithmetic unit among the plurality of arithmetic units, and is configured to receive data processed by the second-stage arithmetic unit. The arithmetic-unit data-output component of the first-stage arithmetic unit is connected to the control-device data-input component of the control device, and is configured to transmit data processed by the computing device to the control device.

[0006] In certain embodiments, the control device further comprises a control-device clock-signal-output interface. The control-device clock-signal-output interface is connected to the clock-signal-input interface of the first-stage arithmetic unit to transmit a clock signal to the computing device.

[0007] In certain embodiments, at least one of the plurality of arithmetic units comprises an arithmetic-unit clock-signal-output interface. The arithmetic-unit clock-signal-output interface is connected to the clock-signal-input interface of a next-stage arithmetic unit to transmit clock signal to the next-stage arithmetic unit.

[0008] In certain embodiments, the control device further comprises a control-device command-output interface. Each arithmetic unit further comprises a command-input interface and an arithmetic-unit command-output interface. The control-device command-output interface of the control device is connected to the command-input interface of the first-stage arithmetic unit, and is configured to transmit command signals to the first-stage arithmetic unit. The arithmetic-unit command-output interface of the first-stage arithmetic unit is connected to the command-input interface of the second-stage arithmetic unit, and is configured to transmit command signals to the second-stage arithmetic unit.

[0009] In certain embodiments, the computing device further comprises a data interface. The data interface is connected to both the arithmetic-unit data-output component of the first-stage arithmetic unit of the computing device and the control-device data-input component of the control device.

[0010] In certain embodiments, the computing device further comprises a signal conversion unit connected to at least two of the plurality of arithmetic units to match a signal voltage range.

[0011] In certain embodiments, the computational system further comprises at least one additional of the control device.

[0012] In certain embodiments, each of the control devices comprises a control-device data-output component; and the control devices are connected to each other through their respective control-device data-input components and control-device data-output components.

[0013] In certain embodiments, the computational system further comprises one or more crystal oscillators. Each crystal oscillator comprises: a power-input interface connected to a power source; and a crystal-oscillator clock-signal-output interface connected to the clock-signal-input interface of an arithmetic unit in the computing device.

[0014] In another aspect of the present disclosure, an electronic apparatus is provided. The electronic apparatus comprises one or more computational systems in the forgoing description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] In order to more clearly illustrate the technical solutions in the embodiments of the present disclosure, the drawings used in the description of the embodiments will be briefly described below.

[0016] FIG. 1 is an illustrative diagram of a computational system according to an embodiment of the present disclosure;

[0017] FIG 2 is an illustrative diagram of a computational system according to another embodiment of the present disclosure; and

[0018] FIG 3 is an illustrative diagram of a computational system according to another embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0019] Technical solutions of the present disclosure will be described with reference to the accompanying drawings. It should be understood that the described embodiments are some but not all of the embodiments of the present disclosure. Other embodiments derived by those with ordinary skills in the art on the basis of the described embodiments without inventive efforts should fall within the scope of the present disclosure.

[0020] According to an aspect of the present disclosure, a computational system is provided. FIG. 1 is an illustrative block diagram of a computational system according to certain embodiments. As shown in FIG. 1, in certain embodiments, the computational system may include a computing device 11 and control device 12. The computing device 11 may comprise a plurality of arithmetic units 111 that are sequentially connected in series. A first-stage arithmetic unit among the plurality arithmetic units in the computing device 11 is connected to the control unit 12.

[0021] Thus, in certain embodiments, in order to accelerate the computational speed while maintaining a large computational capacity, a plurality of arithmetic units 111 are incorporated in the computing device 11, and the arithmetic units 111 are connected in series. Only one of arithmetic units 111 needs to be connected to the control device 12. For example, the first-stage arithmetic unit may be connected to the control device 12 to receive signal data and command data from the control device 12. The first-stage arithmetic unit may be the arithmetic unit that is placed closest to the control device. Thus, operation of multiple arithmetic units may be coordinated to perform parallel processing of multiple computing tasks, and the wiring space and complexity may be reduced.

[0022] In certain embodiments of the present disclosure, the control device 12 may comprise a clock-signal-output interface, a data-input component, and an input-output interface. The control device 12 is connected to external devices through the input-output interface for data exchange. The clock-signal-output interface of the control device is connected to a clock-signal-input interface of the first-stage arithmetic unit in the computing device. The data-input component of the control device is connected to a data-output component of the first-stage arithmetic unit in the computing device.

[0023] Thus, in certain embodiments, the control device 12 comprises a clock-signal-output interface, a data-input component, and an input-output interface capable of satisfying basic data transmission requirements. The clock-signal-output interface of the control device is for transmitting a clock signal to the computing device. The data-input component of the control device is for receiving data processed and sent by the computing device. And the input-output interface of the control device is used to exchange data between the control device and external devices.

[0024] In certain embodiments, each of the arithmetic units 111 comprises a data-input component and a data-output component. The data-input component of an arithmetic unit is connected to the data-output component of a neighboring next-stage arithmetic unit to receive data processed and sent by the neighboring next-stage arithmetic unit. The data-output component of the first-stage arithmetic unit is connected to the data-input component of the control device for transmitting data processed by and sent from the computing device to the control device.

[0025] In certain embodiments, each of the arithmetic units 111 further comprises a clock-signal-input interface and one or more clock-signal-output interfaces. Any one of clock-signal-output interfaces of an arithmetic unit may be connected to the clock-signal-input interface of a next-stage arithmetic unit for transmitting a clock signal. The clock-signal-input interface of the first-stage arithmetic unit is connected to the clock-signal-output interface of the control device for receiving clock signal from the control device.

[0026] Thus, in certain embodiments, the plurality of arithmetic units 111 are connected to each other in series, and each of the arithmetic units 111 comprises a clock-signal-input interface, one or more clock-signal-output interfaces, a data-input component, and a data-output component. The clock-signal-input interface of the first-stage arithmetic unit is connected to the clock-signal-output interface of the control device for receiving clock signal from the control device. The clock-signal-output interface of the first-stage arithmetic unit is connected to the clock-signal-input interface of a second-stage arithmetic unit to transmit the clock signal to the second-stage arithmetic unit, which in turn may pass the clock signal to the third-stage arithmetic unit, and so on, so that all the arithmetic units connected in series may receive the clock signal. If an arithmetic unit at certain stage has two or more clock-signal-output interfaces, one of them may be connected to the clock-signal-input interface of the neighboring next-stage arithmetic unit to transmit the clock signal.

[0027] The data-output component of the last-stage arithmetic unit is connected to the data-input component of the second-last-stage arithmetic unit, and is used for transmitting the data processed by and sent from the last-stage arithmetic unit to the second-last-stage arithmetic unit; and the data-output component of the second-last-stage arithmetic unit is connected to the data-input component of the third-last-stage arithmetic unit, and is used for transmitting the data

processed by and sent from the second-last-stage arithmetic unit to the arithmetic unit above, and so on; until computed data that computed by the computing device is received by the data-input component of the first-stage arithmetic unit, and passed through the data-output component of the first-stage arithmetic unit transmitting to the control device.

[0028] In certain embodiments, the control device 12 further comprises a command-output interface, and each arithmetic unit 111 further comprises a command-input interface and a command-output interface. The command-output interface of the control device 12 is connected to the command-input interface of the first-stage arithmetic unit to send the command signal to the first-stage arithmetic unit. The command-output interface of the first-stage arithmetic unit is connected to the command-input interface of the second-stage arithmetic unit to send the received command signal to the second-stage arithmetic unit, and so on.

[0029] Thus, in certain embodiments, the control device 12 further comprises a command-output interface, and each arithmetic unit 111 further comprises a command-input interface and a command-output interface. The command-output interface of the control device 12 is connected to the command-input interface of the first-stage arithmetic unit in the computing device. Next, the command-output interface of the arithmetic unit at each stage is connected to the command-input interface of the neighboring next-stage arithmetic unit to transmit the command signal to the arithmetic unit at each stage.

[0030] In certain embodiments, the computing device 11 further comprises a data interface 112. The data interface 112 is connected to both the data-output component of the first-stage arithmetic unit and the data-input component of the control device 12 to transmit the computed data from the computing device 11 to the control device 12.

[0031] FIG. 2 is an illustrative diagram of the computational system according to certain other embodiments of the present disclosure. As shown in FIG. 2, in certain embodiments, the computing device 11 further comprises one or more signal conversion units 113. Each signal conversion unit 113 is connected to two arithmetic units 111 for adapting their signal voltage levels.

[0032] In certain embodiments, the operating voltage levels of two arithmetic units 111 that are connected to each other may be different, and data cannot be transmitted between them without voltage level conversion. Thus, the signal conversion unit 113 may be inserted between the two arithmetic units 111 having different operating voltage levels to convert the signal voltage level of the sender into a voltage range that meets the requirement of the receiver.

[0033] For example, when the first-stage arithmetic unit transmits data to the second-stage arithmetic unit, if the operating voltage range of the first-stage arithmetic unit is different from the operating voltage range of the second-stage arithmetic unit, the signal of the first-stage arithmetic unit needs to be converted by the signal conversion unit before being transmitted to the second-stage arithmetic unit. That is, the signal conversion unit converts the signal voltage level of the first-stage arithmetic unit output into a voltage level that is within the acceptable operation voltage range of the second-stage arithmetic unit.

[0034] Similarly, when a present-stage arithmetic unit sends data to its previous-stage arithmetic unit, if the operating voltage range of the present-stage arithmetic unit is different from the operating voltage range of the neighboring previous-stage arithmetic unit, the signal of the present-stage arithmetic unit also needs to be converted by the signal conversion unit before the signal is transmitted to the neighboring previous-stage arithmetic unit, that is, the voltage range

of the present-stage arithmetic unit output is converted into a voltage range that matches the operation voltage range of the neighboring previous-stage arithmetic unit.

[0035] If the operating voltage range of a present-stage arithmetic unit already matches the operating voltage range of the neighboring next-stage arithmetic unit, the present-stage arithmetic unit can directly communicate with the next-stage arithmetic unit without performing signal conversion.

[0036] In certain embodiments, the computational system may comprise a plurality of the control devices 12. Further, the control device 12 may further comprise a data-output component. When there are a plurality of control devices 12, the control devices 12 may be connected to each other through their respective data-output components and the data-input components. Alternatively, the multiple control devices may be integrated into one unit.

[0037] FIG. 3 is an illustrative diagram of a computational system according to certain other embodiments of the present disclosure. As shown in FIG. 3, in certain embodiments, the computational system may further comprise one or more crystal oscillators 114. Further, each crystal oscillator 114 may comprise a power input interface and a clock-signal-output interface. The power input interface is connected to a power source. The clock-signal-output interface of the crystal oscillator is connected to the clock-signal-input interface of one of the arithmetic units.

[0038] If the operating voltage level difference between two arithmetic units 111 connected in series is significant, then relying solely on the same clock signal source may not satisfy the clock signal requirements of the serially connected arithmetic units. Thus, in certain embodiments, crystal oscillators 114 are added for every two arithmetic units 111, or for every certain number of arithmetic units, or at other suitable intervals and locations. The power input interface of each

crystal oscillator is connected to and powered by a power source. The clock-signal-output interface of each crystal oscillator is connected to the clock-signal-input interface of the first-stage arithmetic unit in an arithmetic-unit group that needs to have the clock signal restored to provide clock signal for the arithmetic-unit group.

[0039] The foregoing descriptions are explanatory. Those skilled in the art may determine the numbers of the signal conversion units 113 and the crystal oscillators 114 as well as their specific installation positions according to the requirements of a specific application. These features are not specifically limited in the present disclosure.

[0040] In certain embodiments, the computational integrated circuit chip may be used to perform Hash calculations in a cryptocurrency mining process. The backbone of a cryptocurrency is its blockchain, which is a global ledger formed by linking together individual blocks of transaction data. The blockchain only contains validated transactions, which prevents fraudulent transactions and double spending of the currency. The validation process relies on data being encrypted using algorithmic hashing. The resulting encrypted value is a series of numbers and letters that does not resemble the original data, and is called a hash. Cryptocurrency mining involves working with the hash. Hashing requires processing the data from a block through a mathematical function, which results in an output of a fixed length. Using a fixed length output increases security, since anyone trying to decrypt the hash won't be able to tell how long or short the input is simply by looking at the length of the output. For example, hashing the word "hello" will produce an output that is the same length as the hash for "I am going to the store". The function used to generate the hash is deterministic, meaning that it will produce the same result each time the same input is used; can generate a hashed input efficiently; makes determining the input difficult (leading to mining); and makes small changes to the input result in a very different hash.

[0041] Solving the hash is essentially solving a complex mathematical problem, and starts with the data available in the block header. Each block header contains a version number, a timestamp, the hash used in the previous block, the hash of the Merkle Root, the nonce, and the target hash. The miner focuses on the nonce, a string of numbers. This number is appended to the hashed contents of the previous block, which is then itself hashed. If this new hash is less than or equal to the target hash, then it is accepted as the solution, the miner is given the reward, and the block is added to the blockchain.

[0042] In one example, BitCoin uses the SHA-256 hash algorithm to generate verifiably "random" numbers in a way that requires a predictable amount of CPU effort. Generating a SHA-256 hash with a value less than the current target solves a block and wins coins for mining machines. When a SHA-256 algorithm is used to solve a hash for block in a blockchain, the mining computer may calculate a hash functions of a set of random numbers to find a combination that match the current condition for a new block. As a result, an extremely large amount of computation may be required. The computational integrated circuit chip in the foregoing description may be used as Application Specific Integrated Chips (ASIC) to perform multiple hash calculations in parallel using the multiple arithmetic units. Further, since the multiple arithmetic units are connected in series and may communicate the calculation results to one another, these ASICs may be used to calculate a single hash or an iterated hash in parallel. The arithmetic units may be designed and arranged to optimize a specific computation sequence, and the operating voltage levels of two adjacent arithmetic units may be different. If the operating voltage level difference between two arithmetic units connected in series is significant, direct connection for data transmission may not be reliable. Further, relying solely on the same clock signal source may not satisfy the clock signal requirements of the serially connected

arithmetic units with different operating voltage levels. Thus, in certain embodiments, a signal conversion unit may be inserted between the two arithmetic units having different operating voltage levels to convert the signal voltage level of the sender into a voltage range that meets the requirement of the receiver. Further, in certain embodiments, crystal oscillators may be added at suitable intervals and locations to provide additional clock signal to certain arithmetic units. Embodiments of the present disclosure thus may ensure optimized operation and data communication of the arithmetic units connected in series, and improve the calculation speed of the computational integrated circuit chip in a mining machine by using customized parallel computing.

[0043] According to another aspect of the present disclosure, an electronic apparatus is also provided. The electronic apparatus comprises one or more computational systems in the forgoing descriptions.

[0044] The forgoing description and embodiments are exemplary descriptions of the technical solutions provided by the present disclosure. Other embodiments of the disclosure will be apparent to those skilled in the art. The present disclosure is intended to cover any variations, modifications, equivalent substitutions, uses, or adaptations that are in accordance with the general principles of the present disclosure.

WHAT IS CLAIMED IS:

1. A computational system, comprising a computing device and a control device, wherein:
the control device comprises a data input-output interface connecting the control device to external devices and a control-device data-input component connecting the control device to the computing device;

the computing device comprises a plurality of arithmetic units connected in series, each arithmetic unit comprising an arithmetic-unit data-input component, an arithmetic-unit data-output component, and a clock-signal-input interface;

a first-stage arithmetic unit among the plurality of arithmetic units is connected to the control device;

the arithmetic-unit data-input component of the first-stage arithmetic unit is connected to the arithmetic-unit data-output component of a second-stage arithmetic unit among the plurality of arithmetic units, and is configured to receive data processed by the second-stage arithmetic unit; and

the arithmetic-unit data-output component of the first-stage arithmetic unit is connected to the control-device data-input component of the control device, and is configured to transmit data processed by the computing device to the control device.

2. The computational system according to claim 1, wherein the control device further comprises a control-device clock-signal-output interface, the control-device clock-signal-output interface being connected to the clock-signal-input interface of the first-stage arithmetic unit to transmit clock signal to the computing device.

3. The computational system according to claim 2, wherein:

at least one of the plurality of arithmetic units comprises an arithmetic-unit clock-signal-output interface, the arithmetic-unit clock-signal-output interface being connected to the clock-signal-input interface of a next-stage arithmetic unit to transmit a clock signal to the next-stage arithmetic unit.

4. The computational system according to claim 3, wherein:

the control device further comprises a control-device command-output interface;

the each arithmetic unit further comprises a command-input interface and an arithmetic-unit command-output interface;

the control-device command-output interface of the control device is connected to the command-input interface of the first-stage arithmetic unit, and is configured to transmit command signals to the first-stage arithmetic unit; and

the arithmetic-unit command-output interface of the first-stage arithmetic unit is connected to the command-input interface of the second-stage arithmetic unit, and is configured to transmit command signals to the second-stage arithmetic unit.

5. The computational system according to claim 1, wherein the computing device further comprises a data interface, the data interface being connected to both the arithmetic-unit data-output component of the first-stage arithmetic unit of the computing device and the control-device data-input component of the control device.

6. The computational system according to claim 1, wherein the computing device further comprises a signal conversion unit connected to at least two of the plurality of arithmetic units to match a signal voltage range.

7. The computational system according to claim 2, further comprising one additional control device.

8. The computational system according to claim 7, wherein:
each of the control devices comprises a control-device data-output component; and
the control devices are connected to each other through their respective control-device data-input components and control-device data-output components.

9. The computational system according to claim 1, further comprising one or more crystal oscillators, each crystal oscillator comprising:
a power-input interface connected to a power source; and
a crystal-oscillator clock-signal-output interface connected to the clock-signal-input interface of an arithmetic unit in the computing device.

10. The computational system according to claim 1, wherein the plurality of arithmetic units compute a hash function in parallel.

11. An electronic apparatus comprising one or more computational systems, each computational system comprising a computing device and a control device, wherein:

the control device comprises a data input-output interface connecting the control device to external devices and a control-device data-input component connecting the control device to the computing device;

the computing device comprises a plurality of arithmetic units connected in series, each arithmetic unit comprising an arithmetic-unit data-input component, an arithmetic-unit data-output component, and a clock-signal-input interface;

a first-stage arithmetic unit among the plurality of arithmetic units is connected to the control device;

the arithmetic-unit data-input component of the first-stage arithmetic unit is connected to the arithmetic-unit data-output component of a second-stage arithmetic unit among the plurality of arithmetic units, and is configured to receive data processed by the second-stage arithmetic unit; and

the arithmetic-unit data-output component of the first-stage arithmetic unit is connected to the control-device data-input component of the control device, and is configured to transmit data processed by the computing device to the control device.

12. The electronic apparatus according to claim 11, wherein the control device of the each computational system further comprises a control-device clock-signal-output interface, the control-device clock-signal-output interface being connected to the clock-signal-input interface of the first-stage arithmetic unit in the computing device to transmit a clock signal to the computing device.

13. The electronic apparatus according to claim 12, wherein for the each computational system:

at least one of the plurality of arithmetic units comprises an arithmetic-unit clock-signal-output interface, the arithmetic-unit clock-signal-output interface being connected to the clock-signal-input interface of a next-stage arithmetic unit to transmit clock signal to the next-stage arithmetic unit.

14. The electronic apparatus according to claim 13, wherein for the each computational system:

the control device of the each computational system further comprises a control-device command-output interface;

the each arithmetic unit further comprises a command-input interface and an arithmetic-unit command-output interface;

the control-device command-output interface of the control device is connected to the command-input interface of the first-stage arithmetic unit, and is configured to transmit command signals to the first-stage arithmetic unit; and

the arithmetic-unit command-output interface of the first-stage arithmetic unit is connected to the command-input interface of the second-stage arithmetic unit, and is configured to transmit command signals to the second-stage arithmetic unit.

15. The electronic apparatus according to claim 10, wherein the computing device of the each computational system further comprises a data interface, the data interface being connected

to both the arithmetic-unit data-output component of the first-stage arithmetic unit of the computing device and the control-device data-input component of the control device.

16. The electronic apparatus according to claim 15, wherein the computing device of the each computational system further comprises a signal conversion unit connected to at least two of the plurality of arithmetic units to match a signal voltage range.

17. The electronic apparatus according to claim 11, wherein the each computational system further comprises one additional control device.

18. The electronic apparatus according to claim 17, wherein for the each computational system:

each of the control devices comprises a control-device data-output component; and
the control devices are connected to each other through their respective control-device data-input components and control-device data-output components.

19. The electronic apparatus according to claim 11, wherein the each computational system further comprises one or more crystal oscillators, each crystal oscillator comprising:

a power-input interface connected to a power source; and
a crystal-oscillator clock-signal-output interface connected to an arithmetic unit in the computing device.

20. The electronic apparatus according to claim 11, wherein the plurality of arithmetic units compute a hash function in parallel.

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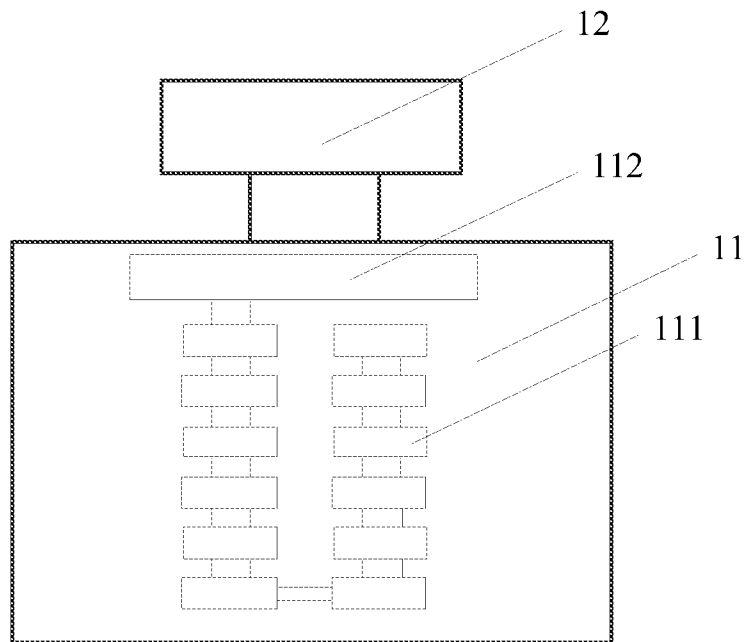


FIG. 1

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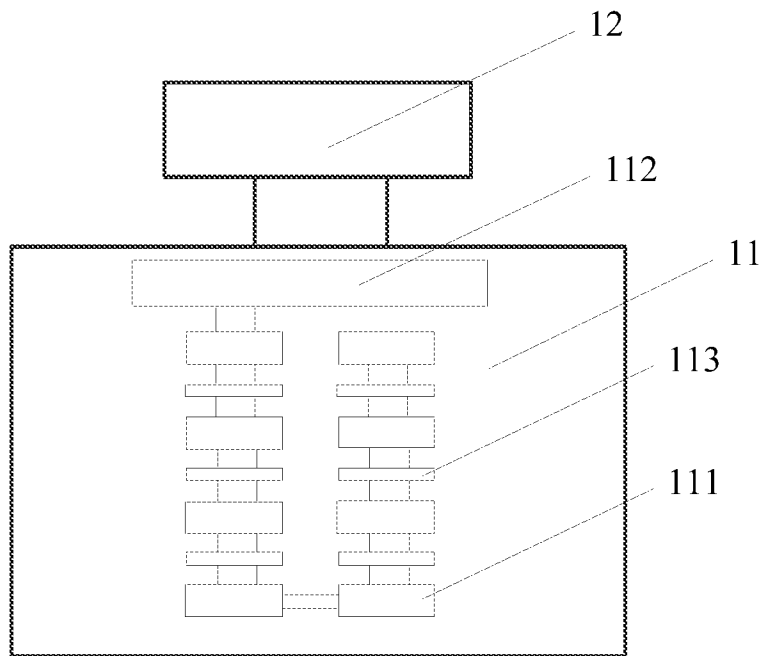


FIG. 2

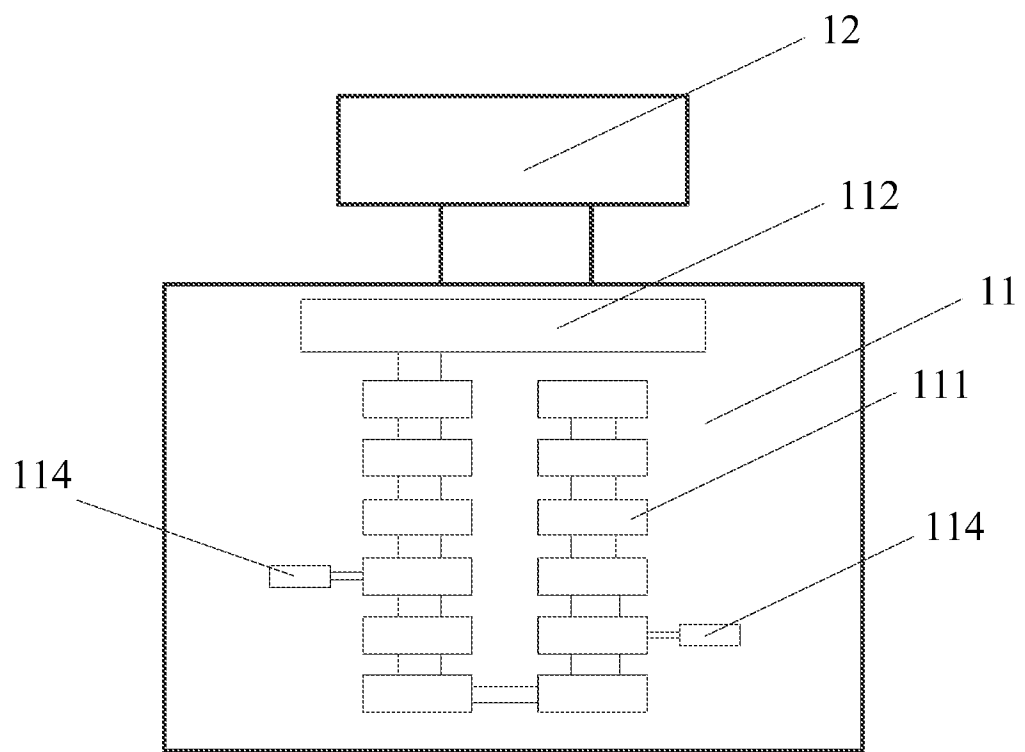


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/117588

A. CLASSIFICATION OF SUBJECT MATTER G06F 15/16(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) G06F Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) CNPAT, EPODOC, WPI, GOOGLE, CNKI: computing, arithmetic, input, output, interface, clock, series		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 207503225 U (BITMAIN TECHNOLOGIES INC.) 15 June 2018 (2018-06-15) description, paragraphs [0034]-[0063], and claims 1-10	1-9, 11-19
X	US 2009187615 A1 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 23 July 2009 (2009-07-23) description, paragraphs [0066]-[0092], and claims 1-11	1-20
A	CN 106407008 A (BITMAIN TECHNOLOGIES INC.) 15 February 2017 (2017-02-15) the whole document	1-20
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Date of the actual completion of the international search 30 January 2019		Date of mailing of the international search report 27 February 2019
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INTERNATIONAL SEARCH REPORT
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International application No.

PCT/CN2018/117588

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