(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
08 October 2020 (08.10.2020)

WIPO | PCT

(10) International Publication Number
WO 2020/204823 A1

(51) International Patent Classification:
H01L 31/06 (2012.01) *H01L 31/18* (2006.01)

(21) International Application Number: PCT/SG2020/050186

(22) International Filing Date: 27 March 2020 (27.03.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10201902849W 29 March 2019 (29.03.2019) SG

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(54) Title: SOLAR CELL AND METHOD FOR FABRICATING A SOLAR CELL

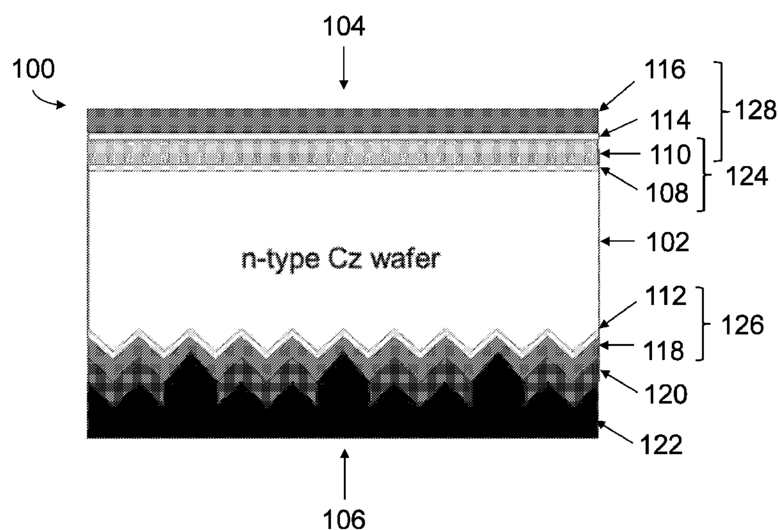

Figure 1

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(57) Abstract: A solar cell is described. In an embodiment, the solar cell (100) comprises a silicon wafer having (102) a front side (104) arranged to receive incident light and a rear side (106), and a first doped semiconductor layer (110) formed on either the front side (104) or the rear side (106) of the silicon wafer (102). The solar cell (100) further comprises (i) a dielectric tunnel layer (112) deposited on one side of the silicon wafer (102) opposites to the side at which the first doped semiconductor layer (110) is formed, (ii) a front side second doped semiconductor layer (116) deposited on the front side (104) of the silicon wafer (102); and (iii) a rear side second doped semiconductor layer (118) deposited on the rear side (106) of the silicon wafer (102), the front side and the rear side second doped semiconductor layers (116), (118) each having a doping of an opposite polarity to the first doped semiconductor layer (110). The first doped semiconductor layer (110) cooperates with either the front side second doped semiconductor layer (116) or the rear side second

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

doped semiconductor layer (118) to form a tunnel junction, and the dielectric tunnel layer (112) cooperates with either the rear side second doped semiconductor layer (118) or the front side second doped semiconductor layer (116) to form a passivated contact.

Solar cell and Method for fabricating a solar cell

Technical Field

The present disclosure relates to a solar cell and also a method for fabricating a solar cell, in particular, a contact passivated solar cell with a tunnel junction.

Background

The photovoltaic market is currently dominated by wafer based, crystalline silicon (Si) solar cells. In order to realise Si solar cells having an ultra-high efficiency which reaches the theoretical Auger efficiency limit of 29%, contact passivation is an attractive option. Specifically, contact passivation reduces recombination losses at the solar cell contacts since recombination at the solar cell contacts constitutes a major loss mechanism, thereby enhancing an open-circuit voltage of the solar cell and its efficiency.

At present, in order to form passivated contacts (for example, SiO_x/n^+ poly-Si for electron extraction or SiO_x/p^+ poly-Si for hole extraction), one usually deploys double-side deposition methods which typically include processes performed in tubes. For example, low pressure chemical vapour deposition (LPCVD) may be used to form a SiO_x tunnel layer followed by an intrinsic polysilicon (poly-Si) capping layer. A tube diffusion process is then subsequently performed for doping the intrinsic poly-Si capping layer. Due to the nature of performing these processes in tubes, all layers and diffusion processes needed to form the SiO_x/poly-Si passivated contacts will typically form on both sides of a wafer. However, as a passivated contact of each type (either SiO_x/n^+ poly-Si for electron extraction or SiO_x/p^+ poly-Si for hole extraction) is required on each side of the wafer, numerous process steps including deploying masking layers and the subsequent removal of those masking layers are needed if a double-side contact passivated solar cell is to be fabricated. It is therefore desirable to provide a method for fabricating a solar cell and a solar cell which address the aforementioned problems and/or provides the public with a useful alternative.

Furthermore, other desirable features and characteristics will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and this background of the disclosure.

Summary

Aspects of the present application relate to a method for fabricating a solar cell and the solar cell thereof, in particular, a contact passivated solar cell with a tunnel junction.

In accordance with a first aspect, there is provided a solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side, and a first doped semiconductor layer formed on either the front side or the rear side of the silicon wafer, the solar cell comprising:

a dielectric tunnel layer deposited on one side of the silicon wafer opposites to the side at which the first doped semiconductor layer is formed;

a front side second doped semiconductor layer deposited on the front side of the silicon wafer; and

a rear side second doped semiconductor layer deposited on the rear side of the silicon wafer, the front side and the rear side second doped semiconductor layers each having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the first doped semiconductor layer cooperates with either the front side second doped semiconductor layer or the rear side second doped semiconductor layer to form a tunnel junction, and the dielectric tunnel layer cooperates with either the rear side second doped semiconductor layer or the front side second doped semiconductor layer to form a passivated contact.

By incorporating the first doped semiconductor layer with either the front side second doped semiconductor layer or the rear side second doped semiconductor layer, a tunnel junction can be formed correspondingly either on the front side or the rear side of the silicon wafer. In an embodiment where the tunnel junction is formed on the front side of the silicon wafer, a front-side tunnel junction needed in order to separate the top cell voltage from the bottom cell voltage for tandem solar cell integration would have been integrated in the above solar cell. This advantageously minimizes the number of process steps in fabricating the tandem solar cell. On the other hand, if the tunnel junction is formed on the rear side of the silicon wafer, a rear-side emitter region is formed on the rear side of the solar cell. This is advantageous in particular in embodiments of single-junction silicon high-efficiency solar cell since having the tunnel junction (or the rear side emitter) at a rear side of the Si wafer reduces parasitic absorption given that a highly

doped layer (e.g. a high diffusion doped semiconductor layer) is not formed on the front side of the Si wafer for receiving incident light.

Further, in either of these cases, a passivated contact, comprising the dielectric tunnel layer and either the rear side second doped semiconductor layer or the front side second doped semiconductor layer, is formed. The passivated contact advantageously reduces recombination losses and thereby enhances an open-circuit voltage and an efficiency of the solar cell. Instead of forming a direct (localized) metal contact with the Si wafer, the passivated contact comprising the dielectric tunnel layer (e.g. a wet-chemically formed or ozone assisted or thermally grown ultra-thin SiO_x) and the second doped semiconducting layer (e.g. a highly doped LPCVD or PECVD deposited n^+ poly-Si or p^+ poly-Si layer) is formed to contact the Si wafer of the solar cell. The passivated contact not only provides an excellent surface passivation towards the Si wafer (with recombination current densities j_0 for example in the order of up to several 10 fs cm^{-2}), it also provides a reasonable low contact resistivity (in the order up to several 100 mΩ cm^2) and at the same time enables a high carrier extraction selectivity (i.e. an ability to extract only electrons or only holes at the contact with a carrier selectivity of higher than 10).

Further, the aforementioned solar cell may be fabricated by directly leveraging on conventional, double-side deposition methods for forming passivated contacts (e.g. LPCVD) with minimized processing steps in order to form contacts of different carrier selectivity (i.e. electron extracting or hole extracting) on each side of the Si wafer. For example, the front side second doped semiconductor layer and the rear side second doped semiconductor layer can be deposited in a double-side deposition process, where one of the second doped semiconductor layers forms the aforementioned passivated contact on one side of the Si wafer and the other second doped semiconductor layer forms a tunnel junction with the first doped semiconductor layer (which has an opposite polarity to the second doped semiconductor layer). In this way, further masking layer depositions and corresponding removal of masking layer process steps can be avoided. Further, in case of using conventional diffusion to extract one excess carrier type (electrons or holes), only one type of carrier selective contact (either hole extracting, i.e. SiO_x/p^+ poly-Si or electron extracting, i.e. SiO_x/n^+ poly-Si) has to be deposited. This is discussed further, for example, in relation to Figure 11A.

Embodiments of the aforementioned solar cell can therefore be advantageously deployed as either (i) a bottom cell comprising the required tunnel junction for tandem solar cell integration (see for example Figure 1 below), or (ii) a contact passivated single-junction solar cell with a rear side emitter (see for example Figure 3 below).

5 The front side second doped semiconductor layer and the rear side second doped semiconductor layer may be deposited using low pressure chemical vapor deposition (LPCVD) in a single deposition process. By using LPCVD, the front side second doped semiconductor layer and the rear side second doped semiconductor layer may be deposited in a single process step, thereby advantageously minimizing the number of 10 process steps needed for fabricating a solar cell.

The solar cell may comprise an interlayer dielectric tunnel layer deposited on the first doped semiconductor layer, wherein the interlayer dielectric tunnel layer is sandwiched between the first doped semiconductor layer and the front side second doped semiconductor layer or the rear side second doped semiconductor layer to form the 15 tunnel junction.

The solar cell may comprise a surface dielectric tunnel layer deposited on a surface of the silicon wafer, the surface dielectric tunnel layer being sandwiched between the surface of the silicon wafer and the first doped semiconductor layer, wherein the surface dielectric tunnel layer and the first doped semiconductor layer form another passivated 20 contact. This second passivated contact formed in this case shares the same advantages as described above for passivated contacts.

The first doped semiconductor layer may comprise a p-doped polysilicon layer, and the front side second-doped semiconductor layer and the rear side second doped semiconductor layer may each comprise an n-doped polysilicon layer.

25 The solar cell may comprise a contact formation layer deposited on at least one of the front side second doped semiconductor layer and the rear side second doped semiconductor layer.

The solar cell may comprise a rear metal contact formed on the rear side of the silicon wafer, the rear metal contact being in electrical contact with the rear side second doped 30 semiconductor layer.

The rear metal contact may be formed using screen printing, inline plating or evaporation.

The solar cell may comprise a front metal contact formed on the front side of the silicon wafer, the front metal contact being in electrical contact with the front side second doped semiconductor layer.

5 The front metal contact may be formed using screen printing, inline plating or evaporation.

In accordance with a second aspect, there is provided a method for fabricating a solar cell, the solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side, and a first doped semiconductor layer formed on either the front side or the rear side of the silicon wafer, the method comprising:

10 (i) depositing a dielectric tunnel layer on one side of the silicon wafer opposites to the side at which the first doped semiconductor layer is formed; and

(ii) depositing a front side second doped semiconductor layer on the front side of the silicon wafer and a rear side second doped semiconductor layer on the rear side of the silicon wafer, the front side and the rear side second doped semiconductor layers 15 each having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the first doped semiconductor layer cooperates with either the front side second doped semiconductor layer or the rear side second doped semiconductor layer to form a tunnel junction, and the dielectric tunnel layer cooperates with either the rear side second doped semiconductor layer or the front side second doped semiconductor 20 layer to form a passivated contact.

Depositing the front side second doped semiconductor layer and the rear side second doped semiconductor layer may comprise depositing the front side second doped semiconductor layer and the rear side second doped semiconductor layer using low pressure chemical vapor deposition (LPCVD) in a single deposition process.

25 The method may comprise depositing an interlayer dielectric tunnel layer on the first doped semiconductor layer.

The interlayer dielectric tunnel layer and the dielectric tunnel layer may be deposited using LPCVD in a single deposition process. In other words, on one hand, the first doped semiconductor layer and the interlayer dielectric tunnel layer together with the front side 30 second doped semiconductor layer or the rear side second doped semiconductor layer form the tunnel junction, while on the other hand, the dielectric tunnel layer and the rear

side second doped semiconductor layer or the front side second doped semiconductor layer (i.e. the second doped semiconductor layer which is not involved in forming the tunnel junction) form the passivated contact. In embodiments where the interlayer dielectric tunnel layer, the dielectric tunnel layer, the front side second doped
5 semiconductor layer and the rear side second doped semiconductor layer are deposited by LPCVD, these layers can advantageously be deposited in a single process step as described below.

The first doped semiconductor layer may be formed using plasma enhanced chemical vapor deposition (PECVD) or low pressure chemical vapor deposition (LPCVD).

10 The method may comprise depositing a surface dielectric tunnel layer on a surface of the silicon wafer prior to the formation of the first doped semiconductor layer, the surface dielectric tunnel layer being sandwiched between the surface of the silicon wafer and the first doped semiconductor layer, wherein the surface dielectric tunnel layer and the first doped semiconductor layer form another passivated contact.

15 The first doped semiconductor layer may comprise a p-doped polysilicon layer and depositing the front side second doped semiconductor layer and the rear side second doped semiconductor layer may comprise depositing an n-doped polysilicon layer on each of the front side and the rear side of the silicon wafer.

The first doped semiconductor layer may be formed by diffusing or implanting ions in the
20 silicon wafer.

The method may comprise depositing a contact formation layer on at least one of the front side second doped semiconductor layer and the rear side second doped semiconductor layer.

The method may comprise forming a rear metal contact on the rear side of the silicon
25 wafer, the rear metal contact being in electrical contact with the rear side second doped semiconductor layer.

Forming the rear metal contact may comprise forming the rear metal contact using screen printing, inline plating or evaporation.

The method may comprise forming a front metal contact on the front side of the silicon wafer, the front metal contact being in electrical contact with the front side second doped semiconductor layer.

Forming the front metal contact may comprise forming the front metal contact using screen printing, inline plating or evaporation.

The front side of the silicon wafer may be textured.

The rear side of the silicon wafer may be textured.

In accordance with a third aspect, there is provided a tandem solar cell comprising:

a top solar cell; and

a bottom solar cell, wherein the bottom solar cell comprises a silicon wafer having a front side arranged to receive incident light and a rear side and a first doped semiconductor layer formed on either the front side or the rear side of the silicon wafer, the bottom solar cell comprising:

a dielectric tunnel layer deposited on one side of the silicon wafer opposites to the side at which the first doped semiconductor layer is formed;

a front side second doped semiconductor layer deposited on the front side of the silicon wafer; and

a rear side second doped semiconductor layer deposited on the rear side of the silicon wafer, the front side and the rear side second doped semiconductor layers each having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the first doped semiconductor layer cooperates with either the front side second doped semiconductor layer or the rear side second doped semiconductor layer to form a tunnel junction, and the dielectric tunnel layer cooperates with either the rear side second doped semiconductor layer or the front side second doped semiconductor layer to form a passivated contact.

The top solar cell and the bottom solar cell may be integrated to form a tandem solar cell structure.

It should be appreciated that features relating to one aspect may be applicable to the other aspects. Embodiments therefore provide a solar cell comprising a tunnel junction on one side of the Si wafer and a passivated contact on the other side of the Si wafer. By incorporating the first doped semiconductor layer with either the front side second

doped semiconductor layer or the rear side second doped semiconductor layer, a tunnel junction can be formed correspondingly either on the front side or the rear side of the silicon wafer. As aforementioned described, the solar cell can therefore be advantageously deployed either as a bottom cell within a thin-film-on-silicon tandem solar cell configuration (see for example Figure 1 below), or as a contact passivated single-junction solar cell with a rear side emitter (see for example Figure 3 below). In either of these cases, a passivated contact is used. The passivated contact advantageously reduces recombination losses and thereby enhances open-circuit voltages and an efficiency of the solar cell. Further, the aforementioned solar cell may be fabricated by directly leveraging on conventional, double-side deposition methods for forming passivated contacts (e.g. LPCVD) with minimized processing steps in order to form contacts of different carrier selectivity (i.e. electron extracting or hole extracting) on each side of the Si wafer. This reduces the need for further masking layer depositions and correspondingly, reduces the need for additional steps to remove the deposited masking layers. It therefore improves an efficiency for the fabrication of the aforementioned solar cell, thereby advantageously cutting the time, costs and resources consumed as compared to a conventional solar cell fabrication process.

Brief description of the drawings

Embodiments will now be described, by way of example only, with reference to the following drawings, in which:

Figure 1 is a schematic structure of a solar cell for tandem integration in accordance with a first embodiment;

Figures 2A and 2B are flowcharts showing methods for fabricating the solar cell of Figure 1, where Figure 2A is a flowchart showing steps of a method for fabricating the solar cell using PECVD in accordance with an embodiment and Figure 2B is a flowchart showing steps of a method for fabricating the solar cell using LPCVD in accordance with an embodiment;

Figure 3 is a schematic structure of a single-junction solar cell in accordance with a second embodiment;

Figures 4A and 4B are flowcharts showing methods for fabricating the solar cell of Figure 3, where Figure 4A is a flowchart showing steps of a method for fabricating the solar cell

using PECVD in accordance with an embodiment and Figure 4B is a flowchart showing steps of a method for fabricating the solar cell using LPCVD in accordance with an embodiment;

Figures 5A, 5B and 5C show schematic structures of three different test samples that 5 have been processed to measure their corresponding tunnelling resistances;

Figures 6A, 6B and 6C show measured dark current-voltage (I-V) curves of the structures of Figures 5A, 5B and 5C respectively for measuring their corresponding tunnelling resistances;

Figures 7A, 7B and 7C show schematic structures for use in investigating a minority 10 carrier lifetime for SiO_x/p^+-poly-Si/SiO_x/n^+-poly-Si tunnel junction, where Figure 7A shows a structure comprising a diffusion optimized SiO_x/p^+-poly-Si passivated contact and a SiN_x passivation layer deposited on each side of an n-doped Si wafer, Figure 7B shows a structure comprising a SiO_x/p^+ poly-Si passivated contact deposited on each side of a p-doped Si wafer, and Figure 10C shows a structure comprising a SiO_x/p^+-poly-15 Si/SiO_x/n^+-poly-Si tunnel junction augmented passivated contact deposited on a rear side of a p-doped Si wafer suited for dark I-V tunnelling resistance measurements;

Figures 8A and 8B illustrate experimental findings of a minority carrier lifetime for the structures of Figures 7A, 7B and 7C, where Figure 8A shows the experimental findings for the structure of Figure 7A, and Figure 8B shows the experimental findings for the 20 structures of Figures 7B and 7C;

Figures 9A to 9F are schematic structures used for investigating a passivation quality of thick and ultra-thin SiO_x/poly-Si passivated contacts, processed on a planar or on a textured wafer surface;

Figures 10A and 10B show refractive indices *k* for inductively coupled plasma enhanced 25 chemical vapour deposition (IC-PECVD) processed poly-Si and LPCVD processed poly-Si, where Figure 10A shows the refractive indices *k* for IC-PECVD n^+ poly-Si as compared to LPCVD n^+ poly-Si, and Figure 10B shows refractive indices k for IC-PECVD processed n^+ poly-Si and p^+ poly-Si;

Figures 11A to 11C show schematic structures of a solar cell for tandem integration in 30 accordance with further embodiments, where Figure 11A shows a solar cell comprising

a p-doped diffused rear-emitter region, Figure 11B shows a solar cell comprising a front side p-doped diffused region and Figure 11C shows a solar cell comprising a front side n-doped diffused region;

Figures 12A to 12F show schematic structures of a single-junction solar cell in accordance with further embodiments, where Figure 12A shows a solar cell comprising a p-doped diffused rear-emitter region, Figure 12B shows a solar cell comprising a p-doped diffused rear-emitter region with a textured rear side surface, Figure 12C shows a solar cell comprising a different rear-side metal contact scheme as compared to the solar cell of Figure 3, Figure 12D shows a solar cell comprising a full rear-side metal layer for forming the rear metal contacts as compared to the solar cell of Figure 3, Figure 12E shows a solar cell comprising a transparent conducting oxide (TCO) layer on each of the front side and the rear side of the solar cell, and Figure 12F shows a solar cell comprising a TCO layer on a front side of the solar cell; and

Figure 13 shows a schematic of a tandem solar cell comprising a thin-film top solar cell and a silicon wafer based bottom solar cell where the bottom solar cell has a similar structure to the solar cell of Figure 1 in accordance with an embodiment.

Detailed description

An exemplary embodiment relates to a method for fabricating a solar cell, in particular, a contact passivated solar cell with a tunnel junction.

Figure 1 is a schematic structure of the solar cell 100 in accordance with an embodiment. The solar cell 100 can be deployed as a high efficiency silicon bottom cell for further thin-film on silicon tandem device integration as discussed later in relation to Figure 13. Variations of the solar cell 100 for deploying as high efficiency silicon bottom cell for further thin-film on silicon tandem device integration are discussed in relation to Figures 11A to 11C.

The solar cell 100 comprises an n-type Czochralski (Cz) grown monocrystalline Si wafer 102 with a front side 104 and a rear side 106. As shown in Figure 1, the front side 104 of the Si wafer 102 has a planar surface while the rear side 106 of the Si wafer 102 has a textured surface. A surface dielectric tunnel layer 108 is deposited on the front side 104 of the Si wafer 102. The surface dielectric tunnel layer 108 may comprise silicon oxide (SiO_x), aluminium oxide (AlO_x), titanium oxide (TiO_x) or silicon nitride (SiN_x). On

top of the surface dielectric tunnel layer 108 is a first doped semiconductor layer 110. In the present embodiment, the first doped semiconductor layer 110 comprises a p^+ doped (e.g. boron doped) polysilicon (poly-Si) layer. As shown in Figure 1, the surface dielectric tunnel layer 108 is therefore sandwiched between a front side surface of the Si wafer 102 and the first doped semiconductor layer 110. The first doped semiconductor layer 110 may be deposited using plasma enhanced chemical vapour deposition (PECVD) or low pressure chemical vapour deposition (LPCVD). The solar cell 100 further comprises a dielectric tunnel layer 112 deposited on a rear side surface of the Si wafer 102 and an interlayer dielectric tunnel layer 114 deposited on the first doped semiconductor layer 110 on the front side 104 of the Si wafer 102. In the present embodiment, the dielectric tunnel layer 112 and the interlayer dielectric tunnel layer 114 comprises SiO_x. The solar cell 100 further comprises a front side second doped semiconductor layer 116 deposited on the front side 104 of the Si wafer 102 and a rear side second doped semiconductor layer 118 deposited on the rear side 106 of the Si wafer 102. Each of the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 is of an opposite polarity to the first doped semiconductor layer 110. In the present embodiment, the second doped semiconductor layers 116, 118 may comprise an n^+ doped (e.g. phosphorous doped) polysilicon (poly-Si) layer. In the present embodiment, the dielectric tunnel layer 112, the interlayer dielectric tunnel layer 114, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 may be deposited using a double-side deposition method such as LPCVD. In this case, the dielectric tunnel layer 112 and the interlayer dielectric tunnel layer 114 may be deposited on the respective side of the Si wafer 102 at the same time using LPCVD, and the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 may subsequently be deposited on the respective side of the Si wafer 102 at the same time using LPCVD. In other words, in the present embodiment, a SiO_x/n^+-poly-Si tunnel layer passivated contact is deposited on each of the front side 104 and the rear side 106 of the Si wafer 102 using a single LPCVD process. In other embodiments, the dielectric tunnel layer 112, the interlayer dielectric tunnel layer 114, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 may be deposited using a single-side deposition method such as PECVD. The method for fabricating the solar cell 100 using either PECVD or LPCVD is described below in relation to Figure 2A and Figure 2B respectively. The solar cell 100 comprises a contact formation layer 120 optionally deposited on the

rear side second doped semiconductor layer 118. The solar cell 100 further comprises a rear metal contact 122 deposited on the contact formation layer 120. The rear metal contact 122 may be deposited using a conventional high-temperature fire-through screen printing paste so that the rear metal contact 122 deposited is in electrical contact with
5 the rear side second doped semiconductor layer 118.

As shown in Figure 1, the solar cell 100 comprises passivated contacts 124, 126 of opposite polarity (i.e. one is electron extracting while the other is hole extracting) formed on each of the front side 104 and the rear side 106 of the Si wafer 102. A hole extracting passivated contact 124, comprising the surface dielectric tunnel layer 108 and the first
10 doped semiconductor layer 110, is formed on the front side 104 of the Si wafer 102, while an electron extracting passivated contact 126, comprising the dielectric tunnel layer 112 and the rear side second doped semiconductor layer 118, is formed on the rear side 106 of the Si wafer 102. In addition, a tunnel junction 128, comprising the first doped semiconductor layer 110, the interlayer dielectric tunnel layer 114 and the front side
15 semiconductor layer 116, is formed on the front side 104 of the Si wafer. In this embodiment, the tunnel junction 128 formed on the front side 104 of the Si wafer 102 functions to separate the top cell voltage from the bottom cell voltage when integrated in a tandem solar cell structure. The solar cell 100 of the present embodiment, which has the tunnel junction 128 integrally formed on the front side 104 of the Si wafer 102,
20 therefore reduces the number of process steps when deployed as a bottom cell in a tandem solar cell structure.

In particular, in the present embodiment, the tunnel junction 128 formed comprises a p^+ poly-Si/SiO_x/n^+-poly-Si stack. The SiO_x/n^+ poly-Si passivated contact can therefore be deployed on both the front side 104 and the rear side 106 of the solar cell 100 using
25 conventional double-side deposition technology (such as LPCVD), where it forms part of the tunnel junction 128 on the front side of the solar cell 100 as aforementioned described, and it forms a SiO_x/n^+ poly-Si electron-extracting passivated contact on the rear side of the solar cell 100. By deploying conventional double-side deposition processes (e.g. LPCVD) to form the tunnel oxide and the poly-Si capping layer in this way, further
30 masking and subsequent mask-removal steps are minimized. The amount of process steps needed are thereby significantly reduced. This is achievable as the deposited passivated contact (i.e. SiO_x/n^+ poly-Si) simultaneously form (i) the tunnel junction by incorporating with the first doped semiconductor layer 110 on the front side of the solar

cell 100, and (ii) the electron-extracting passivated contact at the rear side of the solar cell 100.

Moreover, the solar cell 100 comprises a front side emitter formed by the hole extracting passivated contact 124 which includes a p^+ doped poly-Si layer. Compared to conventional highly doped diffused region within the wafer which is typically in the range of several 100 nm thick, the p^+ doped poly-Si layer can be processed much thinner (e.g. within the range of 3 -15 nm), thereby significantly reduces parasitic near infrared (NIR) absorption. In light of these, the solar cell 100 is particularly advantageous when deployed as a bottom solar cell for tandem solar cell integration.

Further, the solar cell 100 comprises a planar front side and a textured rear side. When deployed as a bottom cell for a tandem solar cell structure, the planar front side of the solar cell 100 enables a conventional front-side perovskite top cell integration, while the textured rear side of the solar cell 100 improves light trapping for the infrared photons. Using a fully processed solar cell 100 as a silicon bottom cell pre-cursor without the rear-side metal contact, conventional spin-coating or dip-coating (which requires a planar surface) for the perovskite top cell depositions can be used. In this case, as a last process step for the tandem solar cell fabrication after completion of a thin-film top cell integration, a low temperature full-area metallisation (e.g. using rear-side thermal evaporation, electron-beam evaporation or sputtering) can be performed.

Accordingly, the solar cell 100 is able to outperform a conventional heterojunction solar cell (in terms of solar cell efficiency as well as costs) which is at present the state-of-the-art silicon bottom cell used for tandem solar cell integration.

Figures 2A and 2B are flowcharts showing methods 200, 220 for fabricating the solar cell 100 of Figure 1. Figure 2A is a flowchart showing steps of a method for fabricating the solar cell using PECVD, while Figure 2B is a flowchart showing steps of a method for fabricating the solar cell using LPCVD.

In each of the methods 200, 220, an n-type Czochralski grown monocrystalline silicon (Si) wafer is used as a starting substrate for fabricating the solar cell 100. As would be appreciated by the skilled person in the art, preparatory steps (e.g. cleaning the Si wafer surface) may be necessary before each fabrication step, and these preparatory steps have been omitted for clarity and succinctness of the present methods 200, 220.

Referring to the method 200 of Figure 2A, in a step 202, the rear side 106 of the Si wafer 102 of the solar cell 100 is textured. Texturing the rear side 106 of the Si wafer 102 may comprise etching the rear side 106 of the Si wafer 102, for example using a wet chemical etch. Please note, the step 102 as described is not necessarily the first process step and it may be performed at a later stage. This is shown, for example, in the method 220 of Figure 2B.

In a step 204, the surface dielectric tunnel layer 108 is deposited on the planar front side 104 of the Si wafer 102. The surface dielectric tunnel layer 108 may comprise aluminium oxide (AlO_x), silicon nitride (SiN_x) or titanium oxide (TiO_x) deposited by atomic layer deposition (ALD) or silicon oxide (SiO_x) deposited by chemical vapour deposition (PECVD or LPCVD). In this embodiment, the surface dielectric tunnel layer 108 is deposited by PECVD.

In a step 206, the first doped semiconductor layer 110 is formed on the surface dielectric tunnel layer 108. The first doped semiconductor layer 110 comprises p^+ doped poly-Si for the purpose of forming a contact that can selectively extract holes. The first doped semiconductor layer 110 together with the surface dielectric tunnel layer 108 form a hole extracting passivated contact (e.g. SiO_x/p^+ poly-Si stack). The first doped semiconductor layer 110 is deposited by PECVD. In the present embodiment where the surface dielectric tunnel layer 108 and the first doped semiconductor layer 110 are both deposited by PECVD, the steps 204 and 206 are effectively combined into one process step since these two layers can be deposited using the same CVD machine (e.g. by introducing process gases for the deposition of the surface dielectric tunnel layer 108 and the first doped semiconductor layer 110 one after the other).

After the deposition of the surface dielectric tunnel layer 108 and the first doped semiconductor layer 110, SiO_x/n^+ poly-Si layers are formed on each of the front side 104 and the rear side 106 of the Si wafer 102 in steps 208, 210 and 212 as described below. In the present embodiment, the SiO_x/n^+ poly-Si layers form an electron extracting passivated contact on the rear side 106 of the Si wafer 102 (i.e. on an opposite side of the first doped semiconductor layer) and a tunnel junction augmented hole extracting passivated contact (i.e. SiO_x/p^+ poly-Si/SiO_x/n^+ poly-Si layers) on the front side 104 of the Si wafer 102.

In the step 208, the dielectric tunnel layer 112 is deposited on the textured rear side 106 of the Si wafer 102. The dielectric tunnel layer 112 can be deposited as a full-area deposition on the rear side of the Si wafer 102. The dielectric tunnel layer 112 comprises SiO_x deposited, for example, by PECVD or LPCVD.

5 In the step 210, the interlayer dielectric tunnel layer 114 is deposited on the first doped semiconductor layer 110. The deposition of the interlayer dielectric tunnel layer 114 comprises a full-area deposition on the front side 104 of the Si wafer 102. Similar to the dielectric tunnel layer 112, in the present embodiment, the interlayer dielectric tunnel layer 114 comprises SiO_x deposited by PECVD. In an embodiment, the dielectric tunnel 10 layer 112 and the interlayer dielectric tunnel layer 114 may be deposited in a same deposition step if a double-side deposition technology such as LPCVD is used.

After the deposition of the dielectric tunnel layer 112 and the interlayer dielectric tunnel layer 114 in the step 208 and the step 210 respectively, the front side second doped semiconductor layer 116 is deposited on the interlayer dielectric tunnel layer 114 at the 15 front side 104 of the Si wafer 102 and the rear side second doped semiconductor layer 118 is deposited on the dielectric tunnel layer 112 at the rear side 106 of the Si wafer 102 in the step 212. In the present embodiment, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 are deposited by single-side deposition technology such as PECVD. In this case, the front 20 side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 may be deposited using separate single-side deposition processes. Alternatively, as will be described below, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 may be deposited using LPCVD. The dielectric tunnel layer 112 together with the rear side 25 second doped semiconductor layer 118 formed an electron extracting passivated contact. In the present embodiment, the rear side second doped semiconductor layer 118 comprises n^+ doped poly-Si for the purpose of forming a contact that can selectively extract electrons.

In a step 214, the contact formation layer 120 is deposited on the rear side second doped 30 semiconductor layer 118. The deposition of the contact formation layer 120 comprises a full area deposition on the rear side 106 of the Si wafer 102. In the present embodiment, the contact formation layer 120 comprises a SiN_x layer which acts as an insulating

transparent passivation layer. In this case, contact openings may be formed either by fire-through screen printing paste used in a high temperature screen printing process or by local laser ablation in the SiN_x layer, in order to form electrical contacts for the solar cell 100. In another embodiment, the contact formation layer 120 comprises a
5 transparent conducting oxide (TCO) layer. The TCO forms a conductive transparent contact formation layer.

In a step 216, a rear metal contact 122 is deposited on the contact formation layer 120 to form an electrical contact for the rear side passivated contact 126. The rear metal contact 122 may be screen printed on top of the contact formation layer 120 using
10 conventional screen printing technology. In the present embodiment where the contact formation layer 120 comprises a SIN_x layer, a conventional high-temperature fire-through screen printing paste is used to form the rear metal contact 122. Alternatively, local laser ablation can be used to form contact openings in the SiN_x contact formation layer 120 before the conventional screen printing process, followed by using a non-fire through
15 screen printing paste to form the rear metal contact 122. In an embodiment where the contact formation layer 120 comprises a TCO layer, subsequent low-temperature screen printing can be used to form the rear metal contact 122.

The method 220 of Figure 2B is described below. The method 220 showing steps for fabricating the solar cell using LPCVD in accordance with an embodiment. The method
20 220 is similar to the method 200 except for the use of LPCVD (instead of PECVD) in forming the surface dielectric tunnel layer 108, the first doped semiconductor layer 110, dielectric tunnel layer 112, the interlayer dielectric tunnel layer 114, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118. The differences are shown in the first five process steps 222, 224, 226, 202 and
25 228 of the method 220. The rest of the steps 208, 210, 212, 214, 216 are similar to those of the method 200, but with the following difference: in the present embodiment where the dielectric tunnel layer 112, the interlayer dielectric tunnel layer 114, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 are all deposited by LPCVD, the steps 208, 210 and 212 are effectively
30 combined into one process step since these layers 112, 114, 116 and 118 can be deposited using the same CVD machine by introducing process gases for each of the aforementioned double-side deposition process one after the other (e.g. double-side deposition to form firstly the dielectric tunnel layer 112 on the rear side 106 and the

interlayer dielectric tunnel layer 114 on the front side 104 of the Si wafer 102, followed by double-side deposition to form the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118).

Referring to the method 220 of Figure 2B, instead of having a first step of texturing the
5 rear side 106 of the Si wafer 102 of the solar cell 100, a step 222 is first performed to deposit the surface dielectric tunnel layer 108 on each of the front side 104 and the rear side 106 of the Si wafer 102. In the present embodiment, the surface dielectric tunnel layer 108 comprises silicon oxide (SiO_x) deposited by chemical vapour deposition (e.g. LPCVD).

10 In a step 224, the first doped semiconductor layer 110 is formed on each of the surface dielectric tunnel layers 108 deposited on the front side 104 and the rear side 106 of the Si wafer 102. In the present embodiment, the first doped semiconductor layer 110 comprises p^+ doped poly-Si for the purpose of forming a contact that can selectively extract holes. In this case, the first doped semiconductor layer 110 together with the
15 surface dielectric tunnel layer 108 form a hole extracting passivated contact (e.g. SiO_x/p^+ poly-Si layer stack). The first doped semiconductor layer 110 is deposited by LPCVD. In the present case where the surface dielectric tunnel layer 108 and the first doped semiconductor layer 110 are both deposited by LPCVD, the steps 222 and 224 are effectively combined into one process step since these two layers can be deposited using
20 the same CVD machine (e.g. by introducing process gases for the deposition of the surface dielectric tunnel layer 108 and the first doped semiconductor layer 110 one after the other).

After the steps 222 and 224, a mask is formed on the front side 104 of the Si wafer 102 in a step 226. The mask functions to protect the SiO_x/p^+ poly-Si layer stack formed on
25 the front side 104 of the Si wafer 102 during a subsequent etching process. The mask may be formed by a suitable material to achieve this function, for example, PECVD deposited SiN_x.

Once the mask is formed on the front side 104 of the Si wafer 102 in the step 226, the step 202 is performed to texture the rear side 106 of the Si wafer 102. Texturing the rear
30 side 106 of the Si wafer 102 may involve a wet chemical etch. In this case, for example, the entire Si wafer 102 may be exposed to a chemical etchant during the etch and therefore the mask serves to protect the SiO_x/p^+ poly-Si layer stack formed on the front

side 104 of the Si wafer 102 in the previous steps 222, 224. In the step 102 for texturing of the rear side 106 of the Si wafer 102, the SiO_x/p^+ poly-Si layer stack formed on the rear side 106 of the Si wafer 102 is also etched away, while the rear side 106 of the Si wafer 102 is textured.

5 In a step 228, the mask which was deposited on the front side 104 of the Si wafer 102 is removed. The mask may be removed by physical etching or selective chemical etching.

After the removal of the mask in the step 228, SiO_x/n^+ poly-Si layers are formed on each of the front side 104 and the rear side 106 of the Si wafer 102 in steps 208, 210 and 212 as previously described. However, in the present embodiment, the steps 208, 210 and 10 212 are performed using LPCVD.

In a step 208, the dielectric tunnel layer 112 is deposited on the textured rear side 106 of the Si wafer 102. The dielectric tunnel layer 112 can be deposited as a full-area deposition on the rear side of the Si wafer 102. In a step 210, the interlayer dielectric tunnel layer 114 is deposited on the first doped semiconductor layer 110. The deposition 15 of the interlayer dielectric tunnel layer 114 comprises a full-area deposition on the front side 104 of the Si wafer 102. In the present embodiment, the dielectric tunnel layer 112 and the interlayer dielectric tunnel layer 114 may be deposited in a same deposition step using LPCVD.

Similar to the method 200, after the deposition of the dielectric tunnel layer 112 and the 20 interlayer dielectric tunnel layer 114 in the step 208 and the step 210 respectively, the front side second doped semiconductor layer 116 is deposited on the interlayer dielectric tunnel layer 114 at the front side 104 of the Si wafer 102 and the rear side second doped semiconductor layer 118 is deposited on the dielectric tunnel layer 112 at the rear side 106 of the Si wafer 102 in a step 212. In the present embodiment, the deposition of the 25 front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 comprises a double-side full-area deposition using LPCVD. In other words, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118 can be deposited in a single deposition step. The dielectric tunnel layer 112 together with the rear side second doped semiconductor 30 layer 118 form an electron extracting passivated contact. The rear side second doped semiconductor layer 118 may comprise n^+ doped poly-Si for the purpose of forming a contact that can selectively extract electrons. On the other hand, in the present

embodiment, a tunnel junction augmented hole extracting passivated contact (i.e. SiO_x/p^+ poly-Si/SiO_x/n^+ poly-Si layers) is formed on the front side 104 of the Si wafer 102.

In the present embodiment where the dielectric tunnel layer 112, the interlayer dielectric tunnel layer 114, the front side second doped semiconductor layer 116 and the rear side 5 second doped semiconductor layer 118 are all deposited by LPCVD, the steps 208, 210 and 212 are effectively combined into one process step since these layers 112, 114, 116 and 118 can be deposited using the same CVD machine by introducing process gases for each of the aforementioned double-side deposition process one after the other (e.g. double-side deposition to form firstly the dielectric tunnel layer 112 on the rear side 106 10 and the interlayer dielectric tunnel layer 114 on the front side 104 of the Si wafer 102, followed by double-side deposition to form the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118).

In a step 214, the contact formation layer 120 is deposited on the rear side second doped semiconductor layer 118. The deposition of the contact formation layer 120 comprises a 15 full area deposition on the rear side 106 of the Si wafer 102. The contact formation layer 120 comprises either SiN_x or TCO as described above.

In a step 216, a rear metal contact 122 is deposited on the contact formation layer 120 to form an electrical contact for the rear side passivated contact 126. The rear metal contact 122 may be screen printed using a fire through or a non-fire through screen 20 printing paste as previously described.

For the present embodiments as aforementioned described, the quality of the resulting tunnel junction 128 formed is critical for effectively converting minority hole current into a majority electron current. This requires that the effective doping of the first doped semiconductor layer 110 (e.g. p^+ doped poly-Si) and the front side second doped 25 semiconductor layer 116 (e.g. n^+ doped poly-Si) to be sufficiently high in order to form an ohmic tunnel junction (in contrast to a rectifying p/n junction). As discussed in relation to Figures 6A, 6B and 6C below, it has been successfully demonstrated that a high quality tunnel junction can be formed by using two highly oppositely doped poly-Si capping layers or by using a highly doped diffused surface of a silicon wafer and a highly 30 oppositely doped poly-Si capping layer. It is shown that these tunnel junctions maintain high passivation quality as demonstrated by the high minority carrier lifetime and a

correspondingly high implied open circuit voltage, for example, as shown in relation to Figures 8A and 8B.

Figure 3 is a schematic structure of the solar cell 300 in accordance with a second embodiment. This solar cell 300 can be deployed as a single-junction, high efficiency
5 solar cell. Variations of the solar cell 300 for deploying as single-junction solar cells are discussed in relation to Figures 12A to 12F.

The solar cell 300 comprises an n-type Czochralski (Cz) grown monocrystalline Si wafer 302 with a front side 304 and a rear side 306. Differing from the solar cell 100, the solar cell 300 includes a rear emitter provided by a tunnel junction which is formed on a rear
10 side 306 of the Si wafer 302. In this case, a surface dielectric tunnel layer 308 is deposited on the rear side 306 of the Si wafer 302. In the present embodiment, the surface dielectric tunnel layer 308 comprises SiO_x. The surface dielectric tunnel layer 308 may comprise AlO_x, TiO_x or SiN_x. The solar cell 300 further comprises a first doped semiconductor layer 310 formed on the surface dielectric tunnel layer 308 at the rear
15 side 306 of the Si wafer 302. Similar to the solar cell 100, the first doped semiconductor layer 310 comprises a p^+ doped (e.g. boron doped) polysilicon (poly-Si) layer. As shown in Figure 3, the surface dielectric tunnel layer 308 is therefore sandwiched between the rear side surface of the Si wafer 302 and the first doped semiconductor layer 310. The first doped semiconductor layer 310 may be deposited by PECVD or LPCVD. The solar
20 cell 300 further comprises a dielectric tunnel layer 312 deposited on a surface of the front side 304 of the Si wafer 302 and an interlayer dielectric tunnel layer 314 deposited on the first doped semiconductor layer 310 at the rear side 306 of the Si wafer 302. In this embodiment, the dielectric tunnel layer 312 and the interlayer dielectric tunnel layer 314 comprises SiO_x. The solar cell 300 further comprises a front side second doped
25 semiconductor layer 316 deposited on the dielectric tunnel layer 312 at the front side 304 of the Si wafer 302 and a rear side second doped semiconductor layer 318 deposited on the interlayer dielectric tunnel layer 314 at the rear side 306 of the Si wafer 302. The front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318 are each of an opposite polarity to the first doped
30 semiconductor layer 310. In the present embodiment, the second doped semiconductor layers 316, 318 may comprise an n^+ doped (e.g. phosphorous doped) polysilicon (poly-Si) layer. The dielectric tunnel layer 312, the interlayer dielectric tunnel layer 314, the front side second doped semiconductor layer 316 and the rear side second doped

semiconductor layer 318 may be deposited using a double-side deposition method such as LPCVD. In this case, the dielectric tunnel layer 312 and the interlayer dielectric tunnel layer 314 may be deposited on their respective side of the Si wafer 302 at the same time using LPCVD, and the front side second doped semiconductor layer 316 and the rear
5 side second doped semiconductor layer 318 may subsequently be deposited on their respective side of the Si wafer 302 at the same time using LPCVD. In other words, in the present embodiment, a SiO_x/n^+-poly-Si tunnel layer passivated contact is deposited on the front side 304 and a tunnel junction augmented SiO_x/p^+-poly-Si passivated contact is deposited at the rear side 306 of the Si wafer 302 using a single LPCVD process. In
10 addition to a contact formation layer 320 deposited on the rear side 306 of the Si wafer 302 (which is in the case for the solar cell 100), the solar cell 300 comprises a contact formation layer 322 deposited on the front side second doped semiconductor layer 316 at the front side 304 of the Si wafer 302. In the present embodiment, the contact formation layers 320, 322 comprise SiN_x layers. In other embodiments as discussed in
15 relation to Figures 12E and 12F and as described above, the contact formation layers 320, 322 comprise TCO layers. The solar cell 300 further comprises a rear metal contact 324 deposited on the rear side contact formation layer 320 and a front metal contact 326 the front side contact formation layer 322. In the present embodiment, the rear metal contact 324 and the front metal contact 326 are deposited using a conventional high-
20 temperature fire-through screen printing paste so that the rear metal contact 324 and the front metal contact 326 deposited are in electrical contact with the rear side second doped semiconductor layer 318 and the front side second doped semiconductor layer 316 respectively. In other embodiments where TCO is used for the contact formation layers 320, 322, low temperature non-fire through screen printing can be used.

25 Similar to the solar cell 100, in this embodiment as shown in Figure 3, passivated contacts 328, 330 of opposite polarity (i.e. one is electron extracting while the other is hole extracting) are formed on each of the front side 304 and the rear side 306 of the Si wafer 302. However, in the solar cell 300, a hole extracting passivated contact 330 comprising the surface dielectric tunnel layer 308 and the first doped semiconductor layer
30 310, is formed on the rear side 306 of the Si wafer 302, while an electron extracting passivated contact 328 comprising the dielectric tunnel layer 312 and the front side second doped semiconductor layer 316 is formed on the front side 304 of the Si wafer 302. In addition, a tunnel junction 332, comprising the first doped semiconductor layer

310, the interlayer dielectric tunnel layer 314 and the rear side semiconductor layer 318, is formed on the rear side 306 of the Si wafer 302.

In this embodiment, the first doped semiconductor layer 310 (i.e. the p^+ doped poly-Si layer) forms an emitter on the rear side 306 of the solar cell 300. The tunnel junction 332 is placed on the rear side so as to reduce parasitic absorption, which occurs in highly doped semiconductor layer. This minimizes front side parasitic UV-VIS absorption, which is highly important in particular for the case of a single-junction silicon cell since the single-junction solar cell receives all high energy photons (including photons of ultraviolet/blue wavelengths), as compared to a silicon bottom cell for tandem application which typically receives only photons in the near infrared wavelengths. The solar cell 300 of the present embodiment therefore comprises a rear side emitter formed by an ultra-thin SiO_x/p^+ poly-Si hole extracting passivated contact 330. In another embodiment, the rear side emitter is formed by a conventionally p^+ diffused or ion implanted layer within the silicon wafer as discussed in relation to Figure 12A below. Compared with the solar cell 100, the solar cell 300 comprises bifacial local metal contacts which include the rear metal contact 324 and the front metal contact 326 (e.g. metal grid fingers) formed at both sides of the solar cell 300. The front metal contact 326 may be formed by inline-plating as conventional screen printing on top of ultra-thin ($\leqslant$10 nm) poly-Si contact passivation layers may damage these layers. In other embodiments where a TCO layer is used for the contact formation layers 320, 322, low temperature non-fire through screen printing can be used to form the rear metal contact 324 and/or the front metal contact 326.

Figures 4A and 4B are flowcharts showing methods 400, 420 for fabricating the solar cell 300 of Figure 3. Figure 4A is a flowchart showing steps of the method 400 for fabricating the solar cell using PECVD and Figure 4B is a flowchart showing steps of the method 420 for fabricating the solar cell using LPCVD.

In these embodiments for fabricating a single-junction silicon solar cell 300, the basic fabrication processes are similar. For example, (i) the texturing process in relation to a surface of the Si wafer, (ii) the deposition processes in relation to the surface dielectric tunnel layer, the dielectric tunnel layer, the interlayer dielectric tunnel layer and the contact formation layer, (iii) the formation of the first doped semiconductor layer and the second doped semiconductor layers and (iv) the formation of the metal contacts are similar to the corresponding ones described in relation to the methods 200 and 220 of

Figures 2A and 2B. In particular, the processing steps for the method 400 of Figure 4A are similar to the processing steps of the method 200 of Figure 2A, while the processing steps for the method 420 of Figure 4B are similar to the processing steps of the method 220 of Figure 2B. The detail of each of these processing steps will therefore not be
5 repeated here in their entirety. Brief descriptions of the method 400 and the method 420 are provided below for completeness.

Referring to Figure 4A, similar to the method 200, an n-type Czochralski grown monocrystalline silicon (Si) wafer is used as a starting substrate for fabricating the solar cell 300 in the method 400. In a step 402, the front side 304 of the Si wafer 302 of the
10 solar cell 300 is textured (as compared to texturing the rear side 106 of the Si wafer 102 of the solar cell 100). Similar to the step 202, texturing the front side 304 of the Si wafer 302 may comprise etching the front side 304 of the Si wafer 302, for example, using a wet chemical etch. Again, this texturing step 402 may be performed at a later stage. An example of this is shown in the method 420 of Figure 4B.

15 In a step 404, the surface dielectric tunnel layer 308 is deposited on the planar rear side 306 of the Si wafer 302. In the present embodiment, the surface dielectric tunnel layer 308 comprises is SiO_x deposited by PECVD. In other embodiments, the surface dielectric tunnel layer 308 may comprise AlO_x, SiN_x or TiO_x deposited by ALD or SiO_x deposited by LPCVD (as shown in relation to Figure 4B below).

20 In a step 406, the first doped semiconductor layer 310 is formed on the surface dielectric tunnel layer 308. Similar to the solar cell 100, the first doped semiconductor layer 310 of the solar cell 300 comprises p^+ doped poly-Si for the purpose of forming a contact that can selectively extract holes. The first doped semiconductor layer 310 together with the surface dielectric tunnel layer 308 form a hole extracting passivated contact 330. In the
25 present embodiment, the first doped semiconductor layer 310 is deposited by PECVD. In another embodiment for example as shown in the method of Figure 4B, the first doped semiconductor layer 310 is deposited by LPCVD. Similar to the method 200, in an embodiment where the surface dielectric tunnel layer 308 and the first doped semiconductor layer 310 are both deposited by PECVD, the steps 204 and 206 are
30 effectively combined into one process step since these two layers can be deposited using the same CVD machine.

After the deposition of the surface dielectric tunnel layer 308 and the first doped semiconductor layer 310, a SiO_x/n^+-poly-Si layer stack is formed on each of the front side 304 and the rear side 306 of the Si wafer 302. In the present embodiment, the SiO_x/n^+ poly-Si layers form an electron extracting passivated contact on the front side 304 of the
5 Si wafer 302 and a tunnel junction augmented hole extracting passivated contact (i.e. SiO_x/p^+ poly-Si/SiO_x/n^+ poly-Si layers) on the rear side 306 of the Si wafer 302 as described below.

In a step 408, the dielectric tunnel layer 312 is deposited on the textured front side 304 of the Si wafer 302. The dielectric tunnel layer 312 can be deposited as a full-area
10 deposition on the front side 304 of the Si wafer 302. In the present embodiment, the dielectric tunnel layer 312 comprises SiO_x deposited by PECVD. In another embodiment for example the method 420 as shown in Figure 4B, the dielectric tunnel layer 312 comprises SiO_X deposited by LPCVD.

In a step 410, the interlayer dielectric tunnel layer 314 is deposited on the first doped
15 semiconductor layer 310. The deposition of the interlayer dielectric tunnel layer 314 comprises a full-area deposition on the front side 304 of the Si wafer 302. Similar to the dielectric tunnel layer 312, in the present embodiment, the interlayer dielectric tunnel layer 314 comprises SiO_x deposited by PECVD. In another embodiment for example the method 420 as shown in Figure 4B, the interlayer dielectric tunnel layer 314 comprises
20 SiO_X deposited by LPCVD. In an embodiment, for example as shown in Figure 4B, the dielectric tunnel layer 312 and the interlayer dielectric tunnel layer 314 may be deposited in a same deposition step if a double-side deposition technology is used (e.g. LPCVD).

After the deposition of the dielectric tunnel layer 312 and the interlayer dielectric tunnel layer 314 in the step 408 and the step 410 respectively, the front side second doped
25 semiconductor layer 316 is deposited on the dielectric tunnel layer 312 at the front side 304 of the Si wafer 302, and the rear side second doped semiconductor layer 318 is deposited on the interlayer dielectric tunnel layer 314 at the rear side 306 of the Si wafer 302 in a step 412. In the present embodiment, the front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318 are
30 deposited by PECVD. In this case, the front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318 may be deposited using separate single-side deposition processes. The dielectric tunnel layer 312 together with

the front side second doped semiconductor layer 316 formed an electron extracting passivated contact. The rear side second doped semiconductor layer 318 comprises n^+ doped poly-Si for the purpose of forming a tunnel junction with the first doped semiconductor layer 310, thus forming a tunnel junction augmented passivated contact
5 332, that can selectively extract holes. In another embodiment, the front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318 are deposited by LPCVD as described below.

In a step 414, the front side contact formation layer 322 is deposited on the front side second doped semiconductor layer 316 and the rear side contact formation layer 320 is
10 deposited on the rear side second doped semiconductor layer 318. The deposition of the front side contact formation layer 322 and the rear side contact formation layer 320 may comprise a full area deposition on the front side 304 and the rear side 306 of the Si wafer 302 respectively. Similar to the step 214, in the present embodiment, the contact formation layers 320, 322 comprise SiN_x layers which act as insulating passivation layers.
15 Alternatively, they may comprise TCO, which acts as conductive contact layers. The SiN_x layer maybe deposited using PECVD while the TCO may be deposited by sputtering.

In a step 416, a rear metal contact 324 is deposited on the rear side contact formation layer 320 to form a rear electrical contact. In the present embodiment, the rear metal contact 324 is screen printed on top of the rear side contact formation layer 320 using a
20 conventional high-temperature fire-through screen printing paste. Alternatively, contact openings can be formed in the rear side contact formation layer 320 by local laser ablation prior to forming the rear metal contact 324 by inline plating. In an embodiment where the rear side contact formation layer 320 comprises TCO, a screen printing using a conventional low-temperature non-fire through screen printing paste can be performed
25 to form the rear metal contact 324.

In a step 418, a front metal contact 326 is deposited on the front side contact formation layer 322 to form a front electrical contact for the front side passivated contact which comprises the dielectric tunnel layer 312 and the front side second doped semiconductor layer 316. In the present embodiment where the front side contact formation layer 322
30 comprises a SiN_x layer, the front metal contact 326 is formed by inline-plating as conventional high-temperature fire-through screen printing on top of ultra-thin ($\leqslant$10 nm) poly-Si contact passivation layers may damage these layers. In the present embodiment

where the contact formation layer 322 comprises a SiN_x layer, in order to form the front metal contact 326 by inline-plating, contact openings are first formed in the SiN_x layer prior to formation of the front metal contact 326. In another embodiment where the front-side contact formation layer 322 comprises a TCO layer, low-temperature non-fire-
5 through screen printing can be deployed to form the front metal contact 326.

Referring to the method 420 of Figure 4B, instead of having a first step of texturing the front side 304 of the Si wafer 302 of the solar cell 300, a step 422 is first performed to deposit the surface dielectric tunnel layer 308 on each of the front side 304 and the rear side 306 of the Si wafer 302. In the present embodiment, the surface dielectric tunnel
10 layer 308 comprises silicon oxide (SiO_x) deposited by chemical vapour deposition (e.g. LPCVD).

In a step 424, the first doped semiconductor layer 310 is formed on each of the surface dielectric tunnel layers 308 deposited on the front side 304 and the rear side 306 of the Si wafer 302. In the present embodiment, the first doped semiconductor layer 310
15 comprises p^+ doped poly-Si for the purpose of forming a contact that can selectively extract holes. In this case, the first doped semiconductor layer 310 together with the surface dielectric tunnel layer 308 form a hole extracting passivated contact (e.g. SiO_x/p^+ poly-Si layer stack). In the present case, the first doped semiconductor layer 310 is deposited by LPCVD. In the present embodiment where the surface dielectric tunnel
20 layer 308 and the first doped semiconductor layer 310 are both deposited by LPCVD, the steps 422 and 424 are effectively combined into one process step since these two layers can be deposited using the same CVD machine (e.g. by introducing process gases for the deposition of the surface dielectric tunnel layers 308 and the first doped semiconductor layers 310 one after the other).

25 After the steps 422 and 424, a mask is formed on the rear side 306 of the Si wafer 302 in a step 426. The mask functions to protect the SiO_x/p^+ poly-Si layer stack on the rear side 306 of the Si wafer 302 during a subsequent etching process. The mask may be formed by a suitable material to achieve this function, for example PECVD deposited SiN_x.

30 Once the mask is formed on the rear side 306 of the Si wafer 302 in the step 426, the step 402 is performed to texture the front side 304 of the Si wafer 302. Texturing the front side 304 of the Si wafer 302 may involve for example a wet chemical etch. In this case,

for example, the entire Si wafer 302 may be exposed to a chemical etchant during the etch and therefore the mask serves to protect the SiO_x/p^+ poly-Si layer stack formed on the rear side 306 of the Si wafer 302 in the previous steps 422, 424. In the step 402 for texturing of the front side 304 of the Si wafer 302, the SiO_x/p^+ poly-Si layer stack formed
5 on the front side 304 of the Si wafer 302 is also etched away while the front side 304 of the Si wafer 302 is textured.

In a step 428, the mask which was deposited on the rear side 306 of the Si wafer 302 is removed. The mask may be removed by physical etching or selective chemical etching.

After the removal of the mask in the step 428, SiO_x/n^+ poly-Si layers are formed on each
10 of the front side 304 and the rear side 306 of the Si wafer 302 in steps 408, 410 and 412 as previously described. However, in the present embodiment, the steps 408, 410 and 412 are performed using LPCVD.

Following the step 428, the dielectric tunnel layer 312 is deposited on the textured front side 304 of the Si wafer 302 in the step 408. In the present embodiment, the dielectric
15 tunnel layer 312 is deposited as a full-area deposition on the front side 304 of the Si wafer 302. The dielectric tunnel layer 312 comprises SiO_x deposited, in this case, by LPCVD.

In the step 410, the interlayer dielectric tunnel layer 314 is deposited on the first doped semiconductor layer 310 on the rear side 306 of the Si wafer 302. The deposition of the
20 interlayer dielectric tunnel layer 314 comprises a full-area deposition on the front side 304 of the Si wafer 302. Similar to the dielectric tunnel layer 312, the interlayer dielectric tunnel layer 314 comprises SiO_x deposited by LPCVD. In the present embodiment, the dielectric tunnel layer 312 and the interlayer dielectric tunnel layer 314 are deposited in a same deposition step by using LPCVD which is a double-side deposition technology.
25 This advantageously cut down on the number of deposition steps required

After the deposition of the dielectric tunnel layer 312 and the interlayer dielectric tunnel layer 314, the front side second doped semiconductor layer 316 is deposited on the dielectric tunnel layer 312 at the front side 304 of the Si wafer 302, and the rear side second doped semiconductor layer 318 is deposited on the interlayer dielectric tunnel
30 layer 314 at the rear side 306 of the Si wafer 302 in a step 412. In the present embodiment, the deposition of the front side second doped semiconductor layer 316 and

the rear side second doped semiconductor layer 318 comprises a double-side full-area deposition using LPCVD. In this case, the front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318 can be deposited in a single deposition step. The dielectric tunnel layer 312 together with the front side second
5 doped semiconductor layer 316 formed an electron extracting SiO_x/n^+ poly-Si passivated contact on the front side 304. The front side second doped semiconductor layer 316 comprises n^+ doped poly-Si for the purpose of forming a contact that can selectively extract electrons. The rear side second doped semiconductor layer 318 comprises n^+ doped poly-Si for the purpose of forming a tunnel junction with the first doped
10 semiconductor layer 310, thus forming a tunnel junction augmented passivated contact 332 (i.e. SiO_x/p^+ poly-Si/SiO_x/n^+ poly-Si layers), that can selectively extract holes.

In the present embodiment where the dielectric tunnel layer 312, the interlayer dielectric tunnel layer 314, the front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318 are all deposited by LPCVD, the steps 408, 410
15 and 412 are effectively combined into one process step since these layers 312, 314, 316 and 318 can be deposited using the same CVD machine by introducing process gases for each of the aforementioned double-side deposition process one after the other. For example, a double-side deposition can be performed to form the dielectric tunnel layer 312 on the front side 304 and the interlayer dielectric tunnel layer 314 on the rear side
20 306 of the Si wafer 302, followed by a double-side deposition to form the front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318.

After deposition of the front side second doped semiconductor layer 316 and the rear side second doped semiconductor layer 318 in the step 412, contact formation layers
25 320, 322 are formed in the steps 414 followed by the formation of the rear metal contacts 324 and the front metal contacts 326 in the steps 416 and 418 respectively. These steps 414, 416 and 418 are similar to the ones described above for the method 400 and their descriptions are therefore not repeated here for succinctness.

Figures 5A – 5C, 6A – 6C, 7A – 7C, 8A – 8B, 9A – 9F and 10A – 10B provide
30 experimental results in relation to the tunnel junctions formed in embodiments of the solar cell 100, 300.

Figures 5A, 5B and 5C show schematic structures of three different test samples 500, 510, 520 which have been processed to measure a corresponding tunnelling resistance of the tunnel junction augmented passivated contact formed by the dielectric tunnel layer 108, 308 (e.g. SiO_x) / first doped semiconductor layer 110, 310 (e.g. p^+-poly-Si) / the interlayer dielectric tunnel layer 114, 314 (e.g. SiO_x) / the second doped semiconductor layer 116, 318 (i.e. n^+ poly-Si) stack, (e.g. as shown in Figure 5B), and a corresponding tunnelling resistance of the tunnel junction formed by a highly doped diffused surface of a silicon wafer and a highly oppositely doped poly-Si capping layer (e.g. in the case of Figure 5C). In order to test, if a tunnel junction between a doped poly-Si capping layer and an oppositely doped poly-Si capping layer or if a tunnel junction between a doped poly-Si capping layer and an oppositely diffused silicon wafer surface can be formed, various test samples, as outlined in relation to Figures 5A, 5B and 5C have been processed. These experiments confirm, that indeed, after some diffusion optimization, a tunnel junction can be formed between two oppositely doped poly-Si capping layers as well as between a poly-Si capping layer and an oppositely doped diffused silicon wafer surface.

The quality of the tunnel junctions formed is important for the performance of the solar cell 100, 300. In order to test a quality of the tunnel junctions formed, test samples 500, 510, 520 as shown in Figures 5A, 5B and 5C are fabricated.

Figure 5A shows a symmetric test-structure 500 to measure the effective contact resistance of a conventional hole extracting SiO_x/p^+-poly-Si passivated contact. The test-structure 500 comprises a p-type Si wafer 502, a SiO_x layer 504 deposited on each side of the p-type Si wafer 502, a p^+-poly-Si layer 506 deposited on each of the SiO_x layers 504 and a silver metal layer 508 deposited on each of the p^+-poly-Si layers 506. As shown in Figure 5A, this multi-layer stack (i.e. SiO_x/p^+ poly-Si/Ag) is deposited symmetrically on both sides of the p-type Si wafer 502.

Figure 5B shows a test-structure 510, deploying a conventional hole extracting SiO_x/p^+-poly-Si passivated contact comprising the SiO_x layer 504 and the p^+-poly-Si layer 506 on a front side of the p-type Si wafer 502, and a tunnel junction augmented hole extracting SiO_x/p^+-poly-Si/SiO_x/n^+-poly-Si passivated contact comprising the SiO_x layer 504, the p^+-poly-Si layer 506, a SiO_x interlayer dielectric tunnel layer 512 and an n^+-poly-Si layer 514 on a rear side of the p-type Si wafer 502. By measuring the total series resistance of this

structure 510 and subtracting the series resistance of the wafer 502 as well as the effective contact resistance of a conventional hole extracting SiO_x/p^+-poly-Si passivated contact as measured with the test structure 500, the tunnelling resistance of the p^+-poly-Si/SiO_x/n^+-poly-Si tunnel junction can be determined.

5 Figure 5C shows a test-structure 520 comprising an n-type Si wafer 522 having a front side n^+ diffused region 524 and a rear side n^+ diffused region 526, with a p^+-poly-Si layer 506 deposited on the front side n^+ diffused region 524 and a silver metal layer 508 deposited on both sides of the Si wafer 522. One of the silver metal layers 508 is deposited on the p^+-poly-Si layer 506 at the front side of the n-type Si wafer 522, while 10 the other of the silver metal layers 508 is deposited on the rear side n^+ diffused region 526 at the rear side of the n-type Si wafer 522.

Figures 6A to 6C show measured dark current-voltage (I-V) curves of the structures 500, 510, 520 of Figures 6A, 6B and 6C respectively. The I-V curves 600, 601 as shown in Figures 6A and 6B are used to measure the corresponding tunnelling resistance of the 15 p^+ poly-Si/SiO_x/n^+ poly-Si tunnel junction (i.e. extracted from the total series resistance of the structures 500, 510).

Results in relation to a quality of a tunnel junction formed between two oppositely doped poly-Si capping layers are shown in Figures 6A and 6B. As shown in Figures 6A and 6B, each of the measured dark I-V curves 600, 601 comprises a straight line for each of the 20 structures 500 and 510. This shows that both the structures 500, 510 display an ohmic behaviour in the vicinity of 0 V. The measured dark I-V curves 600, 601 also allows the total series resistance of the structures 500 and 510 to be calculated and thus the associated tunnelling resistance of the tunnel junction in the structure 510 to be extracted. The corresponding tunnelling resistance extracted is in the range of approximately 0.5 25 $Ohm \cdot cm^2$. This range is already well suited for full-area device integration but may be further optimized. Further, since the SiO_x/p^+-poly-Si layers deposited on top of the p-doped Si wafer 502 do form an ohmic contact, upon the addition of the SiO_x layer 512 and the n^+-poly Si layer 514 deposited on the rear side of the p-type Si wafer 502 in the structure 510, the ohmic behaviour is conserved as observed only if the p^+-poly-30 Si/SiO_x/n^+-poly-Si structure formed is indeed a tunnel junction.

Given that the measured dark I-V curves 600, 601 show straight lines in each of Figures 6A and 6B, it is therefore experimentally demonstrated that a tunnel junction p^+-poly-

Si/SiO_x/n^+-poly-Si is formed. Further, as demonstrated in Figure 6B, the tunnelling properties of the tunnel junction p^+-poly-Si/SiO_x/n^+-poly-Si remain (albeit with an increased tunnel resistance R_{series}), even if there is an additional ultra-thin SiO_x tunnel layer sandwiched between the p^+-poly-Si and the n^+-poly-Si layers. Thus it is not
5 necessary to use a p^+-poly-Si/n^+-poly-Si tunnel junction without an interfacial SiO_x interlayer for forming the front side tunnel junction 128 of the solar cell 100. This significantly reduces the required process steps required for forming a passivated contact given that a double-side deposition process can be used. However, this comes at the expense of a slightly increased tunnelling resistance due to the sandwiched SiO_x
10 tunnel layer.

Results in relation to a quality of a tunnel junction formed between a poly-Si capping layer and an oppositely doped diffused silicon wafer surface is shown in Figure 6C. Referring to the structure 520, it is noted that an ohmic contact is always formed between the silver metal layer 508 and the p^+-poly-Si layer 506. Also, it is noted that an ohmic
15 contact is always formed between the silver metal layer 508 and the rear side n^+ diffused region 526. An ohmic behaviour of the measured dark I-V curve for this structure 520 will therefore provide information on the quality of the tunnel junction formed between the p^+-poly-Si layer 506 and the front side n^+ diffused region 524. In the present case, a phosphorous diffused planar surface (providing a highly n^+-doped surface near region
20 within the silicon wafer) has been chosen. Phosphorous diffusion was chosen as it leads to a higher surface concentration of the dopants which facilitates the formation of a tunnel junction when compared to boron diffusion. The curve 602 shows an initial experiment where the diffusion profile of the highly doped n^+ diffusion region has not been optimized. In this case, no straight line is observed and therefore a tunnel junction is not formed.
25 The curve 604 shows a result after diffusion profile optimization. The curve 604 comprises a straight line, thereby demonstrating an ohmic behaviour of the tunnel junction formed between the p^+-poly-Si layer 506 and the front side n^+ diffused region 524. Though not shown in Figure 6C, it is also demonstrated that an n^+-diffused/SiO_x/p^+-poly-Si tunnel junction which exhibits ohmic behaviour can be formed. However, at
30 present, it remains a challenge to deploy a p^+-diffused silicon surface. Further diffusion optimization may be required or ion implantation instead of diffusion may be deployed in order to reach high surface concentrations of the p-type dopants for forming e.g. a p^+-diffused/SiO_x/n^+-poly-Si tunnel junction.

In summary, the results from Figures 6A, 6B and 6C show an ohmic behaviour in the dark IV curves in the vicinity of 0V for the structures 500, 510, 520, thereby demonstrating that a tunnel junction is indeed successfully formed in the structures 500, 510 and 520. The resulting tunnelling resistance is in the range 0.04 – 2 $\Omega\cdot cm^2$ which can be further optimized. Nonetheless, the present range of tunnelling resistances is already well suited for full-area device integration.

Figures 7A, 7B and 7C show schematic structures 700, 710, 720 for use in investigating a minority carrier lifetime for SiO_x/p^+-poly-Si/SiO_x/n^+-poly-Si tunnel junction, where Figure 7A shows a structure 700 comprising a SiO_x/p^+-poly-Si passivated contact and a SiN_x passivation layer deposited on each side of an n-doped Si wafer, Figure 7B shows a structure 710 comprising a SiO_x/p^+ poly-Si passivated contact deposited on each side of a p-doped Si wafer, and Figure 10C shows a structure 720 comprising a SiO_x/p^+-poly-Si/SiO_x/n^+-poly-Si tunnel junction augmented passivated contact 721 (i.e. a passivated contact incorporated with a tunnel junction) deposited on a rear side of a p-doped Si wafer suited for dark I-V tunnelling resistance measurements.

As shown in Figure 7A, the structure 700 comprises an n-type Si wafer 702, a SiO_x layer 704 deposited on the n-type Si wafer 702, a p^+ poly-Si layer 706 deposited on the SiO_x layer 704 and a SiN_x passivation layer 708 deposited on the p^+ poly-Si layer 706. As shown in Figure 7A, this multi-layer stack is deposited symmetrically on both sides of the n-type Si wafer 702. The structure 700 uses the diffusion optimized p^+ poly-Si layer 706 which is used to form a tunnel junction towards an n^+ diffused region 526 as shown in the structure 520 of Fig. 5C. The structure 710 of Figure 7B is similar to the structure 700 except that it does not include the SiN_x layers 708, and that the SiO_x and the p^+ poly-Si layers (i.e. the SiO_x/p^+ poly-Si passivated contacts 711) are formed on a p-type Si wafer 712. The structure 720 of Figure 7C is similar to the structure 710 except that it further comprises a second SiO_x layer 722 deposited on the p^+ poly-Si layer 706, an n^+ poly-Si layer 724 deposited on the second SiO_x layer 722 on a rear side of the p-type Si wafer 712. As shown in Figure 7C, the SiO_x layer 704, the p^+ poly-Si layer 706, the second SiO_x layer 722 and the n^+ poly-Si layer 724 together form the SiO_x/p^+-poly-Si/SiO_x/n^+-poly-Si tunnel junction augmented passivated contact 721 on the rear side of the p-type Si wafer.

Figures 8A and 8B illustrate experimental findings in relation to intensity-dependent minority carrier lifetimes (as a function of the excess minority carrier density within the sample) for the structures 700, 710, 720 of Figures 7A, 7B and 7C, where Figure 8A shows the experimental findings for the structure 700 of Figure 7A, and Figure 8B shows
5 the experimental findings for the structures 710, 720 of Figures 7B and 7C.

As shown in the results of Figures 8A and 8B, by employing SiO_x/poly-Si passivated contacts, it is possible to obtain a high minority carrier lifetime. For example, an implied open-circuit voltages $iV_{oc} \geq 700mV$ can be obtained for a SiO_x/poly-Si passivated contact deposited on an n-type or a p-type crystalline Si wafer. As shown in Figure 8B, this high
10 minority carrier lifetime persists (or even improves!) after including a p^+-poly-Si/SiO_x/n^+-poly-Si tunnel junction (see e.g. the structure 720). It is noted that the structure 720 is a pre-cursor (i.e. before metal contact) of the structure 510 shown in Fig. 5B which is used to measure the tunnelling resistance.

A summary of the minority carrier lifetimes for the different structures 700, 710, 720 of
15 Figures 7A, 7B and 7C respectively is included in Table 1 below.

	Lifetime (μs)	**iV_{oc} (mV)**	**J_0 (fA cm^{-2})**
Structure 1000	2523	725	7
Structure 1010	351	688	46.7
Structure 1020	490	697	35.5

Table 1: Summary of the minority lifetime measurements for the structures of Figures 10A, 10B and 10C.

Figures 9A to 9F are schematic structures used for investigating a passivation quality of thick and ultra-thin SiO_x/poly-Si passivated contacts processed either on a planar or a
20 textured wafer surface.

Figure 9A shows a test structure 900 comprising an n-doped Si wafer 902, a SiO_x layer 904 and a 250nm thick n^+ poly-Si layer 908 deposited on a front side of the n-doped Si wafer 902, and a SiO_x layer 906 and a 250nm thick n^+ poly-Si layer 910 deposited on a rear side of the Si wafer 902. The SiO_x/n^+ poly-Si layer stacks 909, 911 are deposited on
25 the front side and the rear side of the Si wafer 902 respectively using a double-side deposition process e.g. LPCVD.

Figure 9B shows a test structure 912 which is similar to the test structure 900 as described above except that the n^+ poly-Si layers 914, 916 deposited on the front side and the rear side of the n-doped Si wafer 902 respectively are now each 10nm thick. The ultra-thin (10nm thick) n^+ poly-Si layers 914, 916 of the test structure 912 are deposited
5 using a custom tailored phosphorous diffusion recipe with LPCVD.

Figure 9C shows a test structure 918 comprising an n-doped Si wafer 920 with a textured front surface and a textured rear surface. The test structure 920 further comprises a SiO_x layer 922 and a 250nm thick n^+ poly-Si layer 926 deposited on the textured front surface of the n-doped Si wafer 918, and a SiO_x layer 924 and a 250nm thick n^+ poly-Si layer
10 928 deposited on the textured rear surface of the Si wafer 920. Similar to the test structure 900, the SiO_x/n^+ poly-Si layer stacks are deposited on the front side and the rear side of the Si wafer 902 using a double-side deposition process e.g. LPCVD. The difference between the test structure 918 and the test structure 900 is that the front side and the rear side of the test structure 918 are textured, as compared to the planar front
15 side and the planar rear side of the test structure 900.

Figure 9D shows a test structure 930 which is similar to the test structure 918 as described above except that the n^+ poly-Si layers 932, 934 deposited on the textured front side and the textured rear side of the n-doped Si wafer 920 respectively are now each 10nm thick. The ultra-thin (10nm thick) n^+ poly-Si layers 932, 934 of the test
20 structure 930 are deposited using a custom tailored phosphorous diffusion recipe with LPCVD.

Figure 9E shows a test structure 940 which is similar to the test structure 900 as described above except that p^+ poly-Si layers 942, 944 are deposited on the planar front side and the planar rear side of the n-doped Si wafer 902 respectively, in place of the n^+
25 poly-Si layers 908, 910. The SiO_x/p^+ poly-Si layer stacks are deposited on the front side and the rear side of the Si wafer 902 using a double-side deposition process e.g. LPCVD.

Figure 9F shows a test structure 946 which is similar to the test structure 940 as described above except that the p^+ poly-Si layers 948, 950 deposited on the front side and the rear side of the n-doped Si wafer 902 respectively are now each 4nm thick. The
30 ultra-thin (4nm thick) p^+ poly-Si layers 948, 950 of the test structure 946 are formed using an etch-back technology which involves thinning down LPCVD deposited thick standard (e.g. 250nm thick) p^+ poly-Si layers to form the ultra-thin layers.

	Lifetime (μs)	iV_{oc} (mV)	J_0 (fA cm^{-2})
Structure 900	6030	723	5.4
Structure 900 + SiN_x	11307	737	5.0
Structure 912	4229	719	16
Structure 912 + SiN_x	7277	727	10
Structure 918	1756	696	35
Structure 918 + SiN_x	-	-	-
Structure 930	960	686	67
Structure 930 + SiN_x	1928	703	31
Structure 940	1827	698	27
Structure 940 + SiN_x	2123	713	8
Structure 946	1649	689	38
Structure 946 + SiN_x	-	-	-

Table 2: Summary of the minority lifetime measurements for the structures of Figures 9A to 9F in order to measure the passivation quality of both thick and ultra-thin SiO_x/poly-Si tunnel layer passivated contacts processed on a planar or a textured wafer surface.

Table 2 is a summary of the minority lifetime measurements for the structures 900, 912, 918, 930, 940, 946 of Figures 9A to 9F. Besides the structures 900, 912, 918, 930, 940, 946, other similar structures with an additional SiN_x passivation layer deposited on each side of a respective Si wafer have also been tested as shown in the results of Table 2 above. For example "Structure 900 + SiN_x" denotes a structure comprising the structure 900 with an additional SiN_x passivation layer deposited on each side of the structure 900.

As shown by the results of Table 2, the minority lifetime measurements of structures with ultra-thin (≤ 10nm) SiO_x/poly-Si contact passivation layers are similar to those that deploy thicker 250nm doped poly-Si layers. This provides experimental evidence that an excellent passivation quality of the standard 250nm-thick doped poly-Si layer is preserved in these ultra-thin SiO_x/poly-Si contact passivation layers. These layers can therefore be advantageously deployed on a front-side of a solar cell, thereby exhibiting a significantly reduced front parasitic absorption compared to a standard 250nm-thick doped layer while preserving a similar passivation quality.

Table 2 also shows that it is possible to process a high-efficiency ultra-thin (~10nm) electron-extracting SiO_x/n^+-poly-Si passivated contact on a textured surface of a silicon

wafer. This is exemplified by the results shown in relation to the test structures 918 and 930. This means electron-extracting SiO_x/n^+-poly-Si passivated contacts can be applied on a textured silicon wafer surface. These ultra-thin n^+-poly-Si layers can therefore be applied on a front-side of a solar cell which advantageously reduces front-side parasitic absorption as compared to the standard 250nm thick doped poly-Si layer due to their highly reduced thickness. Please note, however, that applying hole-extracting SiO_x/p^+-poly-Si passivated contacts on textured surfaces remain a challenge at present. The passivation quality for hole-extracting SiO_x/p^+-poly-Si passivated contacts is comparatively low on a textured surface, i.e. they work better on planar surfaces.

As shown in Table 2, the minority carrier lifetimes for the test structure 940 is similar to that of the test structure 946, it is therefore shown that it is possible to fabricate a high-efficiency ultra-thin (~4nm) hole-extracting SiO_x/p^+-poly-Si passivated contact on a planar surface of a silicon wafer while preserving the passivation quality of a standard 250nm thick p^+-poly-Si layer. The ultra-thin p^+-poly-Si layer was formed by etch-back technology. However, it is noted that the etch-back technology at present may not be suitable for forming ultrathin n^+ poly-Si layer as the passivation quality of n^+-poly-Si breaks down when an etch-back thickness of the n^+ poly-Si layer reaches less than 75nm. Therefore, on a planar silicon wafer surface, ultra-thin p^+ poly-Si layers can be advantageously deployed on a front-side of a solar cell, thereby exhibiting a significantly reduced front parasitic absorption compared to a standard 250nm thick doped layer while preserving a similar passivation quality. This is especially well suited for a silicon bottom cell designed for tandem cell device integration.

Besides the LPCVD deposited structures and their minority carrier lifetime measurements as shown in Figures 9A to 9F and Table 2 respectively, plasma enhanced chemical vapour deposition (PECVD) has also been developed for forming contact passivation layers. PECVD is a single-side deposition method as compared to the double-side LPCVD deposition. Using PECVD has the advantage of simplifying the fabrication process and device integration process significantly since no masking / etch-off / mask-removal processes are required. Further, it is possible to process ultra-thin ($\leq$ 10 nm) poly-Si/SiO_x contact passivation layers using PECVD which preserve the excellent passivation quality of “moderately thick” (50 nm) standard layers. This can be achieved without using an etch-back technology, or a need to re-optimize a diffusion recipe which are techniques used in the case of LPCVD deposition. In general, the

thinner the contact passivation layers, the less parasitic absorption these layers will exhibit if deployed on a front-side of a solar cell and therefore result in a higher short-circuit current density for the solar cell.

	Thickness [nm]	Lifetime (μs)	J_0 (fA cm^{-2})	iV_{oc} (mV)
IC-PECVD – n (planar)	6	5900	3.8	741
IC-PECVD – n (textured)	≤ 8	1332	17.5	702
IC-PECVD – p (planar)	10	2190	4.5	724
IC-PECVD – p (textured)	≤ 12	338	44.5	669
LPCVD – n (planar)	10	4229	8	719
LPCVD – n (textured)	≤ 12	961	33.5	686
LPCVD – p	No ultra-thin passivation layers using diffusion re-optimization at present			

Table 3: Summary of the minority lifetime measurements for ultrathin passivation layer stacks
5 (SiO_x/n^+ poly-Si and SiO_x/p^+ poly-Si) deposited using IC-PECVD or LPCVD on either a planar or a textured wafer surface.

Table 3 provides a summary of the minority lifetime measurements for ultrathin passivation layer stacks (SiO_x/n^+ poly-Si and SiO_x/p^+ poly-Si) deposited using IC-PECVD or LPCVD on either a planar or a textured wafer surface. The thickness column shows
10 the measured thickness of the corresponding “n” (i.e. SiO_x/n^+ poly-Si) or “p” (i.e. SiO_x/p^+ poly-Si) passivation layer stack. From Table 3, it is shown that high-efficiency ultra-thin electron-extracting n^+ poly-Si/SiO_x passivated contacts can be formed using IC-PECVD (inductive coupled PECVD) on both planar and textured silicon wafer surfaces. Ultra-thin high-efficiency p^+ poly-Si/SiO_x passivated contacts can also be formed by IC-PECVD on
15 a planar silicon wafer surface. The ultra-thin doped poly-Si layers can be formed using IC-PECVD by first depositing ultra-thin doped amorphous silicon layers and then sintering them towards doped poly-Si layers. The passivation properties of the resulting IC-PECVD SiO_x/poly-Si passivated contacts (in terms of effective lifetime τ_{eff}, recombination current density J_0, and implied open-circuit voltage iV_{oc}) are comparable

(or even better) than similar passivated contacts formed using LPCVD layers by diffusion re-optimization.

Figures 10A and 10B show refractive indices *k* for IC-PECVD processed poly-Si and LPCVD processed poly-Si, where Figure 10A shows the refractive indices *k* for IC-PECVD n^+ poly-Si as compared to LPCVD n^+ poly-Si. Figure 10B shows refractive indices *k* for IC-PECVD processed n-doped poly-Si and p-doped poly-Si. All data represented here were measured by spectroscopic ellipsometry.

In particular, the curve 1002 is associated with the *k* values for IC-PECVD n^+ poly-Si and the curve 1004 is associated with the *k* values for LPCVD n^+ poly-Si.

As shown in Figure 10A, the n^+ doped PECVD poly-Si layer has significantly lower *k* values (resulting in less parasitic absorption) than its LPCVD counterpart, especially in the wavelength range of 350 – 600 nm. In other words, PECVD deposited poly-Si layers will have less parasitic absorption for the same layer thickness applied on a front-side of a solar cell, as compared to LPCVD formed poly-Si layers. Therefore, the short-circuit current densities J_{sc} of solar cells comprising a front-side PECVD SiO_x/poly-Si tunnel layer passivated contact are expected to be higher compared to solar cells deploying a front-side LPCVD SiO_x/poly-Si tunnel layer passivated contact. Generally, as shown in Figure 10B, the *k* values for n-doped layers (exemplified by the curve 1010) are observed to be lower than the *k* values for p-doped layers (exemplified by the curve 1012) for a similar/same deposition technology. As a result, rear-emitter cells (exhibiting front-side n-doped layers if an n-type wafer is used) are expected to have less parasitic absorption as compared to front-emitter cells (exhibiting front-side p-doped layers if an n-type wafer is used) for a same deposition technology. The ability of ultra-thin PECVD poly-Si layers to form a p^+/n^+ or n^+/p^+ tunnel junction is expected but has yet to be experimentally realised. From the *k* values, we would expect that PECVD deposited ultra-thin SiO_x/p-poly-Si/n-poly-Si or SiO_x/n-poly-Si/p-poly-Si tunnel junction augmented passivated contacts to exhibit less parasitic absorption than their LPCVD counterparts when deployed on a front side of the solar cell. Nonetheless, even if LPCVD is used for depositing the poly-Si layers of the aforementioned solar cell 100, the ultra-thin tunnel junction 128 deployed on the front side of the solar cell 100 is still valuable for integrating a top solar cell in a tandem solar cell structure.

Figures 11A to 11C and Figures 12A to 12F show different embodiments of the solar cell 100 and 300 respectively. As discussed above, there are generally two embodiments. The first as exemplified by the solar cell 100 is for providing a silicon bottom cell for thin-film on silicon tandem integration, typically deploying a planar front-side and a textured rear-side n-doped silicon wafer. The second as exemplified by the solar cell 300 is for providing a high-efficiency, single-junction, double side contact passivated silicon solar cell which typically deploys a textured front-side and a planar rear-side n-doped silicon wafer. In either case, one type of carrier selective passivated contact (either SiO_x/n^+ poly-Si or SiO_x/p^+ poly-Si) is deposited on both sides of the solar cell 100, 300 (e.g. by using a double-side deposition method such as LPCVD) with one side of the Si wafer forming the aforementioned passivated contact and the other side of the Si wafer forming a tunnel junction augmented passivated contact by combining the carrier selective passivated contact with a diffused, highly-doped p^+/n^+ or n^+/p^+ tunnel junction. As shown in the experimental data of Table 2, it is noted that in case of using p^+-poly-Si to form an emitter for the solar cell, the p^+-poly-Si layer should be deposited on a planar surface. For example, the solar cell 100 deploys the first doped semiconductor layer (i.e. a p^+ poly-Si layer) on a planar front side of the solar cell.

Figures 11A to 11C show schematic structures of solar cells for tandem integration in accordance with further embodiments, where Figure 11A shows a solar cell 1100 comprising a p-doped diffused rear-emitter region, Figure 11B shows a solar cell 1110 comprising a front side p-doped diffused front-emitter region and Figure 11C shows a solar cell 1120 comprising a front side n-doped diffused region.

As shown in Figure 11A, the solar cell 1100 comprises a p-doped diffused rear-emitter region. Compared to the solar cell 100 of Figure 1, the solar cell 1100 comprises a first doped semiconductor layer formed by a p-doped diffused region 1102 at a rear side of the Si wafer 102. Given that the p-doped diffused region 1102 is formed in the Si wafer 102, there is no surface dielectric tunnel layer 108 formed between the p-doped region and the rear side surface of the Si wafer 102. Passivated contacts 1104, 1106, each comprising a SiO_x/n^+ poly-Si layer stack, are deposited on both sides of the Si wafer 102. As shown in Figure 11A, the front side passivated contact 1104 comprises the dielectric tunnel layer 112 (e.g. SiO_x) deposited on a surface of the front side of the Si wafer 102 and the front side second doped semiconductor layer 116 (e.g. n^+ poly-Si), while the rear side passivated contact 1106 comprises the interlayer dielectric tunnel layer 114 (e.g.

SiO_x) deposited on the p-doped diffused region 1102 and the rear side second doped semiconductor layer 118 (e.g. n^+ poly-Si) deposited on the interlayer dielectric tunnel layer 114 at the rear side of the Si wafer 102. Similar to the solar cell 100, the solar cell 1100 comprises a contact formation layer 120 deposited on the rear side second doped semiconductor layer 118. The solar cell 1100 further comprises a rear metal contact 122 deposited on the contact formation layer 120. In an embodiment where the contact formation layer 120 comprises a SiN_x layer, the rear metal contact 122 is formed by first using local laser ablation to form contact openings in the contact formation layer 120 and then depositing a full-area rear metal contact 122 on the rear-side 106 by conventional non-fire-through screen printing or by sputtering or by evaporation. In this embodiment, similar to the solar cell 100, the deposited rear-side SiO_x/n^+-poly-Si layers do not act to selectively extract excess carriers (i.e. electrons, like at the front-side) but are rather forming a tunnel junction, thereby effectively extracting the rear-side collected holes and converting the hole current into electron current. By using conventional diffusion to extract one excess carrier type (electrons or holes), only one type of carrier selective contact (either hole extracting, i.e. SiO_x/p^+ poly-Si or electron extracting, i.e. SiO_x/n^+ poly-Si) has to be deposited. This significantly reduces the number of processing steps for fabricating the solar cell 1100.

Figure 11B shows a solar cell 1110 comprising a front side p-doped diffused region 1112. The solar cell 1110 is similar to the solar cell 1100 as aforementioned described, except that the first doped semiconductor layer, which is formed by a p-doped diffused region 1112, is now at the front side of the Si wafer 102. Since the p-doped diffused region 1112 is at the front side of the Si wafer 112, the tunnel junction comprising the p-doped diffused region 1112, the interlayer dielectric tunnel layer 1116 and the front side second doped semiconductor layer 116 (e.g. n^+ poly-Si) is formed on the front side of the Si wafer 112, whereas the passivated contact comprising the dielectric tunnel layer 1114 and the rear side second doped semiconductor layer 118 is formed at the rear side of the Si wafer 112. In this embodiment, a thin-film solar cell can be directly deposited on top of the front-side n^+-poly-Si layer 116, since a tunnel junction, which is needed for two terminal tandem device integration, is already integrated in the solar cell 1110 which can form the bottom cell of the tandem device. The front side p-doped diffused region may be formed by a moderately deep (~150nm) p^+-surface-layer within the silicon wafer.

Figure 11C shows a solar cell 1120 comprising a front side n-doped diffused region 1122. The solar cell 1120 is similar to the solar cell 1110 of Figure 11B except that (i) the polarity of the diffusion layer (i.e. the first doped semiconductor layer) is n-type instead of p-type, (ii) the front side second doped semiconductor layer 1124 and the rear side
5 second doped semiconductor layer 1126 comprises p^+ poly-Si instead of n^+ poly-Si, and (iii) a single-side rear atomic layer deposited (ALD) AlO_x has been deployed as the dielectric tunnel layer 1114 instead of a SiO_x formed by double-side deposition. Therefore, in the present embodiment, there is no interlayer dielectric tunnel layer sandwiched between the n-doped diffusion region 1122 and the front side second doped
10 semiconductor layer 1124. In this embodiment, the tunnel junction formed on the front side of the solar cell 1120 comprises the first doped semiconductor layer 1122 (i.e. the n-doped diffusion region) and the front side second doped semiconductor layer 1124, but without the interlayer dielectric tunnel layer. In an embodiment (not shown), the n-doped diffusion region is formed on the rear side of the solar cell. In this case, the tunnel
15 junction comprising the rear side n-doped diffusion region and the rear side second doped semiconductor (e.g. p^+ poly-Si) is formed on the rear side of the solar cell while the passivated contact AlO_x/p^+ poly-Si is formed on the front side of the solar cell.

Figures 12A to 12F show schematic structures of solar cells 1200, 1210, 1220, 1230, 1240, 1250 in accordance with further embodiments, where Figure 12A shows a solar
20 cell 1200 comprising a p-doped diffused rear-emitter region, Figure 12B shows a solar cell 1210 comprising a p-doped diffused rear-emitter region with a textured rear side surface, Figure 12C shows a solar cell 1220 comprising a different rear-side metal contact scheme as compared to the solar cell 300 of Figure 3, Figure 12D shows a solar cell 1230 comprising a full rear-side metal layer for forming the rear metal contacts as
25 compared to the solar cell 300 of Figure 3, Figure 12E shows a solar cell 1240 comprising transparent conducting oxide (TCO) on both the front side and the rear side of the solar cell, and Figure 12F shows a solar cell 1250 comprising TCO on a front side of the solar cell.

As shown in Figure 12A, the solar cell 1200 comprises a p-doped diffused rear-emitter
30 region 1202. Compared to the solar cell 300 of Figure 3, the solar cell 1200 comprises a p-doped region 1202 on the rear side of the Si wafer 302 instead of a p^+ poly-Si layer 310 of the solar cell 300. Given that the p-doped diffused region 1202 is formed at the rear side of the Si wafer 302 in the solar cell 1200, there is no surface dielectric tunnel

layer formed between the p-doped diffused region 1202 and the rear side surface of the Si wafer 302. In some embodiments (not shown), as described in the methods 400, 420 above, the contact formation layers 320, 322 of the solar cell 1200 comprise TCO layers. In this case, as previously described, the metal contacts 324, 326 can be formed by low 5 temperature non-fire through screen printing.

As shown in Figure 12B, the solar cell 1210 comprises the p-doped diffused rear-emitter region 1202 with a textured rear side surface. Compared to the solar cell 1200 of Figure 12A the solar cell 1210 comprises an n-type Si wafer 302 with a textured rear side surface instead of a planar rear side surface. In some embodiments (not shown), similar 10 to the solar cell 1200, the contact formation layers 320, 322 of the solar cell 1210 comprise TCO layers. In this case, as previously described, the metal contacts 324, 326 can be formed by low temperature non-fire through screen printing.

As shown in Figure 12C, the solar cell 1220 comprises an alternative scheme for forming the rear side metal contact 1222. As shown in Figure 12C, the solar cell 1220 differs from 15 the solar cell 300 in that the rear-side metal contact scheme has been changed. In the present embodiment, the rear-side metal contact 1222 comprises metal fingers 1224 which are in contact with the rear side second doped semiconductor layer 318 through the contact formation layer 320, and a full area metal deposited on the rear side of the Si wafer 302. In the present embodiment where the contact formation layer 320 20 comprises a SiN_x layer, local laser ablation can be used to form the contact openings (i.e. the areas where the metal fingers 1224 are formed) prior to depositing the rear-side metal contact 1222. The full-area rear-side metal contact 1222 may be deposited by thermal evaporation, sputtering or screen printing. In some embodiments (not shown), the front side contact formation layer 322 of the solar cell 1220 comprises a TCO layer. 25 In this case, as previously described, the metal contacts 326 can be formed by low temperature non-fire through screen printing.

As shown in Figure 12D, the solar cell 1230 comprises an alternative scheme for forming the rear side metal contact 1232. As shown in Figure 12D, the solar cell 1230 differs from the solar cells 300 and 1220 in that the rear-side metal contact scheme has been 30 changed. In the present embodiment, the rear-side metal contact 1232 comprises a full area metal layer deposited on the rear side second doped semiconductor layer 318. In this embodiment, no rear side contact formation layer 320 is deposited on the rear side

second doped semiconductor layer 318 so that the entire rear-side metal contact 1232 is in full contact with the rear side second doped semiconductor layer 318. The rear-side metal contact 1232 can be deposited by conventional non-fire-through screen printing or by sputtering or by evaporation. In some embodiments (not shown), the front side contact formation layer 322 of the solar cell 1230 comprises a TCO layer. In this case, as previously described, the metal contacts 326 can be formed by low temperature non-fire through screen printing.

As shown in Figure 12E, the solar cell 1240 comprises an alternative scheme for forming the contact formation layers 1242, 1244 and the metal contacts 1246, 1248. The solar cell 1240 differs from the solar cell 300 in that the contact formation layers 1242, 1244 and the metal contacts 1246, 1248 have been changed. In the present embodiment, the front contact formation layer 1242 and the rear contact formation layer 1244 each comprises a TCO layer. In this case, each of the front metal contacts 1246 and the rear metal contacts 1248 are formed by low temperature non-fire through screen printing.

As shown in Figure 12F, the solar cell 1250 comprises an alternative scheme for forming the contact formation layer and the metal contacts. The solar cell 1250 is similar to the solar cell 1240 except for the rear contact formation layer 1252 and the rear metal contact 1254. The solar cell 1250 presents a hybrid contacting scheme, where the rear contact formation layer 1252 comprises a SiN_x layer and the rear metal contacts 1254 are formed by high temperature screen printing using a fire-through paste, while the front contact formation layer 1242 comprises a TCO layer and the front metal contacts 1246 are formed by low temperature non-fire through screen printing. In an alternative embodiment (not shown), the contacting schemes for the front side and the rear side of the solar cell 1250 can be swapped such that the rear contact formation layer 1252 comprises a TCO layer and the rear metal contacts 1254 are formed by low temperature non-fire through screen printing, , while the front contact formation layer 1242 comprises a SiN_x layer and the front metal contacts 1246 are formed by high temperature screen printing using a fire-through paste or by inline plating.

As discussed above, the solar cell 100 of the present embodiments may be deployed as a bottom cell for two-terminal tandem solar cell integration.

Figure 13 shows a schematic of a tandem solar cell 1300 comprising a thin-film top solar cell 1302 and a silicon wafer based bottom solar cell 1304 where the bottom solar cell

has a similar structure to the solar cell 100 of Figure 1 in accordance with an embodiment. Since the bottom solar cell 1304 employs a similar structure as the solar cell 100, descriptions of similar components as the solar cell 100 are not repeated here for the bottom solar cell 1304. In the present embodiment, the planar front-side of the n-type Si
5 wafer 102 advantageously simplifies formation of the top solar cell 1302 (for example, a thin film top solar cell 1306) by already providing the tunnel junction in the bottom solar cell 1304. Examples of tandem solar cell are perovskite-on-Si tandem cells or GaAs-on-Si tandem cells.

In order to form the tandem solar cell 1300, once the bottom Si solar cell 1304 has been
10 fabricated, several coupling layers 1308 may be deposited on the front-side of the bottom Si solar cell 1304. It is noted that in the present case, less coupling layers 1308 (compared to conventional tandem solar cell structures) may be required because a tunnel junction has already been formed in the bottom Si solar cell 1304. The thin film top solar cell 1306 (e.g. a thin-film perovskite solar cell, consisting of an hole transport
15 layer, a perovskite absorber layer and an electron transport layer) for forming the device integrated top solar cell 1302 is then deposited on top of the coupling layers 1308 using a process that does not damage the underlying coupling layer 1308 and the bottom Si solar cell 1304. A top transparent electrode 1310 (e.g. a transparent conductive oxide (TCO) is then deposited on the thin film top solar cell 1306. The top transparent electrode
20 1310 has a low sheet resistance and a high transparency. Metal gridlines 1312 are then deposited on the top transparent electrode 1310 to minimise series resistance through the top transparent electrode 1310. Further, although SiO_x which has a moderate positive charge density has been used as the tunnel layer in the previously described embodiment, in a variation, the surface dielectric tunnel layer 108, the dielectric tunnel
25 layer 112 and/or the interlayer dielectric tunnel layer 114 can be formed by atomic layer deposited AlO_x or TiO_x (exhibiting a high negative interface charge, i.e. suitable for selective hole extraction) or by PECVD deposited or atomic layer deposited SiN_x (exhibiting a high positive interface charge, i.e. suitable for selective electron extraction).

Alternative embodiments of the invention include: (1) the use of a double-side planar
30 wafer, (2) the use of additional multi-layered front-side anti-reflection and rear-side internal back reflection layers in order to enhance the light trapping within the planar silicon wafer, (3) the use of a double-side textured wafer, see e.g. Figure 12B, (4) the deployment of different rear-side metallisation schemes, e.g. as shown in Fig. 12C and

Figure 12D, (5) the use of the opposite polarities regarding the doped layers, for example as shown in Figure 11C, (6) the use of a single-side atomic layer deposited ALD-AlO_x tunnel layer (substituting the SiO_x tunnel layer in case of hole-extraction), for example as shown in Figure 11C, (7) the use of a front-side diffused or ion-implanted emitter, instead of a rear-side one, for example as shown in Figure 11B, (8) the use of a p-doped Si wafer instead of a n-doped Si wafer, and (9) the use of a multi-crystalline Si wafer instead of a monocrystalline Si wafer.

As shown in the methods 200, 220, 400 and 420, it may be feasible to deploy single-side deposited PECVD layers to form the passivated contacts (i.e. SiO_x/n^+ poly-Si and SiO_x/p^+ poly-Si). The formation of the tunnel junction augmented passivated contact (i.e. the tunnel junction/passivated contact stack) may be further optimized to reduce its tunnelling resistance, for example by optimizing the doping profile within the contact passivation layers and/or by removing the SiO_x dielectric tunnel layer which is sandwiched in between the two doped semiconductor layers. Alternatively, an ultra-thin conductive (TCO) interlayer could be deposited in between the two poly-Si layers, in order to further improve the tunnel junction properties

Although only certain embodiments of the present invention have been described in detail, many variations are possible in accordance with the appended claims. For example, features described in relation to one embodiment may be incorporated into one or more other embodiments and vice versa. For example, it will be appreciated that the use of PECVD or LPCVD to form different layers (such as the surface dielectric tunnel layer 108, the first doped semiconductor layer 110, dielectric tunnel layer 112, the interlayer dielectric tunnel layer 114, the front side second doped semiconductor layer 116 and the rear side second doped semiconductor layer 118) can be performed in a mix and match manner.

Claims

1. A solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side and a first doped semiconductor layer formed on either the front side or the rear side of the silicon wafer, the solar cell comprising:

5 a dielectric tunnel layer deposited on one side of the silicon wafer opposites to the side at which the first doped semiconductor layer is formed;

a front side second doped semiconductor layer deposited on the front side of the silicon wafer; and

a rear side second doped semiconductor layer deposited on the rear side of the 10 silicon wafer, the front side and the rear side second doped semiconductor layers each having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the first doped semiconductor layer cooperates with either the front side second doped semiconductor layer or the rear side second doped semiconductor layer to form a tunnel junction, and the dielectric tunnel layer cooperates with either the rear 15 side second doped semiconductor layer or the front side second doped semiconductor layer to form a passivated contact.

2. The solar cell of claim 1, wherein the front side second doped semiconductor layer and the rear side second doped semiconductor layer are deposited using low pressure chemical vapor deposition (LPCVD) in a single deposition process.

20 3. The solar cell of claim 1 or claim 2, further comprising an interlayer dielectric tunnel layer deposited on the first doped semiconductor layer, wherein the interlayer dielectric tunnel layer is sandwiched between the first doped semiconductor layer and the front side second doped semiconductor layer or the rear side second doped semiconductor layer to form the tunnel junction.

25 4. The solar cell of claim 3, wherein the interlayer dielectric tunnel layer and the dielectric tunnel layer are deposited using LPCVD in a single deposition process.

5. The solar cell of any one of claims 1 to 4, wherein the first doped semiconductor layer is deposited using plasma enhanced chemical vapor deposition (PECVD) or low pressure chemical vapor deposition (LPCVD).

30 6. The solar cell of claim 5, further comprising a surface dielectric tunnel layer deposited on a surface of the silicon wafer, the surface dielectric tunnel layer being sandwiched

between the surface of the silicon wafer and the first doped semiconductor layer, wherein the surface dielectric tunnel layer and the first doped semiconductor layer form another passivated contact.

7. The solar cell of claim 5 or claim 6, wherein the first doped semiconductor layer
5 comprises a p-doped polysilicon layer, and the front side second-doped semiconductor layer and the rear side second doped semiconductor layer each comprises an n-doped polysilicon layer.

8. The solar cell of any one of claims 1 to 4, wherein the first doped semiconductor layer is formed by diffusing or implanting ions in the silicon wafer.

10 9. The solar cell of any one of claims 1 to 8, further comprising a contact formation layer deposited on at least one of the front side second doped semiconductor layer and the rear side second doped semiconductor layer.

10. The solar cell of any one of claims 1 to 9, further comprising a rear metal contact formed on the rear side of the silicon wafer, the rear metal contact being in electrical
15 contact with the rear side second doped semiconductor layer.

11. The solar cell of claim 10, wherein the rear metal contact is formed using screen printing or inline plating or evaporation.

12. The solar cell of any one of claims 1 to 11, further comprising a front metal contact formed on the front side of the silicon wafer, the front metal contact being in electrical
20 contact with the front side second doped semiconductor layer.

13. The solar cell of claim 12, wherein the front metal contact is formed using screen printing or inline plating or evaporation.

14. The solar cell of any one of claims 1 to 13, wherein the front side of the silicon wafer is textured.

25 15. The solar cell of any one of claims 1 to 14, wherein the rear side of the silicon wafer is textured.

16. A method of fabricating a solar cell, the solar cell comprising a silicon wafer having a front side arranged to receive incident light and a rear side and a first doped

semiconductor layer formed on either the front side or the rear side of the silicon wafer, the method comprising:

(i) depositing a dielectric tunnel layer on one side of the silicon wafer opposites to the side at which the first doped semiconductor layer is formed; and

5 (ii) depositing a front side second doped semiconductor layer on the front side of the silicon wafer and a rear side second doped semiconductor layer on the rear side of the silicon wafer, the front side and the rear side second doped semiconductor layers each having a doping of an opposite polarity to the first doped semiconductor layer,

wherein the first doped semiconductor layer cooperates with either the front side 10 second doped semiconductor layer or the rear side second doped semiconductor layer to form a tunnel junction, and the dielectric tunnel layer cooperates with either the rear side second doped semiconductor layer or the front side second doped semiconductor layer to form a passivated contact.

17. The method of claim 16, wherein depositing the front side second doped 15 semiconductor layer and the rear side second doped semiconductor layer comprises depositing the front side second doped semiconductor layer and the rear side second doped semiconductor layer using low pressure chemical vapor deposition (LPCVD) in a single deposition process.

18. The method of claim 16 or 17, further comprising depositing an interlayer dielectric 20 tunnel layer on the first doped semiconductor layer.

19. The method of claim 18, wherein the interlayer dielectric tunnel layer and the dielectric tunnel layer are deposited using LPCVD in a single deposition process.

20. The method of any one of claims 16 to 19, wherein the first doped semiconductor layer is formed using plasma enhanced chemical vapor deposition (PECVD) or low 25 pressure chemical vapor deposition (LPCVD).

21. The method of claim 20, further comprising depositing a surface dielectric tunnel layer on a surface of the silicon wafer prior to the formation of the first doped semiconductor layer, the surface dielectric tunnel layer being sandwiched between the surface of the silicon wafer and the first doped semiconductor layer, wherein the surface 30 dielectric tunnel layer and the first doped semiconductor layer form another passivated contact.

22. The method of claim 20 or claim 21, wherein the first doped semiconductor layer comprises a p-doped polysilicon layer and (ii) depositing the front side second doped semiconductor layer and the rear side second doped semiconductor layer comprises depositing an n-doped polysilicon layer on each of the front side and the rear side of the
5 silicon wafer.

23. The method of any one of claims 16 to 19, wherein the first doped semiconductor layer is formed by diffusing or implanting ions in the silicon wafer.

24. The method of any one of claims 16 to 23, further comprising depositing a contact formation layer on at least one of the front side second doped semiconductor layer and
10 the rear side second doped semiconductor layer.

25. The method of any one of claims 16 to 24, further comprising forming a rear metal contact on the rear side of the silicon wafer, the rear metal contact being in electrical contact with the rear side second doped semiconductor layer.

26. The method of claim 25, wherein forming the rear metal contact comprises forming
15 the rear metal contact using screen printing or inline plating or evaporation.

27. The method of any one of claims 16 to 26, further comprising forming a front metal contact on the front side of the silicon wafer, the front metal contact being in electrical contact with the front side second doped semiconductor layer.

28. The method of claim 27, wherein forming the front metal contact comprises forming
20 the front metal contact using screen printing or inline plating or evaporation.

29. The method of any one of claims 16 to 28, wherein the front side of the silicon wafer is textured.

30. The method of any one of claims 16 to 29, wherein the rear side of the silicon wafer is textured.

25 31. A tandem solar cell comprising:

a top solar cell; and

a bottom solar cell, wherein the bottom solar cell comprises a silicon wafer having a front side arranged to receive incident light and a rear side and a first doped

semiconductor layer formed on either the front side or the rear side of the silicon wafer, the bottom solar cell comprising:

a dielectric tunnel layer deposited on one side of the silicon wafer opposites to the side at which the first doped semiconductor layer is formed;

5 a front side second doped semiconductor layer deposited on the front side of the silicon wafer; and

a rear side second doped semiconductor layer deposited on the rear side of the silicon wafer, the front side and the rear side second doped semiconductor layers each having a doping of an opposite polarity to the first doped semiconductor layer,

10 wherein the first doped semiconductor layer cooperates with either the front side second doped semiconductor layer or the rear side second doped semiconductor layer to form a tunnel junction, and the dielectric tunnel layer cooperates with either the rear side second doped semiconductor layer or the front side second doped semiconductor layer to form a passivated contact.

15 32. The tandem solar cell of claim 31, wherein the top solar cell and the bottom solar cell are integrated to form a tandem solar cell structure.

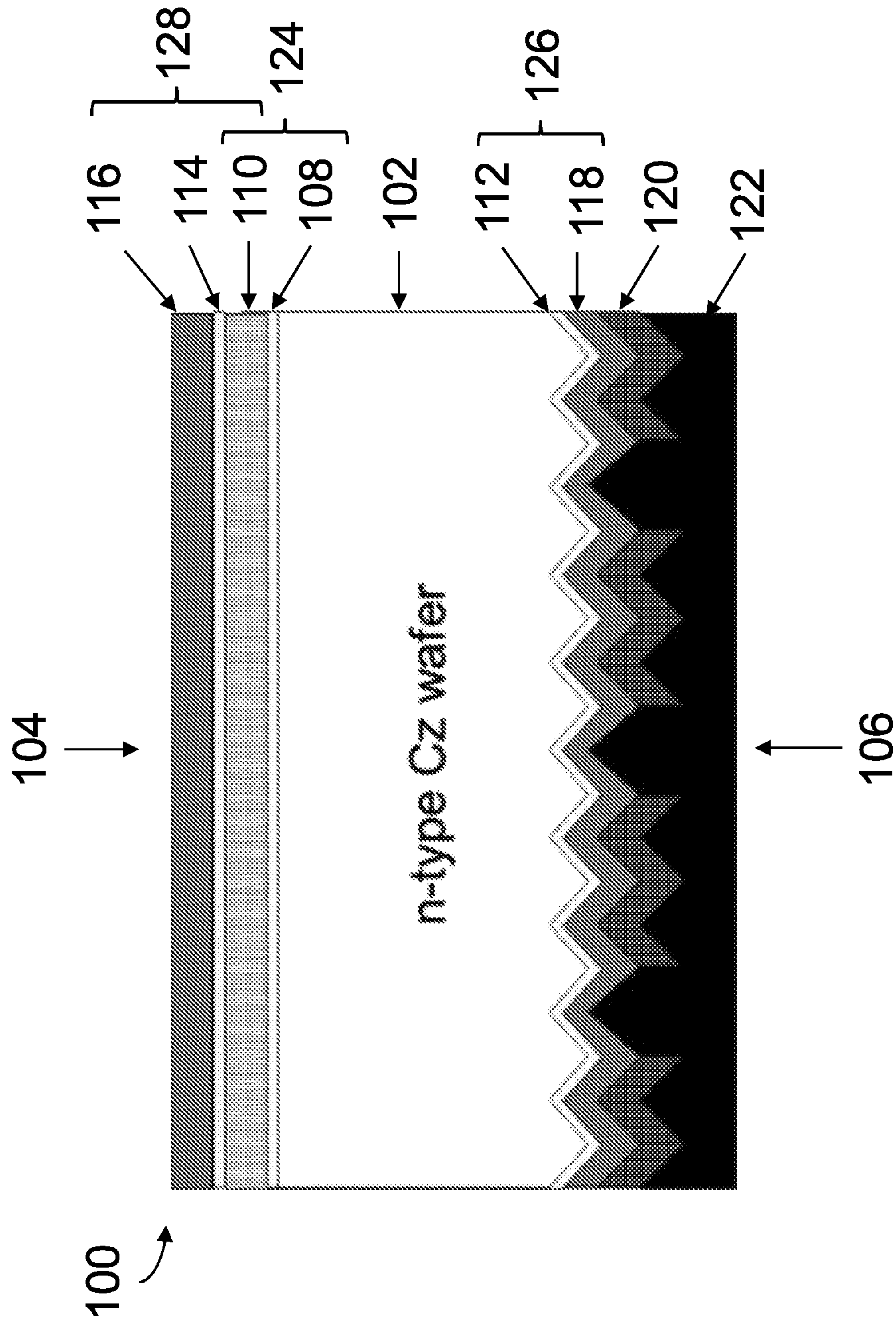


Figure 1

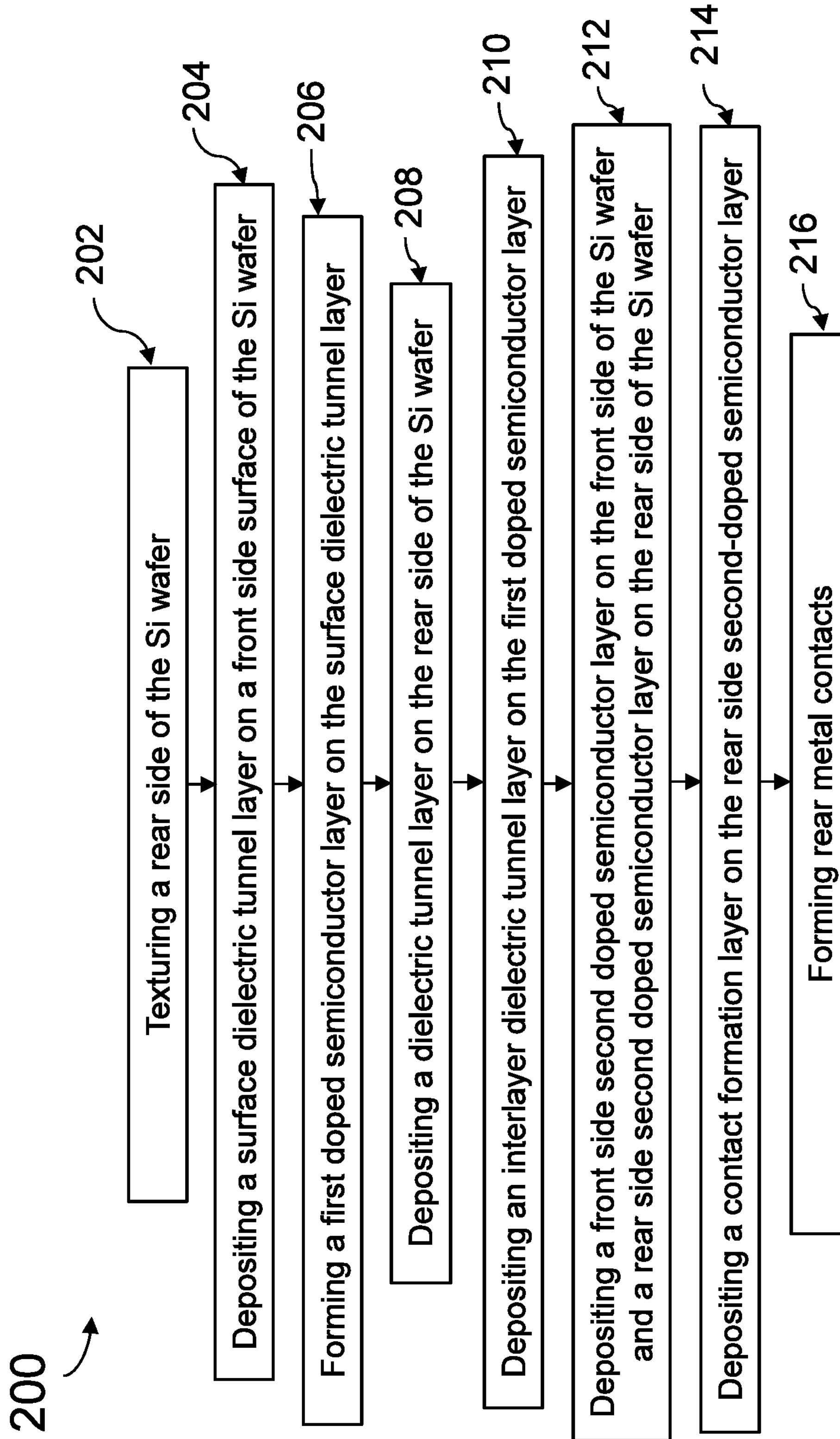


Figure 2A

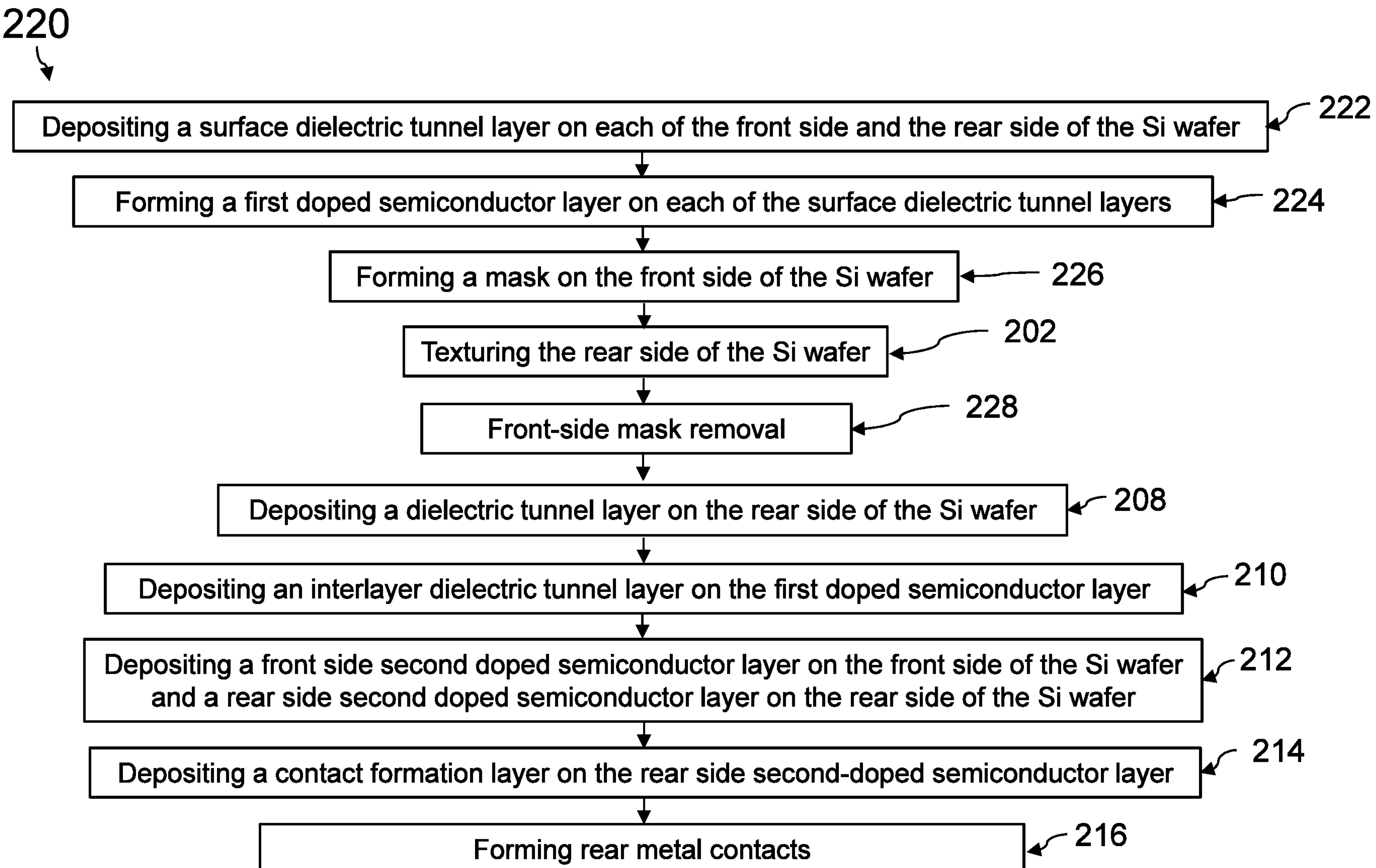


Figure 2B

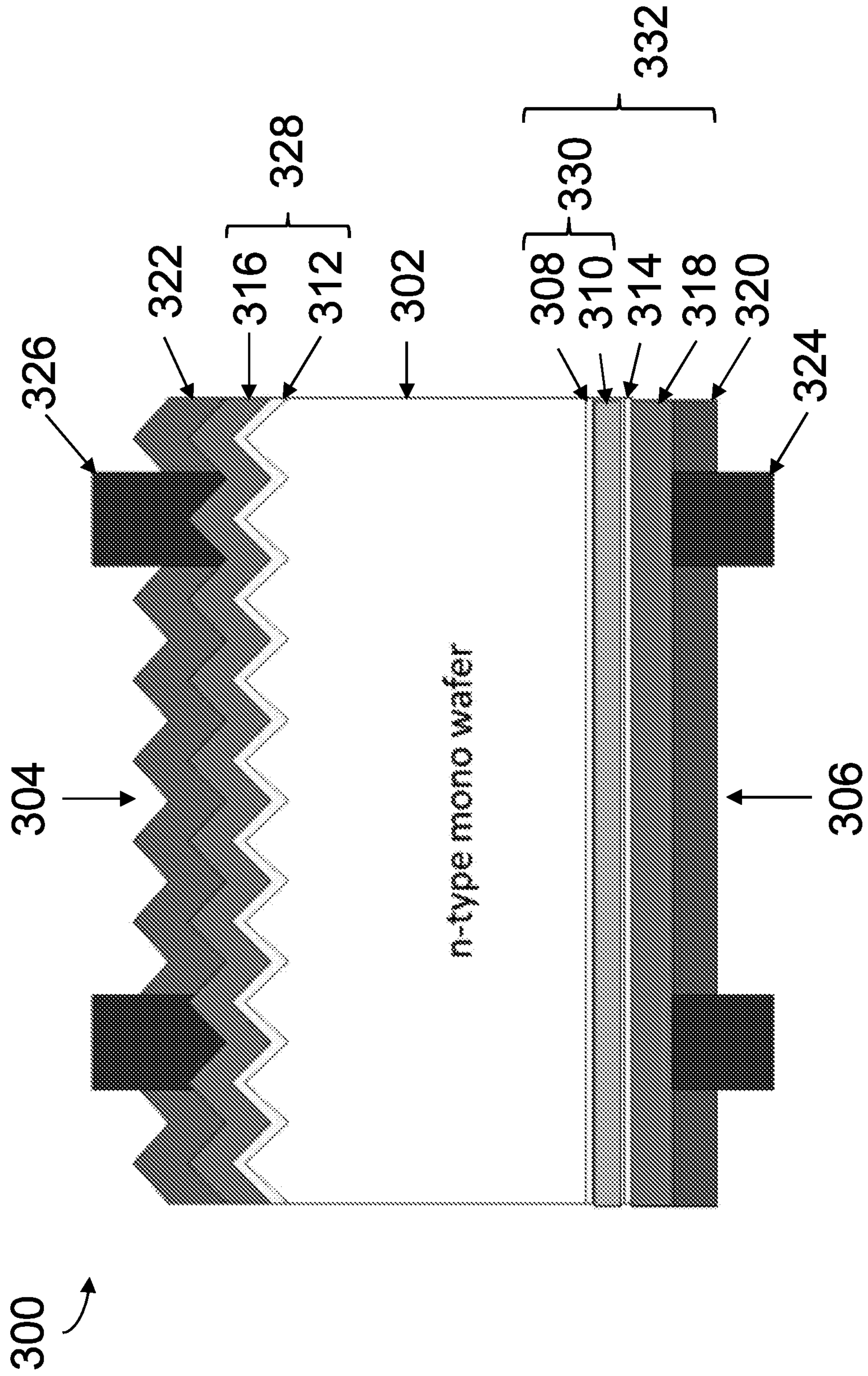


Figure 3

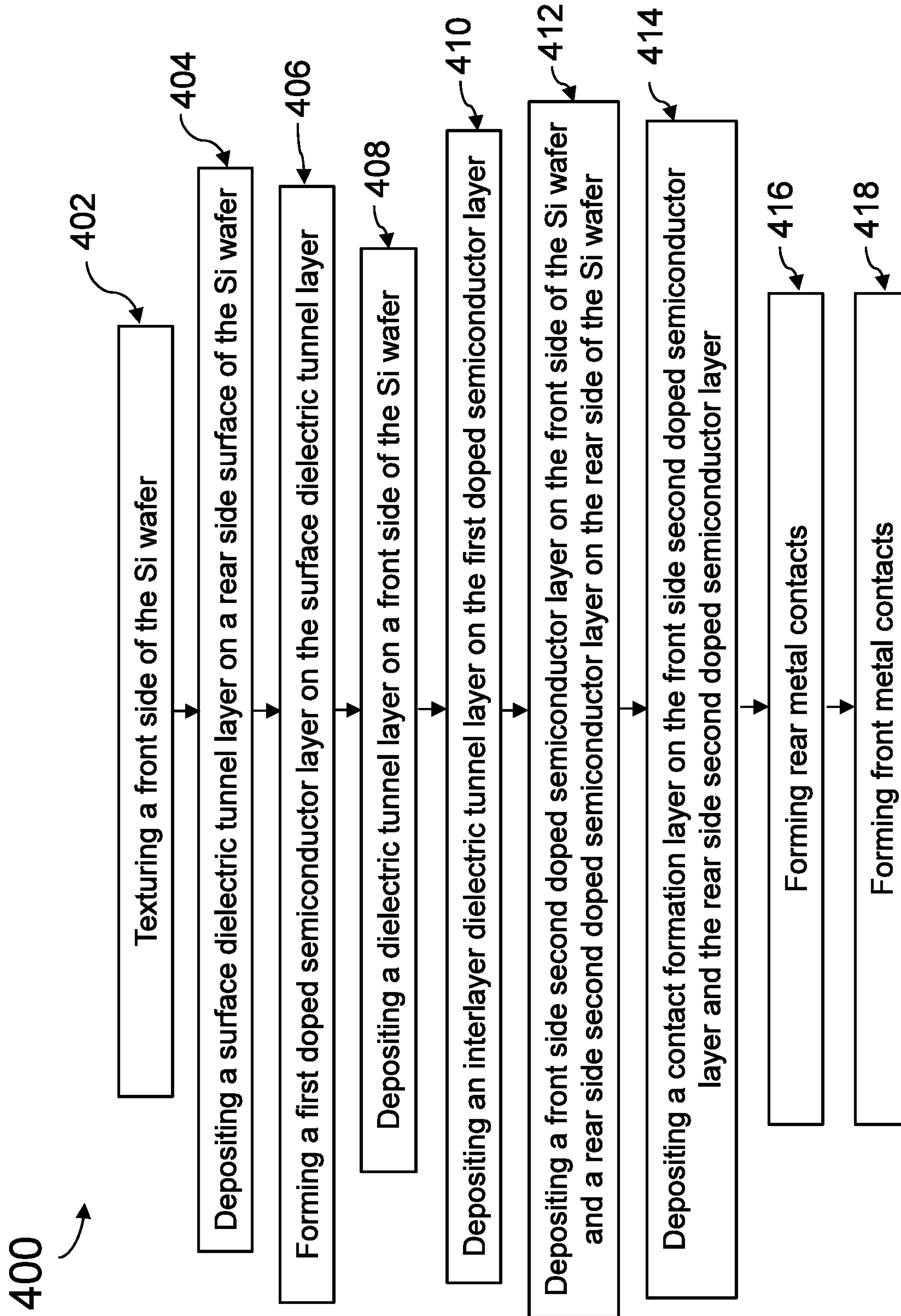


Figure 4A

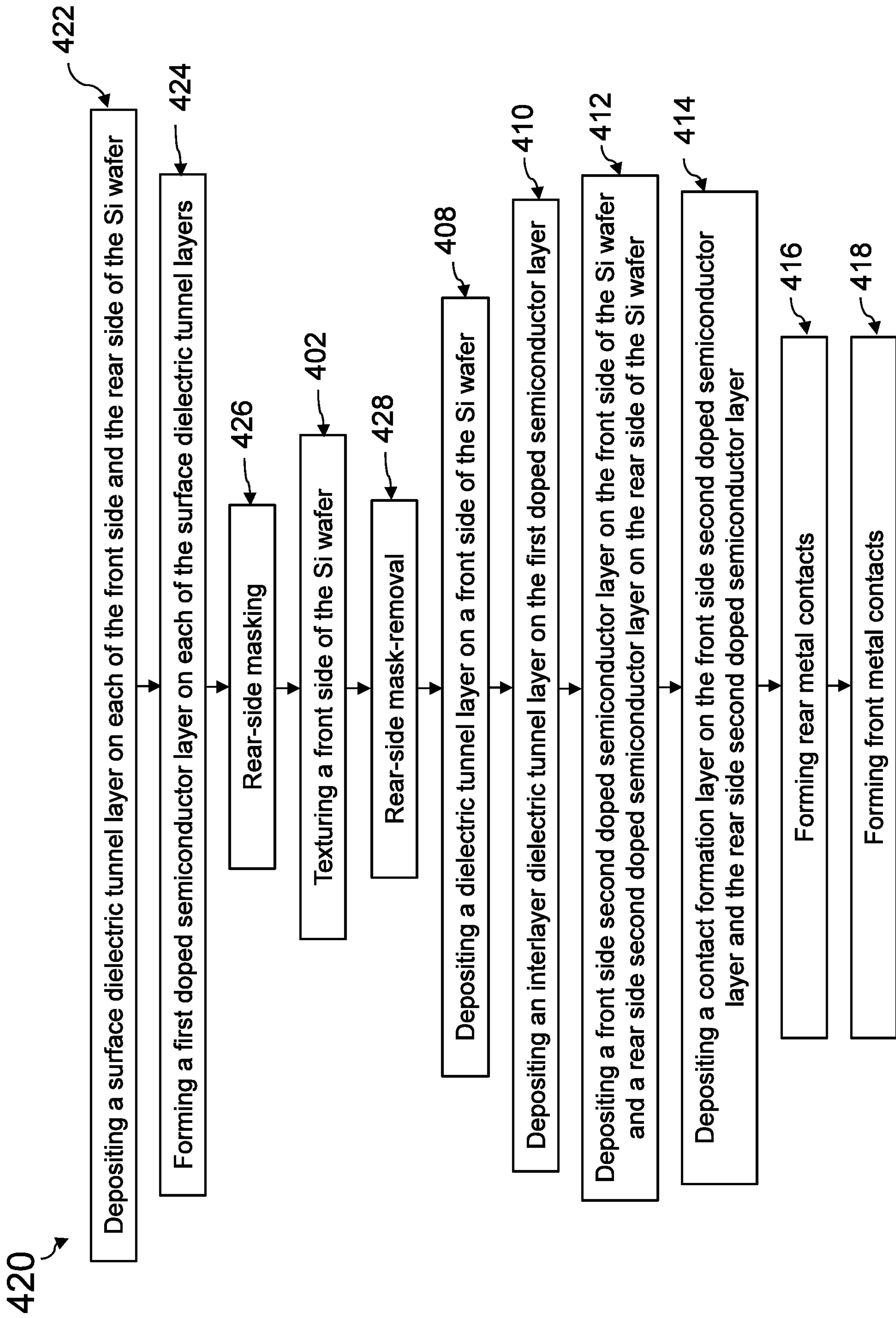


Figure 4B

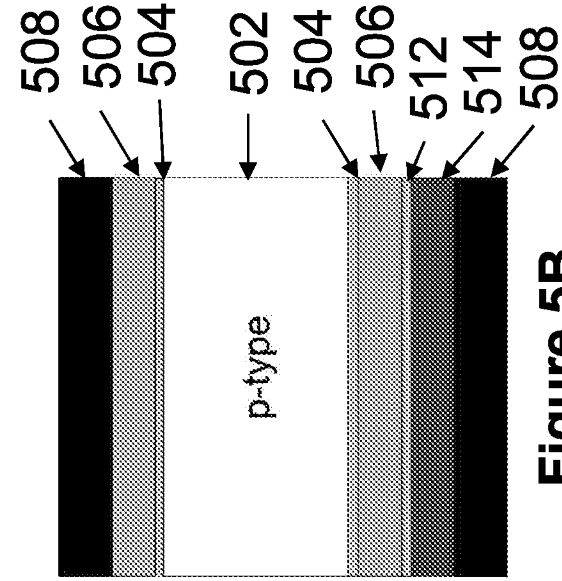


Figure 5B

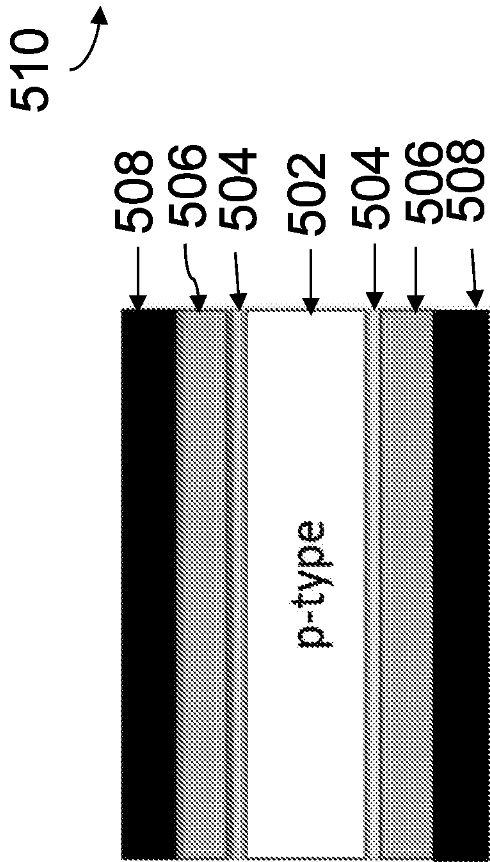


Figure 5A

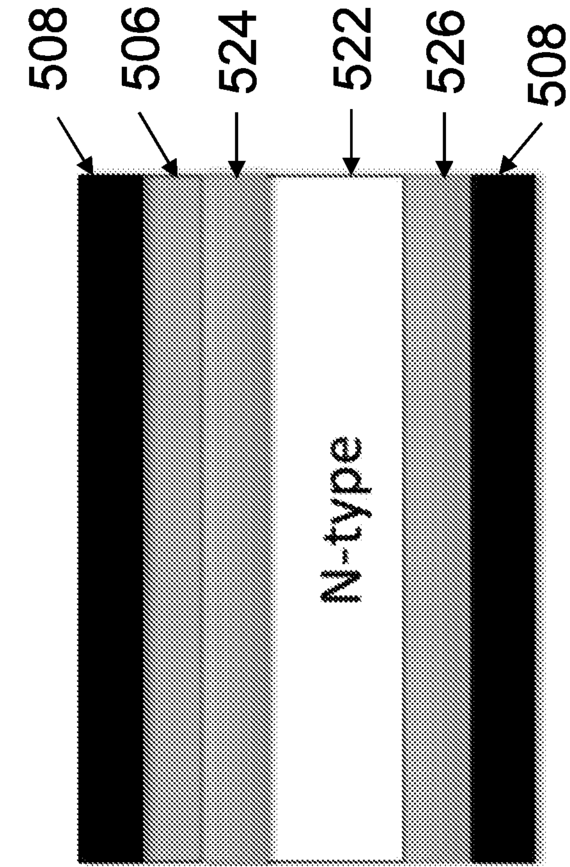


Figure 5C

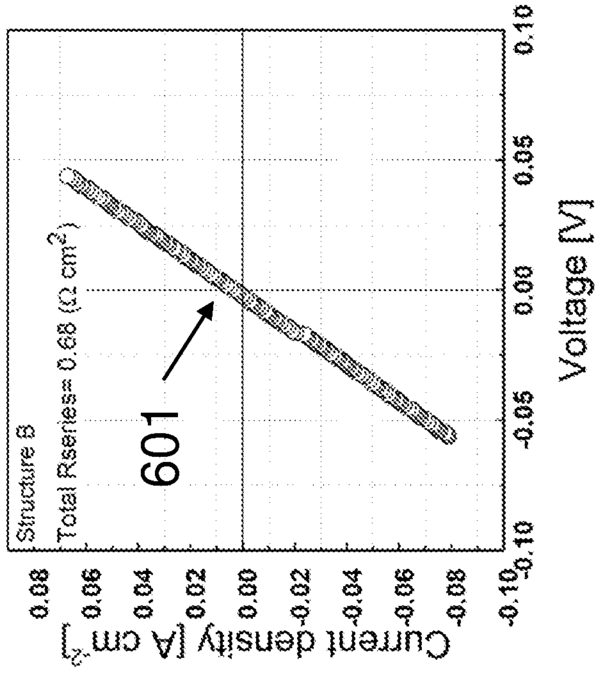


Figure 6B

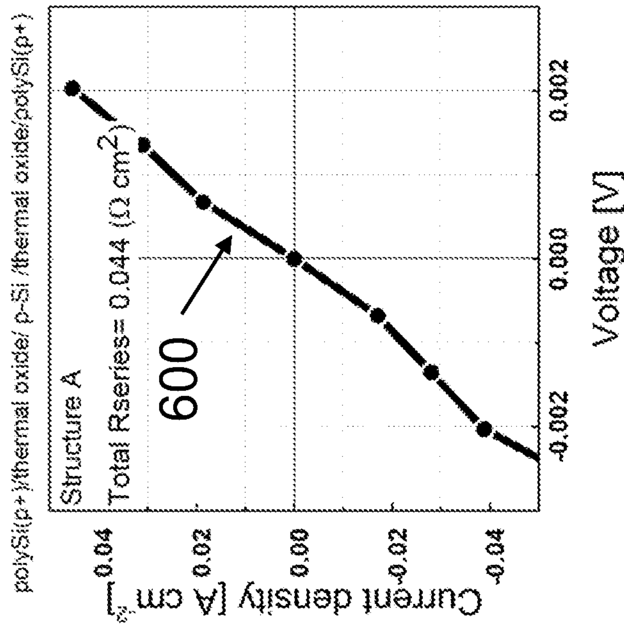


Figure 6A

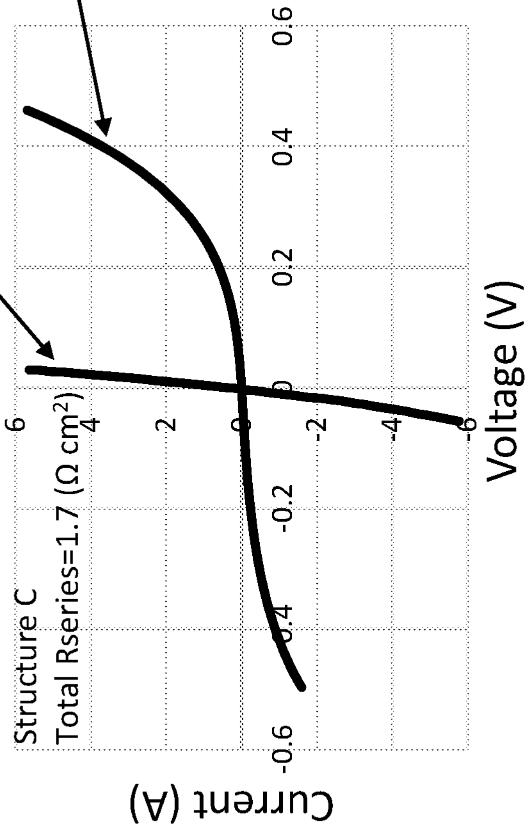


Figure 6C

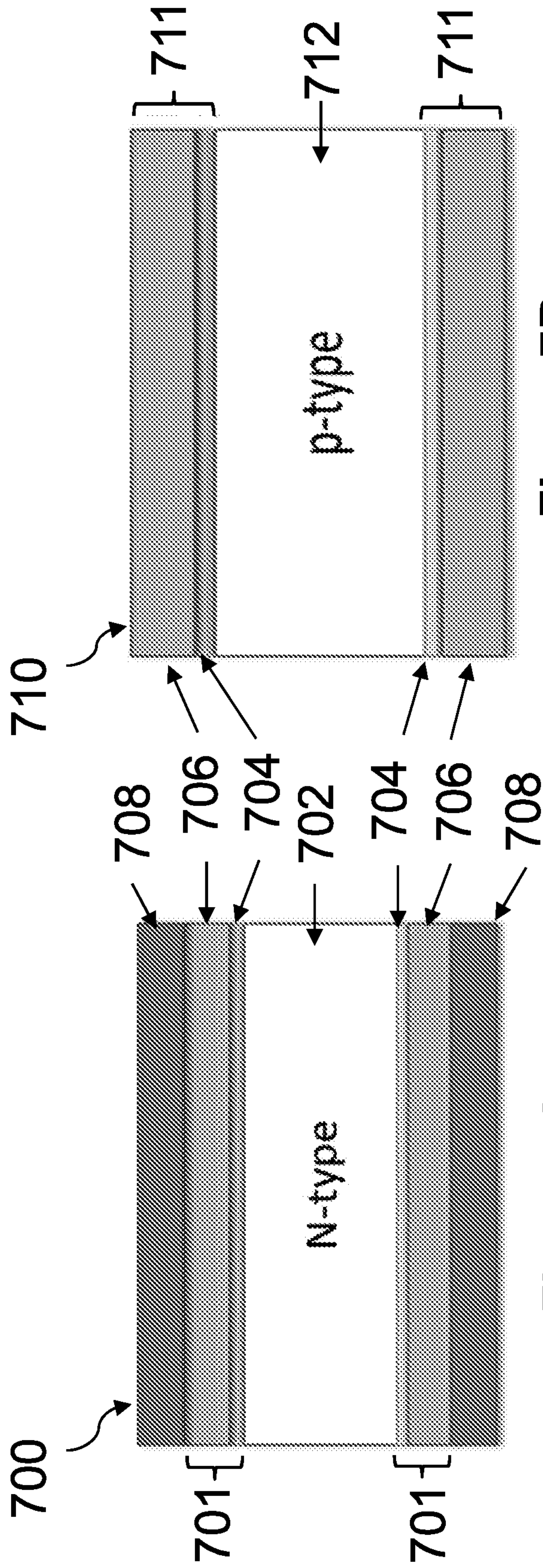


Figure 7A

Figure 7B

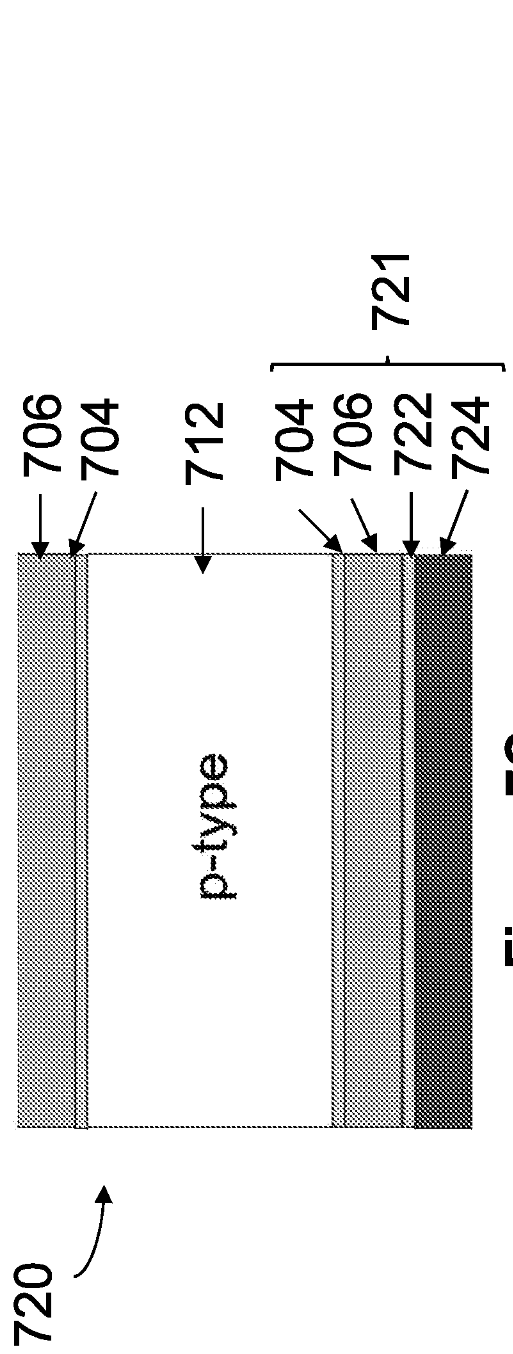


Figure 7C

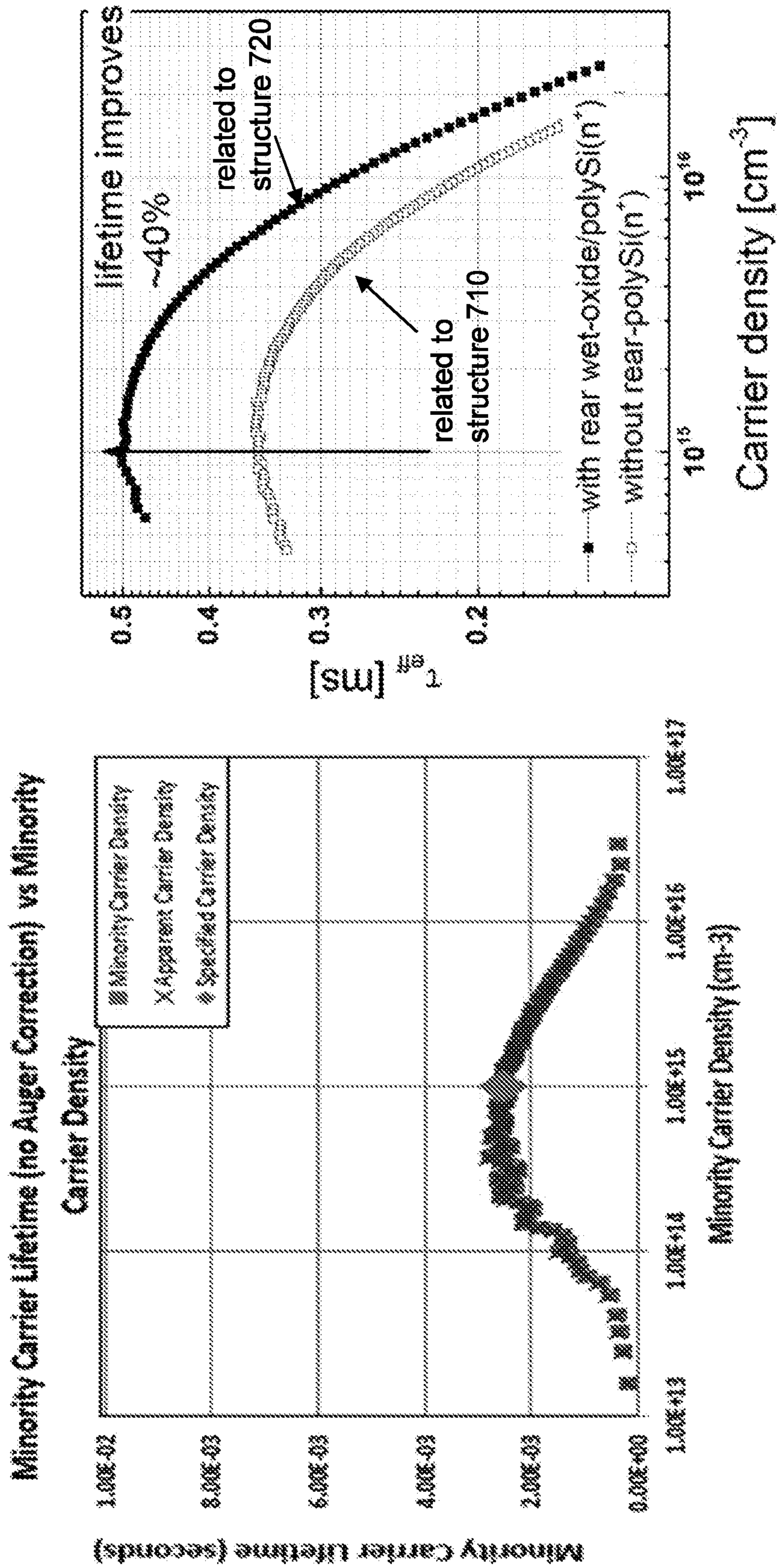


Figure 8A

Figure 8B

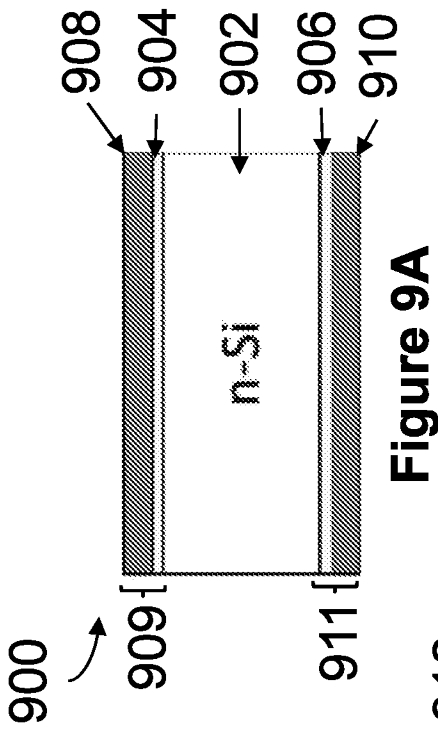


Figure 9A

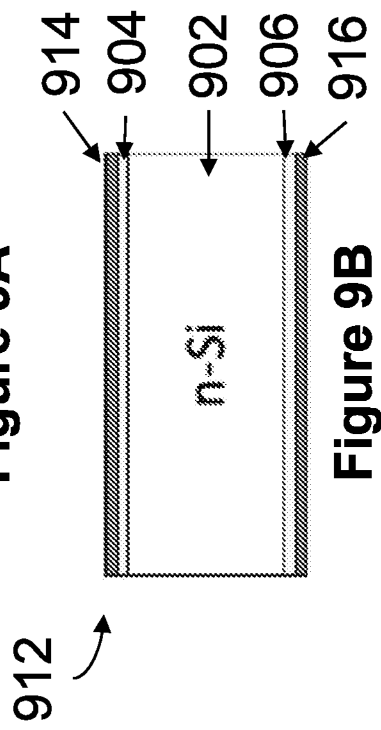


Figure 9B

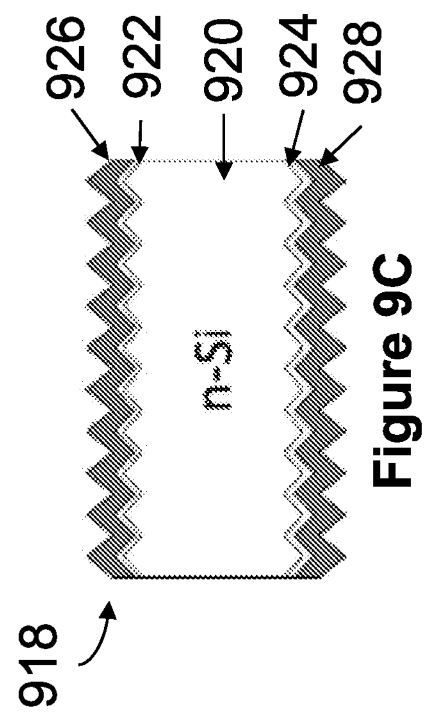


Figure 9C

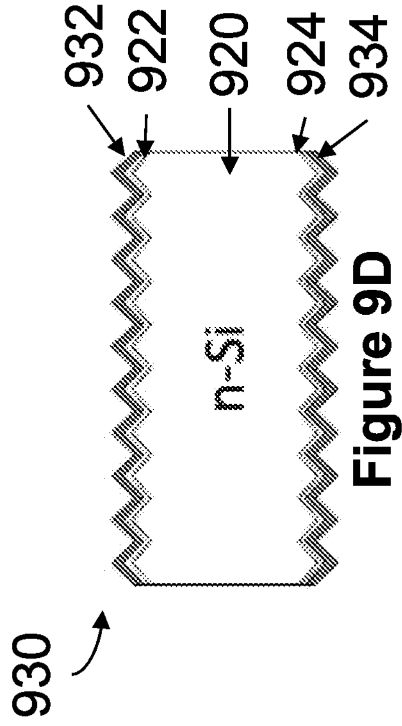


Figure 9D

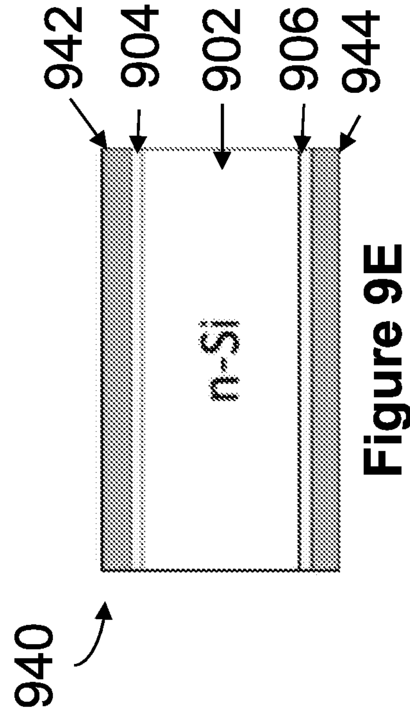


Figure 9E

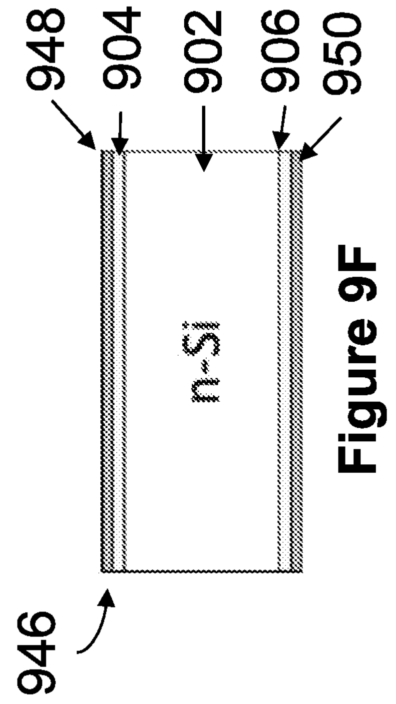


Figure 9F

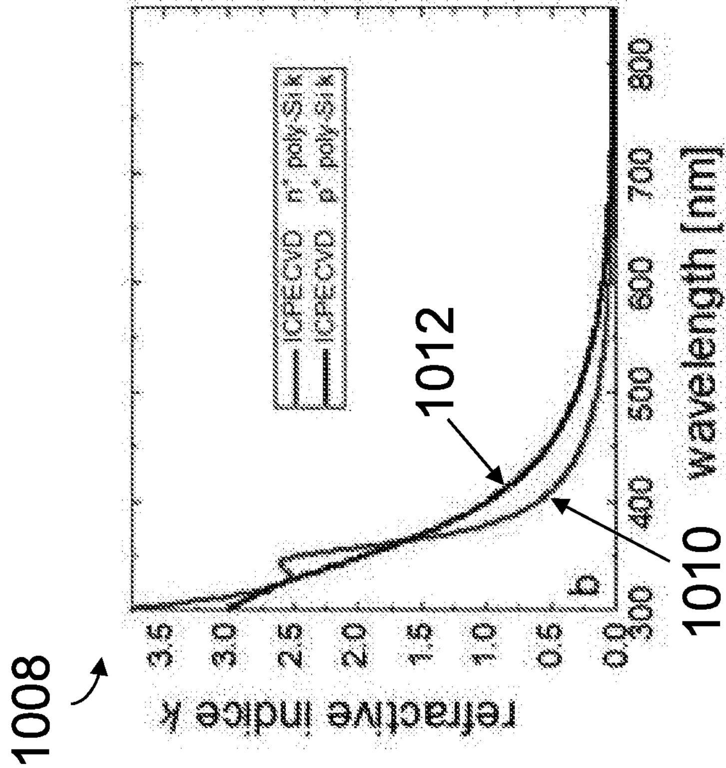


Figure 10B

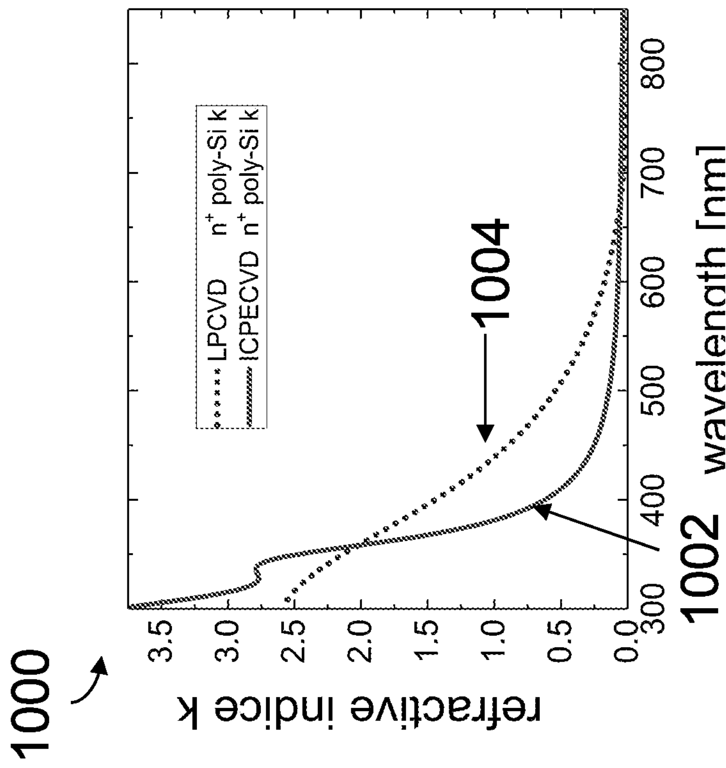


Figure 10A

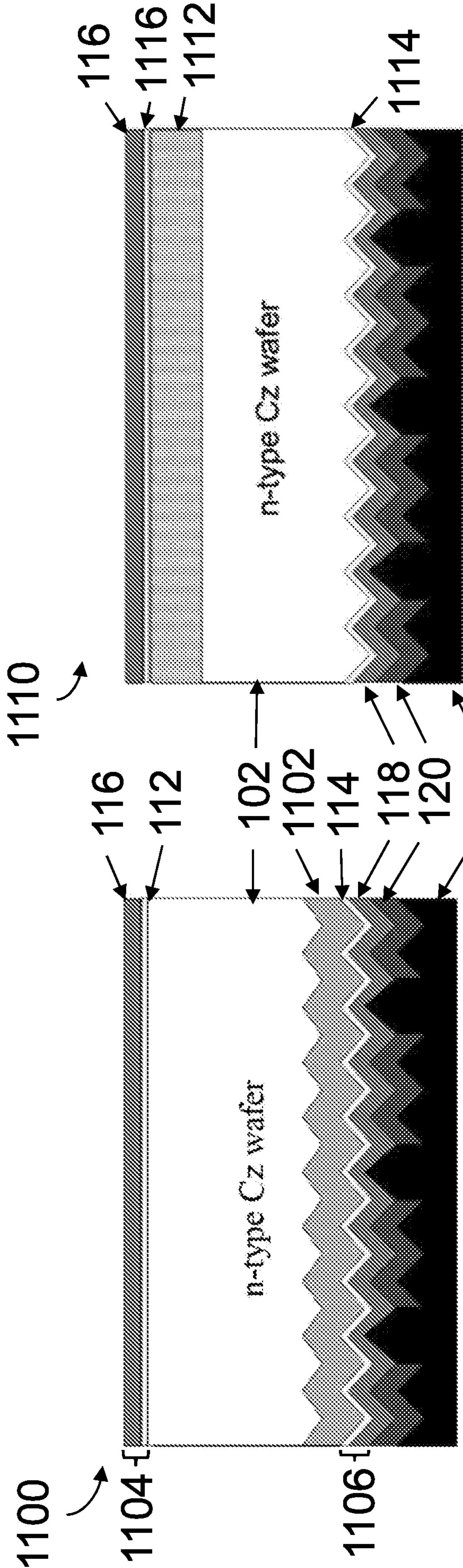


Figure 11A

Figure 11B

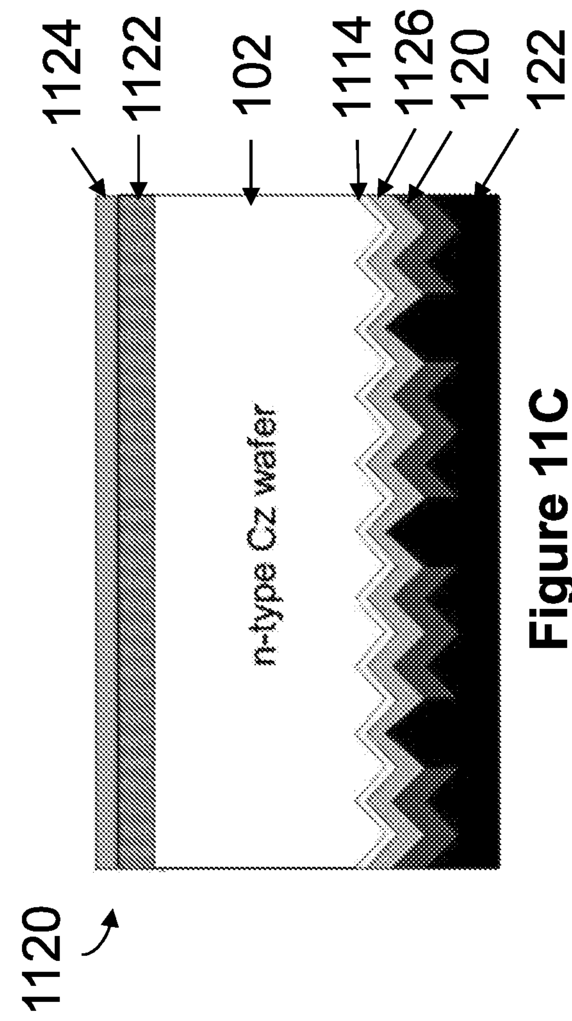
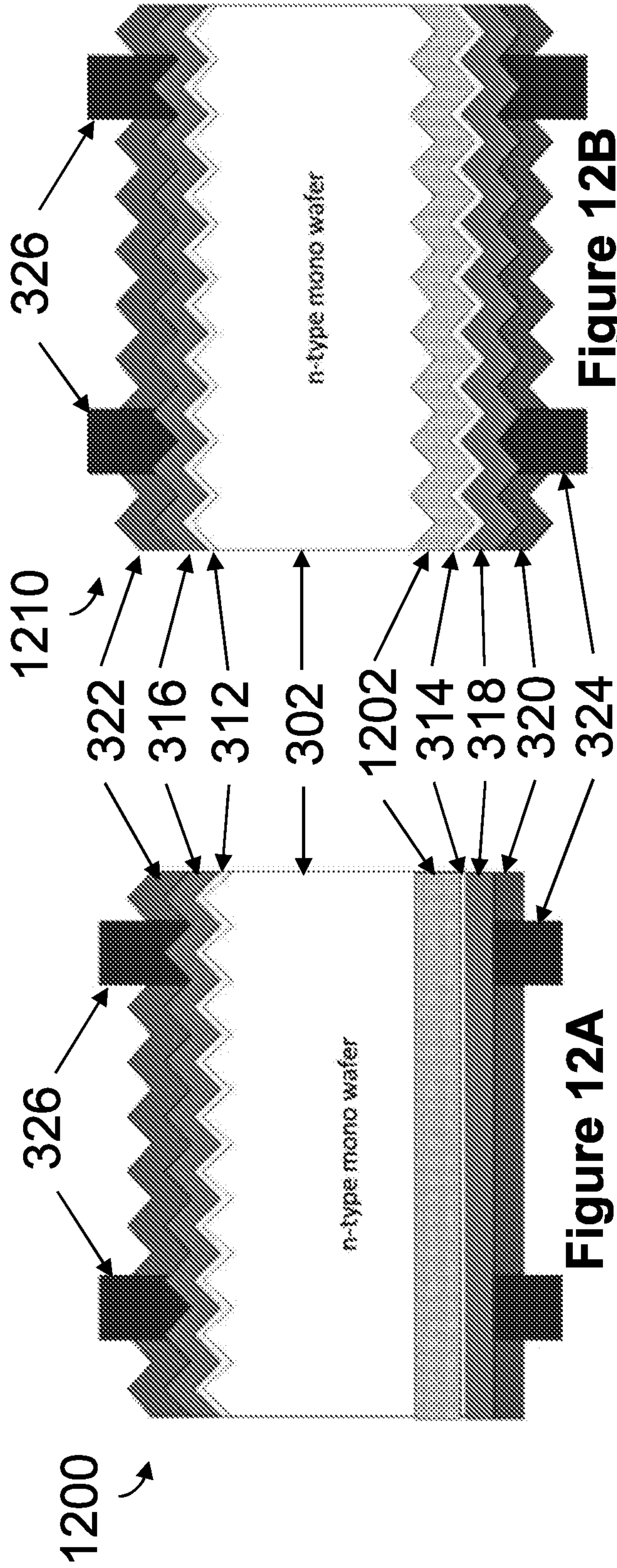
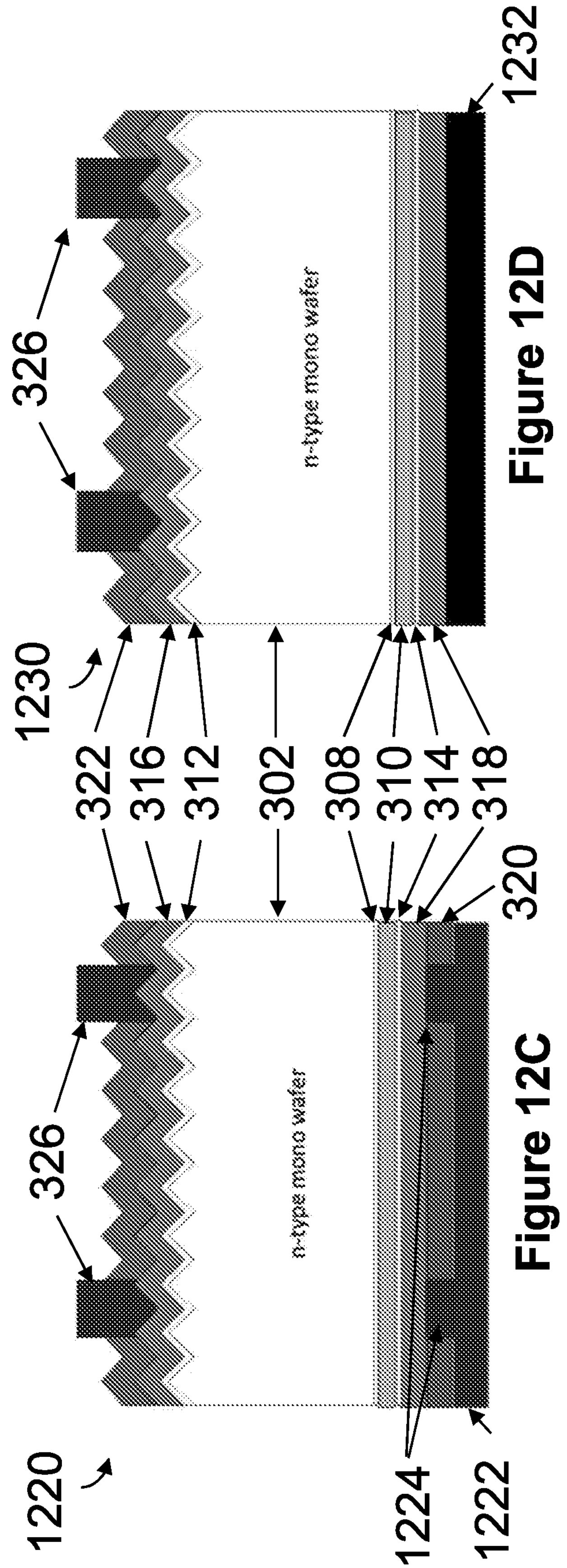


Figure 11C


1200
326
n-type mono wafer
Figure 12A
322
316
312
302
1202
314
318
320
324
1210
326
n-type mono wafer
Figure 12B


1220
326
n-type mono wafer
Figure 12C
1224
1222
322
316
312
302
308
310
314
318
320
1230
326
n-type mono wafer
Figure 12D
1232

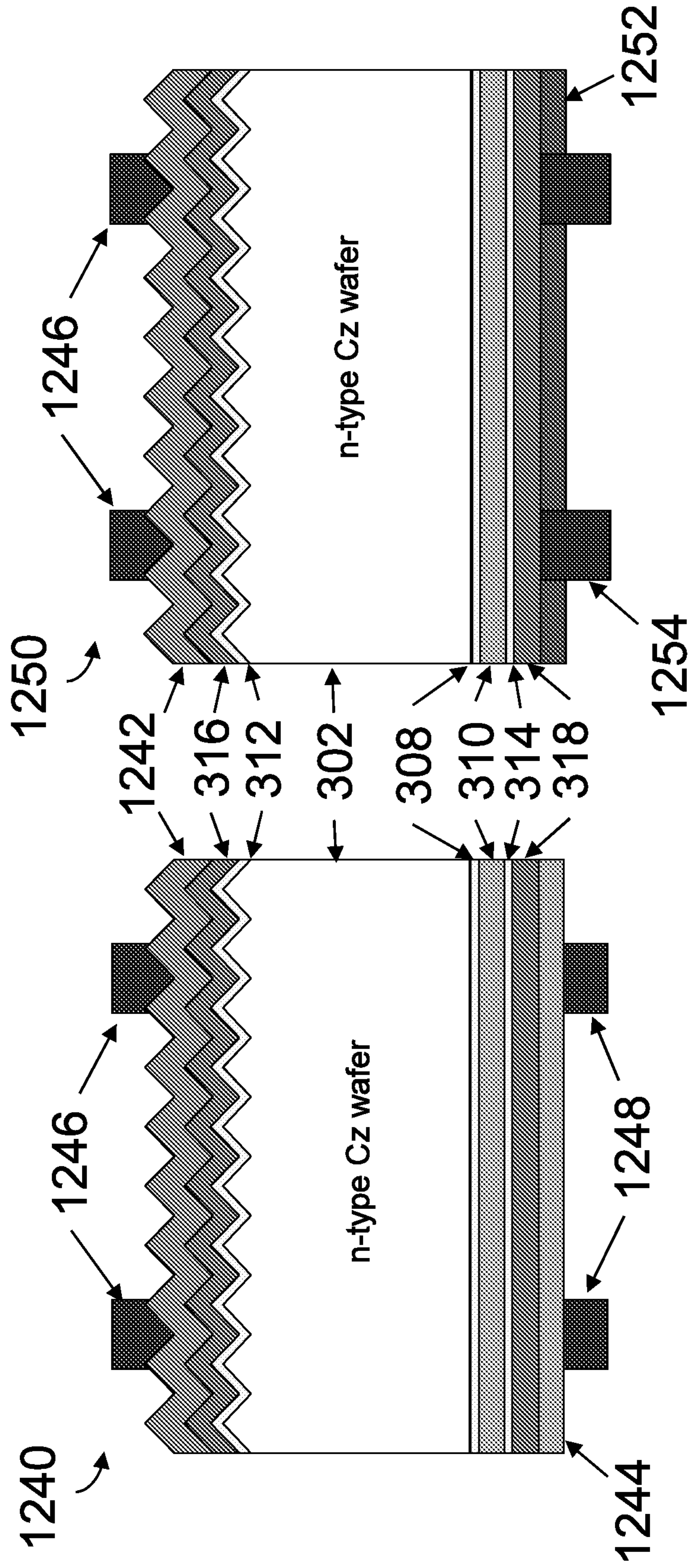


Figure 12F

Figure 12E

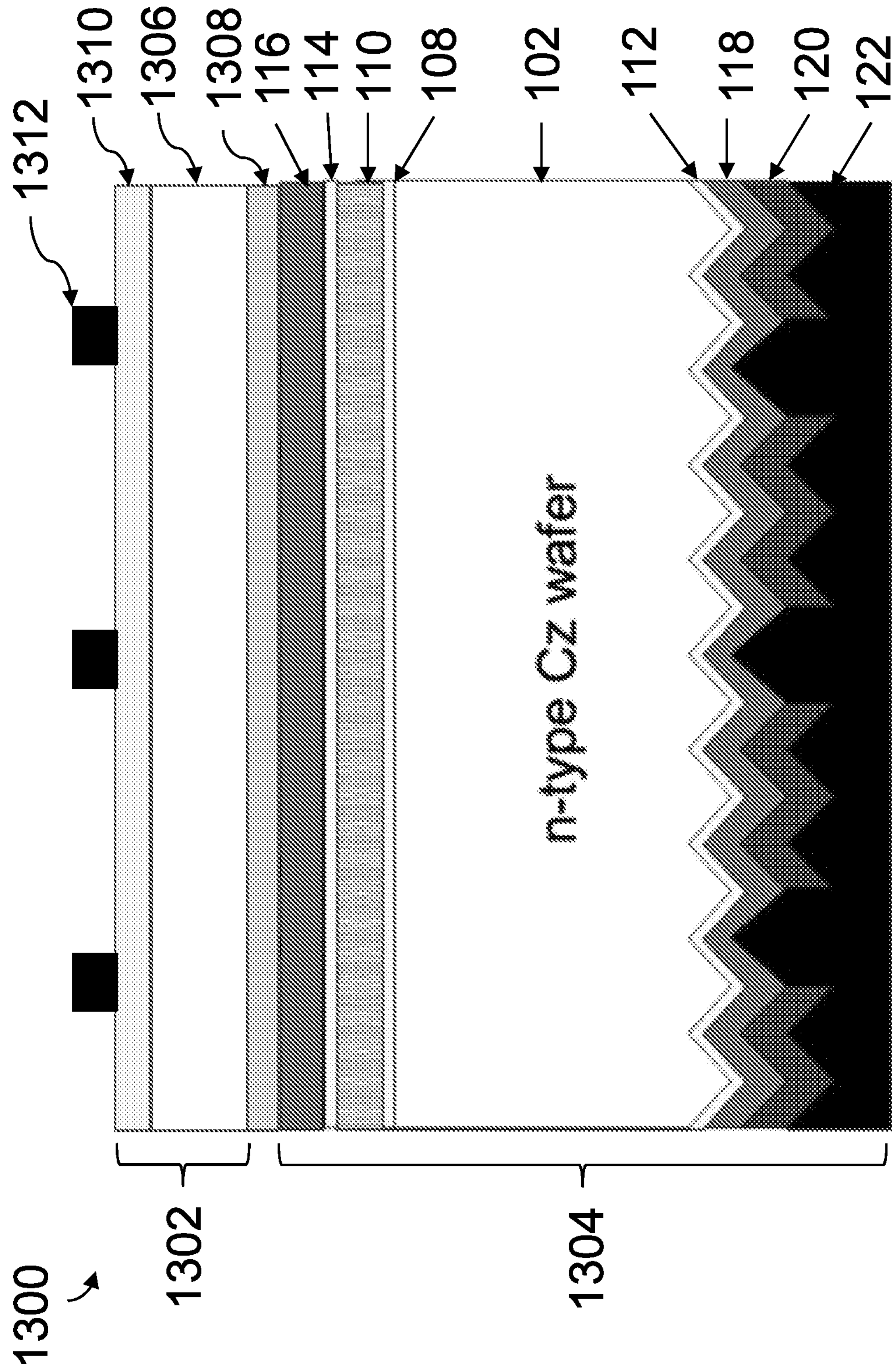


Figure 13

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2020/050186

A. CLASSIFICATION OF SUBJECT MATTER

H01L 31/06 (2012.01) H01L 31/18 (2006.01)

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT: solar, photovoltaic, cell, dielectric, front, top, back, rear, junction, passivate, tunnel, junction, diode, contact, electrode, texture, LPCVD, double side, single process, 太阳能，光电, 光伏, 电池, 介电, 正, 顶, 背, 反, 结, 遂穿, 钝化, 电极, 接触, 织构, 低压化学气相沉积, 双面, 单步 and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 202977494 U (ALTUSVIA ENERGY TAICANG CO LTD) 5 June 2013 Fig. 1, para. [0014], [0018]-[0026], [0034] of the original non-English language document (a machine translation is enclosed **only** for your reference)	1, 10-16, 25-32
Y	TOMASI, A. ET AL., Simple processing of back-contacted silicon heterojunction solar cells using selective-area crystalline growth. *Nature Energy*, 24 April 2017, Vol. 2, pages 17062 [Retrieved on 2020-08-19] <DOI: 10.1038/NENERGY.2017.62> Fig. 1e	1-9, 16-24
Y	US 2018/0374977 A1 (GEERLIGS L. J. ET AL.) 27 December 2018 Fig.2, para. [0073]-[0076]	1-9, 16-24

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

*Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19/08/2020 *(day/month/year)*	*18/09/2020* *(day/month/year)*

Name and mailing address of the ISA/SG	Authorized officer
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	CN 110061083 A (DONGFANG RISHENG CHANGZHOU NEW ENERGY CO LTD) 26 July 2019 Para. [0018] of the original non-English language document (a machine translation is enclosed **only** for your reference)	
E	CN 111416017 A (TAIZHOU ZHONGLAI PHOTOELECTRIC TECHNOLOGY CO LTD) 14 July 2020 Para. [0006]-[0017] of the original non-English language document (a machine translation is enclosed **only** for your reference)	

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/SG2020/050186

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN 202977494 U	05/06/2013	NONE	
US 2018/0374977 A1	27/12/2018	NL 2017380 B1	01/03/2018
		NL 2015987 A	27/06/2017
		EP 3391423 A1	24/10/2018
		CN 108604615 A	28/09/2018
		WO 2017/105247 A1	22/06/2017
		TW 201733140 A	16/09/2017
		CN 108604608 A	28/09/2018
		EP 3391419 A1	24/10/2018
CN 110061083 A	26/07/2019	NONE	
CN 111416017 A	14/07/2020	NONE	