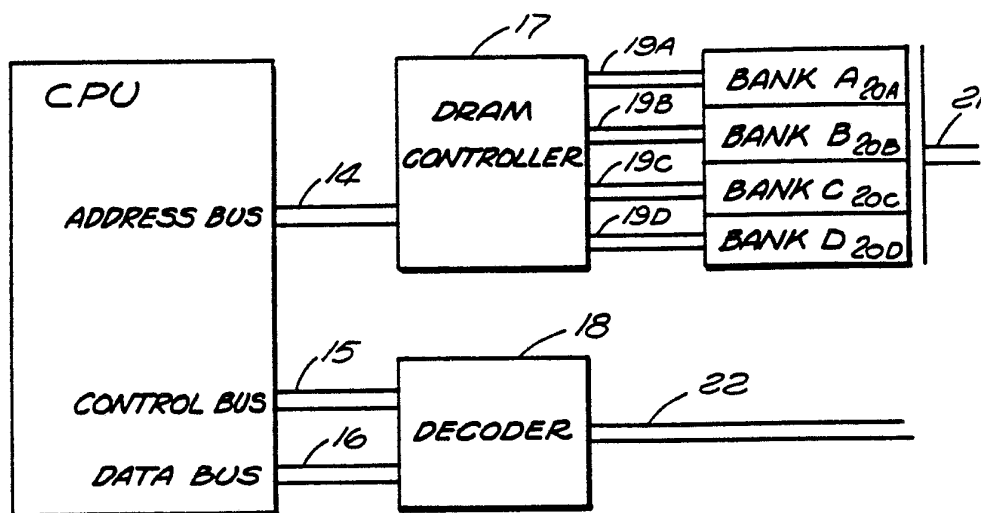




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/US91/06714 (22) International Filing Date: 17 September 1991 (17.09.91) (30) Priority data: 583,283 17 September 1990 (17.09.90) US (71) Applicant: SAMSUNG SEMICONDUCTOR, INC. [US/US]; 2735 North First Street, San Jose, CA 95134 (US). (72) Inventor: SPONRING, Otto ; 1740 Barberry Lane, San Jose, CA 95122 (US). (74) Agents: HECKER, Gary, A. et al.; Hecker & Harriman, 2049 Century Park East, Suite 1200, Los Angeles, CA 90067 (US).		(81) Designated States: AT, AT (European patent), AU, BB, BE (European patent), BF (OAPI patent), BG, BJ (OAPI patent), BR, CA, CF (OAPI patent), CG (OAPI patent), CH, CH (European patent), CI (OAPI patent), CM (OAPI patent), CS, DE, DE (European patent), DK, DK (European patent), ES, ES (European patent), FI, FR (European patent), GA (OAPI patent), GB, GB (European patent), GN (OAPI patent), GR (European patent), HU, IT (European patent), JP, KP, KR, LK, LU, LU (European patent), MC, MG, ML (OAPI patent), MN, MR (OAPI patent), MW, NL, NL (European patent), NO, PL, RO, SD, SE, SE (European patent), SN (OAPI patent), SU ⁺ , TD (OAPI patent), TG (OAPI patent). Published <i>With international search report.</i>

(54) Title: METHOD AND APPARATUS FOR MEMORY SIZE SELECTION**(57) Abstract**

A memory controller (17) for defining memory size in an interleaved multiple bank (20A, 20D) dynamic random access memory or DRAM memory system is described. The system ensures that an associated central processing unit or CPU (10) can access a continuous memory array. The offset is selected according to the memory size. A memory controller (17) that is capable of controlling a given size DRAM selects memory below the maximum size by asserting a high or low level on the most significant address pins (Q6-Q11). By reading the input, the controller (17) can determine that memory space is not available on the higher address locations and the offset for the next bank can be determined.

+ DESIGNATIONS OF "SU"

Any designation of "SU" has effect in the Russian Federation. It is not yet known whether any such designation has effect in other States of the former Soviet Union.

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METHOD AND APPARATUS FOR MEMORY SIZE SELECTIONBACKGROUND OF THE PRESENT INVENTION1. FIELD OF THE INVENTION

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This invention relates to the field of a multiple bank dynamic random access memory (DRAM) systems and in particular to a method and apparatus for selecting bank memory size.

10 2. BACKGROUND ART

A computer system consists of a number of modules or components. Computer systems typically include a central processing unit (CPU) such as a microprocessor. The microprocessor is a program-controlled device that
15 obtains, decodes and executes instructions. A computer system also includes program storage components for storing program instructions, and data storage components for storing data. These storage components may be read only memory (ROM), random access memory (RAM), disc or tape storage, or any other suitable storage means.

20

A computer system also includes input/output (I/O) components for connecting external devices to the microprocessor. Special purpose components, such as memory management units or co-processors may also be part of the computer system.

25

The memory component, also known as a "main memory", is a scarce resource that is dynamically allocated to users, programs, or processes. Main memory is typically a silicon based memory such as a random access

memory (RAM). In many prior art applications, dynamic random access memory (DRAM) is used as the main memory.

A disadvantage of the use of DRAM as main memory for a CPU or
5 other processor are limitations on the memory access time. As
microprocessor technology has improved, the clock rate of operation of the
microprocessor has increased. This increases the memory access time
requirements of the main memory associated with the microprocessor. The
access time of DRAM has not kept pace with the requirements of present
10 microprocessor technology. For example, 16 and 32 bit microprocessors may
require memory access rates of 20 to 40 nanoseconds. Present day DRAM
has access times of 60 to 80 nanoseconds. To satisfy the access requirements
of present-day microprocessors, memory caching schemes or page access
schemes are utilized.

15

Memory caching schemes have the disadvantage of higher cost due to
the use of static RAM (SRAM) components. In addition, caching schemes
suffer from performance penalties in task switching environments and
from physical to virtual address conversion time penalties.

20

One memory scheme used to achieve high performance without the
cost, task switching or conversion penalties of caching schemes is known as
"bank switching". This scheme utilizes a number of banks of DRAM and
interleaves access to the DRAMs to "hide" the precharge time of individual
25 banks. One such scheme is described in U. S. patent application number
604,785 entitled "METHOD AND APPARATUS FOR PAGE PREDICTION
OF MULTIPLE PAGE DRAM", filed on October 26, 1990 and assigned to the
assignee of the present invention.

It is often desired to configure the memory banks to provide various sizes for different applications. In the prior art, this is accomplished by providing additional I/O ports and selecting memory configuration using software. This adds expense and requires complex controller circuitry.

5

Therefore, it is an object of the present invention to provide a method and apparatus for selecting different memory sizes in a multiple bank DRAM environment.

10 It is another object of the present invention to provide a method and apparatus for selecting different memory sizes using a single memory controller.

SUMMARY OF THE PRESENT INVENTION

15

A memory controller for defining memory size in an interleaved multiple bank DRAM memory system is described. The system ensures that an associated CPU can access a contiguous memory array. The offset is selected according to the memory size. A memory controller that is capable
20 of controlling a given size DRAM selects memory below a maximum size by asserting a high or low level on the most significant address pins. By reading the input, the controller can determine that memory space is not available on the higher address locations and the offset for the next bank can be determined.

25

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of the present invention.

Figure 2 is a block diagram of a memory array configuration of the present invention.

Figure 3 is a detailed block diagram of the controller of Figure 1.

Figure 4 is a block diagram of a memory bank of this invention.

Figure 5 is a flow diagram of the operation of this invention.

DETAILED DESCRIPTION OF THE INVENTION

A method and apparatus for memory size selection for a multiple page DRAM is described. In the following description, numerous specific details such as number of bits, number of memory banks, etc. are set forth in detail in order to provide a more thorough description of the invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known features have not been described in detail so as not to unnecessarily obscure the present invention.

A microprocessor or central processing unit (CPU) is a device for obtaining, decoding and executing instructions. A microprocessor requires an associated memory to hold information. This memory is referred to as "main memory" and is used to hold instruction sequences (programs) and to store data. Two characteristics that affect the performance of a microprocessor memory system are capacity and speed.

The speed of a memory depends on the "access time", "write time", and "memory cycle time". The "access time" of a memory corresponds to

the time required to provide a read control signal to the memory and apply the address bits to memory, until the output of the memory is valid. "Write time" is the time between the sending of a write signal to memory and new data has been written to the memory. "Memory cycle time" is the time period required to complete a specific memory function, such as a read/write operation, a read/read operation, a write/write operation, or a write/read operation.

Main memory in a computer system has a logical organization and a physical organization. The physical organization of the main memory of a computer system typically consists of a memory array coupled to a computer system bus for communication with a microprocessor and other computer system components. Each address location in the main memory is accessed by a "physical address". The physical main memory location in which informational items may be stored is called the physical address space or the physical memory space.

An address used by or generated by a program to specify a particular informational item is called a "logical address." The set of logical addresses used by a program to identity informational items is called the "logical address space." The logical organization of a memory must include a mapping means for converting a logical address space to a physical address space. (It should be noted that the logical address space need not be equal to the physical address space.)

25

In many applications, it is desired to provide a greater logical address space than the physical address space of main memory. This is accomplished through a technique known as "virtual memory." In a virtual memory scheme, the logical address space is represented in the

physical main memory and in secondary mass storage such as hard disk drives or floppy disk drives. A virtual memory scheme requires a mechanism to determine whether an addressed element resides in physical memory or in secondary mass storage. When an addressed item does not
5 reside in physical memory, it must be transferred from secondary storage in a process known as "swapping".

A memory paging scheme permits main memory to be allocated in small blocks of equal size called "page frames". A "page" (set of contiguous
10 logical addresses) fits within a page frame. Paging permits the implementation of a logical address space larger than the installed physical memory. If a reference page is missing from a physical memory, it is swapped in from secondary storage as a single unit; that is, the entire page is swapped into physical memory.

15

Many computer applications, particularly those in the personal computer environment, require the use of different sizes of physical memory (DRAM) for efficient operation. The maximum memory size that is addressable by a memory controller depends on the number of pins
20 available. If a memory size less than the maximum is used, certain of the pins (the most significant address bits) are not used. Separate and additional I/O pins are provided for software control of memory selection, adding to device complexity and expense.

25 PRESENT INVENTION

The present invention is a method and apparatus for providing a memory controller for controlling various memory sizes in a multiple bank DRAM environment without the need for additional I/O pins. This

invention interleaves multiple banks of DRAM's to reduce the effective cycle time of the DRAM. An interleaving scheme can provide improved operation if the memory accesses are sequential. The interleave scheme is used to "hide" the precharge time of the DRAM's (which affect access time) 5 for sequential addressing.

A block diagram of the present invention is illustrated in Figure 1. A microprocessor or CPU 10 includes an address bus 14, control bus 15 and data bus 16. The address bus 14 is coupled to a DRAM controller 17. The 10 memory controller 17 permits the definition of various size memory arrays without the need for additional I/O lines. The DRAM controller communicates on buses 19A-19D to DRAM memory banks 20A -20B, respectively. The control bus 15 and data bus 16 are coupled to a decoder 12 which provides output on bus 22. The DRAM memory banks communicate 15 with an auxiliary memory on bus 21.

The four memory banks are driven by four independent channels 19A-19D. The memory array is between 1 and 256 megabytes in the present invention but can be any suitable size. Each DRAM can be 250 k bit, 1 20 megabit, 4 megabit or 16 megabit. While one of the memory banks is accessed, the three remaining banks are loaded in advance in order to avoid wait states when the program advances from the current bank or page. The memory banks are interleaved so that the physical addresses on any given page of memory are stacked above each other. An example of the memory 25 organization of the DRAM memory banks is as follows. In this example, a 256k x 4 DRAM having a 9 bit wide row address equivalent to 512 pages is utilized:

8

Address MSB A21 Row	Bank	LSB A2 Column	Bank	Page
000000000	00	000000000	0	0
=		=	=	=
=		=	=	=
000000000	00	111111111	0	0
000000000	01	000000000	1	0
=		=	=	=
=		=	=	=
000000000	01	111111111	1	0
000000000	10	000000000	2	0
=		=	=	=
=		=	=	=
000000000	10	111111111	2	0
000000000	11	000000000	3	0
=		=	=	=
=		=	=	=
000000000	11	111111111	3	0
000000001	00	000000000	0	1
=		=	=	=
=		=	=	=
000000001	00	111111111	0	1
000000001	01	000000000	1	1
000000001	01	111111111	1	1
=		=	=	=
=		=	=	=
=		=	=	=
111111111	11	000000000	3	511
=		=	=	=
111111111	11	111111111	3	511

A high hit rate is accomplished by mapping the address space in contiguous banks so that a linearly progressing program will access distinguished pages. Therefore, a page change will not result in a wait state 5 for precharging the memory.

A memory configuration used in the present invention is illustrated in Figure 2. In this example, the memories are divided into four separate arrays of 9 memories each, identified as bank A through D. Bank A contains 10 memories 30A-38A; Bank B contains memories 30B-38B; Bank C includes memories 30C-38C, and Bank D includes memories 30D-38D. Each memory can be 64 kilobits by 4, 256 kilobits by 4 or one megabyte x 4. Memories 38A-38D receive parity bits for data validation.

Row address select signals RASA-RASD are provided to memory banks A-D respectively, to select a row in the memory array. Column select signals then select the appropriate column so the desired memory element may be read. Referring to bank A, column select signals CASA 0-CASA 3 are provided. CASA 0 is coupled to memory banks 36A and 37A. Signal CASA 1 is coupled to banks 34A and 35A. Signal CASA 2 is coupled to banks 32A and 33A. Signal CASA 3 is coupled to banks 30A and 31A. Similarly, column select signals CAS B0 - B3 are provided to the memories of bank B; signal CAS C0-C3 are provided to bank C, and signal CAS D0-D3 are provided to bank D.

MEMORY CONTROLLER

A detailed view of the DRAM controller 17 of Figure 1 is illustrated in Figure 3. The DRAM controller 17 is coupled to the processor control bus 15. The processor control bus 15 provides control signals to control block 43. The signals include W/R, D/C, M/O, Reset, ADS, Clock, RS16, and A20 gate signals. The processor address bus 14 provides address information to address latch 44. The control block 43 provides output signal 46 to delay line block 68 and signal 47 to the RAS/CAS generator block 69. The delay line block 68 provides output signal 70 to the RAS/CAS generator block 69. A byte enable signal 40 provided by a microprocessor is also coupled to the control block 17 and is provided as signal 48 to the RAS/CAS generator block 69. The address latch 44 provides output 45 to a page replacement block 53, logic block 55 and program flow detector block 59.

Mode select signals 41 are provided to mode control block 49. Mode control block 49 provides an output 50 to RAS/CAS generator block 69. A disable refresh signal 42 is provided to refresh block 51. Refresh block 51

includes a counter so that appropriate rows and columns can be refreshed as desired. The refresh block 51 provides an output signal 52 to the RAS/CAS generator block 69. The RAS/CAS generator block 69 is also coupled on line 54 to replacement block 53. The page replacement block 53 includes an
5 up/down counter and provides outputs 56, 57, and 58 to logic block 55. The program flow detector block 59 provides an output signal 72 to flag block 60. Flag block 60 provides an increment/decrement signal 61 to page replacement block 53. Blank block 55 provides output signal 71 to the up/down counter of page replacement block 53.

10

The RAS/CAS generator block 69 provides output 62 to output block 64A, 64B, 64C and 64D. The page replacement block 53 provides output on bus 63 to output block 64A-64D, respectively. The output blocks 64A-64D provide address information on Q busses 19A-19D respectively, to memory
15 banks A through D. The output blocks 64A-64D also provide the row address signals, column address signals CAS 0-CAS 3 for each of the memory blanks and a write enable signal.

Each Q bus, for example, is 12 bits wide and can address a maximum
20 of 16 megabits in a memory bank. If a memory bank is resized to a smaller size than the maximum, then certain of the Q lines are not used. The present invention provides a method for using these unused address lines to convey memory sizing information to the controller.

25 The memory depth in this invention is selectable for each individual bank from 16K to 16 megabits. The memory of banks 2, 3 and 4 is mapped to contiguous boundaries to achieve a linear address space for improved operation. Size selection is accomplished by connecting unused Q outputs to VCC or VSS. After power up or reset, the controller asserts a current on

the five highest order Q outputs (Q7-Q11). By reading the input, the controller can determine the memory size and the offset for each bank. The offset is a function of the memory depth and is equal to memory size multiplied by memory width. This is a cost effective way to provide various memory sizes and to allow upgrades without having to replace existing memory devices.

If a memory bank is not populated at all, Q6 is tied to VSS. In such a case, Q7-Q11 can be left open. The banks populate in sequential order and may not have a gap in between. The memory organization can be by eight, by four and by one.

Referring now to Figure 1, consider where bank A, B, C and D are each 1 megabit DRAM's. A user wishes to upgrade bank B to 4 megabits. This invention provides a method to identify the mapping of the memories to the DRAM controller.

Referring to Figure 4, banks 64A-64D each have 12 bit Q lines 19A-19D, respectively. For bank A, the 16 megabit bank, all 12 address lines are used. For bank B, only 10 bits are used because only 1 megabit of memory is addressed. The unused address bits are used to provide information about the memory mapping. Lines Q10-Q11 of bank B are tied to VSS. Only the address lines Q0-Q9 of bank B are utilized.

Bank D is not populated at all. Therefore, address line Q6 is tied to VSS. This invention utilizes this convention to indicate that the bank is not populated. Any single one of the the Q lines can be set to VSS to indicate this state, or any combination of Q lines can be utilized without

departing from the scope of this invention. Alternatively, each line Q0-Q11 can be coupled to VSS to indicate that the bank is unpopulated.

In operation, the memory controller executes an algorithm on power-
5 up to determine the memory size of the DRAM banks. This algorithm is illustrated in the flow diagram of Figure 5. At step 80, the DRAM and DRAM controller are powered up. At step 81, the DRAM controller reads line Q6 of the first memory bank, bank A.

10 At decision block 82, the argument "Is Q6 at VSS?" is made. If the argument at decision block is true, the system proceeds to step 83 and the memory controller identifies block A as not populated. If the argument at decision block 82 is false, the system proceeds to step 84. At step 84, the address lines Q7-Q11 are polled.

15 At decision block 85, the argument "Is at least one line of lines Q7-Q11 at VSS?" is made. If the argument at decision block 85 is false, (i.e. none of the lines Q7-Q11 are at VSS), the system proceeds to step 86 and the bank is identified as being of maximum size.

20 If the argument at decision block 85 is true, the system proceeds to step 87 and the memory of the memory block is determined by identifying which Q lines are at VSS and referring to a table to locate memory size. At step 88, the offset for the memory is determined based on the memory size.
25 Steps 83, 86 and 88 all proceed to step 89. At step 89, the process is repeated for each memory bank.

The memory size and offset for each memory bank is determined by referring to Table 1 below:

Q lines at VSS	Memory Size	Offset
Q11	4 Meg	4 Meg x Memory Width
Q11, Q10	1 Meg	1 Meg x Memory Width
Q11, Q10, Q9	256K	256K x Memory Width
Q11, Q10, Q9, Q8	64K	64K x Memory Width
Q11, Q10, Q9, Q8, Q7	16K	16K x Memory Width

Table 1

Thus, a method and apparatus for sizing of a multiple bank DRAM
5 has been described.

CLAIMS OF THE INVENTION

1. A method of identifying the size of a memory bank having a plurality of address lines for accessing data storage locations in said memory bank, said method comprising the steps of:

coupling certain of said address lines to a first voltage level;

determining, with a processing means, the voltage level on each of said address lines to identify said certain lines;

generating a table address dependent on said certain lines; and

reading an entry stored in a table at said table address to identify a size of said memory bank.

2. The method of claim 1 wherein said memory size is dependent on the number of most significant bits coupled to said first voltage level.

3. The method of claim 2 wherein a memory size when three most significant bits are coupled to said first voltage level is smaller than a memory size when two most significant bits are coupled to said first voltage level.

4. In a computer system having a plurality of memory banks, each of said memory banks having a plurality of address lines, and a processing means coupled to said memory banks, a method of identifying the size of each memory bank comprising the steps of:

coupling certain of said address lines of each of said memory banks to
a first voltage level;

determining, with a processing means, the voltage level on each of
5 said address lines of said memory banks to identify said certain lines;

generating a table address for each memory bank dependent on said
certain lines; and

10 for each memory bank, reading an entry stored in a table at said table
address to identify a size of said memory bank.

5. The method of claim 4 wherein said memory size is dependent
on the number of most significant bits coupled to said first voltage level.
15

6. The method of claim 5 wherein a memory size when three
most significant bits are coupled to said first voltage level is smaller than a
memory size when two most significant bits are coupled to said first voltage
level.
20

7. A method of identifying the size of a memory bank having a
plurality of address lines for accessing data storage locations in said memory
bank, said method comprising the steps of:

25 defining N most significant lines of said address lines;

selectively coupling M most significant address lines of said N most
significant address lines to a first voltage level where $M \leq N$;

generating a table address dependent on the number of address lines
M coupled to said first voltage level; and

reading an entry stored in a table at said table address to identify a size
5 of said memory bank.

8. The method of claim 7 further including the step of coupling a
single one of said lines to said first voltage level when said memory bank
has a memory size of zero.

10

9. The method of claim 8 wherein said single one of said lines is a
line other than the most significant of said lines.

10. A method of identifying the size of a plurality of memory
15 banks each having a plurality of address lines for accessing data storage
locations in said memory banks, said method comprising the steps of:

for each memory bank,

20 defining N most significant lines of said address lines;

selectively coupling M most significant address lines of said N
most significant address lines to a first voltage level where $M \leq N$;

25 generating a table address dependent on the number of address
lines M coupled to said first voltage level; and

reading an entry stored in a table at said table address to identify
a size of said memory bank.

11. The method of claim 10 further including the step of coupling a single one of said lines to said first voltage level when said one of said memory banks has a memory size of zero.

5

12. The method of claim 11 wherein said single one of said lines is a line other than the most significant of said lines.

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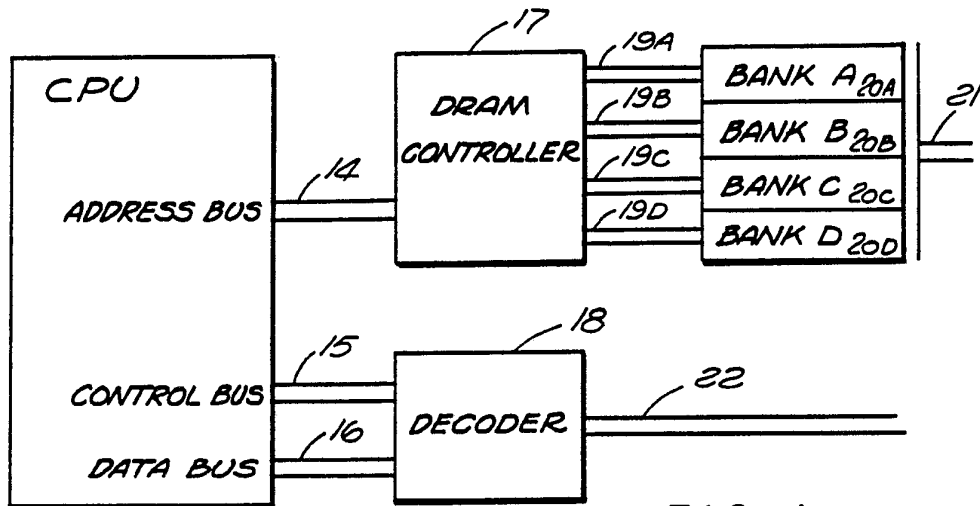
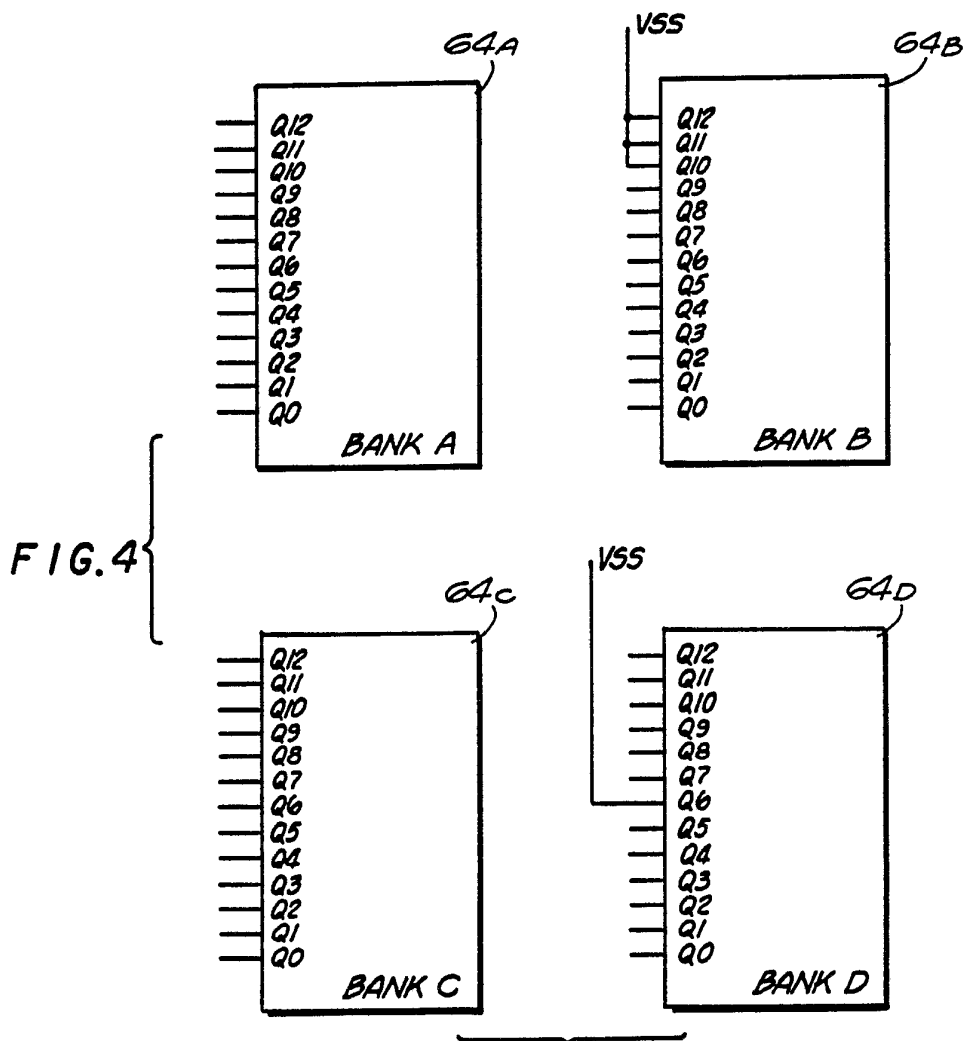


FIG. 1



2/4

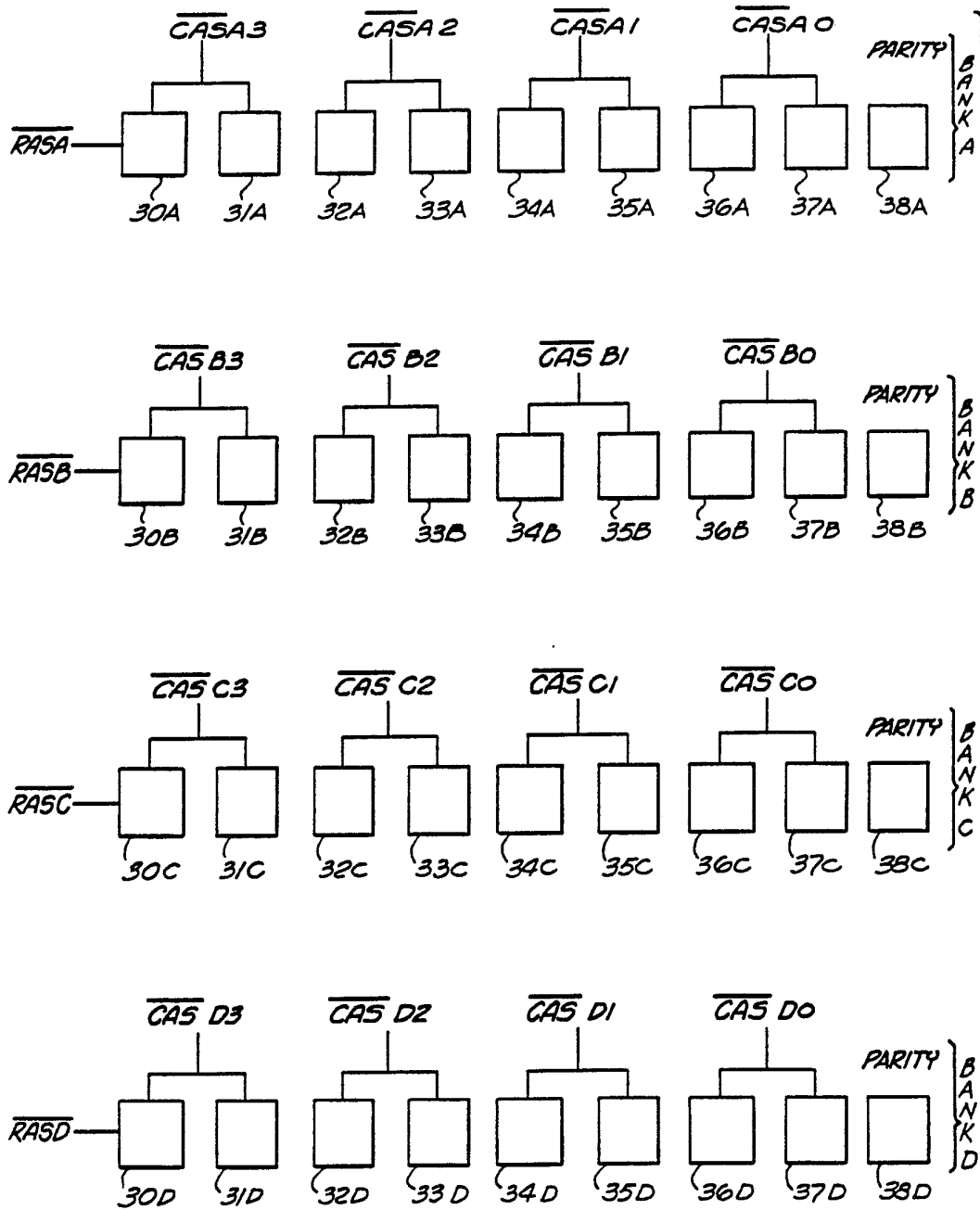


FIG. 2

3/4

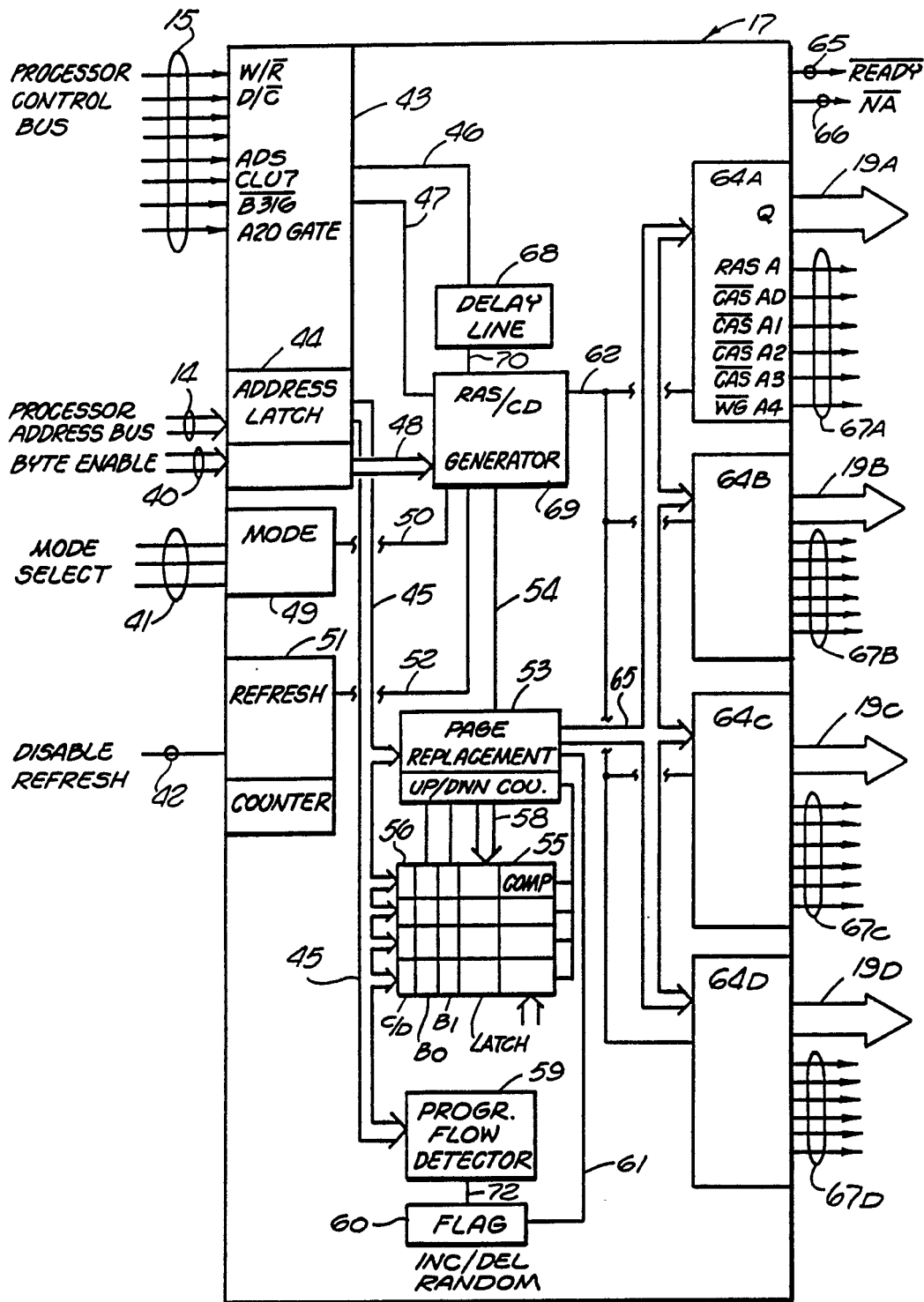
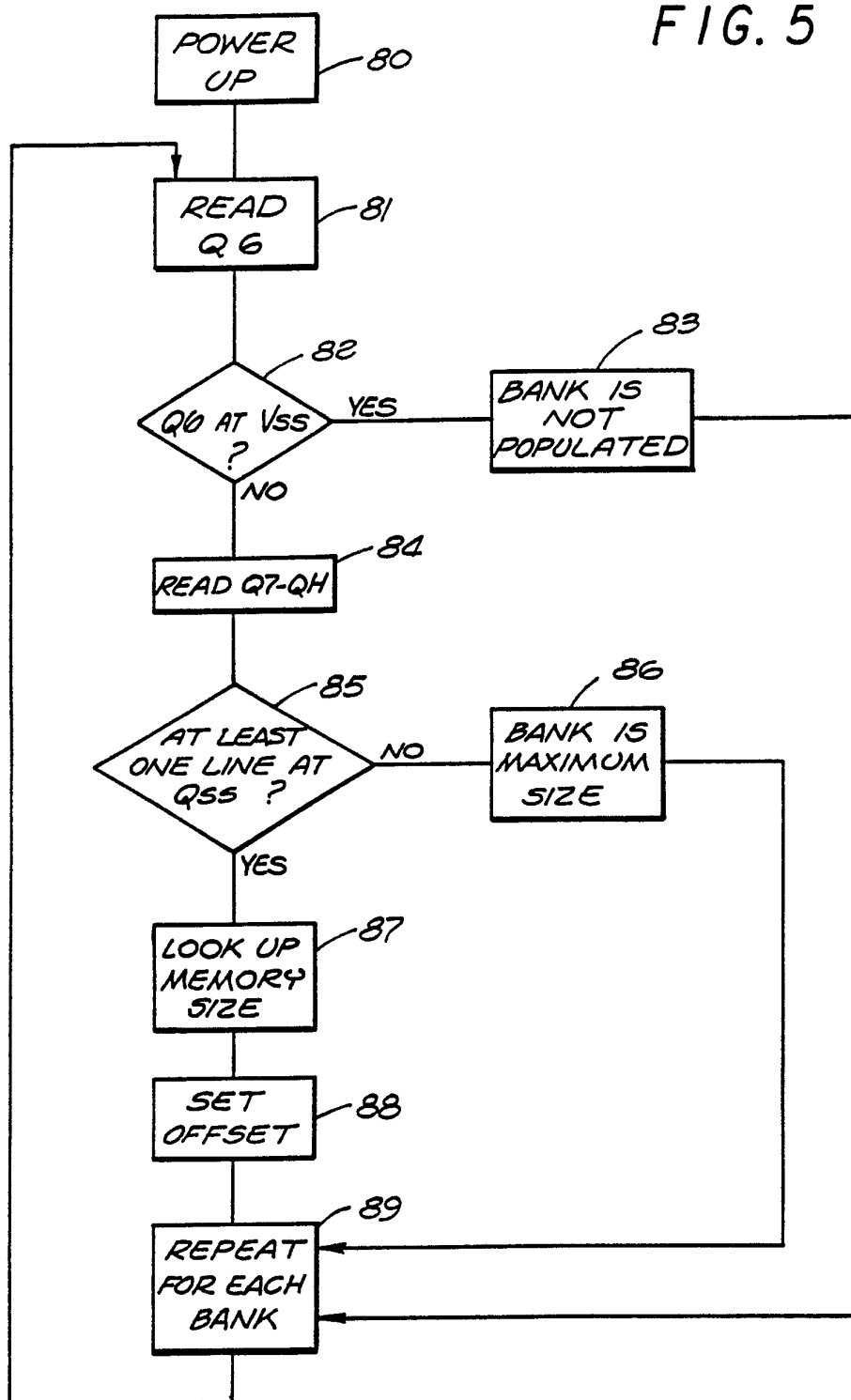


FIG. 3

414

FIG. 5



INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/06714

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC(5): G06F 12/00		
US CL : 395/425		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
US CL	364/200MSFILE, 900MSFILE; 365/52,63,230.03; 395/400,425	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category [*]	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
Y	US, A, 4,234,934 (THORSRUD) 18 NOVEMBER 1980 See column 1, line 55 to column 2, line 28; column 9, line 18 to column 10, line 25 and figure 11.	1-12
Y,P	US, A, 5,027,313 (CULLEY) 25 JUNE 1991 See column 2, line 7 to column 3, line 10; column 5, line 32 to column 6, line 40 and figure 2.	1-12
A	US, A, 4,566,082 (ANDERSON) 21 JANUARY 1986 See column 2, lines 6-50; column 3, lines 46-52; column 4, lines 1-10 and figure 2A and 2B.	
A	US, A, 4,809,234 (KUWASHIRO) 28 FEBRUARY 1989 See column 2, lines 31-52; column 3, lines 22-33; column 4, lines 18-28 and figures 1 and 4.	
A	US, A, 4,951,248 (LYNCH) 21 AUGUST 1990 See column 1, line 50 to column 2, line 24; column 4, lines 6-19 and column 5, lines 8-23.	
A	US, A, 4,908,789 (BLOKKUM ET AL.) 13 MARCH 1990 See column 4, line 21 to column 5, line 16.	
[*] Special categories of cited documents: ¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
27 NOVEMBER 1991	23 DEC 1991	
International Searching Authority	Signature of Authorized Officer	
ISA/US	NGUYEN NGOC HO INTERNATIONAL PATENT COMMISSION GLENN GOSSAGE	

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

- | | |
|-----|--|
| A | US, A, 4,354,258 (SATO) 12 OCTOBER 1982
See column 1, line 63 to column 2, line 10 and
column 5, line 48 to column 6, line 15. |
| A,P | US, A, 5,012,408 (CONROY) 30 APRIL 1991
See column 3, lines 2-16; column 6, lines 19-31 and
column 8, lines 24-39. |
| A | US, A, 4,330,825 (GIRARD) 18 MAY 1982
See entire document. |

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE ¹

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers _____, because they relate to subject matter ¹² not required to be searched by this Authority, namely:
2. ☐ Claim numbers _____, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out ¹³, specifically:
3. ☐ Claim numbers _____, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING ²

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

- ☐ The additional search fees were accompanied by applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.