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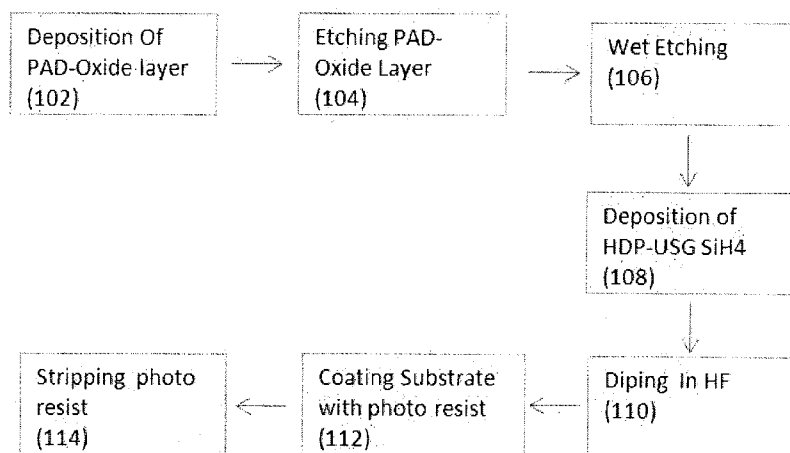
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(54) **Title:** FABRICATION METHOD OF THICK BOTTOM OXIDE IN DEEP TRENCH OF METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS



(57) **Abstract:** A method of fabrication of an oxide layer at the bottom of a trench in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is provided. The method includes deposition of a pad oxide layer on a semiconductor substrate of the MOSFET; etching the pad oxide layer and the semiconductor substrate to form a trench in the semiconductor substrate; depositing a silicone oxide layer to fill the trench in the semiconductor substrate; etching the silicone oxide layer to remove the silicone oxide layer from a plurality of sidewalls of the trench; coating the silicone substrate and silicone oxide layer with a photoresist to protect them of etching; etching the photoresist and the silicone oxide layer until surface of the silicone substrate is reached; and removing the photoresist from inside the trench to obtain a thick bottom oxide (TBO) layer in the trench.



**FABRICATION METHOD OF THICK BOTTOM OXIDE IN DEEP TRENCH OF
METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS**

Field of Invention

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The present invention relates to semiconductor devices, and more particularly to fabrication method of thick bottom oxide in deep trench of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

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Background of the Invention

One of the key components in power electronic applications is a solid state switch. From applications in automobiles to
15 consumer electronics to power converters in industrial applications, a power switch is required to optimally meet demand of the particular application. Power Metal oxide Semiconductor Field Effect Transistors (Power MOSFETs), insulated gate bipolar transistor (IGBT) are some of the
20 examples of solid state switches that are in much use. Double Diffused structure (DMOS) with lateral channels, an example of MOSFET, trenched gate structure has been developed to address differing requirements.

Performance of a power switch such as MOSFETs is its on-resistance, breakdown voltage, switching speed and gate capacitance. The IGBT exhibits lower on-resistance making it preferred switch for applications that require more than 400
5 Volts. For higher frequency and low voltage applications, power MOSFETs is the preferred devices. Voltage requirements often determine structural make up of a switch. For example, in power MOSFET on-resistance R_{Dson} and voltage have a proportional relationship which, therefore, makes it
10 challenging to improve voltage performance while keeping on-resistance low at same time along with high input impedance and high switching speed.

Owing to increasing popularity of MOSFETs, which is also
15 largely driven by portable electronics, has led to greater efforts to try to reduce their specific on-resistance, to minimize die sizes, and to reduce cost, especially for low voltage to have high performance, extended battery life etc.

20 As such, various device structures have been postulated to address such conflicting issues of voltage and on-resistance in case of power MOSFETs. Trench Metal Oxide Semiconductors (Trench-MOS) are the MOSFET structure with a trench gate i.e. the gate electrode is buried in a trench etched in the
25 silicon resulting into a vertical channel. Such non-planar

structures with trench gate structures provide high cell densities along with reduced on-state resistance per unit cell due to MOS gates formed along etched silicon regions. Further, device performance is also influenced by
5 fabrication methods.

To form trenches that provide MOSFETs with various advantages; it is required to develop a thick bottom oxide layer inside of trench. With many processes to develop thick
10 bottom oxide layer inside trench available, there remain problems regarding control of thickness of bottom oxide layer with minimum processes and yet, maintaining the trench profile from any defect caused by the processes to develop it. Limitation from equipment like low selectivity oxide to
15 silicon etching can cause defect to the silicon surface. Moreover, repeating process to get the required thickness of bottom oxide layer can increase production cost.

Moreover, with increasing demand for converters, inverters
20 and the likes MOSFETs are further required lower gate capacitance $R_{on}Q_{gd}$ along with low on-resistance. This may be achieved by a thick bottom oxide layer with controlled thickness at the bottom of the trench.

Accordingly, there is a need for developing a process that can control thickness of bottom oxide layer and at the same time avoid defects in trench profile with maintenance of low gate capacitance.

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Summary of the Invention

In view of the foregoing, embodiments herein provide a method of fabrication of thick bottom oxide in a trench of
10 MOSFET.

In an aspect, a method of fabrication of an oxide layer at the bottom of a trench in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is provided. The method includes
15 deposition of a pad oxide layer on a semiconductor substrate of the MOSFET; etching the pad oxide layer and the semiconductor substrate to form a trench in the semiconductor substrate; depositing a silicone oxide layer to fill the trench in the semiconductor substrate; etching
20 the silicone oxide layer to remove the silicone oxide layer from a plurality of sidewalls of the trench; coating the silicone substrate and silicone oxide layer with a photoresist to protect them of etching; etching the photoresist and the silicone oxide layer until surface of
25 the silicone substrate is reached; and removing the

photoresist from inside the trench to obtain a thick bottom oxide (TBO) layer in the trench.

The method further includes removing the pad oxide layer to obtain the semiconductor substrate with the trench and the pad oxide layer is deposited by using a Plasma Enhanced Chemical Vapour Deposition (PECVD) process. The pad oxide layer is deposited at a rate of 100-200 Angstrom Units per second.

10

The pad oxide layer has thickness between 3800 Angstrom Units - 4200 Angstrom Units, the silicone oxide layer has thickness between 5000-5500 Angstrom units and the photoresist layer has thickness between 9000-9500 Angstrom units. The semiconductor substrate is silicone. And the pad oxide layer and the semiconductor substrate are etched by dry etching process. The silicone oxide layer is deposited to fill the trench by High Density Plasma - Undoped Silicate Glass Silane (HDP-USG SiH_4). The silicone oxide layer is thicker at a bottom than on the sidewalls and the thick bottom oxide serves as an insulating layer to make MOSFET of low gate capacitance.

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The silicone oxide layer from the sidewalls of the trench is etched by a wet etching process and the wet etching process

25

is treating the silicone oxide layer with Hydrofluoric Acid. The photoresist and the silicone oxide layer is removed by anisotropic plasma etching or dry etching.

5 **Brief Description of the Drawings**

Other objects, features, and advantages of the invention will be apparent from the following description when read with reference to the accompanying drawings. In the
10 drawings, wherein like reference numerals denote corresponding parts throughout the several views:

Figure 1 illustrates a process of fabrication of thick bottom oxide layer in deep trench of power MOSFETs.

15

Figure 2 illustrates a pad oxide layer is deposited on a silicon substrate using a plasma enhanced chemical vapour deposition (PECVD) process according to an embodiment herein;

20

Figure 3 illustrates a trench formed by etching pad oxide layer and silicon substrate according to an embodiment herein;

Figure 4 illustrates a trenched silicon substrate with removed pad oxide layer according to an embodiment herein;

Figure 5 illustrates deposition of a High Density Plasma -
5 Undoped Silicate Glass Silane (HDP-USG SiH_4) with a thick oxide layer at the bottom and a thin oxide layer on the sidewall of the trench of Figure 3 according to an embodiment herein;

10 Figure 6 illustrates the silicon substrate dipped in Hydrofluoric (HF) acid according to an embodiment herein;

Figure 7 illustrates the silicon substrate of Figure 5 coated with a photoresist according to an embodiment herein;

15

Figure 8 illustrates a partially filled trench of the substrate of Figure 6 with the photo-resistive material according to an embodiment herein; and

20 Figure 9 illustrates the silicon substrate with photo-resistive material stripped with TBO formed in trench according to an embodiment herein.

Detailed Description of the Preferred Embodiments

The present invention will now be described in detail with reference to the accompanying in drawings.

5

As stated above, there is a need for developing a process that can control thickness of bottom oxide layer and at the same time avoids defects in trench profile with maintenance of low gate capacitance. The embodiments herein provide a method of fabricating thick bottom oxide layer in deep trench of power MOSFETs.

Figure 1 illustrates a process of fabrication of a thick bottom oxide layer in deep trench of power MOSFETs. In step (102) a pad oxide layer is deposited on surface of a silicon substrate as illustrated in Figure 2. Pad oxide is a thin, thermally grown oxide that separates adjacent layers on a silicon wafer or substrate. In one embodiment, the thickness of the pad oxide layer is 4000 Angstrom Units. The thickness of pad oxide layer is preferably between 3800 and 4200 Angstrom units. There are various methods of depositing pad oxide layer on a silicon substrate. In one embodiment, the pad oxide layer is deposited by using a Plasma Enhanced Chemical Vapour Deposition (PECVD) process which is used to deposit thin films from a vapour state to a solid state such

as substrate. In it, plasma of reacting gases is formed, usually, by DC discharge between two electrodes.

Thereafter, in step (104), trench mask is patterned and
5 etched from the pad oxide layer and the silicon substrate to form trench as illustrated in Figure 3. The trench may have round bottom. In ensuing step (106), the pad oxide layer is removed using wet etching to form a silicone substrate with a deep trench as illustrated in Figure 4. In wet etching,
10 the substrate with pad oxide layer is dipped in a bath of etchant such as Hydrofluoric Acid. Different specialised etchants may be used for different surfaces.

In step (108), silicone oxide layer is deposited at the
15 bottom and sidewall of the trench as illustrated in Figure 5. In one embodiment, the silicone oxide layer is deposited using High Density Plasma-Undoped Silicate Glass Silane (HDP-USG SiH_4). The thickness of the silicone oxide layer is preferably between 5000 and 5500 Angstrom units. The
20 deposition of the silicone oxide layer is thicker at the bottom of the trench than on its sidewalls. The thickness of the silicone oxide layer at the sidewalls of the trench is preferably between 1000 and 1500 Angstrom units. The thick
25 silicone oxide layer at the bottom of the trench may be called as thick bottom oxide (TBO). The thickness of TBO

depends on user application and requirements. It may be varied from 1000-5000 Angstrom Units.

Further, in step (110) oxide layer on the sidewalls in the
5 deep trench is removed by wet etching. In one embodiment, the wet etching is achieved by dipping substrate of Figure 5 in a bath of Hydrofluoric Acis (HF) to remove oxide layer on the sidewalls in the deep trench as illustrated in Figure 6. Simultaneously, it may also etch some of the thick bottom
10 oxide which may be controlled for its thickness required inside the trench.

In step (112), the substrate of Figure 6 is coated with a photoresist (PR) of a certain thickness as illustrated in
15 Figure 7. Following which, the PR partially fills the trench until it covers the TBO and whole silicon substrate as illustrated in Figure 8. PR acts a protector to TBO during dry etching process that is carried out in ensuing step (114). The thickness of the PR layer is preferably between
20 9000 and 9500 Angstrom units. In step (114), a dry etcher etches the PR until it reaches top oxide layer. The etching process will continue with oxide etching until reach silicon substrate surface using high selectivity oxide to silicon dry etching process. Dry etching is a process of removal of a
25 masking material of a silicone substrate by exposing the

silicone substrate to bombardment of ions which is generally a plasma of gases such as oxygen, chlorine etc. Once the process is completed, PR is stripped and TBO is formed in the trench as illustrated in Figure 9.

5

The deep trench with thick bottom oxide layer thus formed by the process explained above provides MOSFETs with low on-resistance along with a low gate capacitance.

Claims

1. A method of fabrication of an oxide layer at the bottom of a trench in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) comprising:

deposition of a pad oxide layer on a semiconductor substrate of said MOSFET;

etching said pad oxide layer and said semiconductor substrate to form a trench in said semiconductor substrate;

depositing a silicone oxide layer to fill said trench in said semiconductor substrate;

etching said silicone oxide layer to remove said silicone oxide layer from a plurality of sidewalls of said trench;

coating said silicone substrate and silicone oxide layer with a photoresist to protect them of etching;

etching said photoresist and said silicone oxide layer until surface of said silicone substrate is reached; and

removing said photoresist from inside said trench to obtain a thick bottom oxide (TBO) layer in said trench.

2. The method of claim 1 further comprising removing said pad oxide layer to obtain said semiconductor substrate with said trench; wherein said pad oxide layer is deposited by using a Plasma Enhanced Chemical Vapour Deposition (PECVD) process.

3. The method of claim 3, wherein said pad oxide layer is deposited at a rate of 100-200 Angstrom Units per second.

4. The method of claim 1, wherein said pad oxide layer has thickness between 3800 Angstrom Units - 4200 Angstrom Units, said silicone oxide layer has thickness between 5000-5500 Angstrom units and said photoresist layer has thickness between 9000-9500 Angstrom units.

5. The method of claim 1, wherein said semiconductor substrate is silicone.

6. The method of claim 1, wherein said pad oxide layer and said semiconductor substrate are etched by dry etching process.

7. The method of claim 1, wherein said silicone oxide layer is deposited to fill said trench by High Density Plasma - Undoped Silicate Glass Silane (HDP-USG SiH₄).

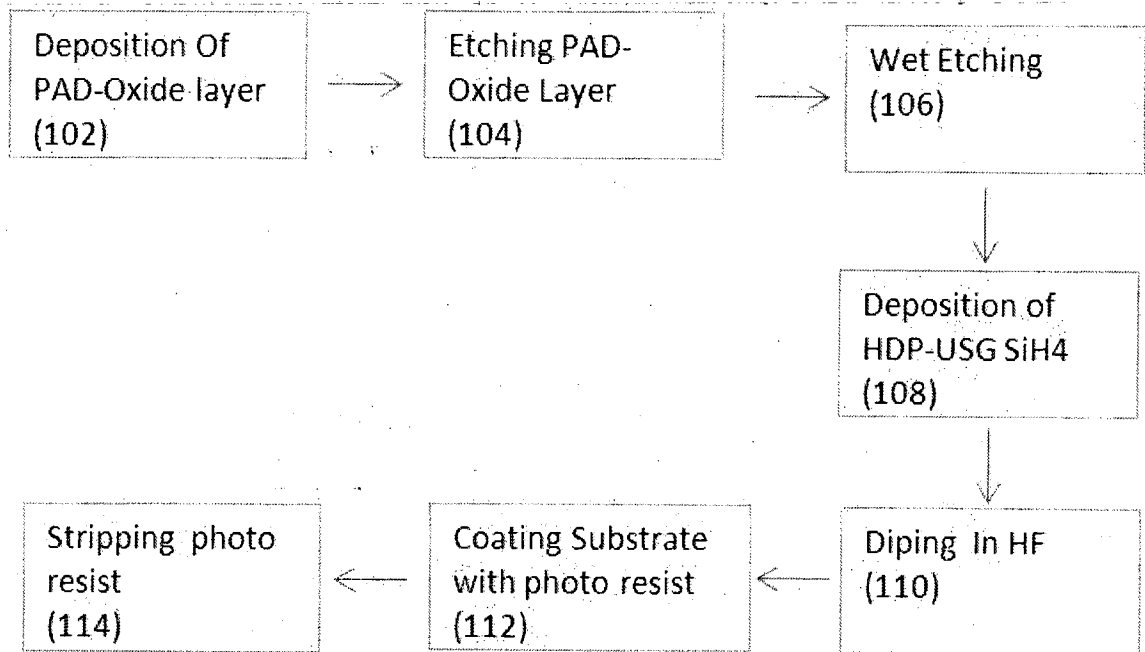
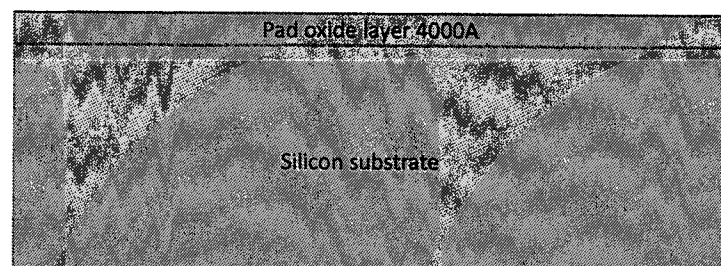
8. The method of claim 1, wherein said silicone oxide layer is thicker at a bottom than on said sidewalls; wherein said thick bottom oxide serves as an insulating layer to make MOSFET of low gate capacitance.

9. The method of claim 1, wherein said silicone oxide layer from said sidewalls of said trench is etched by a wet etching process; wherein said wet etching process is treating said silicone oxide layer with Hydrofluoric Acid.

5

10. The method of claim 1, wherein said photoresist and said silicone oxide layer is removed by anisotropic plasma etching or dry etching.

10

**Figure 1****Figure 2**

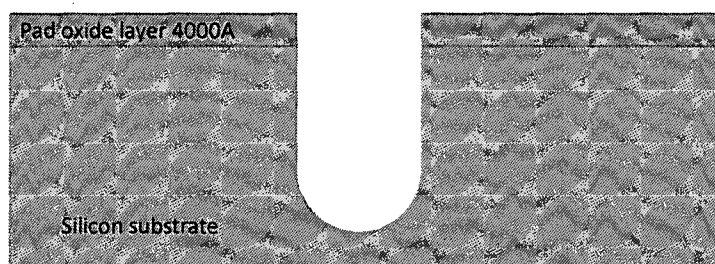


Figure 3

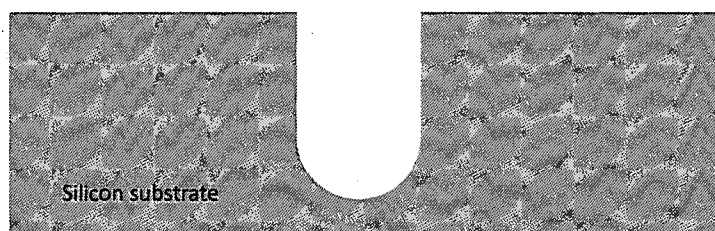


Figure 4

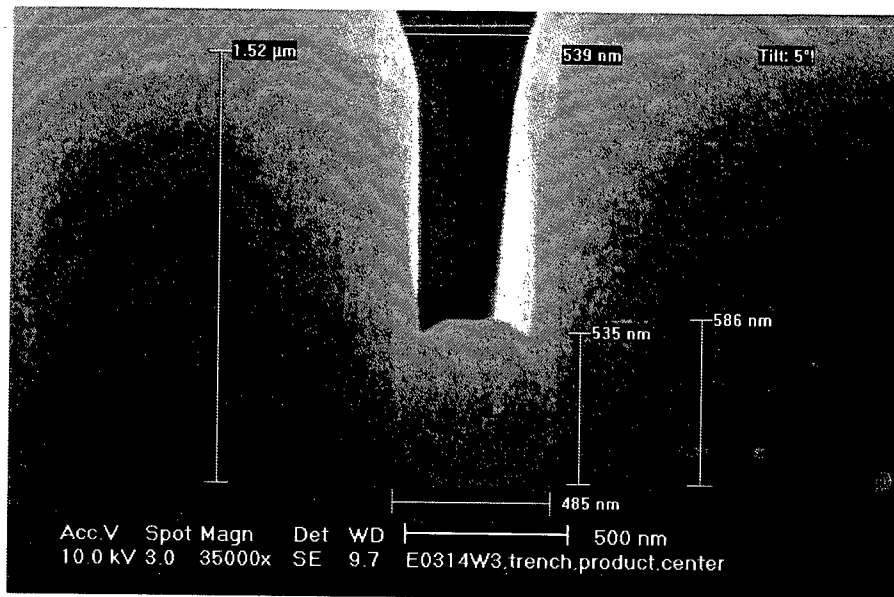


Figure 5

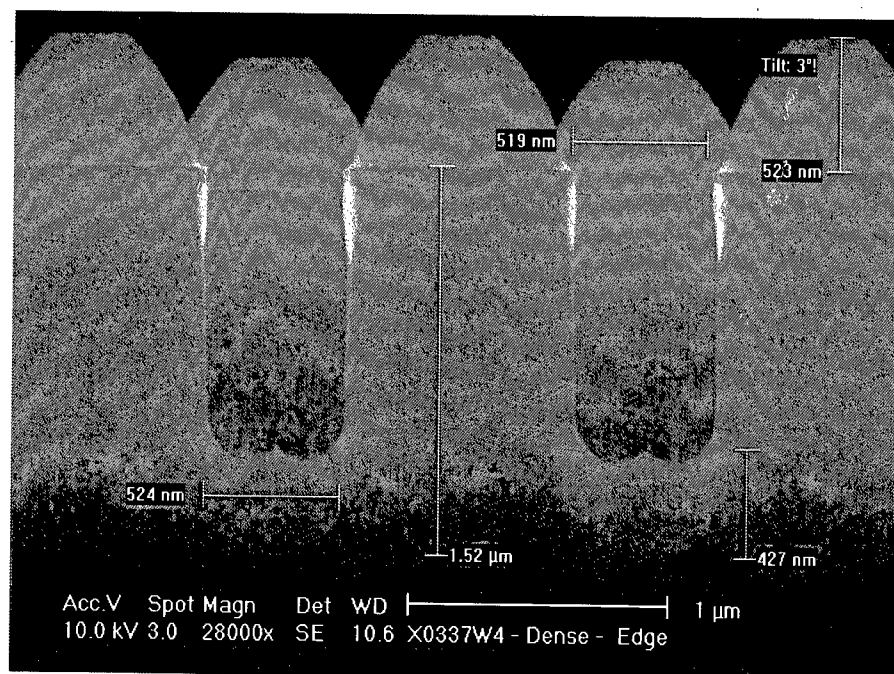
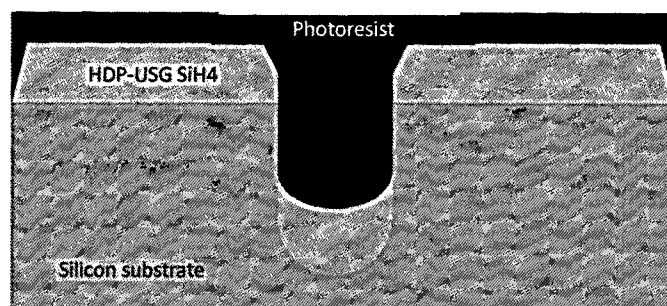
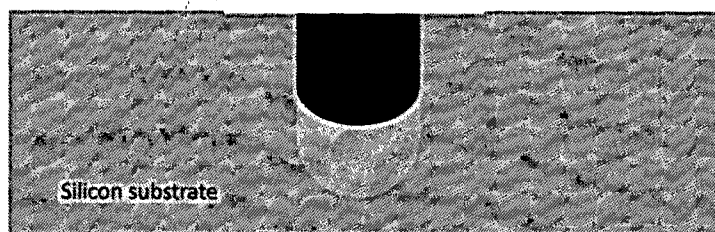


Figure 6

**Figure 7****Figure 8**

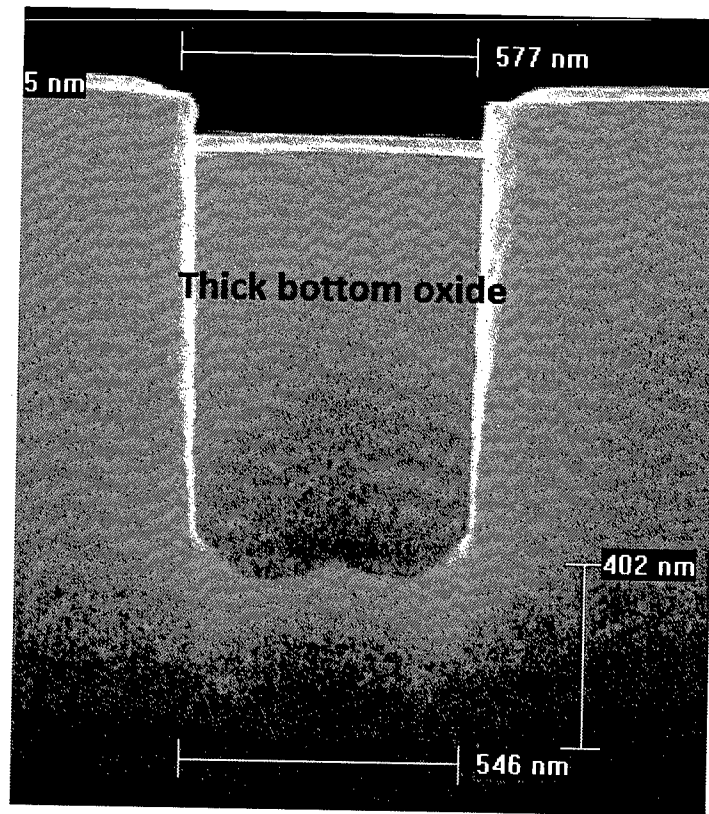


Figure 9

INTERNATIONAL SEARCH REPORT

International application No

PCT/MY2013/000101

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/336 H01L29/423
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	paragraph [0052] - paragraph [0057]; figures 14A-14H	6,8-10
Y	----- US 2008/035990 A1 (MATSUURA HITOSHI [JP] ET AL) 14 February 2008 (2008-02-14) paragraph [0191] - paragraph [0196]; figures 60-63	8-10
Y	----- US 2006/124996 A1 (MIZOKUCHI SHUJI [JP] ET AL) 15 June 2006 (2006-06-15) paragraph [0126]; figures 7C-7F	6,10
A	----- US 6 929 700 B2 (TAN ZHENGQUAN [US] ET AL) 16 August 2005 (2005-08-16) column 11, line 5 - column 14, line 32; figures 2-6B	7



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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