(54) Title: MACROCELL WITH PRODUCT-TERM CASCADE AND IMPROVED FLIP FLOP UTILIZATION

(57) Abstract

A programmable logic device having macrocells (53, 40, 55) enables gate cascades between macrocells (51, 56) to occur with a faster signal transit time, while preserving the flip flop function of the cascaded macrocells by reallocating a redirectable flip flop reset product term (42) to the flip flop (47) input. All gate product terms are retained during cascading. The macrocell logic is optimized for fast signal transit with selectable flip flop clocking. Multiplex clocking (64) and programming (CB1, CB2, CB3) are done with fewer transistors in the signal path, further reducing signal transit time.
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BACKGROUND OF THE INVENTION

This invention relates to the implementation of custom logic functions in an integrated circuit logic device and more specifically to cascading of product terms.

DESCRIPTION OF THE PRIOR ART

There is a need for flexibility and speed in integrated circuit design. In response, a class of integrated circuits (I.C.'s) known as Programmable Logic Devices (PLDs) was developed. PLDs enable the designer to custom program arbitrary logical functions in an I.C. chip, according to relative ease and flexibility in testing prototypes and making design changes.

Xilinx, Inc. the assignee of the present invention, manufactures PLDs, the architecture of which is shown in Fig. 1 including an array of configurable logic blocks 1, 2, 3, 4 interconnected via a universal interconnect matrix (UIM) 5. The input lines 6 into logic block 1 are programmably combined into a number of AND gates 7 in the AND array 8. The output lines 9 provide product terms. Product terms 9 of each AND gate 7 of the AND array 8 are provided to one of a series of macrocells 10 in each logic block.

Architecture of a typical macrocell 10 is shown in Fig. 2. Macrocell 10 configures the outputs of AND array 8 of Fig. 1 and may perform additional logic on the output signals of AND array 8. Macrocell 10 contains an OR gate 11 into which product terms are gated, and a flip flop 12 for storing the output signal of OR gate 11. Output line 13 of OR gate 11 and the output lines 13a and 13b of flip flop 12 can be
configured programmably by setting the multiplexers (MUXs) 14, 15 and 16 with configuration bits on their control terminals, each specifying the output state of the respective MUX.

The macrocell of Fig. 2 advantageously provides a relatively large count (eight) of product terms 11.1 per macrocell, but is inefficient in macrocell usage. The disadvantage is that a fixed product term count is not flexible enough to handle the product term count variability that arises. User product term requirements for a logic function can vary widely, anywhere from one to sixteen product terms or more, depending on the complexity of the logic function. Single product term functions are quite common. For logic functions requiring less than eight product terms in the macrocell of Fig. 2, the unused product terms are wasted. For functions requiring more than eight product terms, the function must be split up into two or more subfunctions, each of which can be implemented with the available eight product terms of a macrocell. The results of the subfunction operations must make additional passes through the AND array to be recombined in other macrocells, thus incurring a significant time delay in the execution of complex logic functions.

For design of complex integrated circuitry, a more flexible macrocell architecture is needed. More recent PLDs feature macrocells with the ability to direct their OR gate or product term outputs into adjacent macrocell OR gate inputs, a feature known as cascading. Cascading enables product terms normally associated with one macrocell to instead be logically combined into the OR gate of another macrocell. This process is known as product term expansion. Xilinx, Inc., the assignee of the present invention, manufactures a PLD incorporating macrocells which can "share" up to twelve product terms by having a set of twelve undedicated "shared" product terms which may be used by any macrocell within the same logic block. Each macrocell also has four private product terms which can be steered by statically controlled multiplexers to functions within the
macrocell. Hence, a macrocell can be fed by anywhere from one to sixteen product terms. However, logic that requires more than sixteen product terms must be performed with two or more passes through macrocell logic, adding an associated time delay with each pass.

Advanced Micro Devices, Inc. manufactures a PLD incorporating macrocells which allow product term expansion without additional passes through macrocell logic as disclosed in AMD's MACHTM Family Data Book. The MACHTM macrocell works by "stealing" all the product terms of one or more neighboring macrocells, for up to 3 neighbors for a total of up to 16 product terms. However, it is also limited to 16 product terms, and the flip flop and output driver associated with a macrocell whose product terms are stolen are thereby rendered useless.

Fig. 3 shows a macrocell 17 disclosed in Pedersen U. S. Patent 5,121,006. The macrocell of Fig. 3 also "steals" product terms of neighboring macrocells, but has extra logic which "reclaims" (makes available) the flip flop in the macrocell for which the product terms have been stolen. In macrocell 17, cascading is accomplished by programmable MUX 18. Setting the configuration bit (to value 1) of MUX 18 directs the output line 19 of OR gate 20 into OR gate 21 of an adjacent macrocell 22. OR gate 33 from adjacent macrocell 34 is shown cascaded into OR gate 20 of macrocell 17. By cascading a series of macrocells in this way, an arbitrary number of product terms can be gated together as needed.

In Fig. 3, macrocell 17 prevents loss of availability of the flip flop by "stealing" one or more product terms from the OR gate 20 input for this purpose by means of switches 23, 24, 25, 26, 27 and the MUXs 28, 29, 30, 31. This is accomplished by programmably setting a switch 23, 24, 25, 26, 27 to divert the associated product term from an OR input line so that a downstream MUX 28, 29, 30, 31 can allocate the product term to a flip flop 32.

The circuit of Pedersen undesirably increases complexity and so compromises speed. Pedersen utilizes switches 23, 24, 25, 26, 27 to direct product terms from the OR gate for use
in reclaiming the flip flop; switches 23, 24, 25, 26, 27
degrade the performance by adding unnecessary delays in
signal transit time, regardless of the switch settings,
thereby slowing down the configured logic function.
Additional logic in the Pedersen macrocell (i.e. elements 35, 36) also delay signal transit times. Pedersen's flip flop 32
can be made transparent (bypassed) by means of multiplexer 37.

SUMMARY OF THE INVENTION
In accordance with the present invention a PLD has a
macrocell for implementing cascades with a faster signal
transit time, while preserving use of the flip flop and
associated output driver of the cascaded macrocell by
reallocating a dedicated product term normally used for flip
clock reset. The macrocell can be selectively clocked
according to any one of a plurality of clock input signals,
to provide flexibility at the macrocell level.

BRIEF DESCRIPTION OF THE DRAWINGS
Fig. 1 is a block diagram of prior art PLD architecture.
Fig. 2 is a schematic diagram of a prior art macrocell
circuit.
Fig. 3 is a schematic diagram of another prior art
macrocell circuit.
Fig. 4 is a schematic diagram of one embodiment of the
present invention.
Fig. 5 is a schematic diagram illustrating the effect of
cascading the macrocell according to the embodiment of Fig.
4.
Fig. 6 is a circuit diagram of a prior art multiplexer
and flip flop.
Fig. 7a is a circuit diagram of a multiplexer in one
embodiment of the present invention.
Fig. 7b is a diagram of a circuit to produce a composite
signal for the circuit of Fig. 7a.
DETAILED DESCRIPTION OF THE INVENTION

In accordance with the present invention a new macrocell provides fast product term cascade and allocation. As shown in the macrocell 40 of Fig. 4, a 5-input OR gate 41 is fed by product term signal lines 43, 44, 45, 46 from a conventional AND array (not shown) and from OR gate 54 of adjacent macrocell 55 via MUX 56. Product term signal line 42 is a dedicated line from the AND array which can be configured to provide a reset input to the flip flop 47 by programming multiplexer 57 using a cascade configuration bit CB1.

OR gate output line 49 is connected by line 50 to the terminal 1 of programmable multiplexer 51, whose output line DOUT cascades into an input terminal of the OR gate 52 of an adjacent macrocell 53. The cascade signal from the OR gate 54 of adjacent macrocell 55 can be input into the OR gate 41 on the line DIN by programming a multiplexer 56 associated with the adjacent macrocell 55 using configuration bit CB3.

The input product term line 42 is used as a dedicated reset line for the flip flop (D-type flip flop) 47 when the macrocell 40 is in the non-cascade mode (i.e., cascade configuration bit CB1 is not set). The input product line 42 connects, respectively, to input terminals 0 and 1 of multiplexers 57 and 48. Multiplexer 57 directs the signal on input product term line 42 to the reset (R) input terminal of flip flop 47 when the cascade configuration bit CB1 is not set (has value 0). When the cascade configuration bit CB1 is set (to value 1), indicating a cascade mode for the macrocell 40, the multiplexer 57 will give the flip flop 47 reset input line 58 a static low signal. The various configuration bits CB1, CB2, CB3 are set conventionally via fuses, antifuses, memory cells, EPROMs, EEPROMs, or the like.

When the cascade control bit CB1 is not set (i.e., non-cascade mode), multiplexer 48 directs the signal from the OR gate output line 49 to the D input of flip flop 47. When the cascade control bit CB1 is set to implement cascading, multiplexer 48 redirects the signal from product term line 42 to the D input of flip flop 47 to provide the flip flop data signal and therefore preserve the use of flip flop 47.
In accordance with one embodiment, the three programmable multiplexers 48, 51 and 57 are controlled by one configuration bit CBl. In other embodiments, these multiplexers are independently controlled by separate configuration bits. Of course, when a multiplexer receives a constant input signal, as provided in multiplexers 51 and 57 of Fig. 4, it can be implemented by a logical equivalent such as a 2-input AND gate.

Setting the cascade bit CBl causes multiplexer 51 to direct the output signal of OR gate 49 along the DOUT line which connects to the input line of OR gate 52 in adjacent macrocell 53. Thus, the effect of setting the cascade configuration bit CBl is to enable the OR gate cascade feature and reclaim flip flop 47 with the dedicated product term signal of line 42. Although the cascade mode sacrifices the reset capability of the flip flop 47, a known value is entered in the flip flop when the device is first powered up, enabling the user to load the flip flop in the cascade mode by a signal on the product term line 42. There is provided a conventional circuit (not shown) that forces either a set or a reset into the flip flop during one cycle of the configuration loading sequence upon power up.

The effect of setting the cascade bit CBl on the macrocell 40 of Fig. 4 is shown in the equivalent circuit of Fig. 5. The OR gate output line 49 of the cascaded macrocell 40 (macrocell 40 for which the cascade bit CBl is set) is cascaded into the OR gate 52 of an adjacent macrocell 53 by means of multiplexer 51 of Fig. 4. Signals on dedicated product term line 42 are directed from the flip flop reset input by multiplexers 48 and 57 of Fig. 4, providing a data signal to the flip flop D input. Thus, as shown in Fig. 5, the effect of cascading reclaims the flip flop 47 without "stealing" an OR gate product term signal from lines 43, 44, 45, 46.

By multiple cascading through adjacent macrocells, this macrocell enables an arbitrary number of product terms to be logically combined, thus providing the user with the ability to program logical functions of arbitrary complexity. In
some embodiments, the cascading circuitry may provide that
either of two connected macrocells may be configured to be
downstream of the other. Such embodiments are not shown in a
figure. One additional input per OR gate gives this option.

In another feature (see Fig. 4), multiplexer 64 selects
between two external clock input signals Global CLK0 and
Global CLK1 to clock the flip flop 47. Multiplexer 64 is
controlled by the clock select control bit CB2. The
embodiment of Fig. 4 shows a choice of two global clock
signals. In another embodiment one clock signal can be
derived from a product term output signal as was done in Fig.
3. Implementing clock selection at the flip flop eliminates
the delay incurred by including multiplexers 30 or other
circuit elements in the speed path of product terms, as in
the prior art Fig. 3 macrocell.

In one embodiment, the output signal Q of the flip flop
47 on line 65 is inverted by a conventional inverter 66. The
inverted output signal from inverter 66 is then directed to a
conventional chip pad output circuit (not shown) and the
universal interconnect matrix (UIM, not shown here, see 5 in
Fig. 1). In another embodiment, the inverted output signal Q
is used as the chip pad output signal. Inversion of the
output signal allows fast active-low signals to be generated.
This is consistent with many signals on other devices such as
chip enables that tend to be active-low.

At the transistor level, signal transit time is
decreased further by novel multiplexer and flip flop
circuits. Fig. 6 is a circuit diagram of a prior art
multiplexer 67 and associated flip flop 67.1. The control
bit CB (inverted and non-inverted respectively) controls the
gates of two transistors 68 and 69, thereby selecting among
two input lines 70 and 71. Transistor 72 is controlled by a
master latch clock signal CKM allowing the selected signal to
be stored by master latch 73. Slave clock signal CKS,
controlling the gate of transistor 74, allows the stored
signal to pass through to the slave latch 75.

A novel multiplexer and flip flop in accordance with one
embodiment of the present invention is shown in Fig. 7a with
most elements identical to the corresponding elements of
Fig. 6. The multiplexer 76 is used for multiplexers 48, 51,
57, 64 in Fig. 4. The flip flop 76.1 is used for the flip
flop 47 of Fig. 4. In the multiplexer 76 composite signals
CB•CKM and CB•CKM, formed, for instance, by the logic circuit
of Fig. 7b using two NOR gates, (where • denotes the logical
AND operation) control the gates of two transistors 77 and
78, selecting between the two input lines 79 and 80. Latches
81, 82 and pass gate transistor 83 are identical to the
corresponding elements (respectively 73, 75 and 74) of the
prior art circuit of Fig. 6. Conventionally, the flip flop
clock signal is used to generate a clock signal CKM for the
master latch 81 and a clock signal CKS for the slave latch
82. By using the composite signals CB•CKM and CB•CKM to
control the gates of transistors 77 and 78, multiplexer 76
achieves the same function as does the prior art multiplexer
67 of Fig. 6 with reduced signal transit time, by eliminating
from the signal path the pass gate transistor 72 of Fig. 6.
In the embodiment of Fig. 4, static configuration bit CB of
Fig. 7b is the cascade control bit CBI.
Flip flop 47 of Fig. 4 (identical to flip flop 76.1 of
Fig. 7a) may be put into transparent mode by bypassing the
master latch of flip flop 47 with a passgate. In transparent
mode the flip flop simply passes the D input signal along as
an output without storing it. As shown in Fig. 7a, to
implement the transparent mode, either transistor 86 or
transistor 87 is turned on when configuration bit CBREG is not
set. Thus configuration bit CBREG when set to "0" prevents
the signal from master latch 81 from passing to slave latch
82 when slave latch clock signal CKS goes high. Otherwise,
with CBREG set at "1", flip flop 76.1 is in the storage mode
and passes the D input signal stored in latch 81 to latch 82
when clock signal CKS goes high.
When CBREG is not set, transistor 83 is turned off and
transistor 86 directs the signal on input line 79 of
multiplexer 76 through an inverter to the input terminal of
slave latch 82, or transistor 87 directs the signal on input
line 80 through an inverter to the input terminal of slave
latch 82. In the embodiment of Fig. 4, this feature gives
the user the added flexibility of not latching data into flip
flop 47 during the cascade mode, while using the redirectable
product term line 42 to pass signals to output line 65.

While the present invention is illustrated with
particular embodiments, it includes all variations and
modifications of the disclosed embodiments falling within the
scope of the appended claims. In particular, the
redirectable line used for the flip flop reset operation in
the non-cascaded mode may instead serve as a flip flop set
line, output enable line, or provide some signal other than
those that feed OR gate 41 of Fig. 4.
CLAIMS

We Claim:

1. A programmable logic circuit comprising:
   a plurality of input lines;
   a dedicated line;
   a flip flop having a flip flop data input terminal
   and a flip flop output terminal;
   a first logic gate receiving input signals from
   said plurality of input lines, said first logic gate
   having a first logic gate output terminal; and
   a cascade circuit having first and second
   programmable states, said cascade circuit connecting
   said first logic gate output terminal to said flip flop
   data input terminal when in said first programmable
   state, said cascade circuit connecting said first logic
   gate output terminal to an input terminal of a second
   logic gate and connecting said dedicated line to said
   flip flop data input terminal when in said second
   programmable state.

2. A programmable logic circuit as in Claim 1 in which
   said dedicated line serves as a flip flop reset signal when
   said cascade circuit is in said first programmable state.

3. A programmable logic circuit as in Claim 1 in which
   said dedicated line serves as a flip flop set signal when
   said cascade circuit is in said first programmable state.

4. A programmable logic circuit as in Claim 1 further
   comprising:
   a third logic gate having an output terminal;
   means for connecting said output terminal of said
   upstream logic gate to one of said plurality of input
   lines.

5. A programmable logic circuit as in Claim 4 in which
   said means for connecting said output terminal of said third
logic gate to one of said plurality of input lines and said
cascade circuit operate together to form a cascade circuit to
pass signals from said third logic gate to said second logic
gate.

6. The programmable logic circuit according to Claim
1, further comprising a clock selection circuit having a
clock output terminal, said clock selection circuit providing
a clock signal at said clock output terminal to a clock
signal terminal of said flip flop, wherein said clock signal
is programmably selected from a plurality of clock signals.

7. The programmable logic circuit according to Claim 1
further comprising an inverter connected to said flip flop
output terminal.

8. A programmable logic circuit comprising:
a plurality of input lines;
a dedicated line;
a first logic gate receiving input signals from
said plurality of input lines, said first logic gate
having a first logic gate output terminal;
a flip flop having a flip flop data input terminal,
a clock input terminal and a flip flop output terminal;
a first multiplexer having a control terminal and
two input terminals, the first input terminal connected
to said first logic gate output terminal, the second
input terminal connected to a reference level, said
first multiplexer having an output terminal connected to
an input terminal of a second logic gate;
a second multiplexer having a control terminal and
two input terminals, the first input terminal connected
to said first logic gate output terminal, the second
input terminal connected to said dedicated line, said
second multiplexer having an output terminal connected
to said flip flop data input terminal;
a cascade control circuit connected to the control
terminals of said first and second multiplexers, said
cascade control circuit having first and second
programmable states,
  said first programmable state:
    causing said first multiplexer to select said
    reference level, and
  causing said second multiplexer to select said
  first logic gate output line;
  said second programmable state:
    causing said first multiplexer to select said
  first logic gate output line, and
    causing said second multiplexer to select said
    dedicated line.

9. A programmable logic circuit as in Claim 8 in which
said first logic gate also receives input signals from an
output terminal of an third logic gate.

10. A programmable logic circuit as in Claim 8 further
comprising a third multiplexer having:
  a first input terminal connected to said dedicated
  line;
  a second input terminal connected to a reference
  voltage level;
  a control terminal connected to said cascade
  control circuit; and
  an output terminal connected to one of reset and
  set inputs of said flip flop;
where in said first state said control circuit connects said
dedicated line to said one of reset and set input of said
flip flop, and in said second state said control circuit
connects said reference level to said reset or set input of
said flip flop.

11. A structure for a programmable logic circuit
comprising:
  a plurality of macrocells each having:
product term input signals;
a logic gate which receives at least said
product term input signals and generates an output
signal therefrom;
a flip flop having an input terminal; and
a multiplexer having a first state and a
second state, wherein said first state directs said
output signal to said flip flop input terminal and
said second state directs another signal to said
flip flop input terminal and directs said output
signal to a logic gate of another macrocell as an
input signal thereof.

12. A structure for a programmable logic circuit as in
Claim 13 in which said another signal directed to said flip
terminal comprises a product term output signal
from an AND array.
FIG. 4
FIG. 5
### A. CLASSIFICATION OF SUBJECT MATTER

IPC(S) : H03K 19/177
US CL : 307/465

According to International Patent Classification (IPC) or to both national classification and IPC

### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 307/465, 465.1;
340/825.83, 825.85, 825.87

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS (output macrocell, set, reset, flip-flop)

### C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>X</td>
<td>US, A, 4,758,746 (Birkner et al.) 19 July 1988, Figure 4e, and cols. 3-4.</td>
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<td>US, A, 4,912,345 (Steele et al.) 27 March 1990, Figure 2.</td>
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<td>US, A, 4,933,577 (Wong et al.), 12 June 1990, col. 3, lines 45-47.</td>
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<td>US, A, 5,121,006 (Pedersen); 9 June 1992, col. 3, lines 1-12 and col. 4, lines 30-39.</td>
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☑️ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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