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Weeks, Jr. et al.

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[54] **MULTIFREQUENCY SEQUENTIAL TONE DECODER**

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[52] **U.S. Cl.** ..... **340/171 PF,** 340/171 R

[51] **Int. Cl.** **H04q 1/45**

[58] **Field of Search** ..... 340/171 PF, 171 R; 325/64

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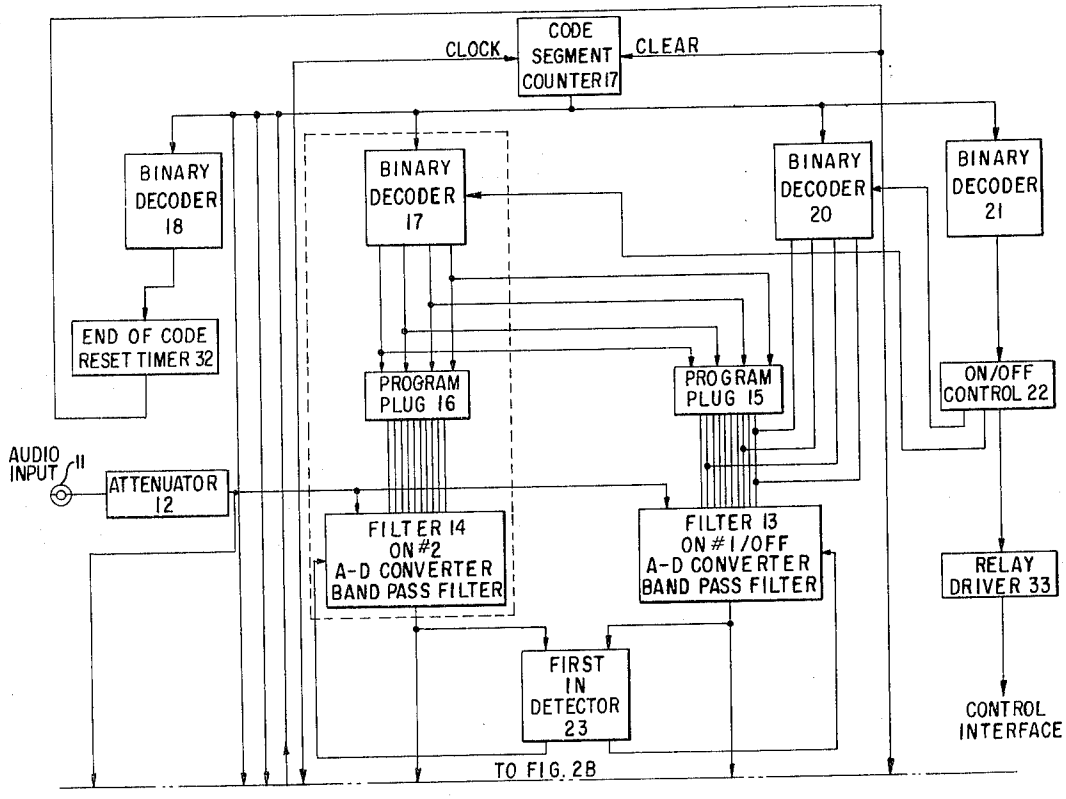
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Attorney, Agent, or Firm—Edward J. Kondracki

[57] **ABSTRACT**

A tone decoder incorporating a plurality of selectable bandpass filters, the frequencies of which are controlled by logic means responsive to the outputs of the filters is presented herein. The logic means are adapted to recognize a plurality of tone bursts having a predetermined duration and repetition rate and provide controlling voltage levels to an active filter providing a selectable one of a plurality of narrow bandpass frequencies in response to the selected voltage levels.

15 Claims, 11 Drawing Figures



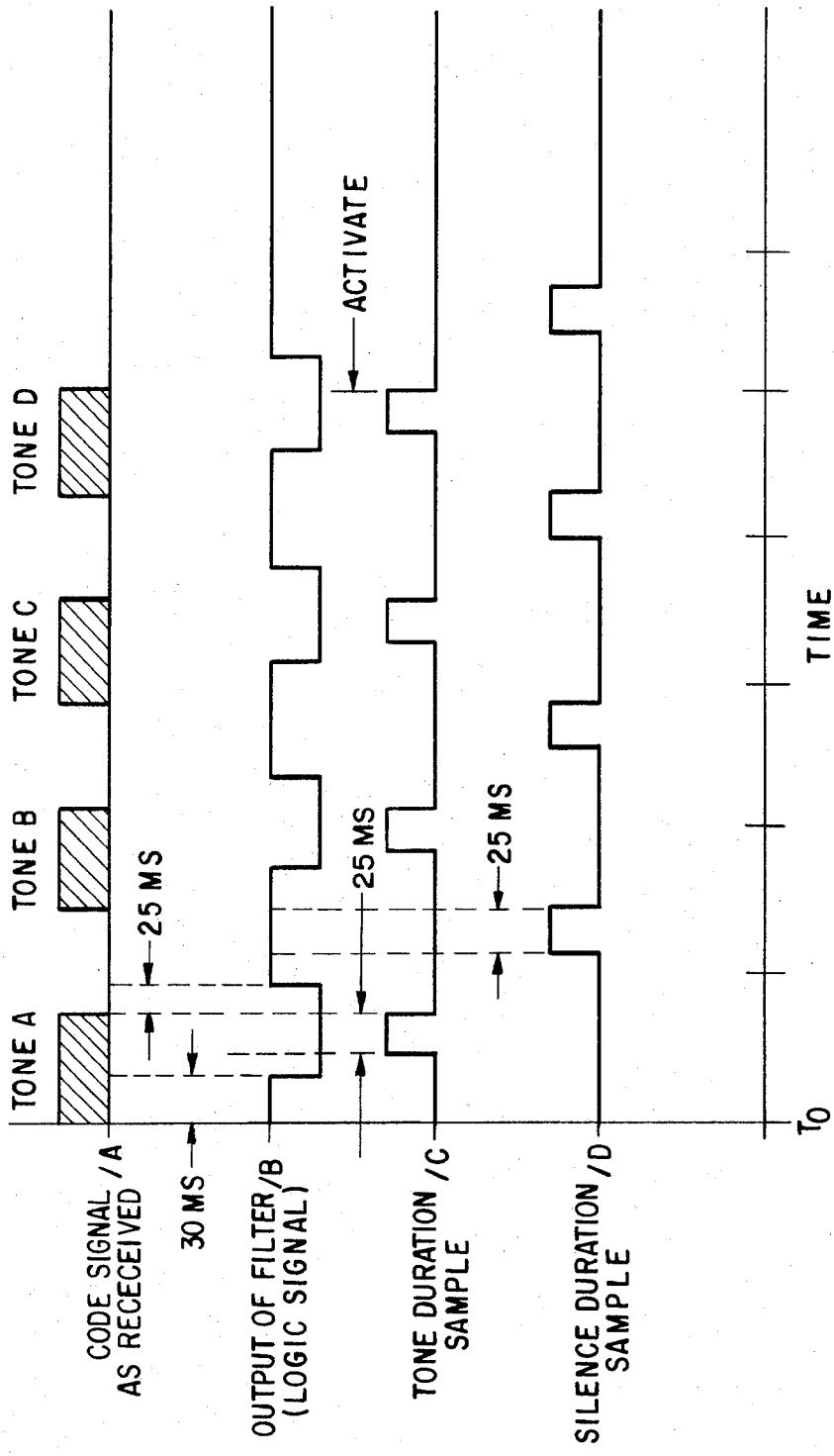

TONE A
TONE B
TONE C
TONE D
25 MS
30 MS
ACTIVATE
25 MS
25 MS
TIME
T0
CODE SIGNAL /A AS RECEIVED
OUTPUT OF FILTER /B (LOGIC SIGNAL)
TONE DURATION /C SAMPLE
SILENCE DURATION /D SAMPLE

FIG 1

FIG 2

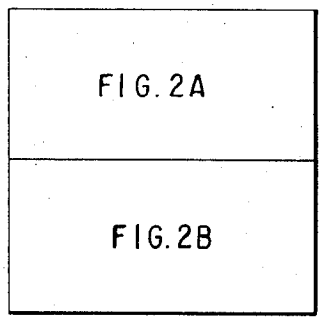


FIG 3

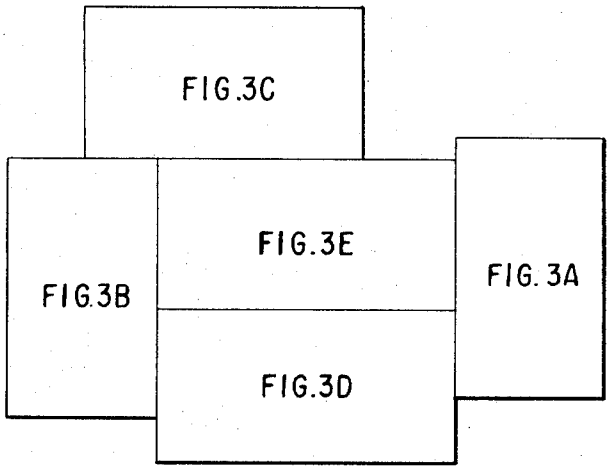
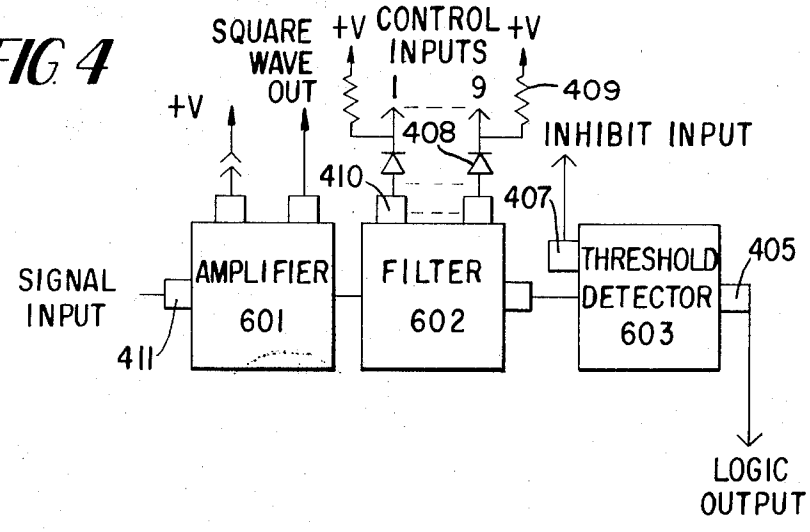


FIG 4



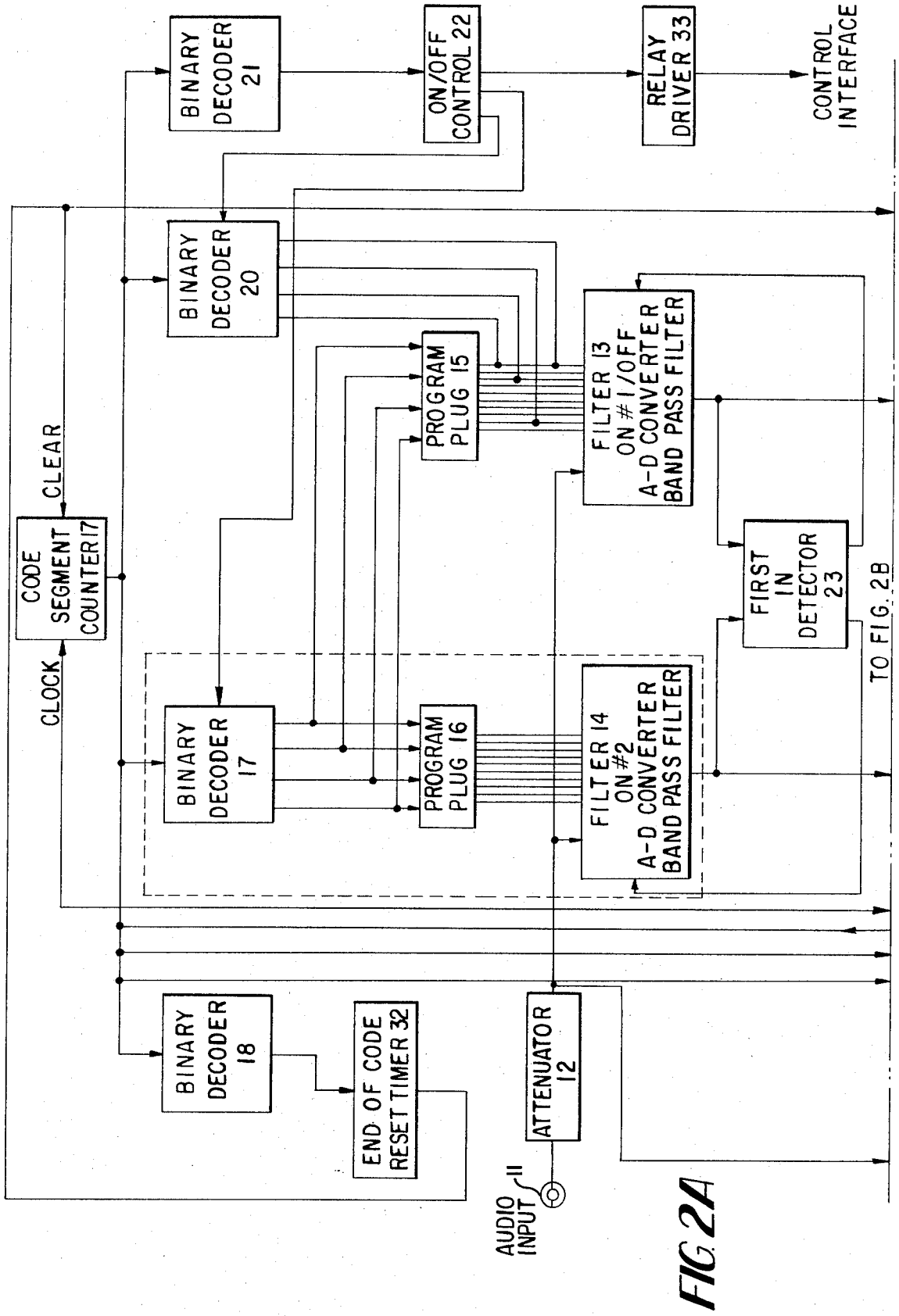

BINARY DECODER 21
ON/OFF CONTROL 22
RELAY DRIVER 33
CONTROL INTERFACE
BINARY DECODER 20
PROGRAM PLUG 15
FILTER 13 ON #1/OFF A-D CONVERTER BAND PASS FILTER
CLEAR
CODE SEGMENT COUNTER 17
FIRST IN DETECTOR 23
TO FIG. 2B
CLOCK
BINARY DECODER 17
PROGRAM PLUG 16
FILTER 14 ON #2 A-D CONVERTER BAND PASS FILTER
BINARY DECODER 18
END OF CODE RESET TIMER 32
ATTENUATOR 12
AUDIO INPUT

FIG 2A

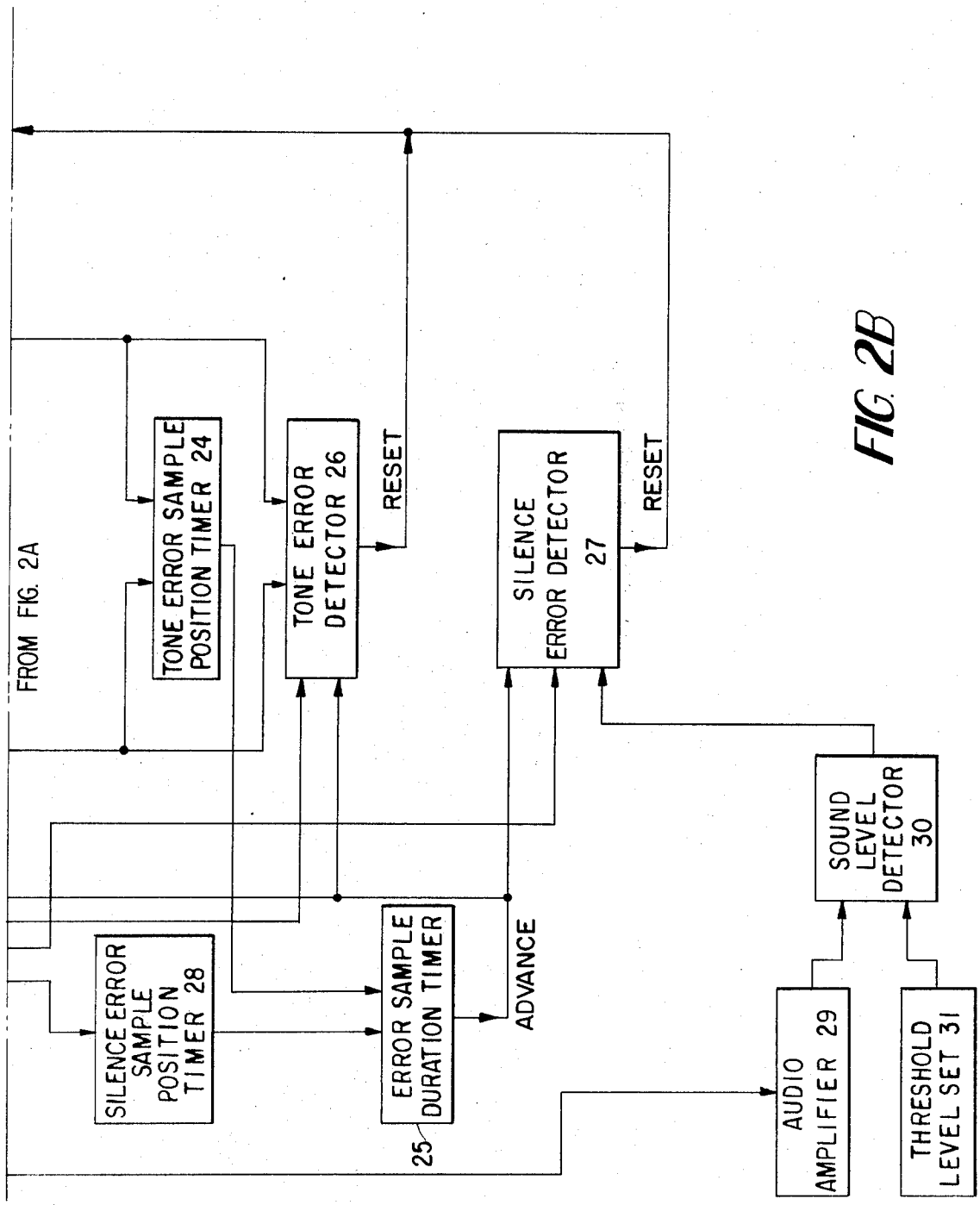
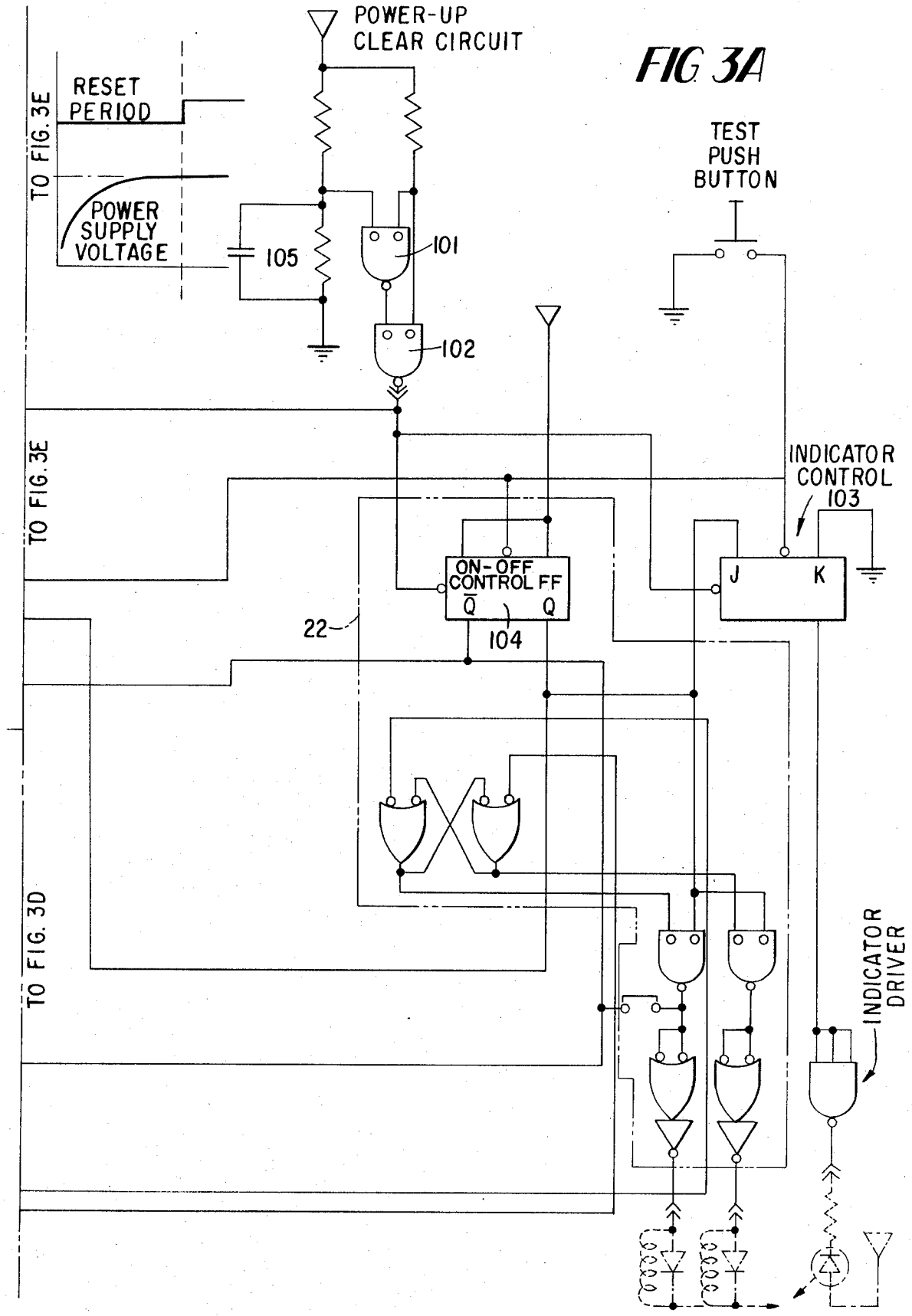

FROM FIG. 2A
TONE ERROR SAMPLE POSITION TIMER 24
TONE ERROR DETECTOR 26
RESET
SILENCE ERROR DETECTOR 27
RESET
SILENCE ERROR SAMPLE POSITION TIMER 28
ERROR SAMPLE DURATION TIMER
25
ADVANCE
SOUND LEVEL DETECTOR 30
AUDIO AMPLIFIER 29
THRESHOLD LEVEL SET 31

FIG. 2B

FIG 3A


POWER-UP
CLEAR CIRCUIT
RESET
PERIOD
POWER
SUPPLY
VOLTAGE
105
101
102
TEST
PUSH
BUTTON
INDICATOR
CONTROL
103
ON-OFF
CONTROL FF
Q
Q
104
J
K
22
INDICATOR
DRIVER
TO FIG. 3E
TO FIG. 3E
TO FIG. 3D

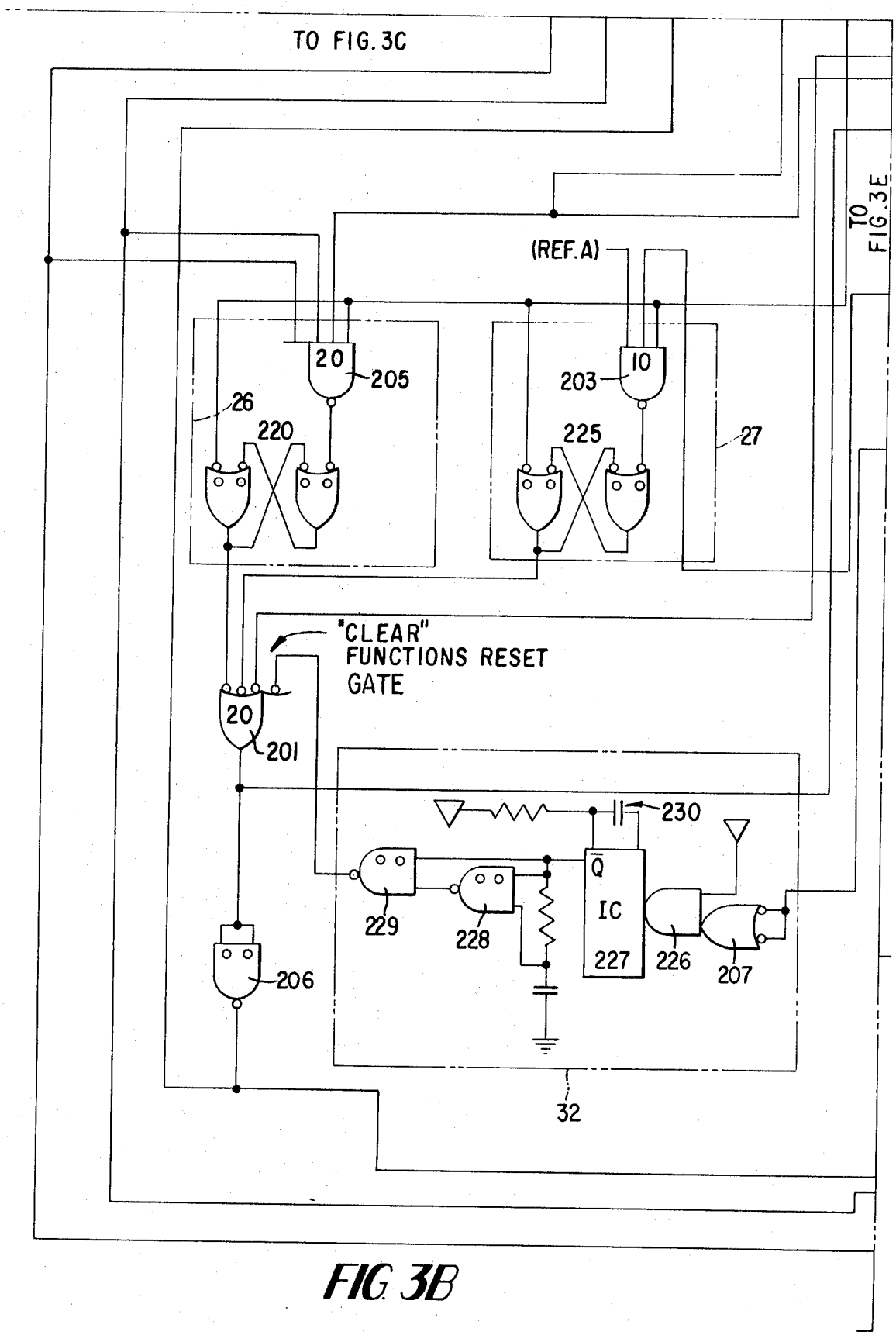
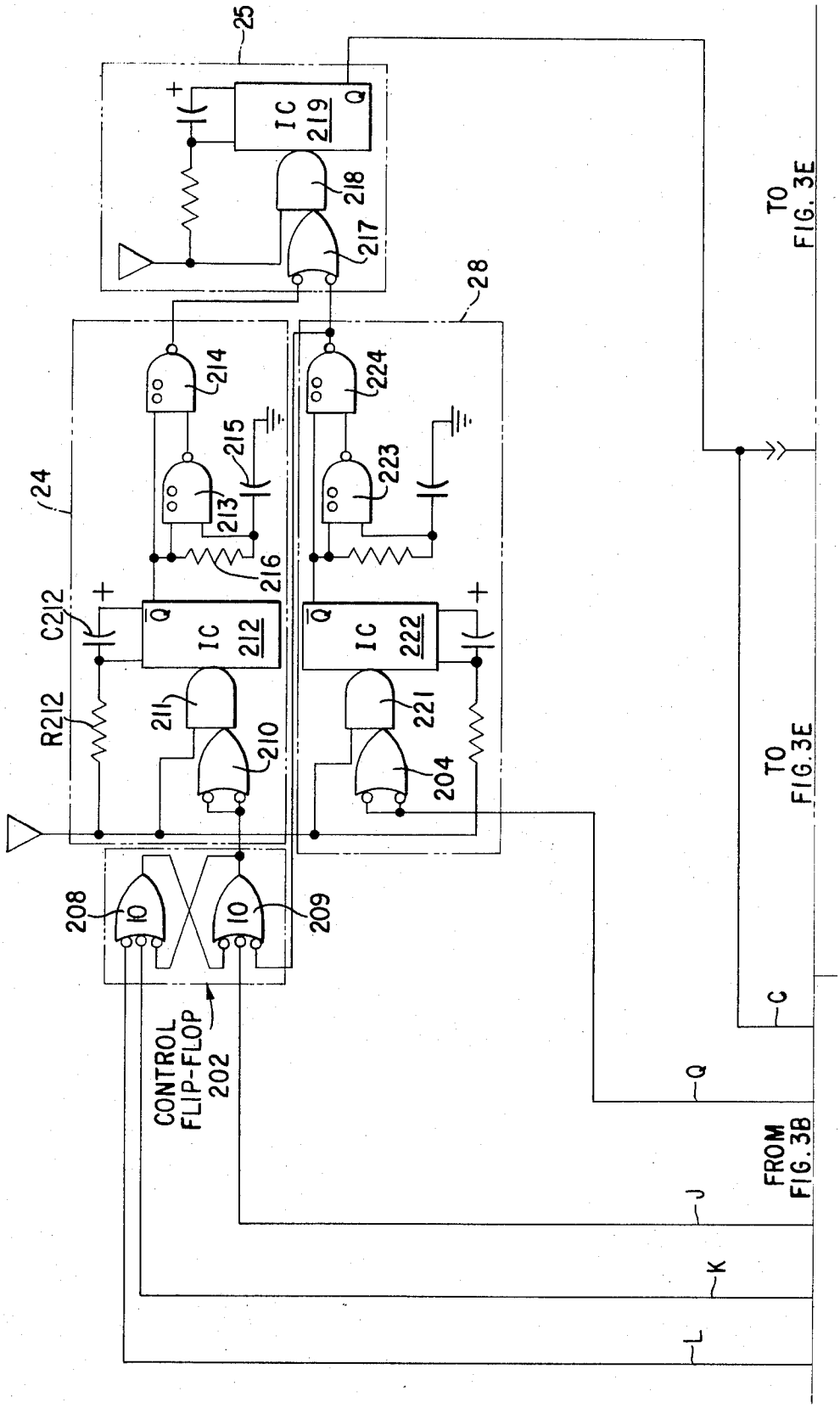

TO FIG. 3C
TO FIG. 3E
(REF. A)
20
205
26
220
10
203
225
27
"CLEAR"
FUNCTIONS RESET
GATE
20
201
230
229
228
Q
IC
227
226
207
206
32

FIG. 3B

FIG. 3C


25
IC 219
Q
218
217
28
214
224
215
213
223
216
24
C212
IC 212
IC 222
R212
211
221
210
204
208
209
CONTROL FLIP-FLOP 202
TO FIG. 3E
TO FIG. 3E
C
Q
FROM FIG. 3B
J
K
L

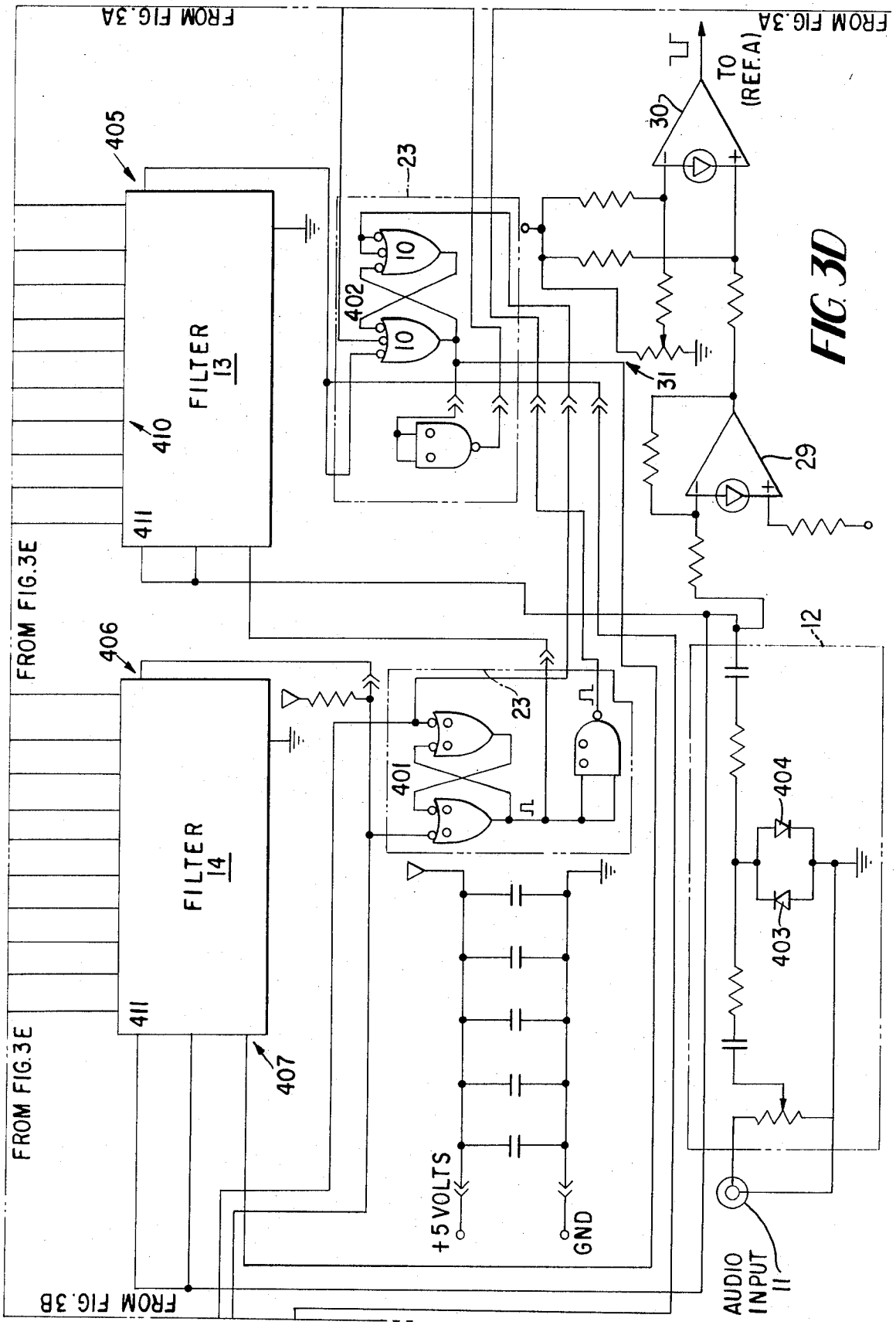
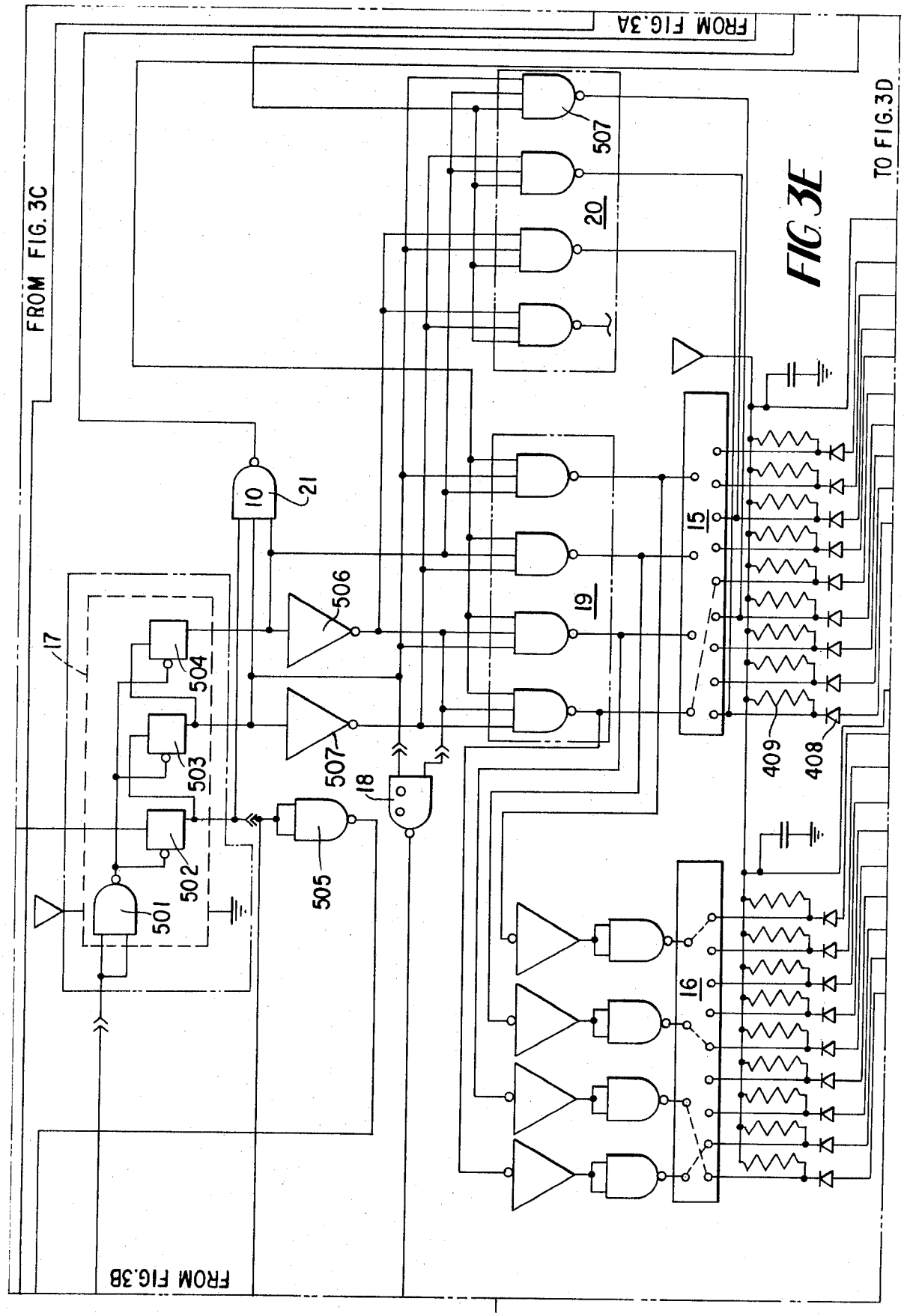

FROM FIG. 3A
FROM FIG. 3A
TO (REF. A)
30
405
23
FILTER 13
410
411
402
10
10
31
29
FROM FIG. 3E
406
FILTER 14
411
23
401
12
404
403
407
+5 VOLTS
GND
FROM FIG. 3E
FROM FIG. 3B
AUDIO INPUT 11

FIG. 3D


FROM FIG. 3A
FROM FIG. 3C
TO FIG. 3D
FROM FIG. 3B
FIG. 3E
10
21
17
18
19
20
15
16
501
502
503
504
505
506
507
507
507
408
409

MULTIFREQUENCY SEQUENTIAL TONE DECODER

BACKGROUND OF THE INVENTION

A need exists for providing reliable control signaling utilizing audio tones in a broadcast medium dominated by random audio tones. This need is generated by the necessity for automatically turning on or off various automated systems in response to standard radio and TV audio transmissions. Such an automated system is described, for example, in U.S. Pat. No. 3,729,581, assigned to the assignee of this invention. The conventional approaches to the problem have been to incorporate elaborate decoders which constantly moniter audio programs to detect codes comprised of unique tone burst sequences. These approaches incorporated separate and distinct bandpass filters for each different frequency of interest. Since the cost of the filters exhibiting acceptable tolerances is relatively great, the systems cannot be used in average non-commercial applications due to their total cost considerations.

Because of the various disadvantages associated with existing audio tone decoders, a need has arisen for a multifrequency sequential tone decoder which will provide reliable control signaling utilizing audio tones in a broadcast medium dominated by random audio tones. The required system must be relatively maintanence free and highly resistent to erroneous responses but at the same time it must be relatively economical to produce. These objectives are accomplished by the invention disclosed herein.

Another objective of this invention is to provide a reliable and stable filter capable of providing a digital output for a selected frequency, wherein the selected frequency may be changed during the course of decoding.

An additional objective is to provide an apparatus which will be relatively insensitive to background noise and tone bursts which meet basic tone code criteria but are too short or too long and are actually random audio tones normally encountered during the course of monitering a broadcast.

An additional objective is to provide a tone responsive decoder which is responsive to several codes.

Other objectives, features and advantages of the presented invention will become apparent from the following description taken in conjunction with the accompanying drawings.

SUMMARY OF THE INVENTION

The multifrequency sequential tone decoder presented by this patent accomplishes the aforestated objectives by providing a reliable decoder for control signaling utilizing audio tones in a broadcast medium dominated by random audio tones. The control tones to which the invention is responsive are broadcast via standard radio and TV audio, and the contemplated use of the system necessitates that the decoder constantly monitor program audio signals consisting of tones having the same basic makeup as the coded audio control tones. Therefore, the code format must be complex enough to preclude the possibility of duplication by music, speech, or any other program audio normally encountered, but simple enough to be highly reliable.

The tone decoder rejects all random audio programming but responds immediately when a proper code is received. This is accomplished by using active, semiconductor bandpass filters which have a high Q and can be electronically switched to pass different frequencies. They are incorporated in a decoder design which provides electronic switching to enable a single active filter to be responsive to different discrete frequencies in accordance with a timed code.

The transmitted code signals which the system is responsive to consists of a number of tone bursts, each being made up of one unique discrete pure sinusoidal frequency. The frequencies utilized are in the medium audio range to enable most home entertainment receiving equipment to easily accommodate their bandpass. The number of tones that may be utilized by the invention is practically limitless, however, for simplicity of presentation, the system described is considered responsive to **4** tones each of which is considered as an individual digit tone. The tones are discrete frequencies which are considered decade digits, that is **10** different frequencies provide **10** digits.

Each digit tone is transmitted for a predetermined length of time and each digit frequency is transmitted for the same period of time. The transmission is followed by a period of silence which is of a constant duration in all instances. This enables the system to decode the signal by first verifying the frequency of each tone segment, second determining the duration of each tone segment, third determining the existance of a period of silence and forth determining the minimum duration of the period of silence.

The duration of the time checks performed by the system as indicated above, is determined by the width of an error sample pulse, which is generated by the same timing circuitry, and is of the same duration. The position of the error sample pulse within the tone segment is determined by a tone error sample position timer and the position of the error sample within the silence segment is determined by a silence error sample position timer. The tone error sample position timer is initiated by the first response of the tone filters, while the silence error sample position timer is initiated at the conclusion of the tone error sample period. This permits the decoder timer to be asynchronous.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a timing chart illustrating the time durations utilized in determining the validity of a code.

FIG. **2** is a diagram showing the layout interconnections for FIGS. **2A** and **2B** which when combined present the multifrequency sequential tone decoder described by this patent.

FIG. **3** is a diagram showing the layout interconnections for FIGS. **3A** through **3E** which combined present a detailed schematic and logic diagram of the multifrequency sequential tone decoder.

FIG. **4** is block diagram of the selectable bandpass filter.

DETAILED DESCRIPTION

FIG. **1** illustrates the timing functions utilized by a tone decoder **10** to ascertain the validity of a received code. The pulse train **1***a* represents the code signal received. In the exemplary embodiment it is a pulse train of four independent tone bursts. The four tone bursts are decoded by the system which is represented by the block diagram presented in FIGS. **2A** and **2B** as follows. The first received code signal Tone A, is applied

to audio input jack **11** which couples the tone to attenuator **12.** The attenuator **12** reduces the amplitude of the input tone to a minimum level and simultaneously applies it to filters **13** and **14.** In this embodiment, the system is configured so that filter **13** responds to a first ON code and to the OFF code and filter **14** responds to a second ON code. Additional codes may be accommodated by providing additional filters in combination with additional binery decoders. However, for simplicity only two filters are illustrated.

Filters **13** and **14** have a very narrow bandpass at a plurality of discreet frequencies but they pass only one frequency at a time. The frequency they will pass at a given instant is a function of the voltage levels on the plurality of inputs from the program plugs **15** and **16,** in other words bandpass frequency control is provided by program plug **15** for filter **13** and by program plug **16** for filter **14.** The filters **13** and **14** function as analog-to-digital converters for the specific frequency to which they are selectively made responsive to. In their quiescent state they provide a logical one output, but upon passing the preselected frequency their output changes to a logical zero and will remain at that level as long as the frequency is present.

In the quiescent state, the code segment counter **17** and binary decoders **18, 19, 20** and **21** are in a reset state, and filters **13** and **14** are set to respond to the first digital frequency of the code. This frequency is determined by the interconnections provided by the program plugs **15** and **16** as previously described.

Considering the exemplary case, the code segment counter **17** and the binary decoders **18, 19, 20** and **21** are reset and the ON-OFF control **22** is in the OFF position, both filters **13** and **14** are OFF and listening for an ON code. When Tone A arrives, filter **13** passes it and applies a logic zero to the first in detector **23** which immediately disables the other filter **14.** Simultaneously, the logic zero is applied to the tone error sample position timer **24.** At the end of a predetermined time, the tone error sample position timer **24** triggers the error sample duration timer **25.** After 25 ms, the error sample duration timer **25** switches to its quiescent state which causes the counter **17** to step one count. When the error sample duration timer **25** was triggered, it produced a positive output which lasted for 25 ms, as shown in FIG. **1C.** This signal was applied to both the tone error detector **26** and the silence error detector **27.** However, the tone error detector **26** is the only one which will respond to an error at this time because the silence error detector **27** is disabled during a tone check; this condition is set by the output of the first stage of the code segment counter **17** and an inverter.

If the logic zero output of filter **13** stops during this **25** ms period, the tone error detector **26** will generate a reset signal which will last until the end of the 25 ms period. Assuming Tone A is of long enough duration to persist for the 25 ms test period, the counter **17** steps one count as stated earlier. When the code segment counter **17** steps ahead one count, the counter's **17** output inhibits the tone error detector **26,** enables the silence error detector **27** and triggers the silence error sample position timer **28.** At the end of a predetermined time, the silence error sample position timer **28** triggers the error sample duration timer **25.** The error sample duration timer **25** produces a **25** ms positive pulse which enables the silence error detector **27** and steps the counter **17** with its trailing edge.

When the tone was initially received at the audio input jack **11,** the attenuated signal output of attenuator **12** was applied to audio amplifier **29** which in turn applied its output to sound level detector **30.** Sound level detector **30** compares the output of audio amplifier **29** with a level determined by threshold level set **31.** When the audio signal applied to sound level detector **30** exceeds the threshold set by threshold level set **31,** it provides a logic zero output. This output is applied to the silence error detector **27** and if it is present during the duration of the silence error sample pulse, illustrated by wave form **1D,** FIG. **1,** it causes the silence error detector **27** to generate a reset pulse which has the same effect as described for the reset pulse generated by tone error detector **26.**

If the tone is a valid tone, the silence error detector **27** will not reset the counter **17** and it will be stepped one count by the trailing edge of the error pulse output of the sample duration timer **25.** The code segment counter **17** now inhibits the silence error detector **27** and enables the tone error detector **26.**

Binary decoder **18** triggers the end of code reset timer **32** which will reset the code segment counter **17** at the end of a predetermined time to provide functions which will be discussed later.

Binary decoder **19** changes the frequency select control for filters **13** and **14.** In the examplary case it changes filter **13** to be responsive to Tone B. This is a function determined by the wiring of the program plugs **15** and **16.** Filter **13** is now responsive to the second discrete frequency of the code.

The previously described sequence repeats itself, as filter **13** responds to the second tone, the tone error sample position timer **24** determines the time at which the error sample duration timer **25** begins the tone error sample test, by generating an advance pulse signal (as shown in FIG. **1C**) whose trailing edge of the pulse steps the code segment counter **17** one step to initiate the silence error sample position timer **28** which determines the beginning of the silence segment test. When the code segment counter **17** advanced one step, the tone error detector **26** was inhibited and the silence error detector **27** was enabled. If no error is detected by the silence error detector **27,** it steps the code segment counter **17** and the filter (**13** or **14**) is set to respond to Tone C.

As the tones are stepped through the decoder, the error sample for the final tone is eventually generated. At the end of that error sample test the code segment counter **17** is advanced to its capacity. Capacity loading of the code segment counter **17** is detected by binary decoder **21** which operates the ON-OFF control **22** to the ON position. When the ON-OFF control **22** is activated to the ON position, it energizes relay driver **33** which operates an external relay device. In addition to activating relay driver **33,** the ON-OFF control **22** disables binary decoders **19** and **20** to prevent the filters from responding to any code programmed by either program **15** or **16** and to therefore respond only to a predetermined, preprogrammed code which is established by the wiring between binary decoder **20** and filter **13.** This later function is a special case for providing a specific OFF code. In general, however, the OFF code may be programmed in a manner similar to that presented for the ON code.

Also, additional binary decoders similar to binary decoder **20** may be provided to allow the use of additional OFF codes.

The end of code reset timer **32** mentioned previously began its timing cycle at the end of the first silence error sample test. It generates a reset pulse shortly after the last tone pulse of a given code format. The purpose of the reset timer **32** is to reset the various elements of the tone decoder **10** in the event of an incomplete code. For instance, in a case where one or more tone bursts detected by the tone decoder **10** correspond to the set codes of the decoder **20,** its counter **17** will step forward until a proper tone burst is not detected by one of the filters **13** and **14.** In this case, rather than allow the decoder **10** to remain in a partially decoded status, the end of code reset timer **23** will time out and reset the decoder **10.**

If the tone detected by the tone decoder **10** is not a valid code, the code segment counter **17** and first in detector **23** are placed in a reset state. For instance assume a proper frequency tone burst is detected but the tone burst is shorter than required. The tone decoder **10** responds to the frequency of the random signal as if it were the first frequency of a valid code. This results in the generation of an error sample pulse at the appropriate time. However, since the duration of the random signal is not long enough, the tone error detector **26** produces an error signal which immediately resets the code segment counter **17** and the first in detector **23.** This causes filters **13** and **14** to be responsive again to the initiate first tone of a valid code.

If a random signal equal to the first tone digital frequency is detected by the decoder **10** but the tone burst is too long, the first in detector **23** cuts off the opposite filter and a first tone error sample is generated, found to be satisfactory, and the position of the first silence segment error sample is determined. When the error sampling takes place, the silence error detector **27** will detect the absence of silence, and the code segment counter **17** and the first in detector **23** will immediately be reset.

If a random tone satisfies a digit frequency requirements but is accompanied by other frequencies, an error will be generated during the silence segment checks due to the presence of the other frequencies.

If a random signal is such that the first tone segment and first silence period are verified and considered acceptable, the tone decoder **10** is placed in a listening mode waiting for the second tone frequency which will not be received. In this case the first silence error sample and it generated and it causes the end of code reset timer **32** to begin timing out. When the end of code reset timer **32** times out, it resets the code segment counter **17** and first in detector **23** as previously discribed.

The detailed functioning of the system can best be comprehended by considering FIGS. **3A** thru **3F** which illustrate the total system in detail.

When power is initially applied, the power up clear circuit comprised of gates **101** and **102** illustrated in FIG. **3** produces a logic zero output which resets indicator control flip-flop **103** and ON-OFF control flip-flop **104.** This signal is also applied to the clear functions reset decoder **201** of FIG. **3B** which resets the control flip-flop **301** of FIG. **3C,** the first in detector flip-flop **401** and **402** of FIG. **3B** and the code segment counter **17** via reset NAND gate **501** of FIG. **3E.** Decoders **19** and **20** of FIG. **3E** are reset by outputs from flip-flop **104** at this time.

Returning to the power-up clear circuit of FIG. **3A,** gates **101** and **102** are inverted NAND gates so when power is initially applied, one input to gate **101** is positive or logic one and the other is logic zero until the RC time circuit **105** charges. Therefore, the initial output of gate **101** is zero. The inputs to gate **102** are initially logic one from the power supply and logic zero from gate **101.** When the RC time constant **105** is charged, both inputs to gate **101** are positive and the gate produces a logic one which causes gate **102** to produce a logic one since both of its inputs are now positive. This removes the reset or clear from the various circuits previously set and the decoder is ready to process incoming tones.

When the tone decoder **10** has been reset and is ready to process incoming tones, all the inputs to the clear functions reset gate **201** are at a logic one and since it is an inverted NOR gate its output is a logic zero. NAND gate **501** is at logic zero and the outputs of stages **502, 503** and **504** are respectively zero, zero, zero. The logic zero from stage **502** is applied to one input of inverted NAND gate **203** of the silence error detector **27,** holding that gate off. The logic zero is also applied to an inverter **505** which applies a logic one to NOR gate **204** of the silence error sample position timer **28** to inhibit that circuit and to inverted NAND gate **205** thus enabling the tone error detector **26.**

The logic zero from the clear functions reset gate **201** is applied to inverter **206** which applies a logic one to the reset inputs of inverted NOR gate flip-flop **401** and **402** of the first in detectors and inverted NOR gate flip-flop **202.**

The logic one output of stage **503** is applied to one input of decoder **18** which is an inverted NAND gate. The other input to decoder **18** is a logic one from amplifier **506** which inverts the output of stage **504.** This causes decoder **18** to produce a logic one which is applied to NOR gate **207** to hold the end of code reset timer off.

The output of error sample duration timer **25** is at a logic zero and the output of end of code reset timer **32** is at a logic one.

When no signal or an improper tone is received and the tone decoder **10** has been reset as previously described, the output terminals **405** and **406** of filters **13** and **14** are at a logic one level. These terminals are connected to the first in detector flip-flops **402** and **401** respectively and to two inputs of control flip-flop **202.**

With the logic set as previously described, the decoder is ready to process a tone of a frequency to which the filters **13** and **14** are set.

The attenuator **12** of FIG. **3B** functions as a limiter as well as an attenuator through the action of diodes **403** and **404.** It provides signals having a predetermined maximum value to audio amplifier **29** and filters **13** and **14** of FIG. **3D.**

To follow the operation of the decoder, assume a tone is received that is the same frequency as filter **13:**

Output terminal **405** of filter **13** assumes a logic zero level immediately and remains at that level as long as the tone persists. The logic zero is sensed by flip-flop **402** and it responds by assuming a logic one output which is applied to inhibit terminal **407** of filter **14.** With a logic one at terminal **407,** filter **14** is cut-off and will not respond to any tone frequency.

The logic zero at terminal **405** is sensed by control flip-flop **202** of FIG. 3C causing inverted NOR gate **208** to go to a logic zero which shifts inverted NOR gate **209** to a logic zero. The logic zero at gate **209** causes NAND gate **210** to assume a logic one and trigger AND gate **211.** AND gate **211** triggers circuit **212** which provides a **25** ms logic zero pulse to inverted NAND gates **213** and **214.** The output of circuit **212** is a logic one in its quiescent state so gates **213** and **214** are normally at a logic one level. When the output of circuit **212** drops to zero, gate **213** assume a logic zero. The discharging of capacitor **215** is prevented from delaying this action by resistor **216.**

Prior to circuit **212** developing a negative pulse at its $\overline{Q}$ terminal, the output of NAND gate **213** is at a logic zero because both inputs are at a logic one. This logic zero output of **213** ensures that the output of NAND gate **214** is at a logic one even though input A is at a logic one. Immediately, as the one-shot monostable circuit, **212,** produces a logic zero at output $\overline{Q}$, the control of NAND circuit **214** changes from input B to input A and the output remains at a logic one. The output of NAND gate **214** changes only as the $\overline{Q}$ output of circuit **212** changes from a logic zero to a logic one. When this ooccurs, the A input of NAND gate **214** immediately changes to a logic one, but the B input does not satisfy the gate until the output of NAND gate **213** switches to a logic one also. This happens at a point in time determined by the RC network consisting of resistor **216** and capacitor **215.** The B input of NAND gate **213** exceeds the positive threshold level only after capacitor **215** changes through resistor **216.** Thus, the output of NAND gate **214** remains unchanged as $\overline{Q}$ of **212** changes from logic one to logic zero but switches to logic zero immediately as $\overline{Q}$ of **212** returns to logic one; the length of time it cotinues to be a logic zero is determined by the time-constant. When gate **214** assumes a logic zero. NOR gate **217** assumes a logic one which trigers AND gate **218.** AND gate **218** sets circuit **219** which is similar to circuit **212,** but the output is taken from the inverted output Q, thus generating a logic one.

This change is sensed by NOR gate **217** and it changes to a logic zero, changing the state of AND gate **218** which causes circuit **219** to produce a **25** ms logic one pulse at its output terminal.

As shown in FIG. 3E, the logic one is applied to stage **502** of counter **17** but this circuit is similar to **219** in that an output is produced only at the termination of the input pulse so the counter does not step. The logic one is also sensed by inverted NAND gate **205** of the tone error detector **26.** This gate now has a logic one input from **219** of error sample duration timer **25,** terminal **406** of filter **14** and NAND gate **505.** It is held in the logic one state by the logic zero from terminal **405** of filter **13.** If the tone stops while the gate is in this state, it will cause gate **205** to assume a logic zero state, which will cause inverted NOR gate flip-flop **220** to assume a logic zero. This changes the clear function reset gate inverted NOR gate to a logic one and the decoder is reset as described for the power-up clear sequence except that the reset logic levels are held until the logic one of **219** of the error sample duration timer **25** shifts to a logic zero. Thus the counter **17** is prevented from stepping and the system is again set to receive a tone.

Coincidentally, the logic one of error sample duration timer **25** is applied to inverted NAND gate **203** of the silence error detector **27** of FIG. **3B** but that gate is held in the logic zero state by the logic zero from stage **502** of the code segment counter **17.**

Assuming the tone lasted until circuit **219** of the error sample duration timer **25** shifted to a logic zero, stage **502** is stepped, shifting its output to a logic one. This zero is applied to stage **503** but has no effect in that the stages of the code segment counter **17** are all similar and only step at the termination of a logic one. The logic one of stage **502** is also applied to one input of inverted NAND gate **203** to enable the silence error detector **27** and to gate **505.** This changes gate **505** to a logic zero and inhibits inverted NAND gate **205** of the tone error detector **26.**

The logic zero at the output of gate **505** is sensed by NOR gate **204** of the silence error sample position timer **28** of FIG. 3C. This NOR gate **204** changes to a logic one and AND gate **221** triggers circuit **222** to operate **204** inverted NAND gates **223** and **224** in a fashion identical to the similar circuitry of the tone error sample position timer **24** which was previously presented. When gate **224** changes to a logic zero, the level is applied to one input of inverted NOR gate **209** to reset flip-flop **202.** This sequence is identical to the sequence which caused circuit **219** to produce a logic one at its output.

The logic zero of gate **224** is also applied to NOR gate **217** of the error sample duration timer **25.** The function is similar to that explained for the tone error position timer **24** sequence. Hence the error sample position timer developes a 25 ms logic one pulse at the output of circuit **219,** 30 MS after the 25 ms logic one pulse developed in response to the tone error sample position timer **24** ends.

This logic one pulse is applied to both inverted NAND gates **203** and **205** as before, but now gate **203** is enabled by the logic one from stage **502** and gate **205** is inhibited by the logic zero from gate **505.**

Inverted NAND gate **203** of the silence error detector **27** in a three input device. Two of the inputs are now at a logic one level and the third is provided by sound level detector **30.**

As shown in FIG. 3A, sound level detector **30** is a differential amplifier which receives one input from audio amplifier **29.** Audio amplifier **29** is driven by the output of attenuator **12,** which is the same signal that is applied to filters **13** and **14.** The output of the amplifier is compared by the sound level detector **30** with a voltage level set by threshold level set **31** and applied to its negative input. When the audio input to sound level detector **30** is less than the threshold level set value, the detector produces a negative output or a logic zero. When the audio is greater than the threshold level set value, the detector produces a logic one.

Therefore, if a significant tone is being received, the third input to inverted NAND gate **203** of FIG. **3B** is logic one. This causes gate **203** to change from a logic one to a logic zero and trigger the inverted NOR flip-flop **225.** This changes its output to a logic zero which causes clear function reset decoder **201** to shift from a logic zero to a logic one and the tone decoder **10** is cleared as previously described for the tone error detector **26.**

Assuming the output tone received is proper and therefore ended and no other tone greater than the level set value is present, the output of the sound level detector **30** will be a logic zero and gate **203** will not change state. In this case, when the logic one output of

circuit **219** ends, it steps stage **502** of the code segment counter **17.** The output of stage **502** goes to a logic zero and steps stage **503** which goes to a logic zero. Stage **504** is not affected for reasons previously discussed with respect to the first setting of stage **503.** The logic zero at **502** inhibits gate **203** and enables gate **205** via gate **505** as previously explained with respect to the status of the logic when the decoder is waiting for a tone. The decoder **10** is ready to repeat the previously described sequence if a tone arrives. However, the logic zero status of code segment counter stage **503** has shifted the inputs to decoders **19** and **20.**

Initially all eight NAND gates which form decoders **19** and **20** were 3A in at a logic one. This can be determined by inspection of FIG. 3a in consideration of the logic status of the decoder after the power-up clear cycle as previously presented. Therefore, the unselected control input through program plugs **15** and **16** and directly to filter **13** from decoder **20** are at a logic one. The diode **408** and resistor **409** to Vcc on each control input to the filters **13** and **14** cause the actual input to be isolated at a high voltage.

Filter response frequency selection is made by driving a selected one out of the nine inputs to each filter to a logic zero and the reset to a logic one. Therefore, the initial frequency to which the filters **13** and **14** are responsive to is determined by the program plugs.

When code segment counter **17** is cleared to a logic zero output, inverters INV. A and **506** are a logic one which causes control input **410** of filter **13** (see FIG. 3D) to be driven to a logic zero, thus establishing the response frequency of filter **13.** Hence the multi frequency tone decoder **10** is now ready to respond to the first tone either via filter **14** or via filter **13.**

When the code segment counter stage **503** shifted to a logic one output, it removed the logic zero from one input to inverted NAND gate **18** and its output went to a logic zero. NOR gate **207** changed state to a logic one and triggered AND gate **226** of the end of code reset timer **32.** This triggers circuit **227** which remains at a logic zero output for a period of time slightly longer than required to complete processing the code and then it goes to a logic one output, and inverted NAND gates **228** and **229** produce a momentary logic zero output and clear functions reset gate **201** changes to a logic one state and resets the system. Circuit **227** is similar to circuits **212, 219** and **222** and functions as a delay circuit at the $\overline{Q}$ output.

Decoder NAND gate **21** remains in a logic zero state until the code segment counter stages **502, 503** and **504** are all stepped to logic one outputs, then it shifts to a logic zero and triggers the ON-OFF control **22** and the indicator control flip-flop **103** to their ON conditions.

In the embodiment illustrated, when flip-flop **104** is set by decoder **21,** it inhibits decoder **19,** enables decoder **20** and inhibits filter **14** through flip-flop **402.** This prevents the system from responding to any code except the OFF code permanently wired between decoder **20** and filter **13.** This is a special case however and the system may be made to respond through both program plugs at all times.

One of the filters, **13** and **14,** which make possible the disclosed multifrequency sequential tone decoder is illustrated in FIG. **4.** They are constructed on a thick film R. C. active microcircuit and include an input amplifier **601** which functions as a limiter squarer and provides a regulated input to the controllable active filter **602.** The active filter **602** incorporates nine voltage input taps **410** which control the narrow bandpass frequency of the device by providing a current path through diodes **408** and resistors **409.** When a given input tap is selected, current flow is enabled because the cathode of the diodes **408** is less positive than the anode. Hence when a cathode is pulled to ground, logic zero, current flow commences and the portion of the active filter associated with that particular input or control line is enabled and the response frequency changed. The output of the active filter **602** is applied to a threshold detector **603** which acts as an output buffer. It provides a positive output or logic one at terminal **405** as long as the output of the active filter **602** is below a preset level. When active filter **602** exceeds the preset level in response to a valid input tone, the threshold detector **603** is cut-off and the output at terminal **405** drops to a logic zero. The module may be used as a digitally controlled oscilator by external strapping.

The actual center frequency of the active filter **602** to any response frequency tone is within ±10 Hz of the nominal response frequency and the bandwidth at any given response frequency is no greater than ±1.5 percent and no less than ±1.0 percent of the nominal response frequency. The nominal response frequencies for the active filter **602** is as follows:

Digit Representation	Frequency
0	1980
1	2100
2	2220
3	2340
4	2460
5	2580
6	2700
7	2820
8	2940
When all inputs 0 thru 8 are logic one	3060

Response frequency tone selection is made by driving the selected one out of nine control inputs **410** to logic zero while maintaining the other eight at logic one as previously explained. However for proper operation the control potential within the active filter circuit must be greater than 4 volts for logic one and less than 0.8 volts for logic zero.

The time between the application of a response frequency tone at the input **407** of the amplifier **601** and the threshold detector **603** changing from a logic one to a logic zero is no greater than 15 milliseconds at any bandpass frequency. The time between the removal of a response frequency tone from the input **411** of the amplifier **601** and the threshold detector **603** changing from a logic zero to a logic one (+5 V) is no greater than 10 ms.

The active filter **602** responds to any given frequency tone selected within 0.2 ms after the specific control input **410** reaches a logic zero level. It becomes unresponsive to any given frequency selected within 0.1 ms after the control input **410** reaches a logic one level.

When the latch control line **407** is a logic one the output **405** of the threshold detector **603** is held at a logic one. This effectively causes the module to be unresponsive. Once the module has responded to a valid signal of at least 75 millivolts RMS, the output will at no time change state as long as the input signal remains above

the minimum theshold, regardless of amplitude or rate of change of amplitude.

The present embodiment of this invention is to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than the foregoing description and all changes which come within the meaning and range of equivalency of the claims therefore are intended to be embraced therein.

What is claimed as a significant advancement to the art for which Letters Patent are desired is:

1. A multifrequency sequential tone decoder adapted to be responsive to an input tone signal, comprising:

a. a frequency responsive bandpass filter adapted to be selectively responsive to an individual one of a plurality of frequencies, said frequency responsive bandpass filter including output means for providing a logic level output in response to an input tone signal of said selected frequency;

b. sample position means responsive to said logic level output for providing a first test pulse after a predetermined period of time;

c. tone timing means **26** responsive to said logic level output for providing a reset signal when said logic level output fails to persist a predetermined period of time;

d. silence position means for providing after a predetermined period of time after the termination of said first test pulse a second test pulse;

e. silence timing means for providing a reset signal when said input tone signal exceeds a predetermined amplitude after a predetermined period of time measured from the termination of said first test pulse; and

f. counter means operative in a first mode upon sequential termination of said first and second test pulses for effecting the switching of said frequency responsive bandpass filter to a second one of said plurality of frequencies and in a second mode in response to any one of said reset signals for switching said frequency responsive bandpass filter to a first one of said plurality of frequencies.

2. A multifrequency sequential tone decoder as defined in claim **1,** further comprising:

a decoder responsive to said counter means reaching a predetermined count for providing an output signal.

3. A multifrequency sequential tone decoder as defined in claim **2,** further comprising:

an end of code timer for providing a reset signal when said counter fails to reach a predetermined count within a predetermined period of time.

4. A multifrequency sequential tone decoder as defined in claim **3,** further comprising:

a code selector disposed between said counter and said frequency responsive bandpass filter for controlling the sequence of selection of the responsive frequencies of said frequency responsive bandpass filters.

5. A multifrequency sequential tone decoder adapted to be responsive to an input tone signal, comprising:

a plurality of frequency responsive bandpass filters adapted to be selectively responsive to individual ones of a plurality of frequencies, said frequency responsive bandpass filters including output means for providing logic level outputs in response to an input tone signal of said selected frequency;

b. sample position means responsive to said logic level output for providing a first test pulse after a predetermined period of time;

c. tone detector means responsive to said logic level output for providing a reset signal when said logic level output fails to persist a predetermined period of time;

d. silence position means for providing a second test pulse after a predetermined period of time after the termination of said first test pulse;

e. silence detector means for providing a reset signal when said input tone signal exceeds a predetermined amplitude after a predetermined period of time measured from the termination of said first test pulse; and

f. counter means operative in a first mode upon sequential termination of said first and second test pulses for switching said frequency responsive bandpass filters to second ones of said plurality of frequencies, and in a second mode in response to said reset signals for switching said frequency responsive bandpass filters to first ones of said plurality of frequencies.

6. A multifrequency sequential tone decoder as defined in claim **5,** further comprising:

a detector responsive to said logic level output for inhibiting the operation of all of said frequency responsive bandpass filters except said frequency responsive bandpass filter which generated said logic level output, and responsive to the termination of said second test pulse for uninhibiting all of said frequency responsive bandpass filters.

7. A multifrequency sequential tone decoder as defined in claim **6,** further comprising:

a decoder responsive to said means reaching a predetermined count for providing an output signal.

8. A multifrequency sequentail tone decoder as defined in claim **7,** further comprising:

an end of code timer for providing upon termination of said second test pulse a reset signal when said counter means fails to reach a predetermined count within a predetermined period of time.

9. A multifrequency sequential tone decoder as defined in claim **8,** further comprising:

code selectors disposed between said counter means and said frequency responsive bandpass filters for controlling the sequence of selection of the responsive frequencies of said frequency responsive bandpass filters.

10. A multifrequency sequential tone decoder adapted to be responsive to an input tone signal, comprising:

A. a plurality of frequency responsive bandpass filters adapted to be selectively responsive to individual ones of a plurality of frequencies, said frequency responsive bandpass filters including output means for providing logic level outputs in response to an input of said selected frequency;

b. detector means responsive to said logic level output for inhibiting the operation of all of said frequency responsive bandpass filters except said frequency responsive bandpass filter which generated said logic level output;

c. sample position means responsive to said logic level output for providing a first test pulse after a predetermined period of time;

d. tone detector means responsive to said logic level output for providing a reset signal when said logic level output fails to persist until the termination of said first test pulse; e. silence position means for providing a second test pulse after a predetermined period of time measured from the termination of said first test pulse;

f. silence detector means for providing a reset signal when said input tone signal exceeds a predetermined amplitude after a predetermined period of time measured from the termination of said first test pulse;

g. a counter means operative in a first mode upon sequential termination of said first and second test pulses for providing in sequence a plurality of coded outputs, and in a second mode for providing the first coded output of said plurality in response to said reset signal;

h. code selectors responsive to said plurality of coded outputs for switching said frequency responsive bandpass filters to predetermined ones of said plurality of frequencies;

i. decoder means responsive to said counter reaching a predetermined count for providing an output signal;

j. said counter means responsive to said reset signal for actuating said detector to uninhibit the operation of all of said inhibited frequency responsive bandpass filters; and

k. an end of code timer for providing upon the occurrence of the termination of said second test pulse a reset signal when said counter means fails to reach a predetermined count within a predetermined period of time.

11. A multifrequency sequential tone decoder for identifying an input signal having an address portion comprised of a tone burst of selected frequency and first predetermined duration followed by a blank portion of relatively lower amplitude and second predetermined duration, said decoder comprising:

a. filter means coupled to receive the input signal and selectively controllable to respond to one of a plurality of frequencies to provide an output signal indicative of the selected one frequency;

b. duration timer means for providing a first output signal corresponding to one of said predetermined durations after the occurrence of the output signal of said filter means;

c. burst timing means responsive to the output signals of said duration timer means and said filter means for providing a reset signal if said output of said filter means does not last for the first predetermined duration;

d. counter means operative in a first mode for effecting the operation of said filter means to be responsive to another one of said plurality of frequencies, and in a second mode in response to the reset signal for effecting the operation of said filter means to be responsive to a first one of said plurality of frequencies; e. said duration timer means for providing a second output signal corresponding to the second duration upon a change of said counter means from its first to its second mode of operation, said counter means responsive to the second output signal of said duration timer means to be disposed in its first mode of operation; and

f. blank timing means responsive to the second output signal of said duration timer means for generating a reset signal to be applied to said counter means when the input signal exceeds the relatively low amplitude.

12. The tone decoder as claimed in claim **11**, wherein there is further included programmable decoder means responsive to the count output of said counter means for selectively controlling the one frequency to which said filter means is responsive as the count output of said counter means advances in response to the output signals of said duration timer means.

13. The tone decoder as claimed in claim **11**, wherein there is further included at least second filter means selectively controllable to be responsive to one of a plurality of frequencies to provide an output signal indicative of the selected one frequency; and detector means responsive to the output of one of said first-mentioned and second filter means for actuating the other of said filter means to respond to its one frequency and for deactuating said one filter means.

14. The tone decoder as claimed in claim **11**, wherein said burst timing means is deactuated when said counter means is operative in its second mode, and said blank timing means is deactuated when said counter means is operative in its first mode.

15. The tone decoder as claimed in claim **11**, wherein there is further included amplitude detecting means responsive to the input signal for providing an output indicative of an input signal exceeding the relatively lower amplitude, and said blank timing means responsive to the output of said amplitude detecting means and the second output signal of said duration timer means for generating a reset signal.

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