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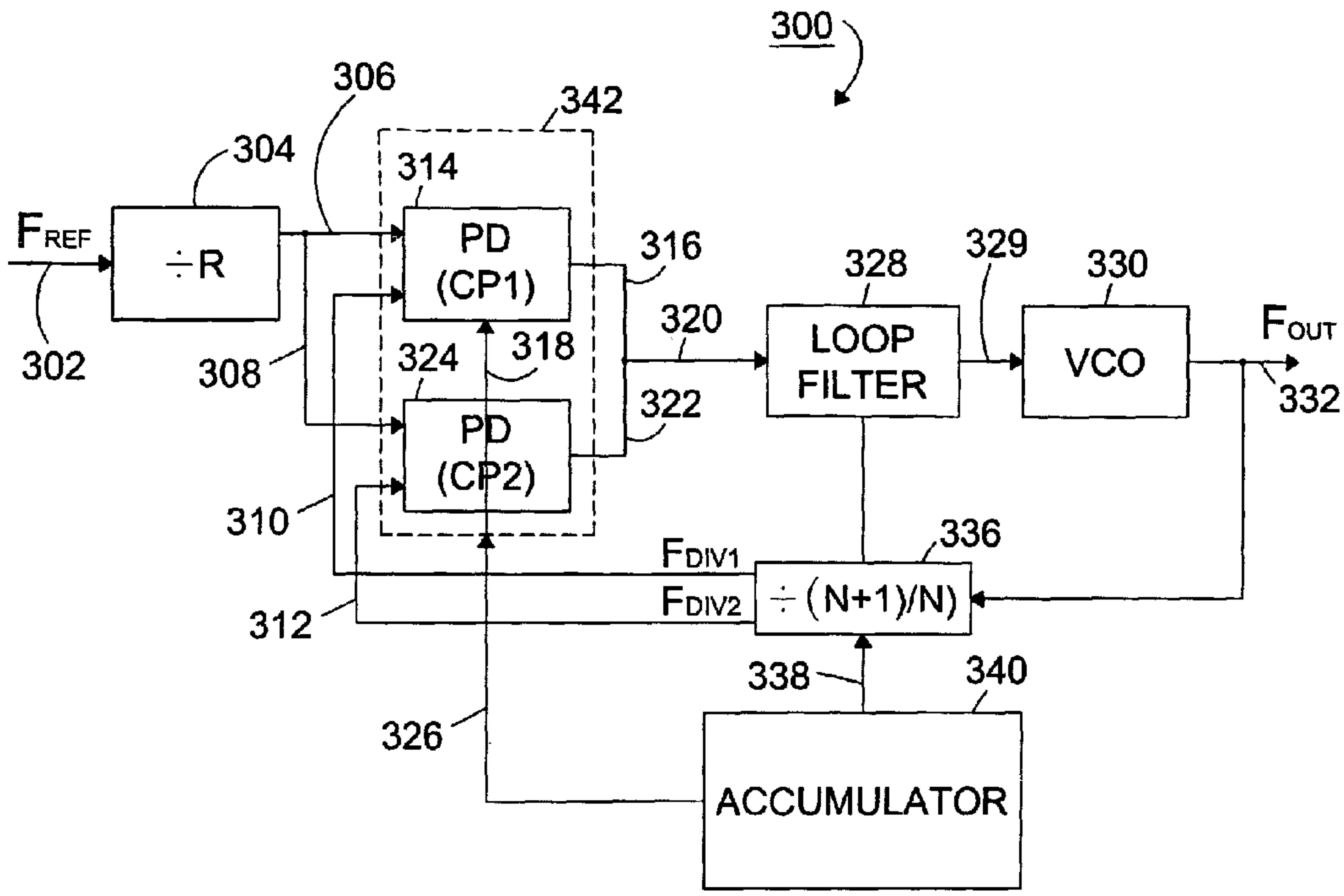
(54) Titre : SYNTHETISEUR DE FREQUENCE N-FRACTIONNAIRE AVEC PROCEDE DE COMPENSATION FRACTIONNAIRE
(54) Title: FRACTIONAL-N FREQUENCY SYNTHESIZER WITH FRACTIONAL COMPENSATION METHOD




(57) Abrégé/Abstract:
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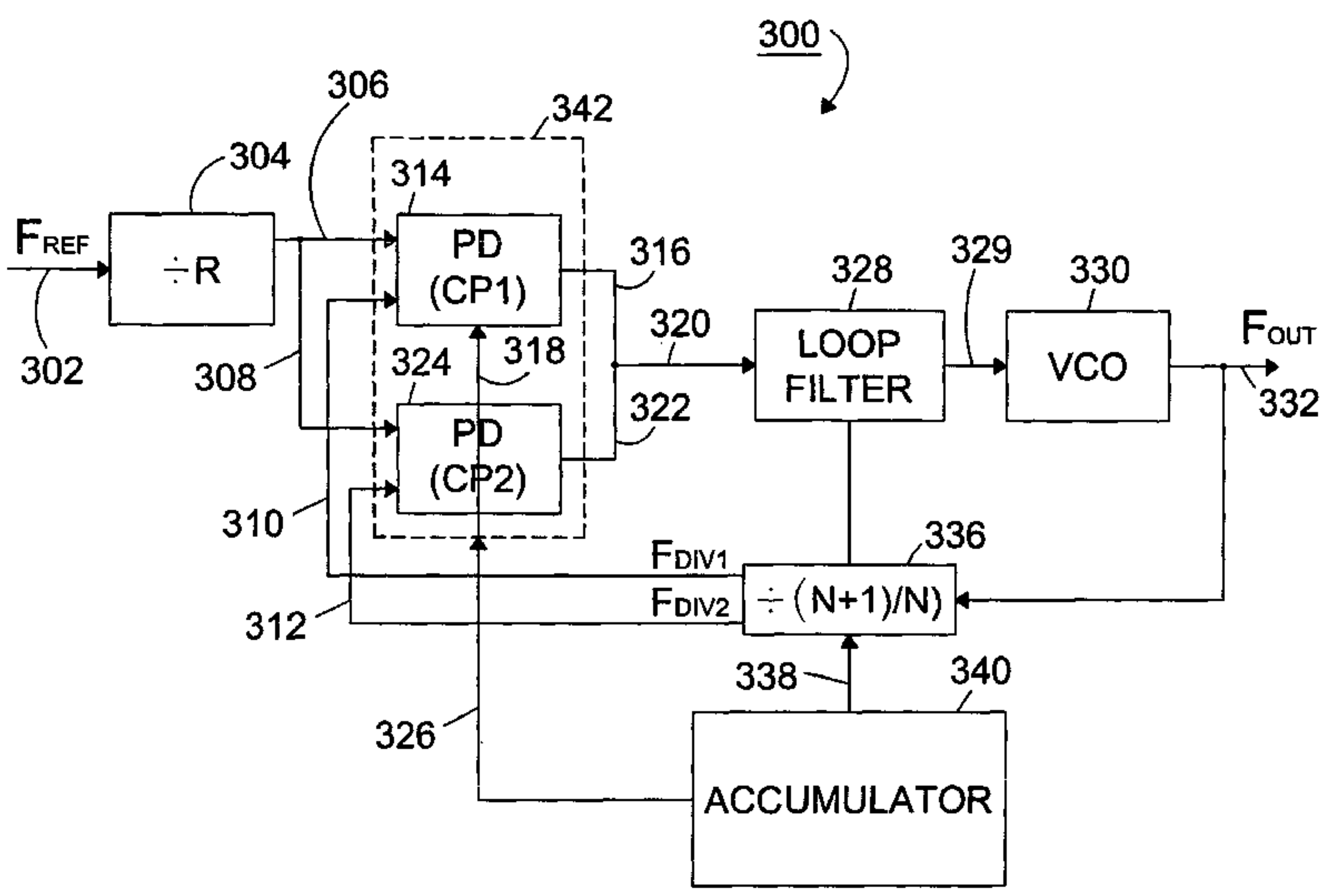
(54) **Title:** FRACTIONAL-N FREQUENCY SYNTHESIZER WITH FRACTIONAL COMPENSATION METHOD




(57) **Abstract:** A phase-locked loop (PLL) frequency synthesizer (Fig. 3) incorporates fractional spur compensation circuitry. This fractional spur compensation circuitry dynamically compensates charge pump ripple whenever a charge pump operates. It can utilize a programmable divider (336), two phase detectors (314 and 324) each using a charge pump stage pumps. A fractional accumulator stage (340) determines the number of charge pumps that operate during a phase comparison. The PLL frequency synthesizer avoids the need for compensation current trimming. Also, fractional compensation is accomplished dynamically and in a manner that is robust to environmental changes. A phase-locked loop (PLL) fractional-N type frequency synthesizer can incorporate a sample-and-hold circuit. The synthesizer can reduce circuit size by eliminating a loop filter. The synthesizer or fractional-N type PLL can use a divider and at least two phase detectors coupled to a sample-and-hold circuit. A lock detecting circuit can initially determine a reference voltage for the sample-and-hold circuit.

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# BACKGROUND OF THE INVENTION

## 1. Field of the Invention

The present apparatus and method can be used for any system that requires fractional resolution of a reference frequency, and relates, in particular, to a PLL-based frequency synthesizer including sample and hold type fractional-N synthesizers for use in a modern wireless or wired communication system.

## 2. Background of the Related Art

Frequency synthesizers are typically used in modern wireless communication systems to produce a desired output frequency in both the receiver and transmitter. Among the various phase locked loop (PLL) based frequency synthesizers, fractional-N frequency synthesizers are suitable for the communication systems where the channel interval is small. Fractional-N architecture allows frequency resolution that is a fractional portion of a reference frequency $F_{REF}$, and an output frequency signal $F_{OUT}$ is related to the reference frequency $F_{REF}$ by the relationship $F_{OUT}=F_{REF}(N+K/F)$, where F is the fractional resolution of the device with respect to the reference frequency. The technique of fractional-N architecture requires generating a divider that is a fractional number rather than an integer. This is performed by changing the divider in the loop dynamically between the values N and N+1. If out of F cycles, division by N+1 is done K times and by N, F-K times, then the average division ratio is N+K/F.

The advantage of the fractional-N architecture is that the reference frequency $F_{REF}$ is not restricted by the channel spacing, and loop bandwidth can be increased. Therefore, phase noise and locking time is reduced. However, the switching of the divisors causes spurious signals in the synthesized output frequency signal $F_{OUT}$. These subharmonic spurs, also referred to as fractional spurs, must be kept below some maximum acceptable limit.

Related art fractional compensation circuit attempt to reduce unwanted spurious signals. For proper fractional compensation, the area of the compensation pulse must be equal to the area of the main charge pump fractional-N ripple. In one related art fractional compensation circuit, however, the amount of the compensation current is statically fixed. Therefore, the spurious signal cancellation cannot track the dynamic change of the spurious signals with time, process, and temperature.

Another related art fractional compensation circuit, typically known as a fractional-N synthesizer, controls the dividing ratio by using a sigma-delta ($\Sigma\Delta$) modulator. A modulus divider receives an output signal from the $\Sigma\Delta$ modulator. The fractional spurious frequencies or phase noise are distributed throughout the frequency spectrum by the operation of the sigma-delta modulator. However, the absolute noise level may be increased above acceptable levels. A more robust and reliable fractional compensation scheme, which does not degrade the spectral purity, is needed.

Frequency synthesizers used in modern wireless communication systems typically utilize a Phase Locked Loop (PLL). PLLs usually include a voltage controlled oscillator (VCO), phase detector (PD) and loop filter (LF). To integrate a PLL on a single integrated circuit, a large LF capacitor, which is used to stabilize the PLL, occupies most of the chip area of the circuit because the capacitance needed in the loop filter (LF) is often on the order of several micro-farads. As recent wireless systems are attempting to integrate the overall receiver and transmitter (including the PLL) on a single chip the required capacitance of the LF capacitor is a significant problem.

One related art approach to reduce the LF capacitance is to use a sample-and-hold circuit as a phase detector or comparator. The capacitor in the sample-and-hold circuit has a much smaller capacitance than that in a typical loop filter. The other advantage of a sample-and-hold phase detector is that the output contains no high frequency harmonics of the input frequency. If the phase is constant, the output voltage is also constant. Hence, the sample-and-hold PD is applicable to a frequency synthesizer.

U.S. Pat. No. 6,137,372 discloses a sample-and-hold type PLL frequency synthesizer that does not need a large LF capacitor. The 6,137,372 sample-and-hold PLL frequency synthesizer uses an integer-N architecture to generate output frequencies that are integer multiples of a reference frequency. However, in the integer-N architecture, the loop bandwidth is limited because the input reference frequency must be equal to the channel spacing. Hence, the attenuation of the close-in phase noise is also limited, because the phase noise of the oscillator is reduced only within the bandwidth of the loop. Another disadvantage of the integer-N architecture is a slow lock time since the lock time of the PLL is also dependent on the loop bandwidth.

To increase the loop bandwidth, fractional-N architectures have been used for frequency synthesizers. Figure 1 illustrates a related art frequency synthesizer using a sample-and-hold circuit. As shown in Figure 1, the reference frequency divider 104 divides an input reference frequency 102 and produces a divided reference signal 106. The phase detector (PD) 110, receives the divided reference signal 106 and an output 108 of an integer divider 128 and generates an output signal 112 responsive to a comparison thereof. A sample and hold circuit 114 receives the output 112 of the PD 110. A voltage controlled oscillator 118 receives an output 116 of the sample and hold circuit 114. An output 120 of the voltage controlled oscillator 118 is an output signal $F_{OUT}$ of the frequency synthesizer circuit and is also input to the integer divider 128.

In operation, the VCO output signal 120 is divided by N in the integer divider 128 and then compared with the divided reference frequency 106 from the reference divider 104. A phase detector (PD) and the sample-and-hold circuit 130 generates a control signal that is dependent on a detected phase difference. The control signal is applied to the voltage controlled oscillator (VCO), which generates the output frequency $F_{OUT}$.

Figure 2(a) is an illustration of the related art phase detector and the sample-and-hold circuit 130. As shown in Figure 2(a), a charge pump 206 receives an output 204 of a phase detector 202. An output 214 of the charge pump 206 is received by the sample and hold circuit 114 at an input connected to a first node n1. In the sample and hold circuit 114, a reference voltage $V_{ref}$ 210 is connected to the first node n1 through a first switch 212. A sample capacitor 220 is connected between a ground reference voltage 222 and the first node n1. A second switch 224 is connected between the first node n1 and a second node n2 that is connected to an output terminal 234. A hold capacitor 230 is connected between the ground reference voltage and the second node n2. The capacitance of the sample capacitor

220 and the hold capacitor 230 is much less than that of the typical loop filter. Before phase comparison occurs in the phase detector 202, the switch SW1 is closed and the sample capacitor is charged to the reference voltage $V_{ref}$. The charge pump 206 following the phase detector 202 increases or decreases the voltage of the sample capacitor 220 from the reference voltage $V_{ref}$ according to the detected phase difference in the phase comparison. When the phase comparison is complete, the charge in the sample capacitor 220 is transferred to the hold capacitor 230 via the second switch SW2.

Figure 2(b) is a timing diagram of the lock state in a related art sample-and-hold type integer-N frequency synthesizer. As shown in Figure 2(b), a relationship between the reference frequency signal and the divider output (i.e., divided VCO output) exists and is a constant phase difference T when the phase is aligned in the typical loop filter type PLL. Hence, the sample-and-hold type PLL is not suitable for application as clock or data recovery where the phase must be aligned between the input reference signal and the VCO output. The phase detector output and voltage of the sample capacitor are also shown in Figure 2(b). In the integer-N frequency synthesizer, however, the phase alignment is not a requirement, and the sample-and-hold type PLL is applicable as long as the phase noise characteristic is satisfied. As shown in Figure 2(b), it is assumed that the phase of the reference frequency signal leads that of the divider output by the time T, and the phase detector generates an UP (HIGH) signal at every phase comparison to increase the voltage of the sample capacitor (Vsample) at a fixed rate from the reference voltage ($V_{ref}$). Hence, the voltage of the hold capacitor (Vhold) and the output frequency of the voltage controlled oscillator are kept constant.

As described previously, however, an integer-N frequency synthesizer has a narrower loop bandwidth than a fractional-N frequency synthesizer. To increase the loop bandwidth above the channel spacing, the fractional-N synthesizer includes a variable modulus programmable divider, which is controlled by an accumulator. The accumulator changes the division ratio of the variable modulus programmable divider regularly to generate the desired fractional division ratio. Accordingly, the control voltage of the VCO in the fractional-N frequency synthesizer is not constant, but the time-averaged value of the control voltage is meaningful. Thus, the related art fractional-N architecture cannot adopt the sample-and-hold circuit to replace the loop filter.

Figure 2(c) is a timing diagram that illustrates problems and disadvantages of a sample-and-hold circuit in the related art fractional-N synthesizer. As shown in Figure 2(c), the reference frequency and the divider output do not have a constant aligned phase difference as shown in the phase detector output of Figure 2(b). The phase detector output, the sample-and-hold circuit output voltage and the state of the fractional accumulator are also shown. In Figure 2(c), the fractional ratio is assumed to be 3/8 (K=3 N=8) where N is the division factor. The state of the fractional accumulator varies according to the fractional ratio. Therefore, the phase of the divider output with respect to the reference frequency signal and the width of the UP pulse of the phase detector also vary. The amount of voltage change of the sample capacitor (Vsample) is not fixed and the voltage of the hold capacitor (Vhold) shows fractional ripple which degrades the spectral purity of the synthesized frequency.

The above references are incorporated by reference herein where appropriate for appropriate teachings of additional or alternative details, features and/or technical background.

## SUMMARY OF THE INVENTION

An object of the present invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

Another object of the present invention is to provide a phase locked loop-based fractional-N synthesizer.

Another object of the present invention is to provide a fractional compensation circuit and method that incorporates two phase detectors.

Another object of the present invention is to incorporate fractional spur compensation circuitry that dynamically compensates fractional spurs or charge pump ripple whenever the charge pump operates.

Another object of the present invention is to provide a phase locked loop-based fractional-N synthesizer and method that uses a plurality of phase detectors to dynamically cancel spurious signals.

Another object of the present invention is to provide a phase locked loop-based fractional-N synthesizer that variously delays at least one output of a plurality of phase detectors to reduce fractional spurs.

Another object of the present invention is to provide a fractional compensation circuit that uses a charge pump stage composed of N charge pumps so that a number of the N charge pumps that operate during a phase comparison is determined by a fractional accumulator stage.

Another object of the present invention is to provide a fractional compensation circuit and method that incorporates a sample-and-hold circuit in a loop filter.

Another object of the present invention is to provide a phase locked loop-based fractional-N synthesizer and method that uses a plurality of phase detectors to dynamically cancel spurious signals and a sample-and-hold circuit.

Another object of the present invention is to provide a fractional compensation circuit that uses a charge pump stage composed of N charge pumps coupled to a sample-and-hold circuit in a loop filter so that a number of the N charge pumps that operate during a phase comparison is determined by a fractional accumulator stage.

An advantage of a fractional-N architecture and method according to the present invention is that a reference frequency is not restricted by the channel spacing and loop bandwidths can be increased.

Another advantage of a fractional-N architecture and method according to the present invention is that subharmonic spurs or fractional spurs can be kept low.

Another advantage of a fractional-N architecture and method according to the present invention is that the spurious signal cancellation can occur dynamically.

Another advantage of a fractional-N architecture and method according to the present invention is that it avoids the need for compensation current trimming.

Another advantage of a fractional-N architecture and method according to the present invention is that it is robust to environmental changes.

Another advantage of a fractional-N architecture and method according to the present invention is that circuit size is reduced.

Another advantage of a fractional-N architecture and method according to the present invention is that it avoids the need for a large loop filter capacitor.

Another advantage of a fractional-N architecture and method according to the present invention is that a sample-and-hold circuit can be implemented in the PLL to provide a stable control voltage.

To achieve the above objects in a whole or in part and in accordance with the purpose of the present invention, as embodied and broadly described, a phase locked loop includes a first phase detector that receives an input signal and a first divided signal to output a first comparison signal, a second phase detector that receives the input signal and a second divided signal to output a second comparison signal, a circuit that receives the first and second comparison signals and generates an output signal responsive to the comparison signals, a voltage-controlled oscillator that receives the output signal from the circuit and generates a prescribed frequency signal, and a programmable modulus divider that receives the prescribed frequency signal and generates the first and second divided signals having a prescribed phase relationship.

To further achieve the above objects in a whole or in part and in accordance with the purpose of the present invention, as embodied and broadly described, a fractional-N frequency synthesizer for a mobile terminal includes a phase detector circuit that includes a first phase detector having a first input port coupled to receive a reference signal, a second input port, a third input port and an output port, and a second phase detector having a first input port coupled to receive the reference signal, a second input port, a third input port and an output port, a circuit having a first input port coupled to the output ports of the first and second phase detectors and an output port, a voltage-controlled oscillator having an input port coupled to the output port of the circuit and transmitting a prescribed frequency signal at an output port, a programmable modulus divider having a first output port coupled to the second input port of the first phase detector to transmit a first divided signal, a second output port coupled to the second input port of the second phase detector to transmit a second divided signal, a first input port coupled to the output port of the voltage-controlled oscillator and a second input port, and an accumulator having a first output port coupled to the second input port of the programmable modulus divider and a second output port coupled to the third input ports of the phase detectors.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following, or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figure 1 shows a related art embodiment of a Integer-N frequency synthesizer using a sample-and-hold circuit;

Figure 2(a) shows a phase detector and a sample-and-hold circuit of Figure 1;

Figure 2(b) shows a timing diagram of a lock state in a related art sample-and-hold type integer-N frequency synthesizer;

Figure 2(c) shows a timing diagram of a sample-and-hold circuit in a related art fractional-N synthesizer;

Figure 3 is a schematic diagram that shows a preferred embodiment of a frequency synthesizer including a phase-locked loop (PLL) according to the invention;

Figure 4 is a diagram that shows a preferred embodiment of a programmable modulus divider of Figure 3;

Figure 5 is a diagram that shows a phase detector circuit having a charge pump bock with a charge pump stage following phase detectors;

Figure 6 is a diagram that shows a control timing diagram of a charge pump block of Figure 5;

Figure 7 is a diagram that shows another embodiment of a phase detector circuit including a charge pump block in which a number of charge pumps is reduced to N compared to a total of 2N charge pumps in Figure 5;

Figures 8(a) and 8(b) show timing diagrams of the phase lag and lead, respectively, of a divided reference frequency and a divided VCO frequency;

Figure 9 shows a timing diagram of a compensation scheme according to a preferred embodiment of the invention;

Figure 10 is a diagram that shows another preferred embodiment of a frequency synthesizer including a PLL with a delay in a phase detector circuit;

Figure 11 is a diagram that shows another preferred embodiment of a phase detector circuit having a delay;

Figure 12 is a timing diagram showing effects of introducing a delay in a phase detector circuit;

Figure 13 is a diagram that shows an exemplary digital control circuit where a number of delay taps switched into the circuit determines the delay;

Figure 14 is a diagram that shows an exemplary analog circuit where the control voltage controls the delay of each delay cell and the total delay of the circuit;

Figure 15 is a diagram that shows a sample-and-hold circuit where each charge pump output is coupled to one sample capacitor;

Figure 16 is a timing diagram that illustrates a preferred embodiment of a method of operating a sample-and-hold fractional-N frequency synthesizer according to the invention;

Figure 17 is a diagram that shows another preferred embodiment of a sample-and-hold type fractional-N frequency synthesizer including a detector circuit to set a reference voltage according to the present invention;

Figure 18 is a diagram that shows a portion of another preferred embodiment of a fractional-N synthesizer including a detector circuit to set a reference voltage according to the present invention; and

Figure 19 is a timing diagram that shows another preferred embodiment of a method of operating a sample-and-hold type fractional-N frequency synthesizer when the reference voltage is matched with the desired control voltage according to the present invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 3 is a schematic diagram that shows a preferred embodiment of a fractional compensation circuit according to the present invention. As shown in Figure 3, a frequency synthesizer 300 includes a phase locked loop (PLL) having a phase detector circuit 342, a loop filter 328, a voltage controlled oscillator (VCO) 330, and a programmable modulus divider 336 coupled to an accumulator 340. In the frequency synthesizer 300, a reference frequency 302 is fed into a reference frequency divider 304. The output of the reference frequency divider 304, is branched into two phase detector feeds 306 and 308. The two phase detector feeds 306 and 308, are respectively input to phase detectors 314 and 324 of the phase detector circuit 342. Outputs 316 and 322, of the phase detectors 314 and 324, are coupled into an input 320 of the loop filter (LF) 328. An output 329 of the loop filter 328 is fed into the voltage controlled oscillator (VCO) 330. The phased detector circuit 342, contains the two phase detectors 314 and 324 that preferably contain two charge pump blocks (not shown). The terms “charge pump,” “charge pump block,” and “CP” refer to the same type circuit and are used interchangeably herein. Where more than one charge pump is referenced, CP1 and CP2 are sometimes used.

The modulus programmable divider 336 divides an output frequency signal $F_{OUT}$ 332 of the VCO 330, alternatively by N and N+1, respectively, depending on the control signal 338 from the accumulator 340. Each of the two divided VCO signals $F_{DIV1}$ and $F_{DIV2}$ from the modulus programmable divider serve as second inputs 310 and 312, respectively, of the phase detectors 314 and 324. The two divided VCO signals $F_{DIV1}$ and $F_{DIV2}$ 310 and 312, produced by the modulus programmable divider 336, preferably have the same frequency and a phase difference that is a period of VCO ($1/F_{OUT}$). N equal charge pumps (not shown) are preferably coupled to each phase detector 314 and 324. The accumulator 340, controls the number of charge pumps to be enabled before the phase comparison in the phase detectors 314 and 324 between the input reference frequency ($F_{REF}$) and the divided VCO clock ($F_{DIV1}$, $F_{DIV2}$) occurs. Thus, the accumulator 340 outputs enable signals 318 and 326, respectively, to the phase detectors 314 and 324.

Figure 4 is a diagram that shows a preferred embodiment of a programmable modulus divider 400, (e.g., dividing an input signal by N+1 or by N, which produces two divided VCO outputs $F_{DIV1}$ and $F_{DIV2}$, 416 and 422. The programmable modulus divider 400 can be used as the programmable modulus divider 336 of Figure 3. The programmable modulus divider 400 can include three flip flops 412, 420, 434 and two logic gates 402, 428. Since the three flip-flops 412, 420 and 434, are preferably clocked by an identical output signal 436, which is preferably the output frequency signal $F_{OUT}$ 336, the phase difference between $F_{DIV1}$ and $F_{DIV2}$, 416 and 422, is a period of a VCO frequency ($T_{VCO}=1/F_{OUT}$).

As shown in Figure 4, a first "OR" gate 402, receives an input 404 from the third flip-flop 434, and receives an input 406 from the second flip-flop 420. The first flip-flop 412 receives and processes an output 408 of the first "OR" gate 402 according to the $F_{OUT}$ signal 436. The second flip-flop 420 receives and processes an output 414 from the first flip-flop 412 according to the $F_{OUT}$ signal 436. In addition to the input 406 from the second flip-flop 420, the second "OR" gate 428 receives a modulus control signal as an input 426. The third flip-flop 434 receives and processes an output 430 from the second "OR" gate 428 according to the $F_{OUT}$ signal 436. The output signals 414 and 406 of the first and second flip flop 412, 420 are preferably the divided VCO signals $F_{DIV1}$ 416 and $F_{DIV2}$ 422 from the programmable modulus divider 400.

Figure 5 is a diagram that shows a preferred embodiment of a phase detector and charge pump circuit 500. As shown in Figure 5, the phase detector and charge pump circuit 500 can be used, for example, as one of the phase detectors 314, 324 in the phase detector circuit 342 shown in Figure 3. The charging or discharging current provided from each charge pump to the LF (not shown) is preferably determined as I/N, where I is the current of a typical fractional-N frequency synthesizer. An enable signal (EN) 515, is generated by the corresponding accumulator (not shown) such as the accumulator 340 according to the fractional accumulator state, and controls whether the charge pump 534 is enabled. As shown in Figure 5, there are preferably N charge pumps 534 coupled to the phase detector 506 that receive an enable signal from an accumulator.

As shown in Figure 5, a phase detector 506 compares an $F_{REF}$ input 502 as a divided reference frequency, and an $F_{DIV}$ input 504 to generate two outputs 508 and 510, each received by a charge pump circuit 534, responsive to the comparison. A first "AND" gate 518 of the charge pump 534 receives an "UP" signal 512 and the "EN" signal 515. A second "AND" gate 520, receives a "DN" signal 514, and the "EN" signal 515. Preferably, the output signal 508 is the "UP" signal 512 and the output signal 510 is the down "DN" signal 514. A first switch 526 and a first current source 522 are coupled in series between a power supply voltage and an output terminal 530. The state of the first switch 526 (e.g., open or closed) is controlled by an output signal 540 from the first "AND" gate 518 responsive to the comparison in the corresponding phase detector and the enable signal EN. A second switch 528 and a second current source 524 are coupled in series between the output terminal 530 and a ground reference voltage. The state of the second switch 528 is preferably controlled by an output signal 542 from the second "AND" gate 520. Thus, the first current source 522 and the second current source 524, are selectively coupled into the single output terminal 530 of the charge pump 534. An output 532 of the N charge pumps 534 of phase detector and charge pump circuit 500 is received by the loop filter (not shown). Output terminals 530 of the N charge pumps 534 are coupled to provide the output 532 to the loop filter. However, the present invention is not intended to be so limited.

The control timing relationship of a charge pump block is described in Figure 6 where the fractional number is assumed as 3/8(K=3,N=8). Accordingly, the modulus divider divides by 8(N) 5 times and by 9(N+1) 3 times out of 8 cycles. The timing relationship shown in Figure 6 can be used for the charge pump block associated with each phase detector 314, 324 of Figure 3. Thus, for example, the phase detector circuit 342 could include 2(N=8) or 16 charge pump stages 534.

The waveforms shown in Figure 6 are the divided reference frequency voltage 602, and the voltages of the outputs of the modulus programmable divider 604 and 606 (e.g., 310, 312). The number of enabled charge pumps for CP1 and CP2 (e.g., within PD 314 and PD 324) are indicated by 608, and the state of the fractional accumulator is indicated by 610. The divider state of the synthesizer is indicated by 612. As shown in Figure 6, the number of charge pumps (CP1 and CP2) enabled during the phase comparison is determined by the accumulator state 610. The total number of charge pumps enabled is always fixed as the division factor N.

Another preferred embodiment of a phase detector circuit including a charge block pump with N charge pumps is illustrated in Figure 7. As shown in Figure 7, a charge pump block 700 receives the output 706 of the first phase detector PD1, which serves as a series of first inputs to switches 726, 728, 730, ..., 732, respectively. The output 708 of the second phase detector PD2 serves as a series of second inputs to the switches 726, 728, 730, ..., 732, respectively. Respective switch outputs 734, 736, 738 ..., 740, of the switches 726, 728, 730 and 732 serve as inputs to the charge pumps 742, 744, 746 ..., 748. Outputs 750, 752, 754, ..., 756 of the preferably N charge pumps 742, 744, 746 ..., 748, are coupled into an output signal 758 to be connected to the loop filter (not shown). In the charge pump block 700, the number of charge pumps is reduced to N, compared to a total of 2N charge pumps of Figure 5, when the accumulator controls the connection of the phase detectors PD1 and PD2 to the charge pumps 726, 728, 730, ..., 732, as shown in Figure 7.

The phase relationship between a divided reference frequency and a divided VCO frequency is shown in Figures 8(a) and 8(b). Figure 8(a) illustrates a relative phase lag of the divided reference signal, and Figure 8(b) shows a relative phase lead of the divided reference signal. For example, Figures 8(a) and 8(b) can show a phase relationship between the divided reference frequency 306 and the divided VCO frequencies 310, 312 of the frequency synthesizer 300 of Figure 3. As shown in Figures 8(a) and 8(b), the relative voltage waveforms include the reference frequency 802, the Divider $Output_1$ 804, the Divider $Output_2$ 806, the PD1 output 808, and the PD2 output 810. The number of enabled charge pumps 812 and 816, which is always the division factor N, and the fractional accumulator state 814, are also indicated relative to the waveforms.

In Figure 8(a), both outputs 808 and 810 of the phase detectors, in response to a phase lag of the divided reference frequency ($F_{REF}$) 802, cause all charge pumps to discharge (e.g., generate a "DOWN" signal) the loop filter to decrease the VCO output frequency. Conversely, in Figure 8(b) a phase lead of the divided reference frequency causes both the outputs 808 and 810 of the phase detectors discharge all the charge pumps (e.g., generate the "UP" signal) and causes the VCO to increase its output frequency. In a locking state, the phase of the divided reference frequency ($F_{REF}$) 802, is laid between two divided VCO frequencies $F_{DIV1}$ and $F_{DIV2}$, 804 and 806, which means that one phase detector (PD1) generates a "DOWN" signal and the other (PD2) generates an "UP" signal. Thus, in the locking state, charge pumps connected to PD1 discharge the loop filter and charge pumps connected to PD2 charge the loop filter to preferably keep the loop filter voltage constant.

Figure 9 is a timing diagram that shows fractional compensation according to a preferred embodiment of the present invention. For example, Figure 9 can show can show a phase relationship between the divided reference frequency 306 and the divided VCO frequencies 310, 312 of the frequency synthesizer 300 of Figure 3. In Figure 9, it is assumed that the fractional number is 3/8 (K=3, N=8) as described above in Figure 6. As shown in Figure 9, the relative voltage waveforms of the divided reference frequency 902, the Divider $Output_1$ 904, the Divider $Output_2$ 906, the PD1 output 908, the PD2 output 910, and the control voltage 918 are shown. Sections of the amplitude 920, 922 and 924 of the control voltage 918 are magnified for clarity in Figure 9. The number of enabled charge pumps 912 and 916, and the fractional accumulator state 914, are also indicated relative to the waveforms.

In a locked state of a frequency synthesizer as shown in Figure 9, the charge pumps (CP1) connected to PD1 always sink current from the loop filter while those (CP2) connected to PD2 always source current to the loop filter. The amount of discharging current by the CP1 is given by the equation:

$$Q_{discharge}=I_{discharge}*T_{discharge}=\{(N-K)*(I/N)\}*\{(K/N)*T_{VCO}\} \qquad \text{(Eq. 1)}$$

where K represents the accumulator state. Similar to Eq.1, the amount of charging current by the CP2 is given by the equation:

$$Q_{charge}=I_{charge}*T_{charge}=\{K*(I/N)\}*[\{(N-K)/N\}*T_{VCO}] \qquad \text{(Eq. 2)}$$

From (Eq. 1) and (Eq. 2), $Q_{charge}$ and $Q_{discharge}$ are always the same. Accordingly, the charging current and the discharging current compensate each other to keep the loop filter output voltage constant in the locked state. The loop characteristic of the PLL preferably keeps the phase relationship to satisfy the above equations and the loop filter voltage is preferably kept constant irrespective of environmental changes such as temperature. Hence, the fractional spur is compensated dynamically. Further, no compensation current trimming is required. Further, the small perturbation of loop filter voltage during phase comparison in Figure 9 shows negligible fractional spur and phase noise compared to the related art fractional-N architecture because it does not change the average level of the control voltage and it occurs during a very short time of a period of VCO frequency.

However, preferred embodiments according to the present invention are not restricted to the above case or intended to be so limited. For example, by changing the phase difference between the divided signals and number of charge pumps used, other combinations to implement the fractional compensation of a reference signal according to the invention are possible.

Another embodiment of a frequency synthesizer including a phase locked loop according to the present invention is illustrated in Figure 10. As shown in Figure 10, a frequency synthesizer 1000 receives a reference frequency 1002 that is input to a first and second phase detector 1010 and 1012, respectively. The first phase detector 1010 also receives a first divided VCO frequency 1004, and the second phase detector 1012 also receives a second divided VCO frequency 1008. The delay 1018 receives an output 1014 of the first phase detector 1010 and preferably outputs the same after a prescribed delay. The first charge pump 1022 receives an output 1020 of the delay block 1018, and the second charge pump 1024 directly receives the output 1016 of the second phase detector 1012. The output 1026 of the first charge pump 1022 and the output 1028 of the second charge pump 1024 are coupled together and serve as the input 1030 to a loop filter such as the loop filter 328. Preferably, the VCO 330, the modulus programmable divider 336 and the accumulator 340 are coupled to the loop filter 328 and a phase detector circuit 1050. In the preferred embodiment of Figure 10, by introducing a delay to the output of one of the first and second phase detectors 1010 and 1012, the perturbation in the loop filter voltage 1030 is further reduced. As shown in Figure 10, the output 1014 of the first phase detector 1010 is delayed to reduce or minimize the perturbation of the loop filter voltage. However, the present invention is not intended to be so limited.

For example, the delay block 1018 as shown in Figure 10 may be placed in front of the first phase detector 1010 to preferably achieve the same effect described above. As shown in Figure 11, another preferred embodiment of a phase detector circuit 1100 for a frequency synthesizer includes a first delay block 1106 that receives the reference frequency input 1002 and a second delay block 1108 that receives the first divided VCO frequency 1004. The first phase detector 1010, receives and processes an output 1110 of the first delay block 1106 and an output 1112 of the second delay block 1108. The second phase detector 1012 and the second charge pump 1024 operate as described above. However, the first charge pump 1022 directly receives an output 1114 from the first phase detector 1010. An output 1126 from the first charge pump 1022 and an output 1128 from the second charge pump 1024 are combined and serve as the input 1130, to the loop filter (not shown).

Operations and effects of delays such as generated in the preferred embodiments shown in Figures 10-11 will now be described. As shown in Figure 12, the voltage output of a first phase detector is represented by the waveform 1202, a delayed output of the first phase detector is represented by the waveform 1204, and an output of a second phase detector is represented by the waveform 1206. A voltage control signal is represented by the waveform 1208, where an illustrated amplitude is exaggerated for clarity in sections 1212, 1214, and 1216. Further, a state of a fractional accumulator is indicated by 1210.

As shown in Figure 12, the "DOWN" signal of PD1 and the "UP" signal of PD2 are overlapped. Hence, the charging current and the discharging current are simultaneously applied to the loop filter and compensate each other to reduce or minimize a peak-to-peak variation of the loop filter voltage. As long as the delayed PD1 signal 1204 and PD2 signal 1206 overlap, operations of the preferred embodiments of Figures 10-11 are effective to reduce the loop filter voltage. However, preferred embodiments of the present invention are not intended to be so limited. For example, the delay could be accomplished in the PD2 signal or both PD1 and PD2 signals. Further, an optimum or prescribed delay according to the division ratio can be set, for example, by the controlling accumulator.

Figures 13 and 14 are diagrams that show exemplary delay control circuits. Figure 13 shows a digital control circuit 1300, where series coupled delay taps 1304, 1312, 1320, and 1328 are coupled between an input terminal 1302 and an output terminal 1340. A number of the delay taps 1304, 1312, 1320 and 1328 that are switched into the circuit determines a prescribed delay between an input signal IN and an output signal OUT. The digital delay control circuit 1300, receives the signal to be delayed as the input signal IN at the input terminal 1302. The delay taps can be, for example, an inverter. A plurality of switches 1332, 1334, 1336, 1338 are respectively connected between outputs of the delay taps 1304, 1312, 1320 and 1328 and the output terminal 1340. On/off states of the switches 1332, 1334, 1336, and 1338, are preferably determined by the control signal 1350. Thus, a total delay of the digital delay control circuit 1300 is controlled by the state of the switches 1332, 1334, 1336, and 1338.

Figure 14 shows an analog delay control circuit where a control voltage controls the delay of each delay cell and thereby a total delay of the circuit. As shown in Figure 14, an analog delay control circuit 1400, receives an input signal IN at an input terminal 1402 coupled to a first delay cell 1404. Delay cells 1412, 1416 and 1422 are connected in series between the first delay cell 1404 and an output terminal 1426. The delay cells 1404, 1412, 1416 and 1422 each receive a control voltage CONTROL 1428, which determines a delay generated by each of the delay cells, and thus, the control voltage 1428 determines a cumulative prescribed delay between the input signal IN and the output signal OUT. As described above, more or less delay taps or delay cells can constitute the exemplary delay circuits.

As described above, preferred embodiments of a frequency synthesizer have various advantages. A frequency synthesizer including a phase-locked loop (PLL) according to the preferred embodiments incorporates fractional spur compensation circuitry to dynamically compensate charge pump ripple whenever a charge pump operates. In the preferred embodiments, a programmable divider produces two output signals that are preferably divided signals from a voltage controlled oscillator (VCO) with the same division ratio for input to two phase detectors of the PLL. Thus, a phase difference of the divided VCO signals is preferably a period of the VCO output. In a locked state of a frequency synthesizer, the phase of the corresponding reference signals occurs between these divider signals. In a preferred embodiment, two phase detectors (PD) are used each having an input terminal connected to receive one of the two divided VCO signals of the divider. A second input terminal of each phase detector is connected to receive a reference signal. Therefore, one PD produces an "UP" signal and the other a "DOWN" signal in the locking stage.

A charge pump block can include N equal charge pump stages and is connected to each phase detector output terminal. The output terminal of each charge pump is combined in the loop filter. The number of charge pumps which operate during a phase comparison is determined by a fractional accumulator stage. In the locking state, the amount of charging current and discharging current is always the same and compensate each other. Hence, no fractional ripple occurs. Thus, preferred embodiments according to the present invention avoids or reduce the need for compensation current trimming. Fractional compensation is dynamic, and is robust to the environmental changes such as circuit age, process and temperature. Thus, preferred embodiments of a frequency synthesizer can be implemented by changing the phase difference of the divided signals of the programmable divider and the number of charge pumps activated.

Figure 15 is a diagram that illustrates a preferred embodiment of a sample-and-hold circuit 1500 where a plurality of phase detectors are respectively coupled to one sample capacitor. As shown in Figure 15, a first charge pump 1506 receives an input from a first phase detector PD1, and a second charge pump 1508 receives an input from a second phase detector PD2. An output 1510 of the first charge pump 1506 and an output 1512 of the second charge pump 1508 are coupled together to an input 1514 of a sample-and-hold circuit 1536 that is coupled to a first node n1. In the sample and hold circuit 1536, a reference voltage $V_{ref}$ 1516 is coupled to the first node n1 through a first switch 1518. A first capacitor 1520, a sample capacitor, is coupled between a ground reference voltage 1522 and the first node n1. A second switch 1524 is coupled between the first node n1 and a second node n2 that is coupled to an output terminal 1534. A second capacitor 1530, a hold capacitor, is coupled between the ground reference voltage 1522 and the second node n2. The capacitance of the sample capacitor 1520 and the hold capacitor 1530 is much less than that of the typical loop filter capacitor. Before phase comparison occurs in the phase detectors PD1 and PD2, the first switch 1518 is closed and the sample capacitor 1520 is charged to the reference voltage $V_{ref}$ 1516. The charge pump blocks 1506 and 1508 respectively following the phase detectors PD1 and PD2 increase or decrease the voltage of the sample capacitor 1520 from the reference voltage $V_{ref}$ 1516 according to the detected phase difference in the phase comparison. When the phase comparison is complete, the charge in the sample capacitor 1520 is preferably transferred to the hold capacitor 1530 via the second switch 1524.

Figure 16 is a timing diagram that shows fractional compensation method of a sample-and-hold type fractional-N frequency synthesizer according to the present invention. For example, Figure 16 can show can show a phase relationship between the divided reference frequency 306 and the divided VCO frequencies 310, 312 of the frequency synthesizer 300 of Figure 3 having a sample-and-hold circuit replace the lo. In Figure 16, it is assumed that the fractional number is 3/8 (K=3, N=8). The fractional accumulator state K determines the number of charge pumps that operate during the phase comparison. For example, (N-K) charge pumps of PD1 and K charge pumps of PD2 are enabled. The total number of charge pumps enabled is always N. In Figure 16, the relative voltage waveforms of the divided reference frequency 1602, the Divider Output1 1604, the Divider Output2 1606, the PD1 output 1608, the PD2 output 1610, and the control voltage 1612 are shown. The number of enabled charge pumps 1616 and 1618, and the fractional accumulator state 1614, are also indicated relative to the waveforms. In Figure 16, a phase lead of the divided reference signal 1602 is uniformly compensated by varying the number of enabled charge pumps corresponding to PD1 and PD2 so that charging increases from PD1 and PD2 to the control voltage (Vhold) from the reference voltage (Vsample) combine to a consistent value.

As described above with respect to Figure 7, a total of N charge pumps are implemented and a switch controlled by an accumulator preferably determines the number of charge pumps connected to PD1 and PD2. As shown in Figure 16, an amount of charge sourced from the charge pump at every phase comparison is given by the equation:

$$Q_{TOTAL} = I_{CP1}*T_{CP1} + I_{CP2}*T_{CP2}$$

$$=[\{(N-K)*(I/N)\}*\{T1-(K/N)*T_{VCO}\}]+ [K*(I/N)*\{(T_1-(K/N)*T_{VCO}) +T_{VCO}\}]$$

$$=I*T_1=\text{constant} \quad \text{(Eq. 3)}$$

Therefore, the voltage change of the control voltage or the sample capacitor is constant and the voltage of the hold capacitor is also kept constant. Consequently, the synthesized output shows a good spectral purity. If the division ratio changes to generate a different frequency, the phase difference $T_1$ between the reference signal and the divided output changes, which determines the control voltage. Further, as shown in Figure 16, the reference signal leads the divided signals 1604 and 1606. However, the present invention is not intended to be so limited. If the phase of the reference signal lags that of the divided output, the voltage of the sample capacitor can be lowered from the reference voltage $V_{ref}$. In addition, preferred embodiments according to the present invention can be implemented in a variety of manners by changing the phase difference of the two divider output signals and the number of charge pumps in each phase detector.

Another embodiment of a sample-and-hold type fraction-N frequency synthesizer including a phase locked loop according to the present invention is illustrated in Figure 17. As shown in Figure 17, a frequency synthesizer 1700 receives a reference frequency 1702 that is input to a first and second phase detector 1710 and 1712, respectively. The first phase detector 1710 also receives a first divided VCO frequency 1704, and the second phase detector 1712 also receives a second divided VCO frequency 1708. A lock detector 1718 and a first charge pump block 1722 receives an output 1714 of the first phase detector 1710. The lock detector 1718 and a second charge pump 1724 receive an output 1716 of the second phase detector 1712. An output 1726 of the first charge pump 1722 and an output 1728 of the second charge pump 1724 are coupled together and serve as an input 1730 to a sample-and-hold circuit 1740 such as the sample-and-hold circuit 1536. Preferably, the VCO 330, the modulus programmable divider 336 and the accumulator 340 or the like are coupled to the sample-and-hold circuit 1740 and the phase detectors 1710 and 1712.

In the preferred embodiment of Figure 17, a Digital to Analog Converter (DAC) 1732 receives an input 1720 from the lock detector 1718, and produces an output 1734 received by the sample-and-hold circuit 1740. Preferably, the output 1734 is a reference voltage $V_{ref}$ used to initialize the sample capacitor.

In a sample-and-hold type PLL, if the reference voltage is initially set too far from the locking control voltage, the loop may not generate the desired frequency. The frequency synthesizer 1700 according to the present invention includes a lock detector so that the loop will generate the desired frequency even when the reference voltage is initially set too far from the locking control voltage. As shown in Figure 17, a detector circuit 1750 can include the lock detector 1718 and the DAC 1732. The lock detector 1718 respectively preferably monitors the output of each phase detector 1710 and 1712. For example, when both outputs of PD1 and PD2 are increase voltage signals (e.g., "UP" signals), the reference signal 1702 leads the divided signals 1704 and 1708. In this case, the DAC 1732 increases the reference voltage 1734 (e.g., $V_{ref}$) to minimize the voltage difference between the reference voltage and the desired voltage. When both outputs of PD1 and PD2 are decrease voltage signals (e.g., "DOWN" signals), the reference signal 1702 is lagging the divided signals 1704 and 1708. In this case, the DAC 1732 decreases the reference voltage 1734. In the case where one phase detector generates an increase signal and another phase detector generates a decrease signal (e.g., where PD1 generates a DOWN signal and PD2 generates an UP signal), the reference voltage 1734 is very close to the desired control voltage. However, the present invention is not intended to be so limited.

Figure 18 illustrates a system for setting the reference voltage according to another embodiment of the invention. As shown in Figure 18, another preferred embodiment of a detector circuit 1850 includes an analog-to-digital circuit (ADC) 1820 and a digital-to-analog circuit (DAC) 1830. The first phase detector 1710, the second phase detector 1712, the first charge pump 1722, the second charge pump 1724 and the sample-and-hold circuit 1740 are described above. Accordingly, a description is omitted here. An output 1810 of the sample and hold circuit 1740, is transmitted to a VCO (not shown) and to the analog to digital converter 1820. An output 1822 of the analog to digital converter 1820 is received by the digital to analog converter 1830. The ADC 1820 determines the control voltage for comparison to a prescribed voltage and preferably sets the reference voltage 1840 (e.g., $V_{ref}$) through the DAC 1830. However, the present invention is not intended to be so limited. For example, the detector circuit 1850 can also be replaced with the detector circuit 1750 where the DAC 1732 output is controlled until it is comparable to a prescribed control voltage using the lock detector 1718 that receives the output voltage 1810 from the sample-and-hold circuit 1740.

Figure 19 illustrates a timing diagram that shows fractional compensation method of a sample-and-hold type fractional-N frequency synthesizer when the reference voltage in the sample-and-hold circuit is matched with the desired control voltage. For example, Figure 19 can show can show a phase relationship between the divided reference frequency 306 and the divided VCO frequencies 310, 312 of the frequency synthesizer 300 of Figure 3. In Figure 19, it is assumed that the fractional number is 3/8 (K=3, N=8) as described above. The relative voltage waveforms are the divided reference frequency 1902, the Divider Output1 1904, the Divider Output2 1906, the PD1 output 1908, the PD2 output 1910, and the control voltage 1918 are shown. The number of enabled charge pumps 1912 and 1916, and the fractional accumulator state 1614, are also indicated relative to the waveforms.

As shown in Figure 19, the reference signal is between the divided signals. Thus, the charge pumps (CP1) coupled to PD1 always sink current from the sample-and-hold circuit while those (CP2) coupled to PD2 always source current to the sample-and-hold circuit of the frequency synthesizer. The amount of charging and discharging is accurately matched through Equation 3 and the control voltage is kept constant. According to Equation 3, the amount of discharging current by the CP1 is given by the equation:

$$Q_{discharge}=I_{discharge}*T_{discharge}=\{(N-K)*(I/N)\}*\{(K/N)*T_{VCO}\} \qquad \text{(Eq. 1)}$$

where K represents the accumulator state. Similar to Eq. 1, the amount of charging current by the CP2 is given by the equation:

$$Q_{charge}=I_{charge}*T_{charge}=\{K*(I/N)\}*[\{(N-K)/N\}*T_{VCO}] \quad \text{(Eq. 2)}$$

From (Eq. 1) and (Eq. 2), $Q_{charge}$ and $Q_{discharge}$ are always the same.

As described above, preferred embodiments of a frequency synthesizer according to the present invention have various advantages. Preferred embodiments of a phase-locked loop (PLL) frequency synthesizer incorporate a sample-and-hold circuit in a fractional-N type synthesizer. The preferred embodiments reduce a circuit size and power requirements because a sample-and-hold circuit replaces a related art loop-filter capacitor in a fractional-N type frequency synthesizer. A frequency synthesizer including a phase-locked loop (PLL) according to the preferred embodiments also incorporates fractional spur compensation circuitry to dynamically compensate charge pump ripple whenever a charge pump operates. In the preferred embodiments, a programmable divider produces two output signals that are preferably divided signals from a voltage controlled oscillator (VCO) with a phase difference being a period of the VCO output. In a locked state of a frequency synthesizer, the phase of the corresponding reference signals occurs between the two divider signals. In a preferred embodiment, two phase detectors (PD) are used each receiving the reference signal and one of the two divided VCO signals so that one phase detector can produce a voltage increase signal and the other phase detector can produce a voltage decrease signal in the locking stage.

A charge pump block can include N equal charge pump stages and can be coupled to one or both phase detector output terminals, and an output of each charge pump is combined in the sample-and-hold circuit. In the locking state, the amount of charging current and discharging current substantially compensate each other. Hence, no fractional ripple occurs. Thus, fractional compensation is dynamic and robust to the environmental changes such as circuit age, process and temperature in the preferred embodiments according to the present invention. Preferred embodiments of a frequency synthesizer can be implemented using a plurality of phase detectors with a sample-and-hold circuit to provide a uniform stable VCO control voltage.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.

WHAT IS CLAIMED IS:

1. A phase locked loop, comprising:

a first phase detector that receives an input signal and a first divided signal to output a first comparison signal;

a second phase detector that receives the input signal and a second divided signal to output a second comparison signal;

a circuit that receives the first and second comparison signals and generates an output signal responsive to the comparison signals;

a voltage-controlled oscillator that receives the output signal from the circuit and generates a prescribed frequency signal; and

a programmable modulus divider that receives the prescribed frequency signal and generates the first and second divided signals having a prescribed phase relationship.

2. The phase-locked loop of claim 1, further comprising a plurality of parallel switches operated by a control line, wherein each of the switches couple a corresponding one of a plurality of charge pumps to a selected one of the first and second comparison signals, depending on the position of said each switch.

3. The phase-locked loop of claim 2, wherein each of the charge pumps performs one of sourcing and sinking a prescribed amount of current to the circuit.

4. The phase-locked loop of claim 1, wherein the first phase detector comprises:

a phase detector portion with a first output port and a second output port; and

a charge pump portion having a plurality of charge pump stages.

5. The phase-locked loop of claim 4, wherein each of the charge pump stages comprises:

a first current source and a first switch coupled in series between a first prescribed voltage and a charge pump output terminal;

a second current source and a second switch coupled in series between a second prescribed voltage and the charge pump output terminal;

a first logic gate with a first input coupled to the first output port of the phase detector portion, a second input that receives a control signal and an output port coupled to the first switch; and

a second logic gate with a first input coupled to the second output port of the phase detector portion, a second input that receives the control signal and an output port coupled to the second switch.

6. The phase-locked loop of claim 5, wherein the first and second logic gates are AND gates, wherein an output of the first and second AND gates select one of the first and second switches to couple the charge pump output terminal to one of the first and second current sources.

7. The phase-locked loop of claim 1, further comprising a signal delay device coupled to delay one of the input signal with the divided signal and the comparison signal for one of the first and second phase detectors.

8. The phase-locked loop of claim 1, further comprising a signal delay device coupled to one of the first and second phase detectors.

9. The phase-locked loop of claim 8, wherein the signal delay device is one of a digital delay control circuit and an analog delay control circuit.

10. The phase-locked loop of claim 1, wherein the first and second divided signals have the same frequency.

11. The phase-locked loop of claim 1, wherein the programmable modulus divider comprises:

a first logic gate;

a second logic gate that receives a control signal;

a first flip-flop coupled to receive an output signal of the first logic gate and a clock signal from the output port of the voltage-controlled oscillator;

a second flip-flop gate coupled to receive an output signal of the first flip-flop, wherein the first and second logic gates receive an output signal of the second flip- flop; and

a third flip-flop coupled to receive an output signal from the second logic gate, wherein the first, second and third flip-flops receive the prescribed frequency signal as a clock signal, wherein an output signal of the third flip-flop is received by the first logic gate, and wherein the output signals of the first and second flip-flops are the divided signals.

12. The phase-locked loop of claim 11, wherein the first and second divided signals differ in phase by a period of the clock signal.

13. The phase-locked loop of claim 1, further comprising a detection circuit coupled to adjust a reference voltage in the circuit.

14. The phase-locked loop of claim 1, wherein the circuit is a sample-and-hold circuit that comprises:

a first switch and a first capacitor coupled at a first node in series between first and second prescribed reference voltages, wherein the first node is coupled to receive the first and second comparison signals;

a second capacitor coupled between the second reference voltage and a second node; and

a switch coupled between the first and second nodes.

15. The phase-locked loop of claim 14, further comprising a detection circuit that sets the first prescribed reference voltage.

16. The phase-locked loop of claim 15, wherein the detection circuit comprises:

a lock detector that receives the comparison signals from the first and second phase detectors; and

a digital-to-analog converter that adjusts a voltage level of the first prescribed reference voltage responsive to a control signal from the lock detector.

17. The phase-locked loop of claim 15, wherein the detection circuit comprises:

an analog-to-digital converter that receives the output of the sample-and-hold circuit; and

a digital-to-analog converter that adjusts a voltage level of the first prescribed reference voltage responsive to a control signal from the analog-to-digital converter.

18. The phase-locked loop of claim 15, wherein the detection circuit comprises:

a lock detector that receives the output signal from the sample-and-hold circuit; and

a digital-to-analog converter that adjusts a voltage level of the first prescribed reference voltage responsive to a control signal from the lock detector.

19. The phase-locked loop of claim 1, wherein the first and second divided signals have the same frequency, wherein the first and second divided signals differ in phase

by a period of the clock signal, and wherein the first phase detector and the second phase detector are of the same design.

20. A fractional-N frequency synthesizer for a mobile terminal, comprising:

a phase detector circuit that comprises,

a first phase detector having a first input port coupled to receive a reference signal, a second input port, a third input port and an output port, and

a second phase detector having a first input port coupled to receive the reference signal, a second input port, a third input port and an output port;

a circuit having a first input port coupled to the output ports of the first and second phase detectors and an output port;

a voltage-controlled oscillator having an input port coupled to the output port of the circuit and transmitting a prescribed frequency signal at an output port;

a programmable modulus divider having a first output port coupled to the second input port of the first phase detector to transmit a first divided signal, a second output port coupled to the second input port of the second phase detector to transmit a second divided signal, a first input port coupled to the output port of the voltage-controlled oscillator and a second input port; and

an accumulator having a first output port coupled to the second input port of the programmable modulus divider and a second output port coupled to the third input ports of the phase detectors.

21. The fractional-N frequency synthesizer of claim 20, wherein the mobile terminal is one of a cellular phone, a personal digital assistant, a digital audio player, an Internet appliance, a remote control device and a laptop computer.

22. The fractional-N frequency synthesizer of claim 20, further comprising a plurality of switches operated by a control line, wherein each of the switches couple a

corresponding one of a plurality of charge pumps to the output port of a selected one of the first phase detector and the second phase detector according to a control signal from the accumulator.

23. The fractional-N frequency synthesizer of claim 20, wherein the first phase detector and the second phase detector are of the same design.

24. The fractional-N frequency synthesizer of claim 20, wherein the first phase detector comprises:

a phase detector portion with a first output port and a second output port; and

a charge pump portion having a plurality of charge pump stages.

25. The fractional-N frequency synthesizer of claim 24, wherein each of the charge pump stages comprises:

a first current source and a first switch coupled in series between a first prescribed voltage and a charge pump output terminal;

a second current source and a second switch coupled in series between a second prescribed voltage and the charge pump output terminal;

a first logic gate with a first input port coupled to the first output port of the phase detector portion, a second input that receives a control signal and an output port coupled to the first switch; and

a second logic gate with a first input coupled to the second output port of the phase detector portion, a second input that receives the control signal and an output port coupled to the second switch.

26. The fractional-N frequency synthesizer of claim 20, further comprising a signal delay device coupled to delay one of the input signal with the divided signal and the comparison signal for one of the first and second phase detectors.

27. The fractional-N frequency synthesizer of claim 20, further comprising a signal delay device coupled to one of the first and second phase detectors.

28. The fractional-N frequency synthesizer of claim 20, wherein the programmable modulus divider comprises:

a first logic gate;

a second logic gate that receives a control signal;

a first flip-flop coupled to receive an output signal of the first logic gate and a clock signal from the output port of the voltage-controlled oscillator;

a second flip-flop gate coupled to receive an output signal of the first flip-flop, wherein the first and second logic gates receive an output signal of the second flip- flop;

a third flip-flop coupled to receive an output signal from the second logic gate, wherein the first, second and third flip-flops receive the prescribed frequency signal as a clock signal, wherein an output signal of the third flip-flop is received by the first logic gate, and wherein the output signals of the first and second flip-flops are the divided signals.

29. The fractional-N frequency synthesizer of claim 20, wherein the first and second divided signals have the same frequency, and wherein the first and second divided signals differ in phase by the period of the prescribed frequency signal from the output port of the voltage-controlled oscillator.

30. The phase-locked loop of claim 20, wherein the circuit is a sample-and-hold circuit that comprises:

a first switch and a first capacitor coupled at a first node in series between first and second prescribed reference voltages, wherein the first node is coupled to receive first and second comparison signals from the output ports of the phase detectors;

a second capacitor coupled between the second reference voltage and a second node; and

a switch coupled between the first and second nodes.

31. The phase-locked loop of claim 30, further comprising a detection circuit that sets the first prescribed reference voltage.

32. The phase-locked loop of claim 31, wherein the detection circuit comprises:

a lock detector that receives the comparison signals from the first and second phase detectors; and

a digital-to-analog converter that adjusts a voltage level of the first prescribed reference voltage responsive to a control signal from the lock detector.

33. The phase-locked loop of claim 31, wherein the detection circuit comprises:

an analog-to-digital converter that inputs an output signal of the sample-and-hold circuit; and

a digital-to-analog converter that adjusts a voltage level of the first prescribed reference voltage responsive to a control signal from the analog-to-digital converter.

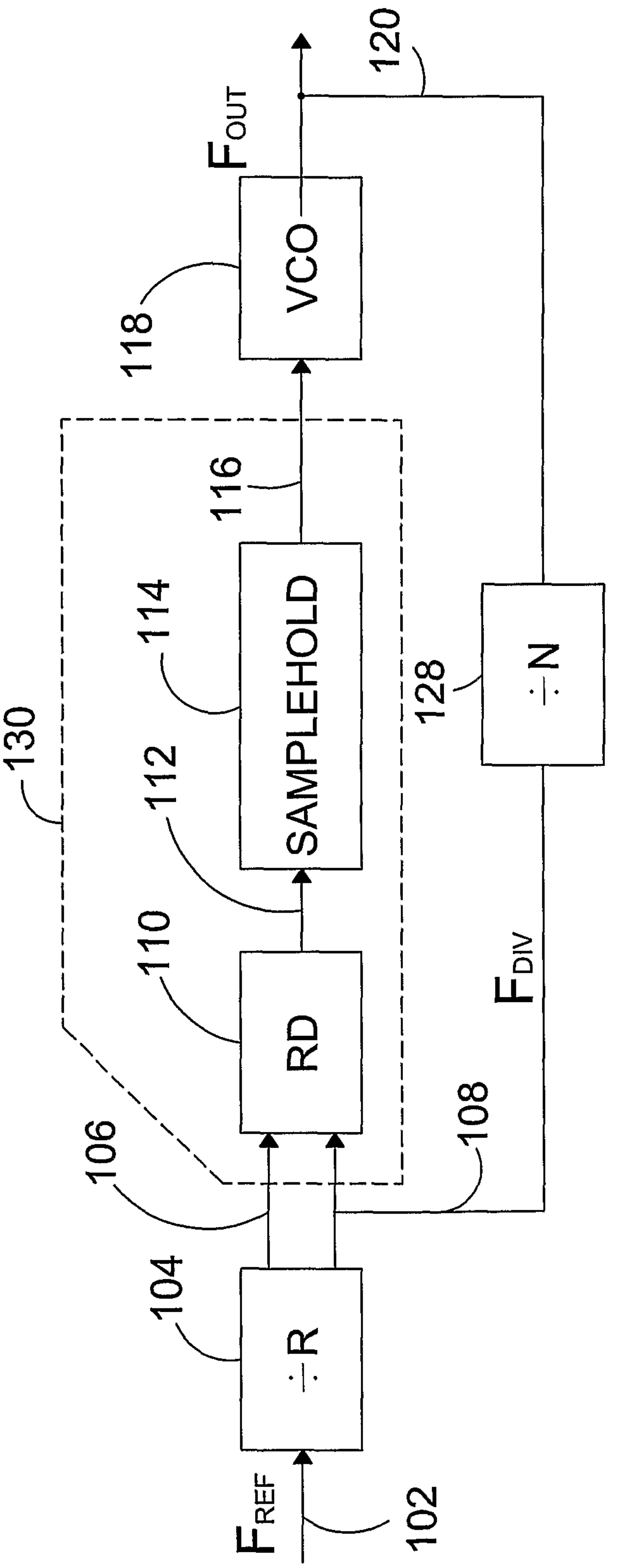
FOUT
120
VCO
118
116
SAMPLEHOLD
114
112
130
128
÷N
RD
110
FDIV
106
108
104
÷R
FREF
102

FIG. 1

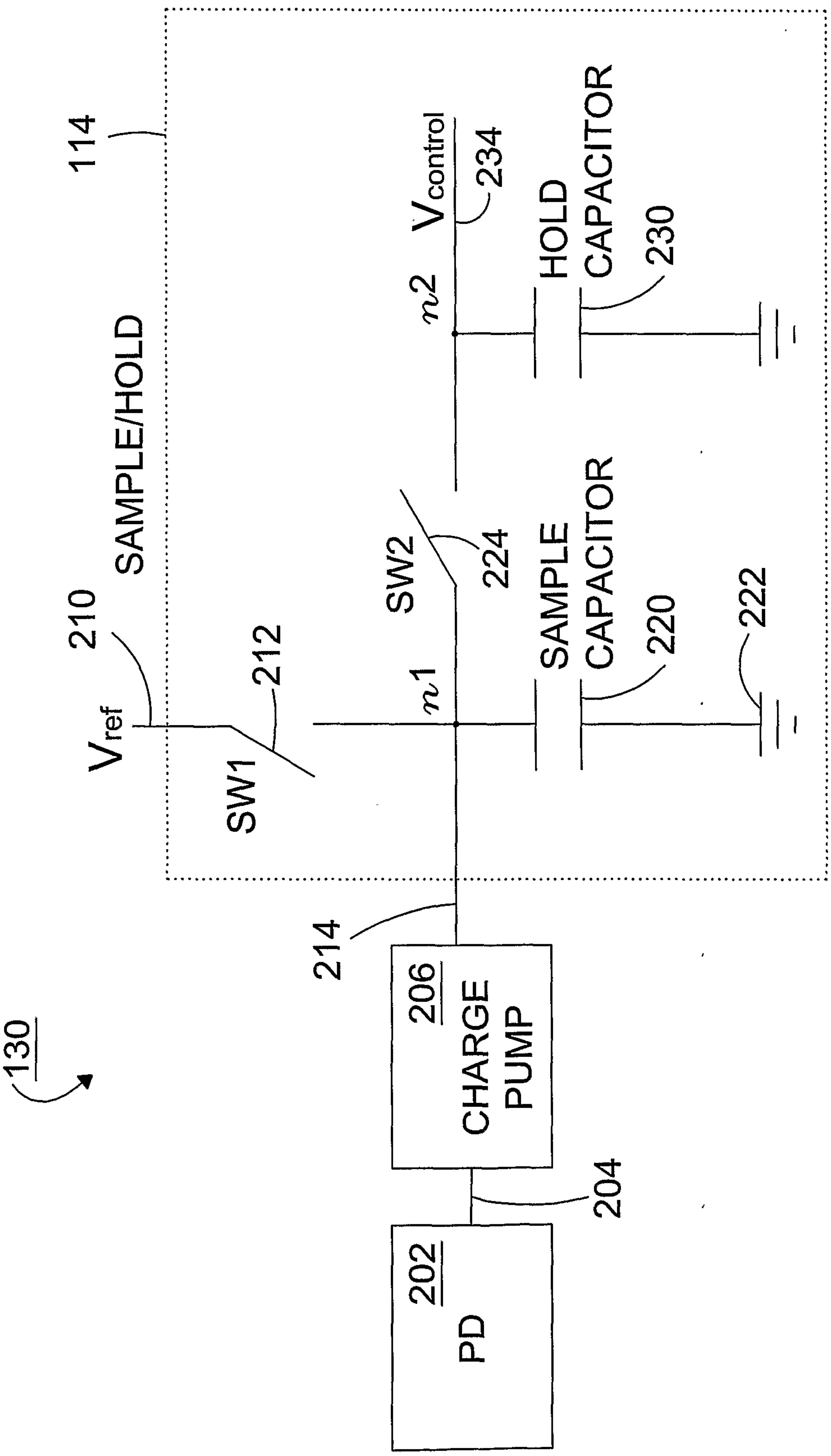
130
114
SAMPLE/HOLD
$V_{ref}$
210
SW1
212
$n1$
SW2
224
SAMPLE
CAPACITOR
220
222
$n2$
$V_{control}$
234
HOLD
CAPACITOR
230
214
206
CHARGE
PUMP
204
202
PD

FIG. 2(a)

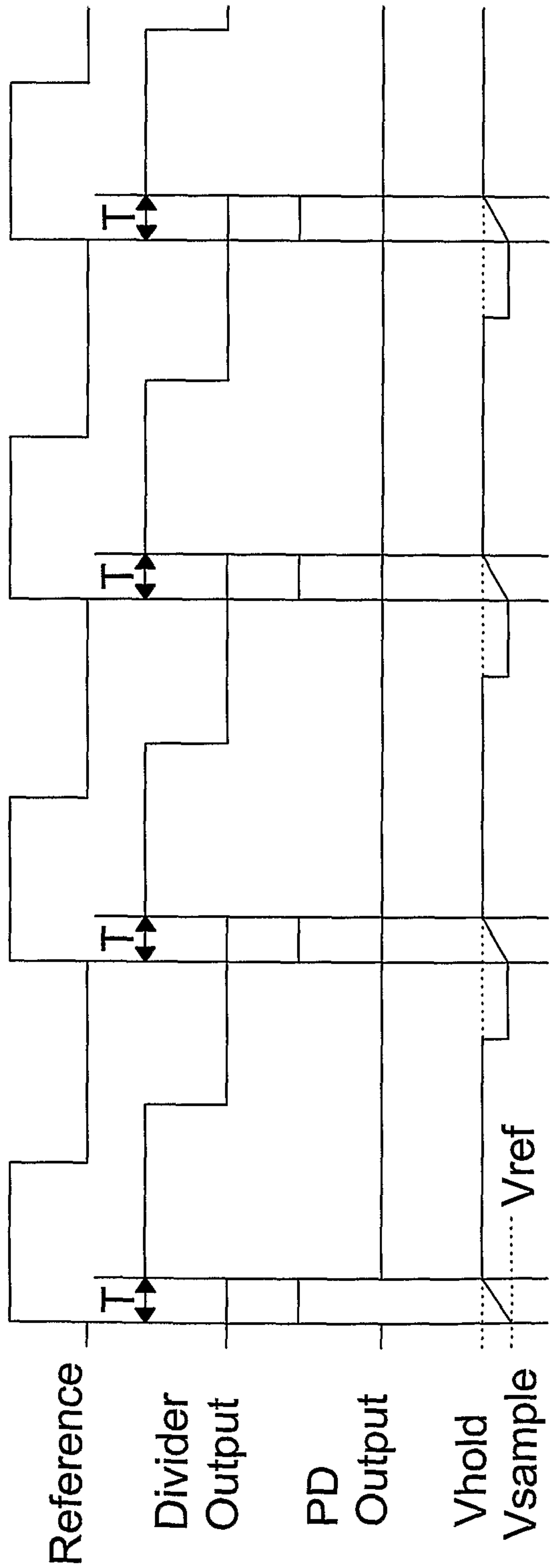
Reference
Divider Output
PD Output
Vhold
Vsample
Vref
T
T
T
T

FIG. 2(b)

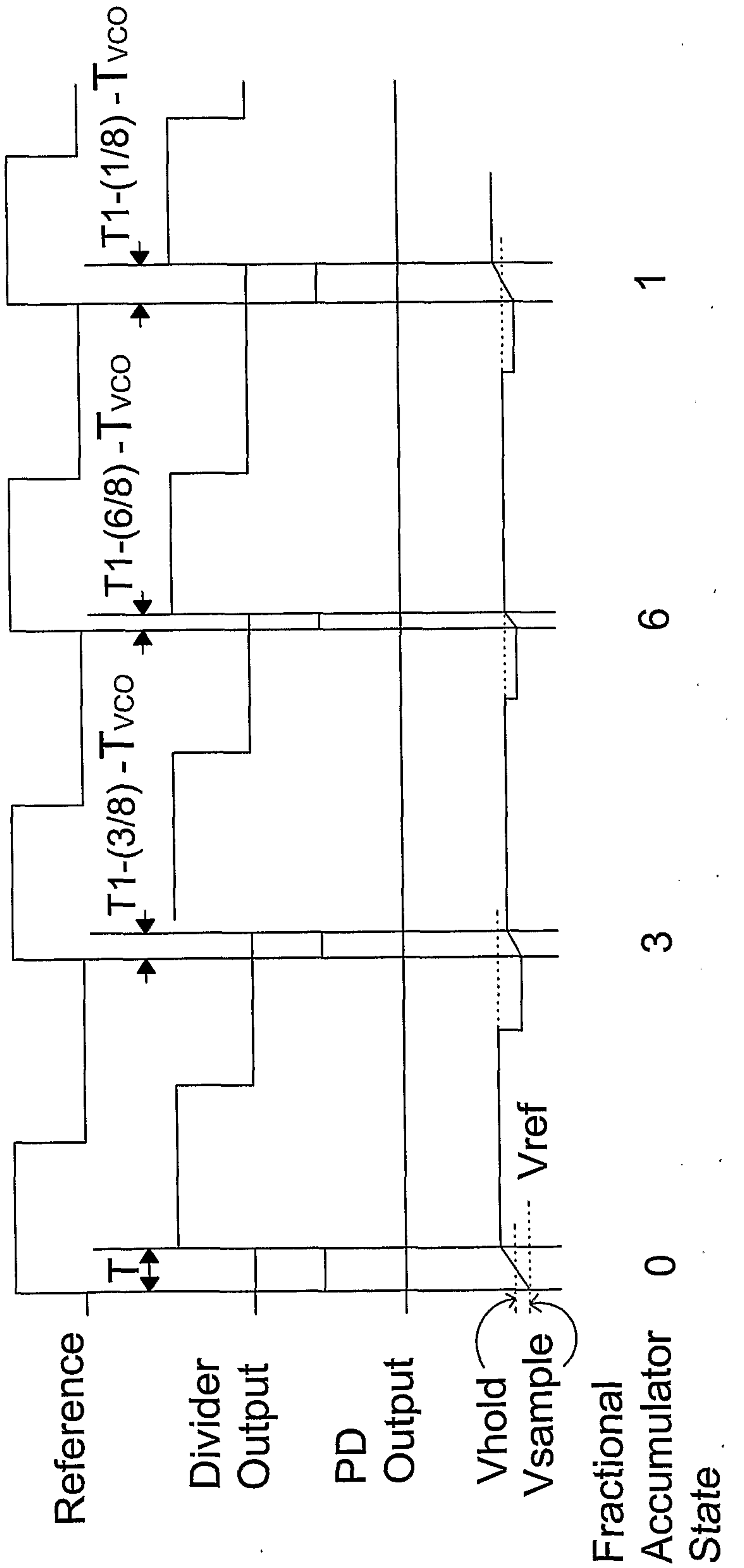
Reference
Divider Output
PD Output
Vhold
Vsample
Vref
Fractional Accumulator State
T
T1-(3/8) -TVCO
T1-(6/8) -TVCO
T1-(1/8) -TVCO
0
3
6
1

FIG. 2(c)

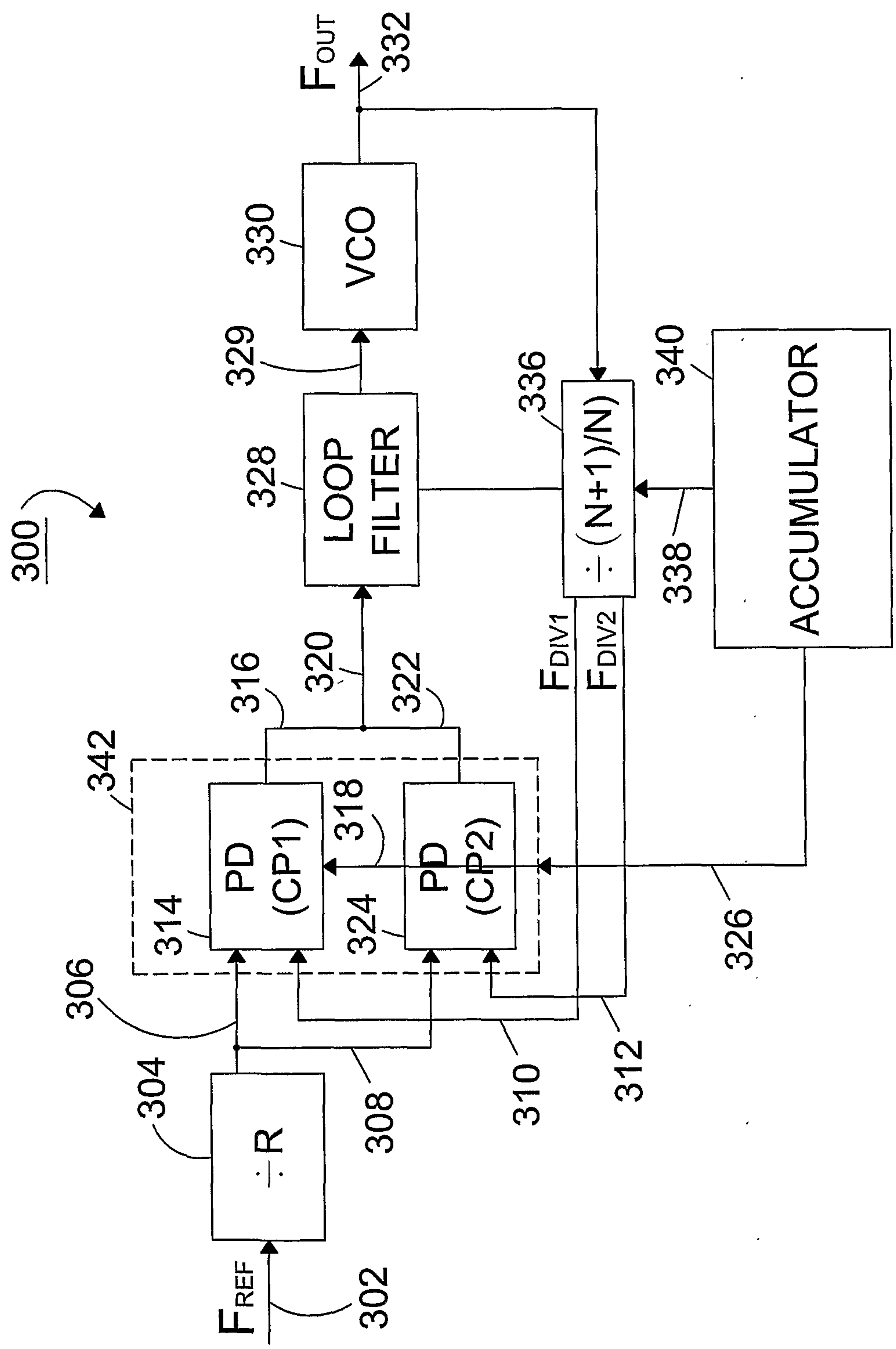
300
FOUT
332
330
VCO
329
328
LOOP FILTER
336
÷ (N+1)/N)
340
ACCUMULATOR
338
316
320
322
FDIV1
FDIV2
342
PD (CP1)
318
PD (CP2)
314
324
326
306
304
÷R
308
310
312
FREF
302

FIG. 3

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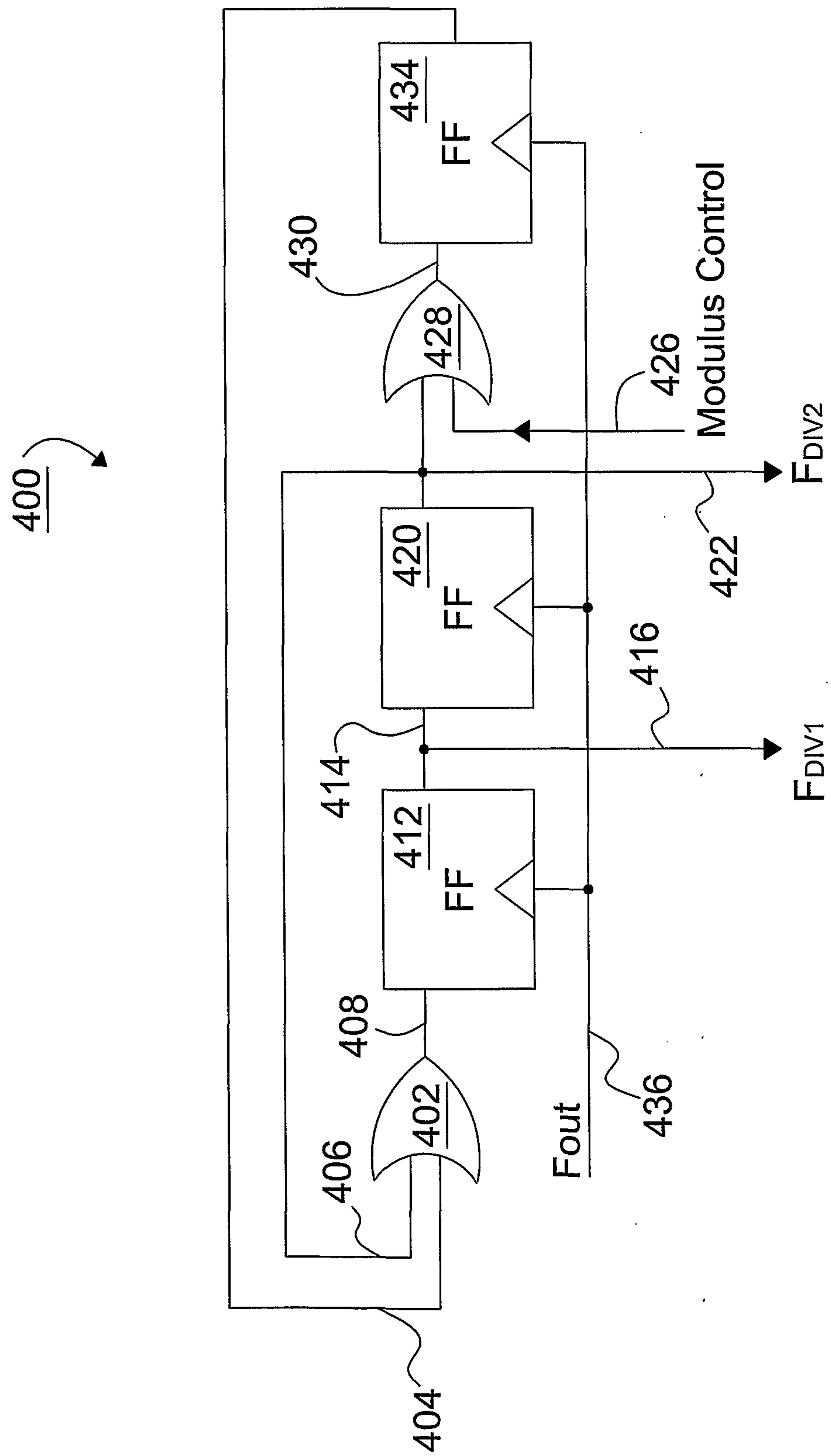

400
434
FF
430
428
426
Modulus Control
FDIV2
422
420
FF
416
FDIV1
414
412
FF
408
402
406
Fout
436
404

FIG. 4

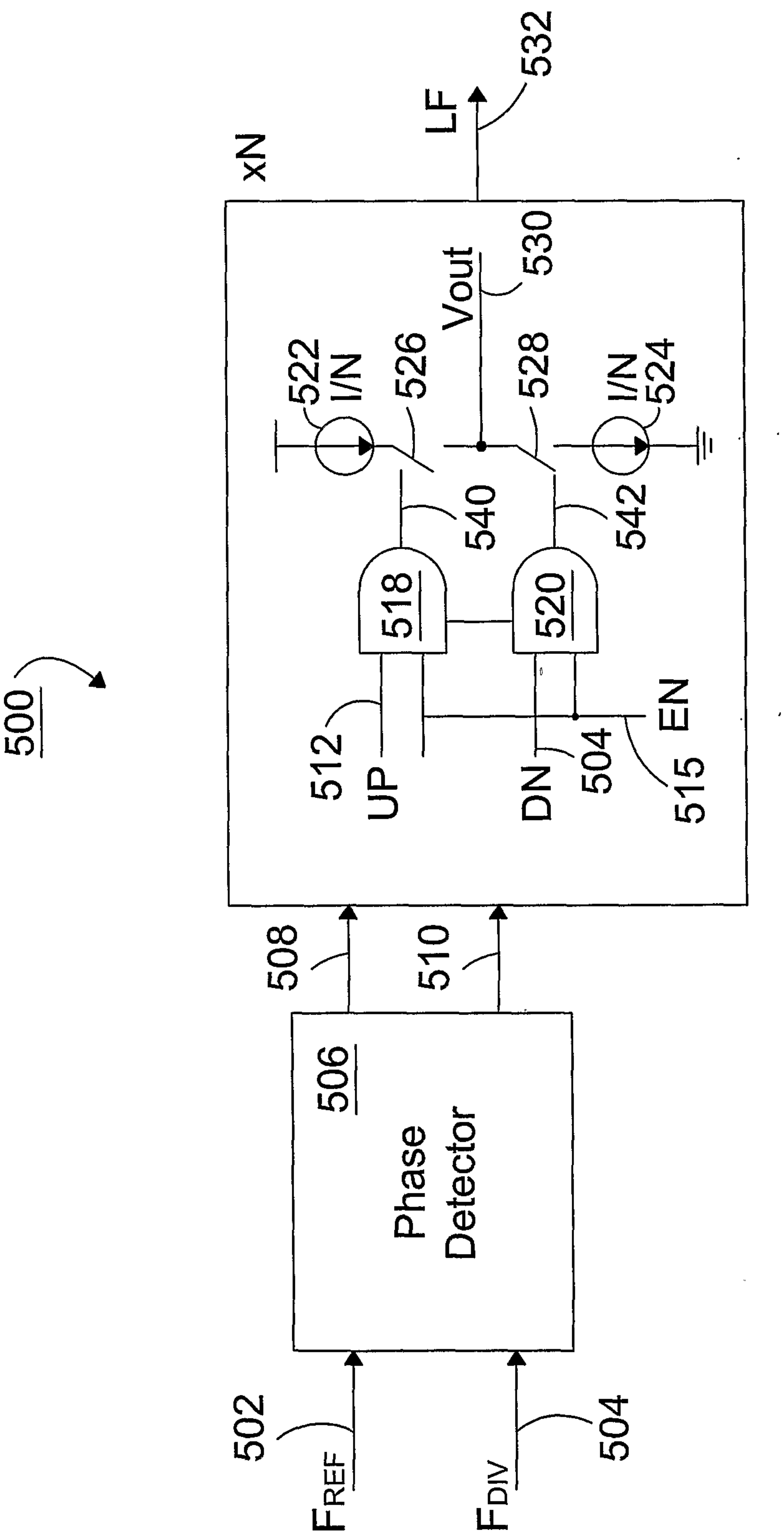

500
xN
LF
532
Vout
530
522
I/N
526
528
I/N
524
540
542
518
520
UP
512
DN
504
EN
515
508
510
506
Phase Detector
502
504
$F_{REF}$
$F_{DIV}$

FIG. 5

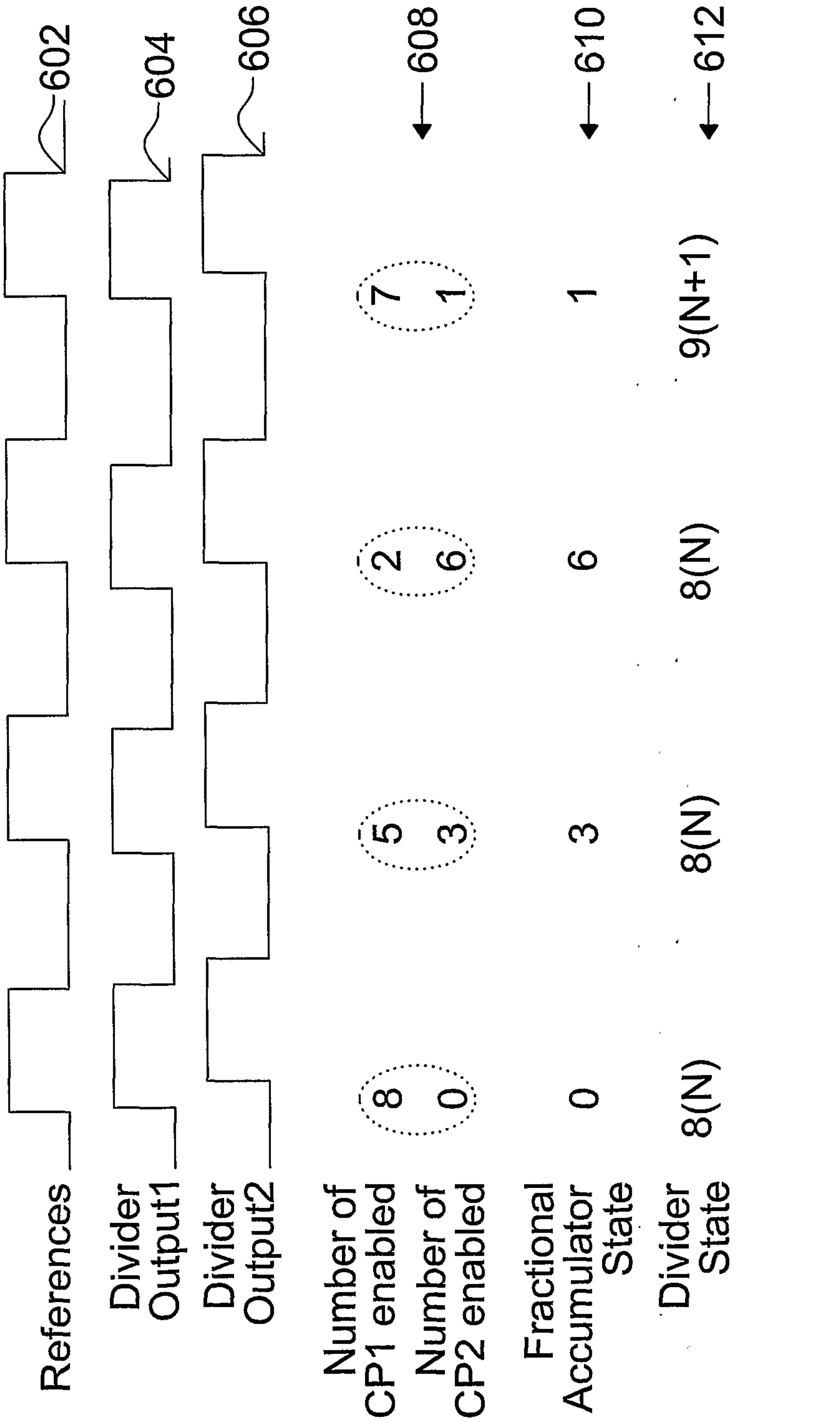

References
Divider Output1
Divider Output2
Number of CP1 enabled
Number of CP2 enabled
Fractional Accumulator State
Divider State
8
0
0
8(N)
5
3
3
8(N)
2
6
6
8(N)
7
1
1
9(N+1)
602
604
606
608
610
612

FIG. 6

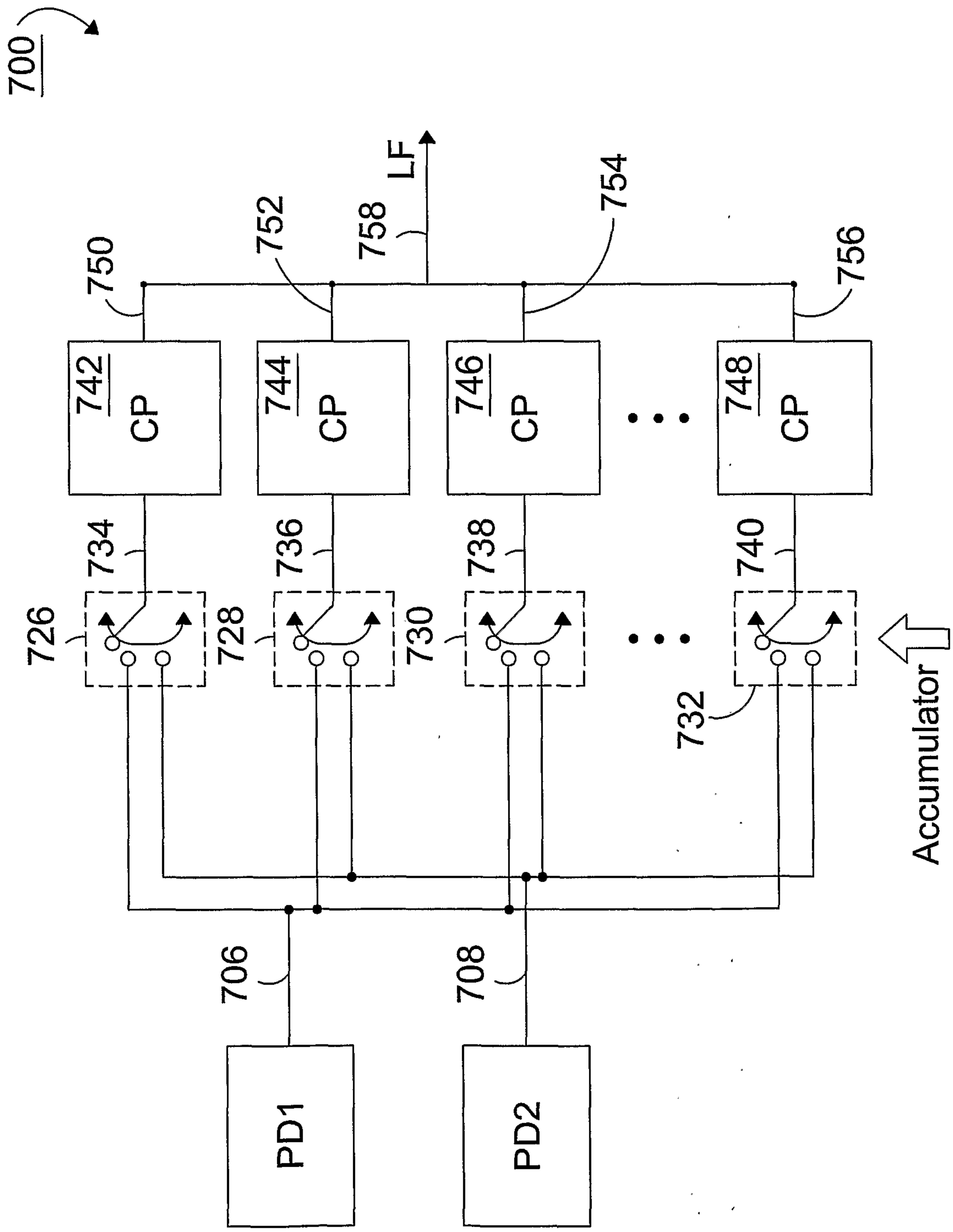

700
LF
750
752
758
754
756
742
CP
744
CP
746
CP
748
CP
734
736
738
740
726
728
730
732
Accumulator
706
708
PD1
PD2

FIG. 7

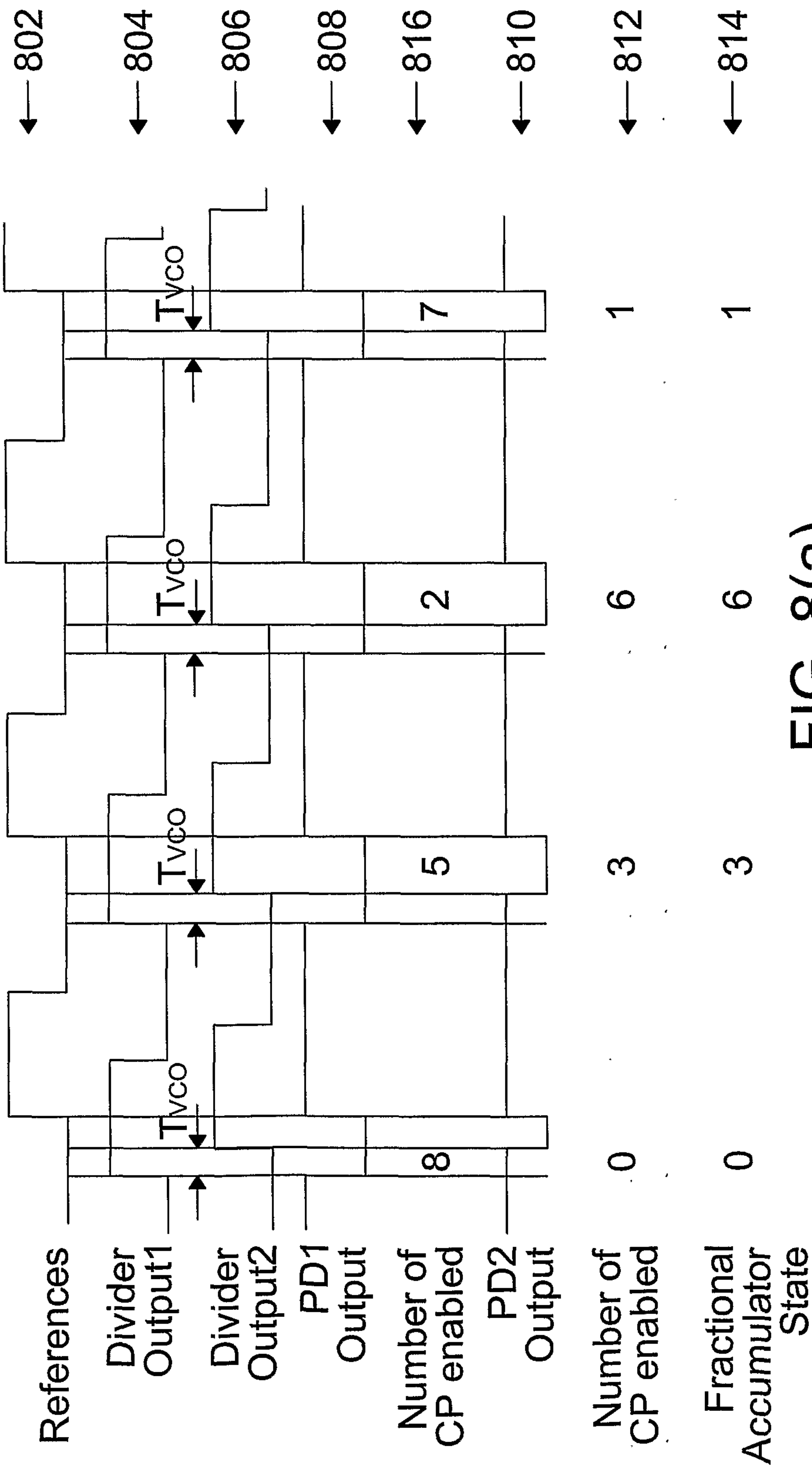

References
Divider Output1
Divider Output2
PD1 Output
Number of CP enabled
PD2 Output
Number of CP enabled
Fractional Accumulator State
802
804
806
808
816
810
812
814
$T_{VCO}$
8
5
2
7
0
3
6
1
0
3
6
1

FIG. 8(a)

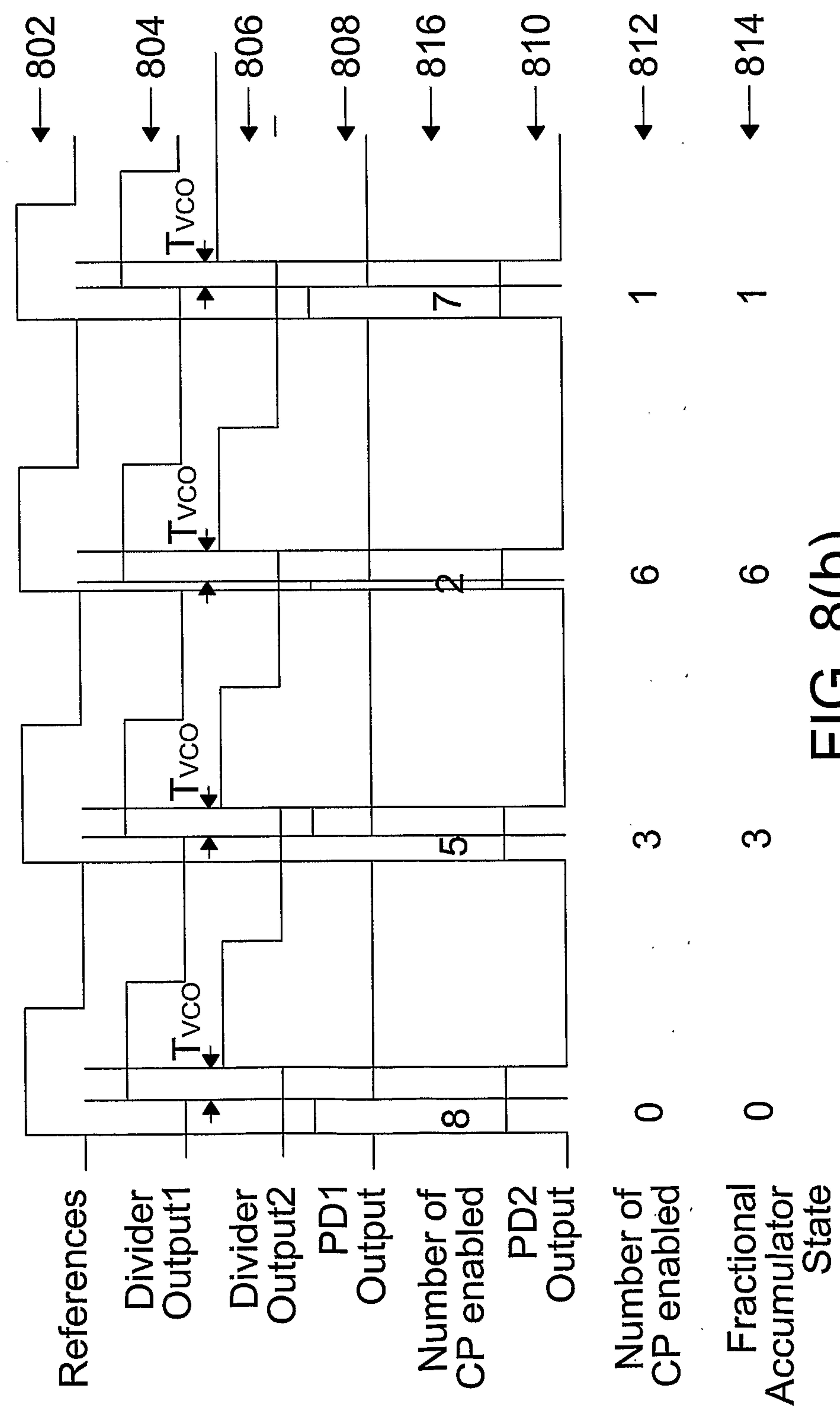

References
Divider Output1
Divider Output2
PD1 Output
Number of CP enabled
PD2 Output
Number of CP enabled
Fractional Accumulator State
802
804
806
808
816
810
812
814
TVCO
TVCO
TVCO
TVCO
8
5
2
7
0
3
6
1
0
3
6
1

FIG. 8(b)

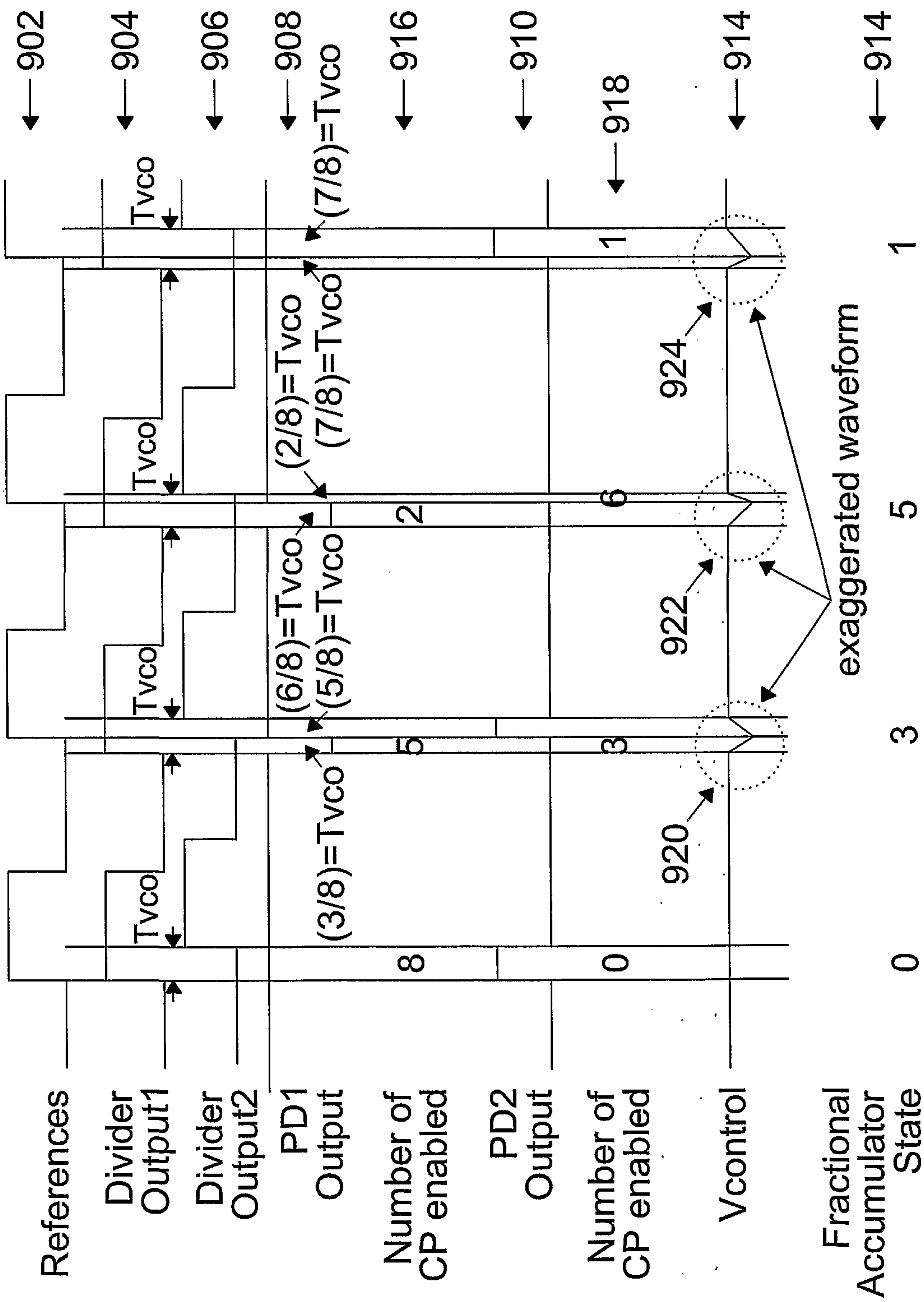

References
Divider Output1
Divider Output2
PD1 Output
Number of CP enabled
PD2 Output
Number of CP enabled
Vcontrol
Fractional Accumulator State
902
904
906
908
916
910
918
914
914
Tvco
Tvco
Tvco
Tvco
(3/8)=Tvco
(6/8)=Tvco
(5/8)=Tvco
(2/8)=Tvco
(7/8)=Tvco
(7/8)=Tvco
8
5
2
1
0
3
6
1
0
3
5
1
920
922
924
exaggerated waveform

FIG. 9

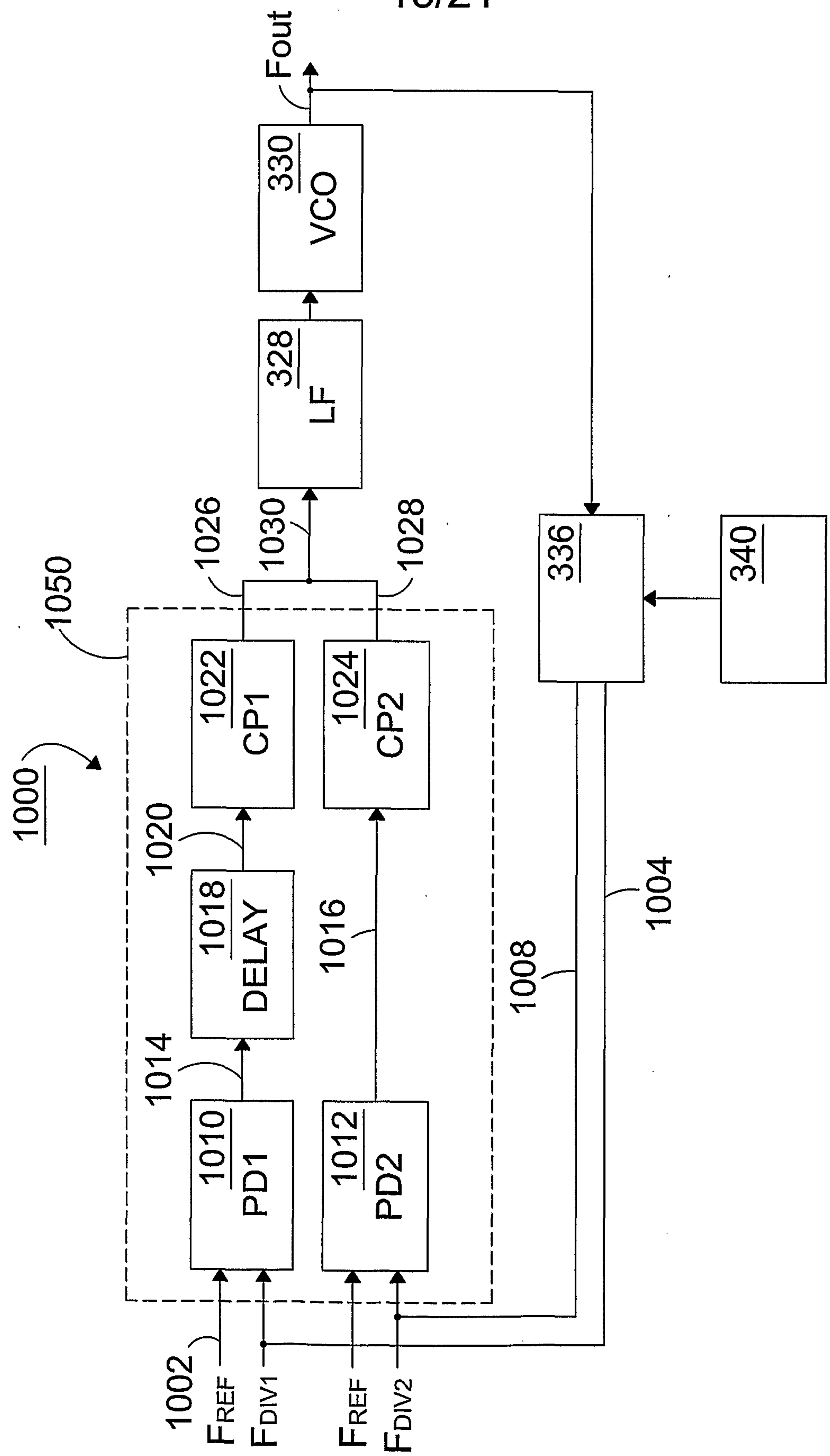

Fout
330
VCO
328
LF
1026
1030
1028
1050
1000
1022
CP1
1024
CP2
336
340
1020
1018
DELAY
1016
1008
1004
1014
1010
PD1
1012
PD2
1002
$F_{REF}$
$F_{DIV1}$
$F_{REF}$
$F_{DIV2}$

FIG. 10

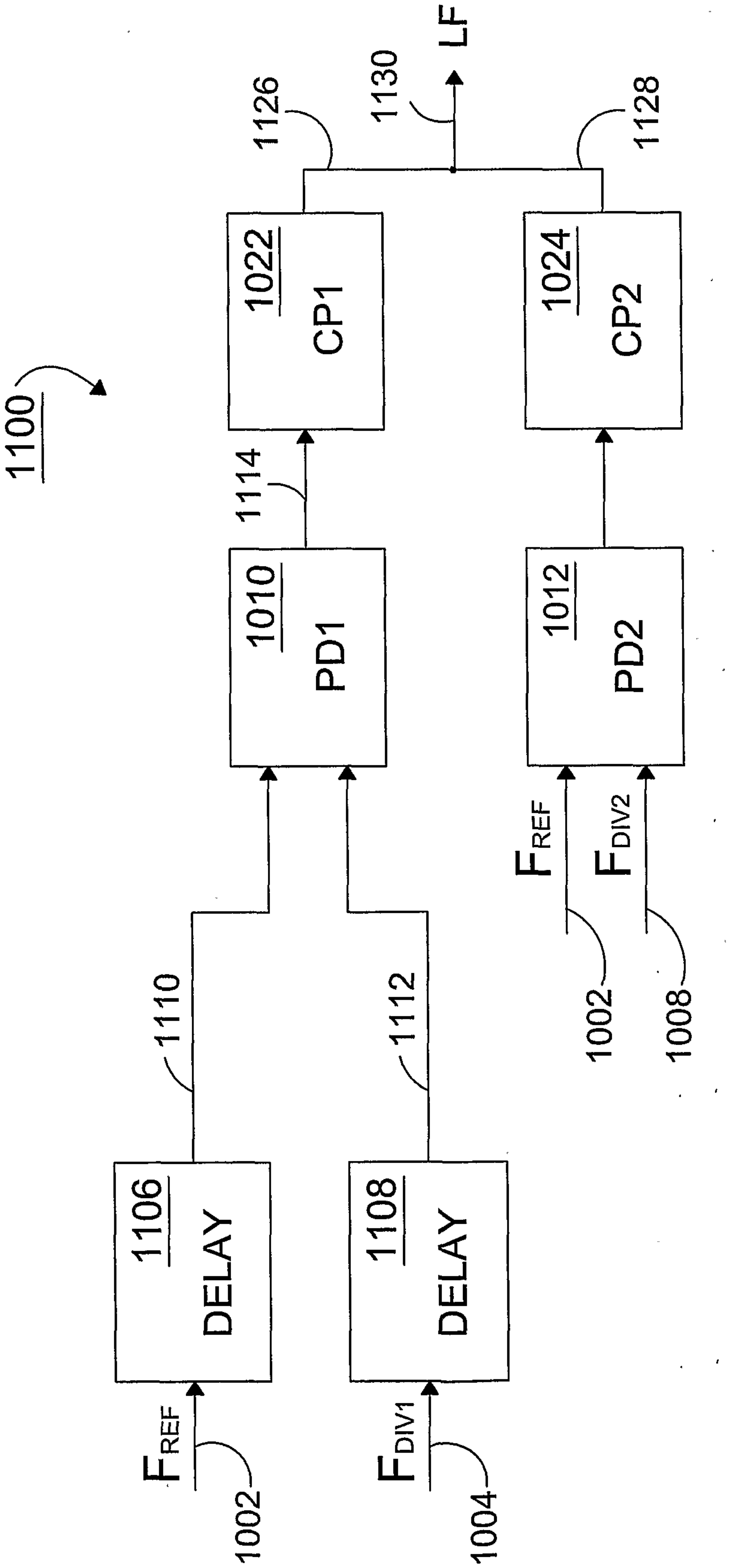

1100
LF
1130
1126
1128
1022
CP1
1024
CP2
1114
1010
PD1
1012
PD2
F_REF
F_DIV2
1002
1008
1110
1112
1106
DELAY
1108
DELAY
F_REF
F_DIV1
1002
1004

FIG. 11

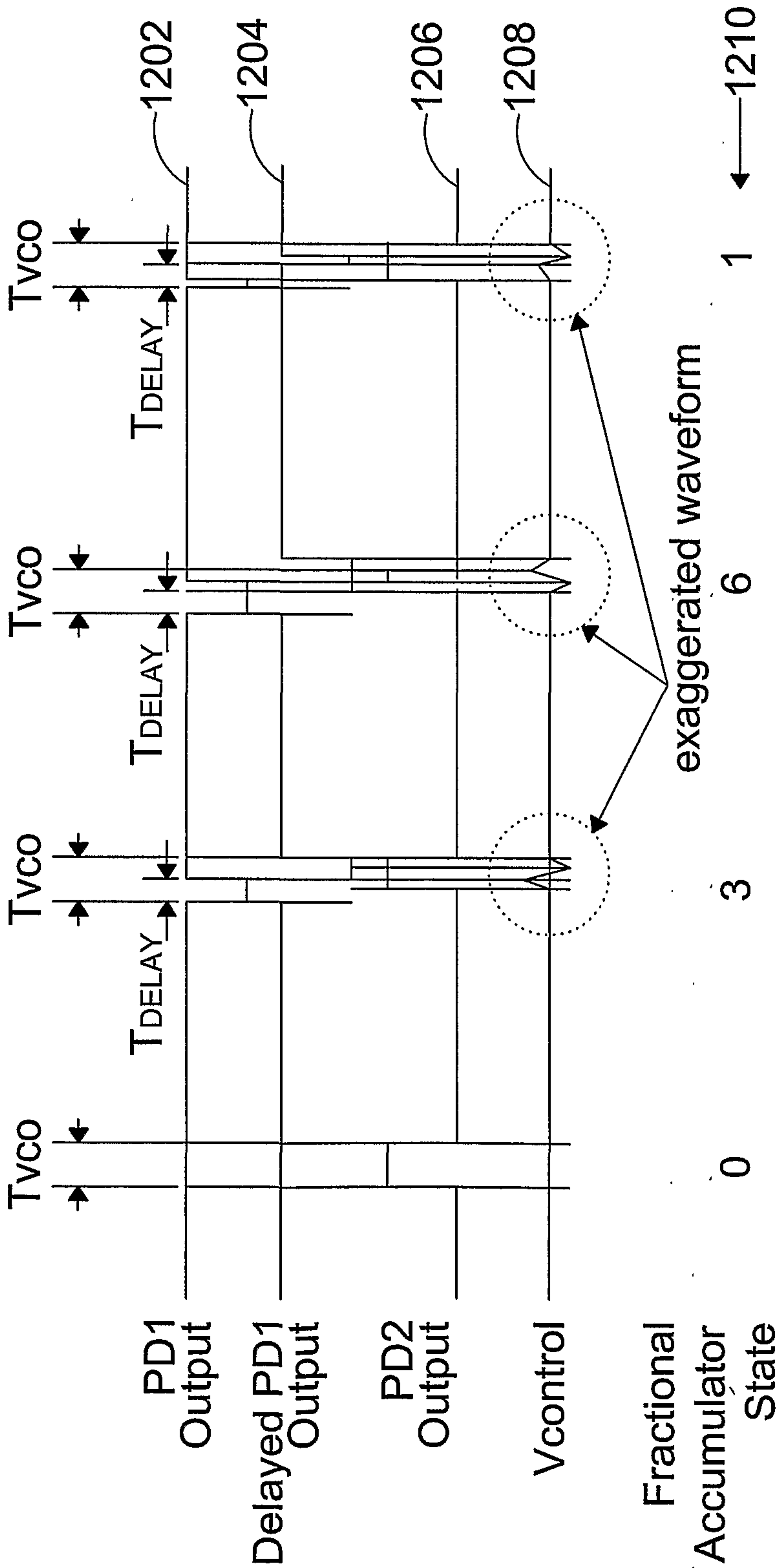

1202
1204
1206
1208
1210
Tvco
TDELAY
exaggerated waveform
1
6
3
0
PD1 Output
Delayed PD1 Output
PD2 Output
Vcontrol
Fractional Accumulator State

FIG. 12

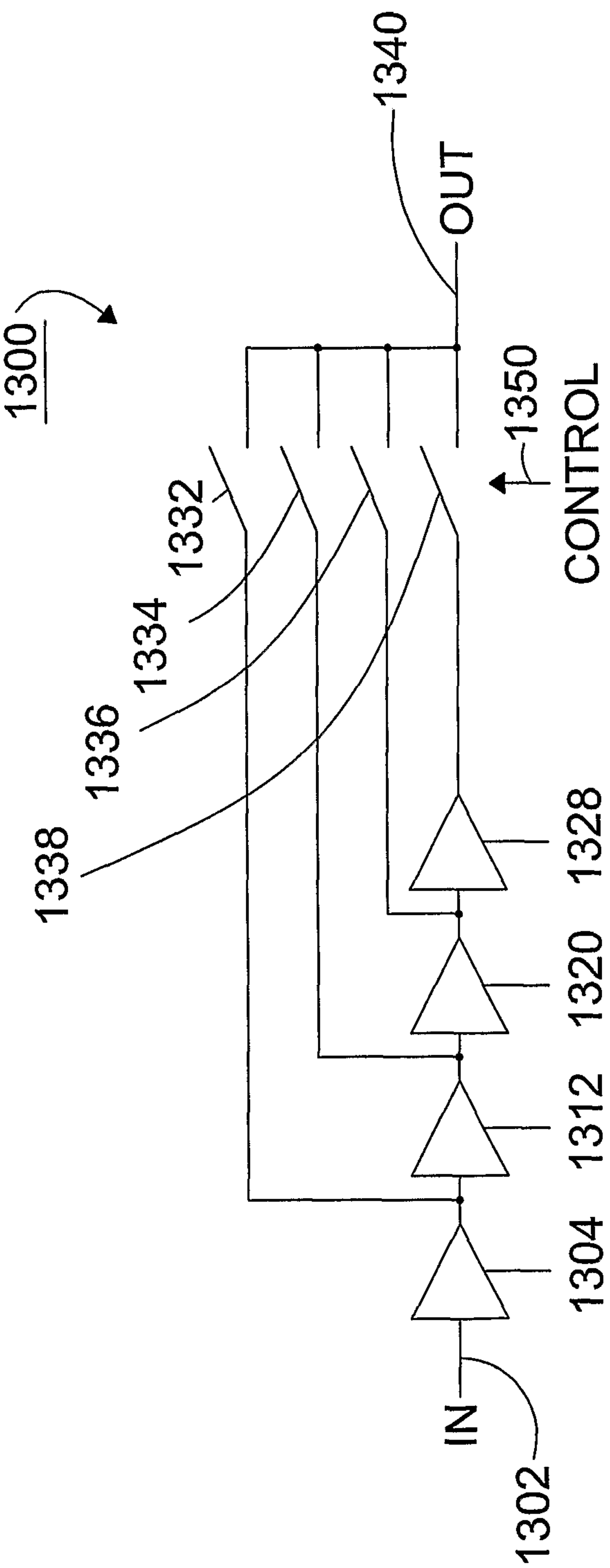

1300
1340
OUT
1350
CONTROL
1332
1334
1336
1338
1328
1320
1312
1304
IN
1302

FIG. 13

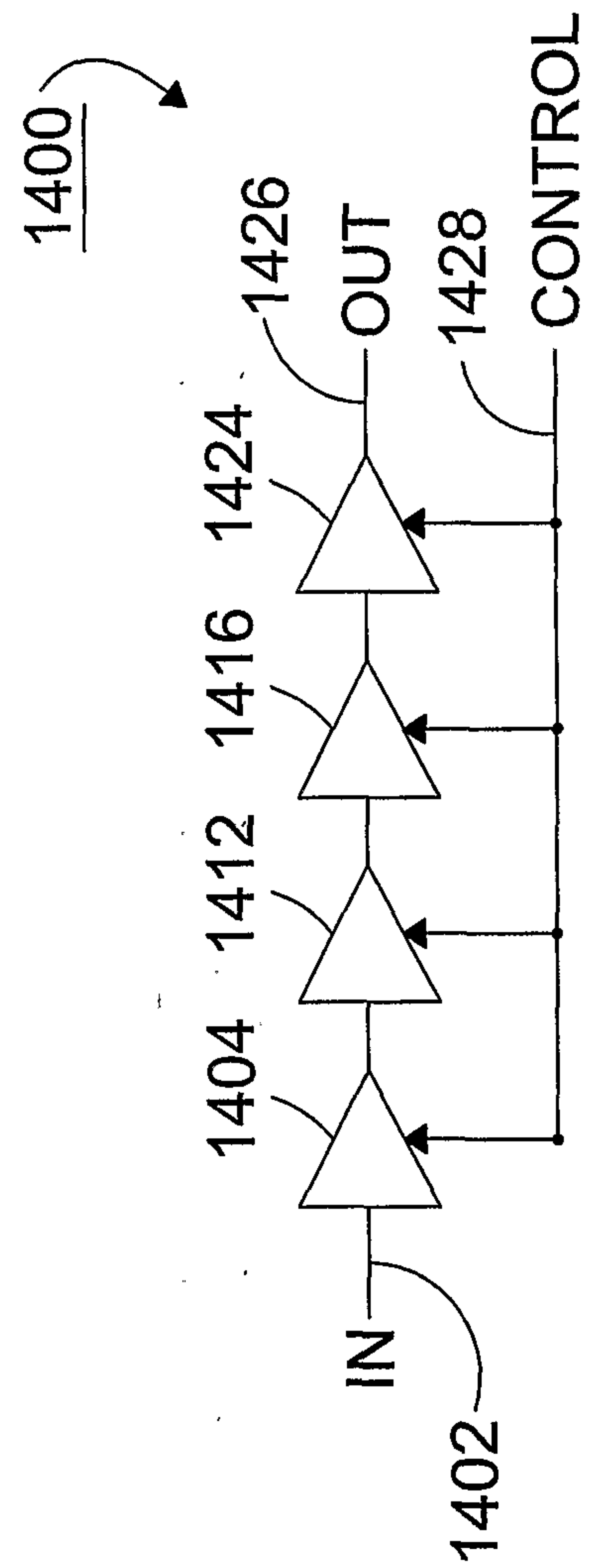

1400
1426
OUT
1428
CONTROL
1424
1416
1412
1404
IN
1402

FIG. 14

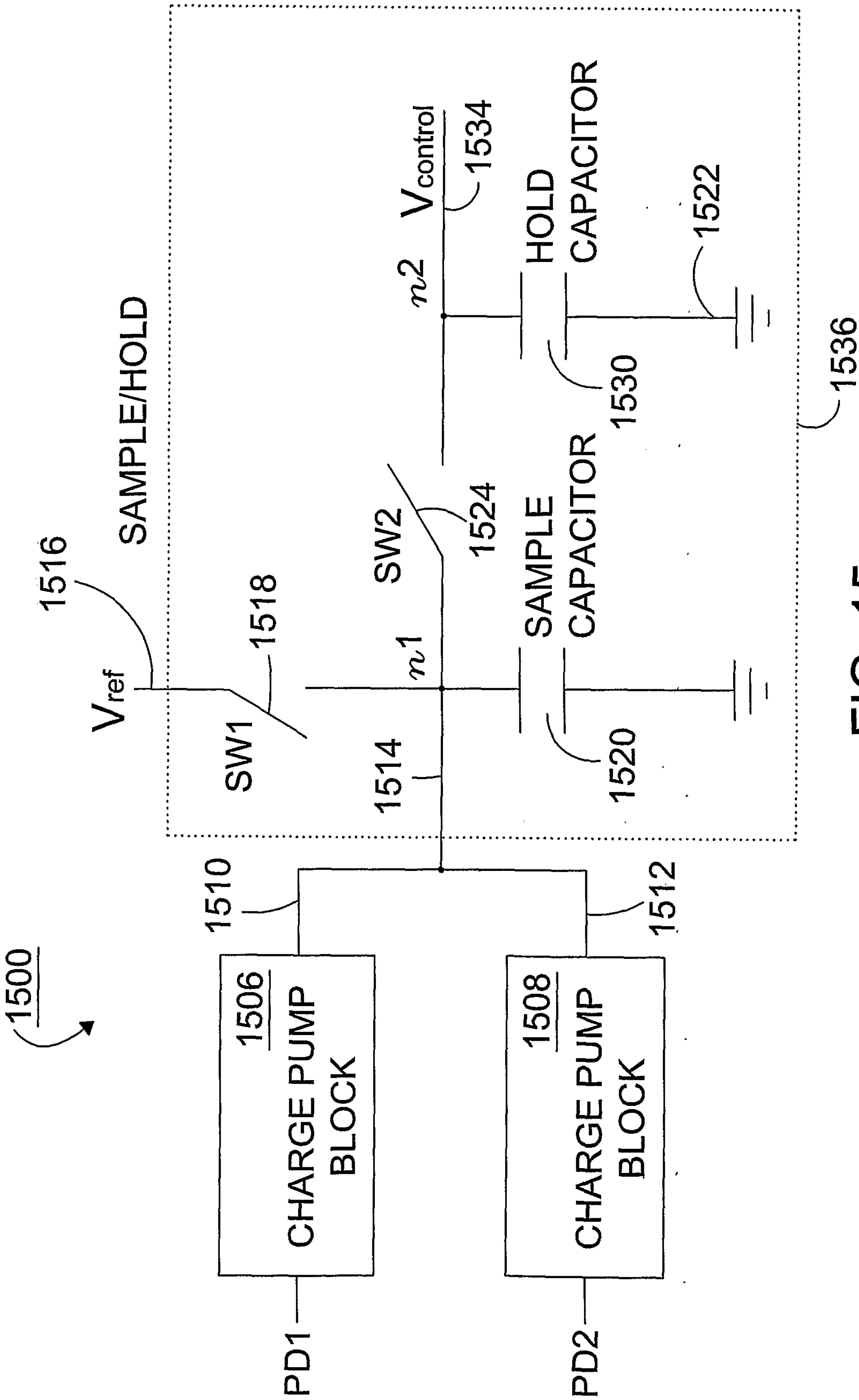

1500
1506
CHARGE PUMP BLOCK
1508
CHARGE PUMP BLOCK
PD1
PD2
1510
1512
1514
SAMPLE/HOLD
$V_{ref}$
1516
SW1
1518
$n1$
SAMPLE CAPACITOR
1520
SW2
1524
$n2$
$V_{control}$
1534
HOLD CAPACITOR
1530
1522
1536

FIG. 15

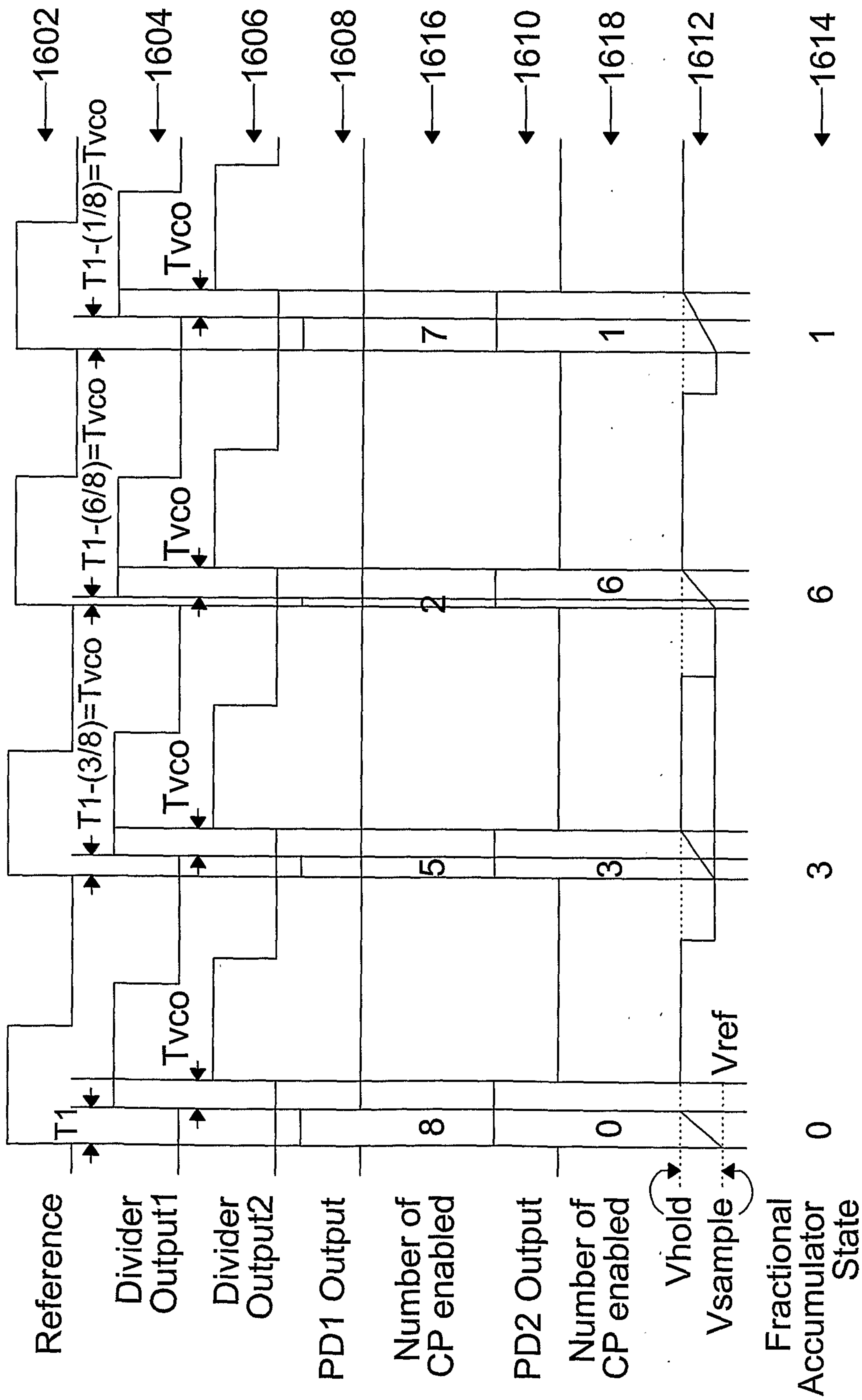

Reference
Divider Output1
Divider Output2
PD1 Output
Number of CP enabled
PD2 Output
Number of CP enabled
Vhold
Vsample
Fractional Accumulator State
1602
1604
1606
1608
1616
1610
1618
1612
1614
T1
Tvco
Vref
T1-(3/8)=Tvco
T1-(6/8)=Tvco
T1-(1/8)=Tvco
8
0
5
3
2
6
7
1
0
3
6
1

FIG. 16

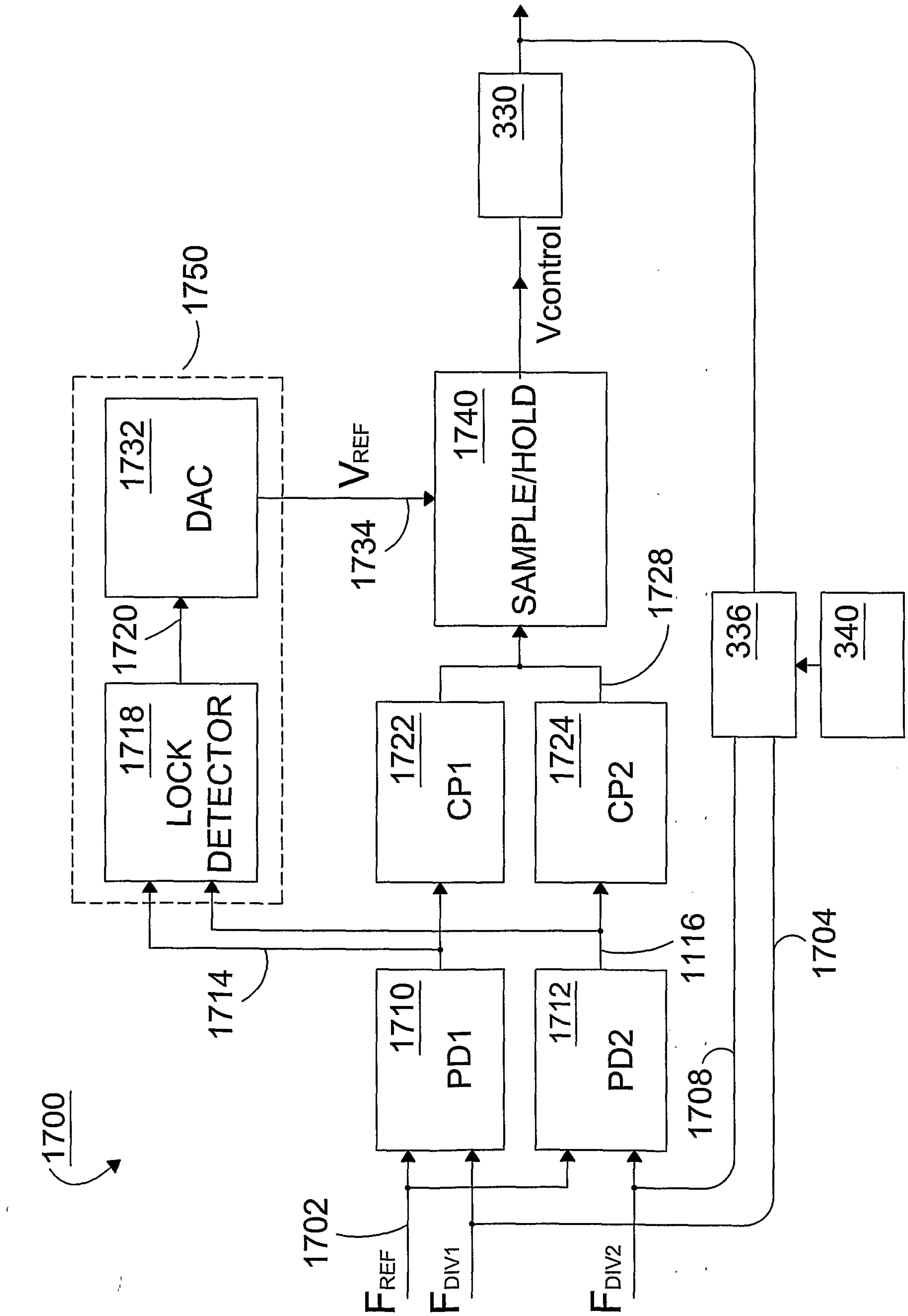

1700
1750
1732
DAC
1718
LOCK DETECTOR
1720
VREF
1734
1740
SAMPLE/HOLD
Vcontrol
330
1722
CP1
1724
CP2
1728
1710
PD1
1712
PD2
1714
1116
336
340
1702
1704
1708
FREF
FDIV1
FDIV2

FIG. 17

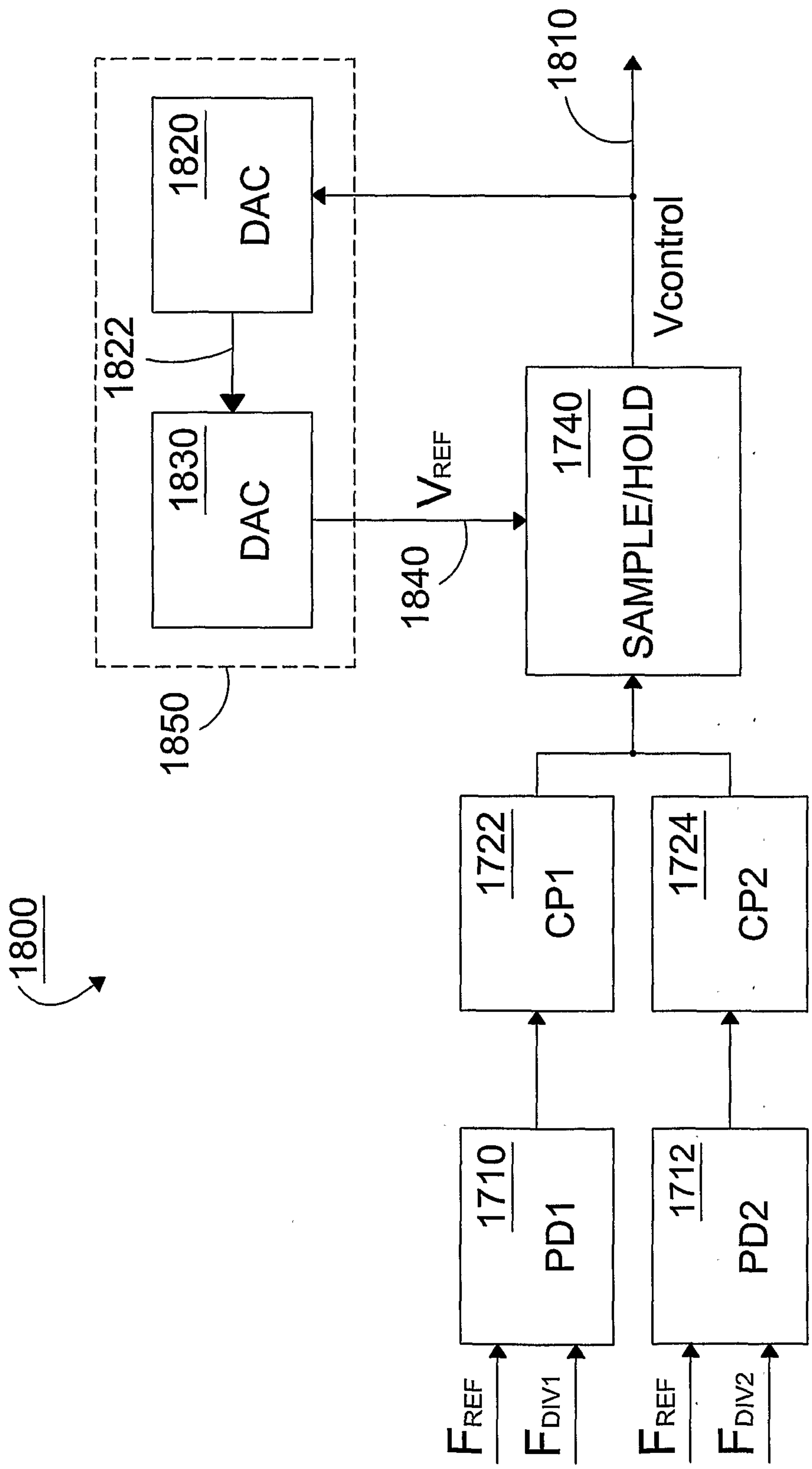

1800
1820
DAC
1822
1830
DAC
1850
1810
Vcontrol
V_REF
1840
1740
SAMPLE/HOLD
1722
CP1
1724
CP2
1710
PD1
1712
PD2
F_REF
F_DIV1
F_REF
F_DIV2

FIG. 18

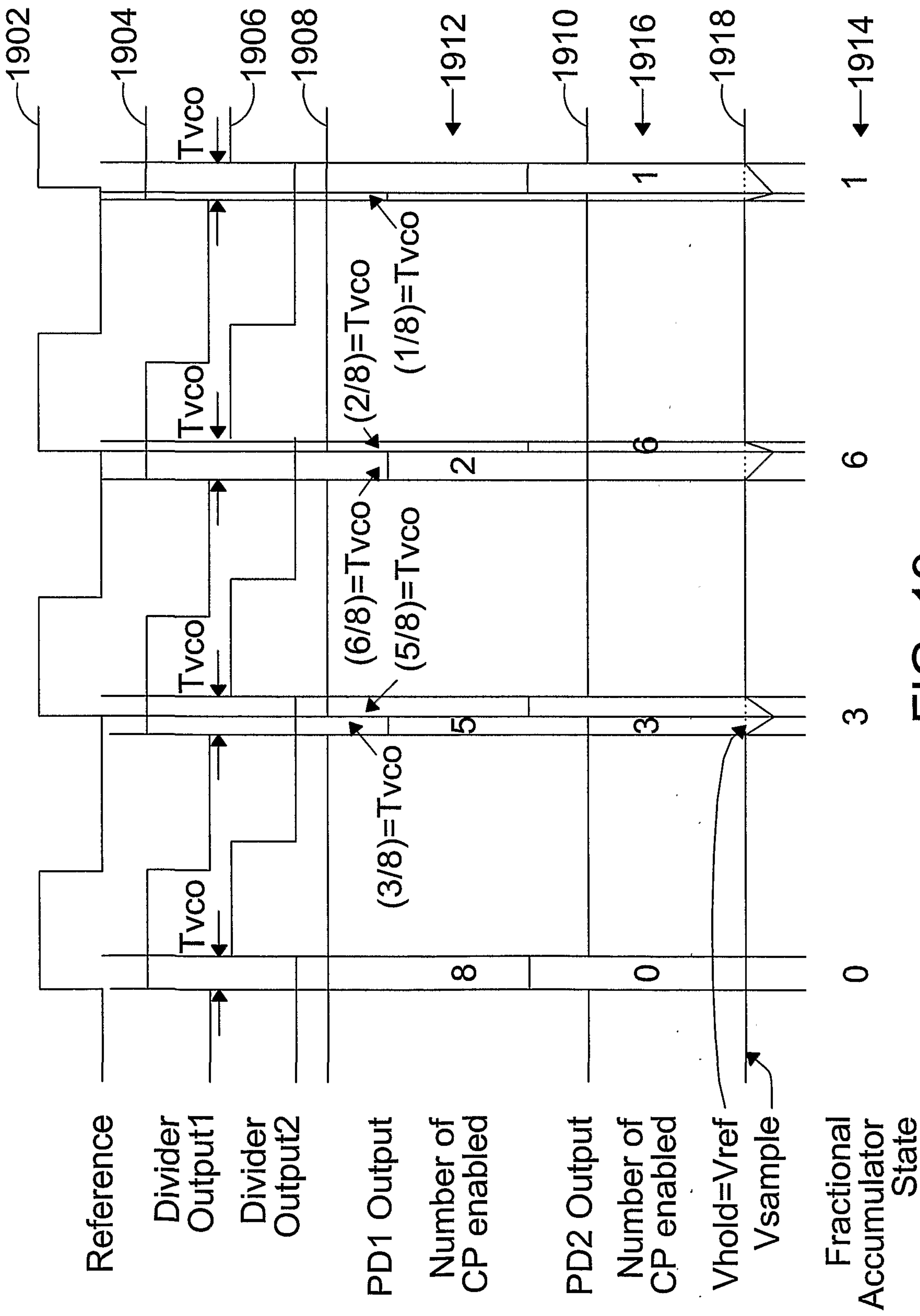
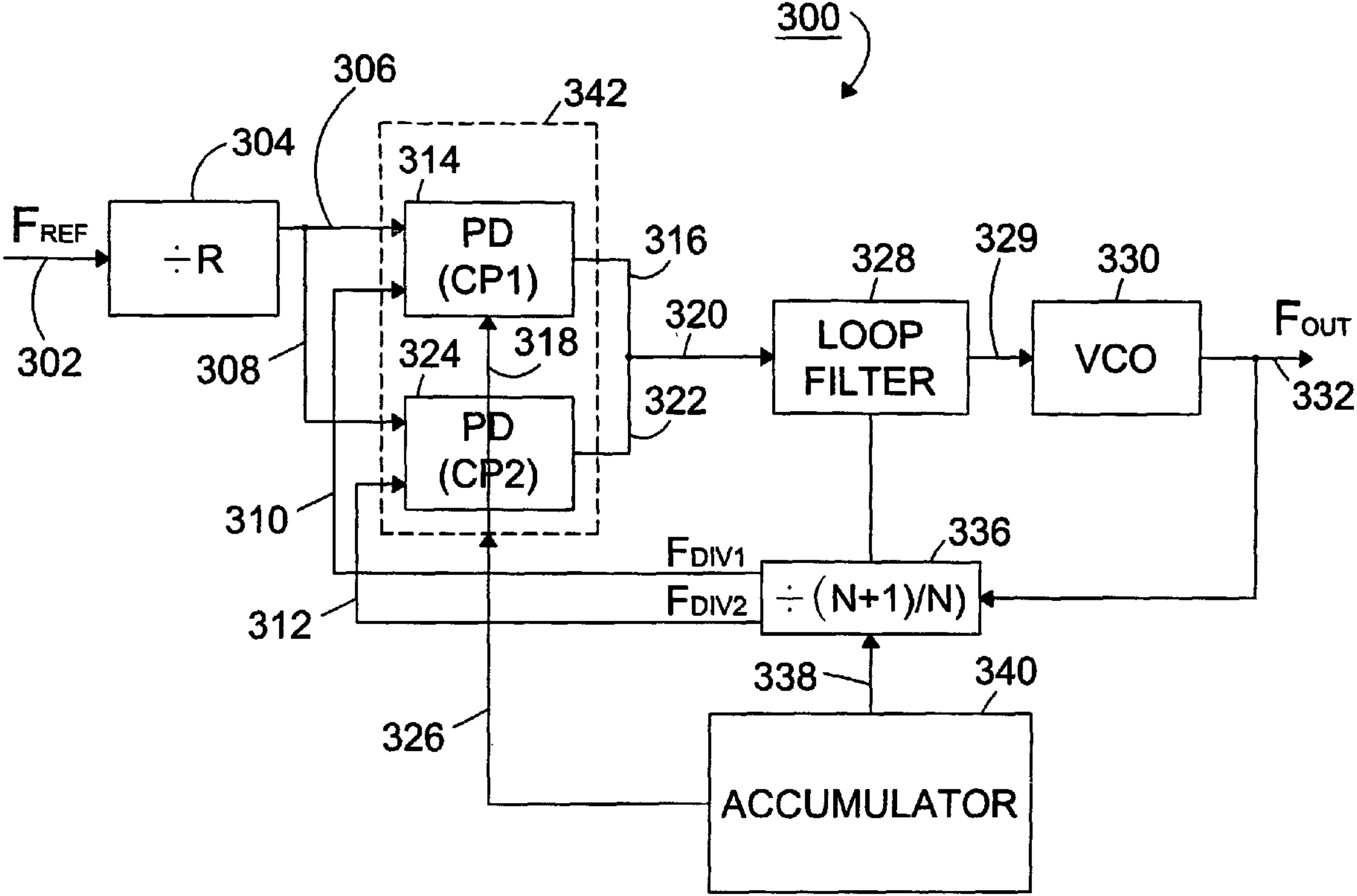

1902
1904
1906
1908
1912
1910
1916
1918
1914
Tvco
Tvco
Tvco
Tvco
(2/8)=Tvco
(1/8)=Tvco
(6/8)=Tvco
(5/8)=Tvco
(3/8)=Tvco
8
5
2
0
3
6
1
0
3
6
1
Reference
Divider Output1
Divider Output2
PD1 Output
Number of CP enabled
PD2 Output
Number of CP enabled
Vhold=Vref
Vsample
Fractional Accumulator State

FIG. 19


300
306
342
304
314
FREF
÷R
PD
(CP1)
316
302
308
318
320
328
329
330
FOUT
324
LOOP
FILTER
VCO
332
PD
(CP2)
322
310
336
FDIV1
FDIV2
÷(N+1)/N)
312
338
340
326
ACCUMULATOR