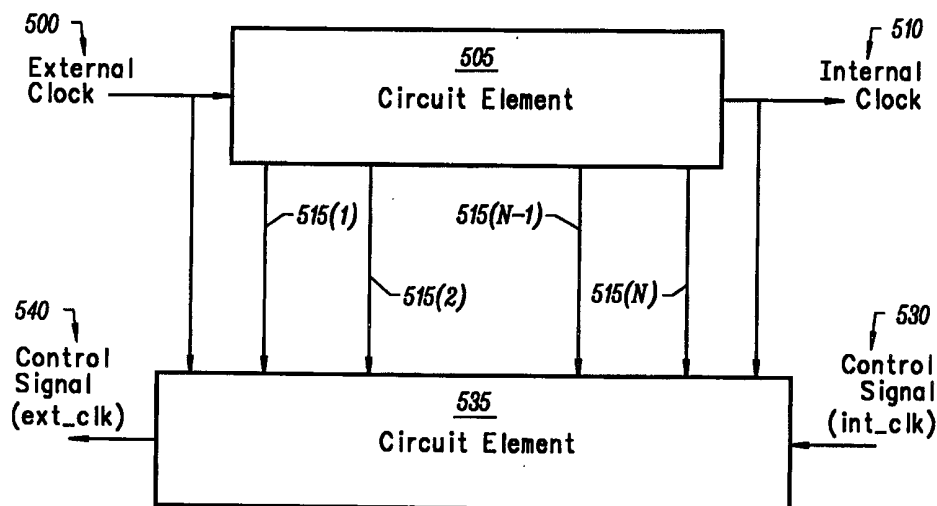




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(54) Title: A METHOD AND APPARATUS FOR SYNCHRONIZING A CONTROL SIGNAL



## (57) Abstract

A synchronization circuit for gradually shifting the phase domain of a control signal (530) to permit synchronization of a signal with a clock signal (500) in a different phase domain in a system with a single frequency, but arbitrary phase relationship. The present invention allows a control signal (530) in the phase domain of an internal clock to be synchronized with an external clock (500), when the phase domain of the external clock differs substantially from that of the internal clock. In synchronizing the control signal (530) to the external clock (500), the present invention avoids the generation of runt pulses while providing a control signal synchronized to the external clock in the least amount of time feasible (i.e. lowest latency time). Because the present invention has no failure modes due to timing relationships, MTBF is infinite for failures caused by such relationships and therefore need not be a concern. This also implies that no risk is posed to the proper operation of the circuits driven thereby.

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5 A METHOD AND APPARATUS FOR SYNCHRONIZING A CONTROL SIGNAL

#### BACKGROUND OF THE INVENTION

Today's complex digital systems contain storage  
devices, finite-state machines, and other such structures  
10 which control the movement of information by various clocking  
methods. Conversely, combinatorial logic devices, which are  
usually asynchronous, do not require time-based control  
signals for their operation. The output of an ideal  
combinatorial logic circuit is completely defined at any time  
15 by its inputs. In many digital circuits, however, it is  
expedient to cause the circuit's output to depend on both  
present and past inputs. Digital circuits whose outputs  
depend on such inputs are known as sequential circuits. A  
subset of this type of circuit is the synchronous sequential  
20 circuit, which requires a control signal to mark the passage  
of time and thereby delineate present inputs from past inputs.  
A clock signal serves this purpose, thereby controlling the  
transfer of digital information from one storage location to  
another.

25 An ideal clock signal is simply a periodic  
alternation between a logic high level and a logic low level.  
Typically, today's logic circuits use multi-phase clocks.  
Such clocking schemes may employ two-phase or four-phase  
clocks, or may use an even greater number of phases. The  
30 various phases are normally non-overlapping to prevent, as  
much as possible, race conditions and hazards, which commonly  
occur in digital circuits.

A hazard occurs when a circuit, under normal  
operating conditions, has the possibility of generating  
35 positive or negative pulses of possibly undefined duration at  
its output, when no such transitions should occur. This might  
occur, for example, where a designer fails to properly reduce  
logic terms. A race condition, on the other hand occurs when  
the output of a circuit is determined in part by which of two  
40 or more rising or falling edges is first received as an input

to the circuit. Such a situation is normally avoided by synchronizing signals to a clock signal, meaning that the signals are related to the clock signal (and each other) in such a way that those signals may safely drive a circuit  
5 clocked by that clock signal. Such a race condition may result in a runt pulse at the circuit's output if no steps are taken to avoid it. Because a well-defined timing relationship is unlikely to exist between such input signals, neither the duration nor amplitude of a runt pulse is defined. One  
10 possible source of races is the improper distribution of clocking signals because the timing relationships involved become undefined.

Because modern digital systems are often very large, the number of devices driven by a clock may exceed the drive capabilities of the clock generation circuits, a common  
15 occurrence. In such a case, a clock signal will be distributed using one or more driver circuits because the clock circuit is unable to drive all of the devices directly. When using multiple clock drivers, the circuits being driven  
20 will be partitioned into logical subcircuits and the output of each clock driver used to drive those subcircuits. The signal propagation delays through each of the clock driver circuits will likely differ. The load presented to each drive circuit will also likely differ, also causing differences in the  
25 outputs of each clock driver circuit. These differences are known as clock skew.

Generally speaking, information transfer from a signal synchronized to a later clock to circuit elements clocked with an earlier clock will function correctly.  
30 However, a transfer of information from an earlier clock to a later clock may encounter problems. For example, if two flip-flops are connected serially with the first flip-flop providing input to the second flip-flop, the circuit should function as a shift register. If two separate clocks are  
35 provided, one to each flip-flop, and the second flip-flop is clocked simultaneously with or before the first flip-flop, both flip-flops may be loaded with the same data, and thus

fail to function as a shift register. In such cases, the two clocks must be synchronized in some way.

Similarly, outputs from a first digital circuit operating using a first clock which are taken as input by a second digital circuit operating on a second clock must often be synchronized to the second clock. This is also true of asynchronous inputs generated by a user, sensors, or other such input sources.

Fig. 1 illustrates several of the proceeding concepts. Fig. 1 shows a clock enable signal `rclk_en` 100 generated by a control signal receiver 102 from a bus control input 104 (received from a bus (not shown)). Clock enable signal `rclk_en` 100 enables the generation of a clock `rclk` 110. A bus clock 112 is also received from the bus. Bus clock 112 is provided to a phase detector 114 and a delay-locked loop 116. Phase detector 114 compares bus clock 112 with a clock `mclk` 120, which also clocks control signal receiver 102. Phase detector 114 generates a phase difference signal 122 that represents the difference in phase between bus clock 112 and `mclk` 120. Delay-locked loop 116 generates a master clock `dllclk` 130 by variably delaying bus clock 112. Delay-locked loop 116 uses phase difference signal 122 to set the amount of delay necessary to keep `mclk` 120 synchronous with bus clock 112.

The circuit of Fig. 1 operates in the following manner. Clock `dllclk` 130 is fed into an inverter 132 which drives a first NAND gate 134 and a second NAND gate 136. The second input of first NAND gate 134 is tied high to voltage  $V_{DD}$  160, causing the output of first NAND gate 134 to follow the input of inverter 132. First NAND gate 134 outputs a delayed version of `dllclk` 130, which then passes through an inverter string 140 and emerges as `mclk` 120. Similarly, second NAND gate 136 drives an inverter string 150 and emerges as `rclk` 110. Inverter string 150 serves as a clock driver circuit, allowing `rclk` 110 to drive large numbers of devices.

The function of second NAND gate 136 is to disable `rclk` 110. The function of first NAND gate 134 is to maintain equality in the delays experienced in generating `rclk` 110 and

mclk 120. Because the delay experienced in generating rclk 110 from dllclk 130 is equal to that experienced in generating mclk 120 from dllclk 130, rclk 110 is synchronous with mclk 120, save for the fact that rclk 110 is not generated until enabled by rclk\_en 100. So long as the delays in generating rclk 110 and mclk 120 are kept equal, other devices may therefore be used in place of first NAND gate 134 and second NAND gate 136, such as NOR gates or tristable devices. However, the delays experienced in generating rclk 110 from dllclk 130 should always be identical to those experienced in generating mclk 120. Because the phase delay experienced in generating mclk 120 from dllclk 130 is defined (i.e., the delay is calculable and/or measurable, although it may not be known), a substantially quantifiable phase relationship exists between mclk 120 and dllclk 130. An example of a delay-locked loop receiver is described in U.S. Patent application Atty Dkt 18081-000300 entitled "DELAY LOCKED LOOP CIRCUITRY FOR CLOCK DELAY ADJUSTMENT," having as inventors Kevin S. Donnelly, Pak Shing Chau, Mark A. Horowitz, Thomas H. Lee, Mark Johnson, Benedict Lau, Leung Yu, Bruno W. Garlepp, Yiu-Fai Chan, Jun Kim, Chanh Vi Tran, and Donald Stark, and assigned to Rambus, Inc., the assignee of the present invention, and is hereby incorporated by reference in its entirety.

Fig. 2A illustrates the waveforms which may be generated by the operation of the circuit illustrated in Fig. 1. Throughout this discussion, references to a signal or element of a preceding figure will use the original reference numbers. Moreover, idealized signal waveforms will be used to simplify the discussion. As illustrated in Fig. 2A, the waveform of dllclk 130 is a square wave having a 50% duty cycle and a period of  $(T_3 - T_0)$ . As is shown in Fig. 2A, rclk 110 and mclk 120 of Fig. 1 are simply delayed versions of dllclk 130, assuming the circuit is operating under nominal conditions and, with regard to rclk 110, rclk\_en 100 is active. These nominal signals are indicated by traces rclk\_nom 202 and mclk\_nom 204.

However, the delay experienced between dllclk 130 and the outputs of the circuit in Fig. 1 are affected by variables such as temperature, supply voltage, process parameters, and other such variables. For example, at a low  
5 operating temperature with a high supply voltage and a fast process, the circuit of Fig. 1 provides a relatively short delay, as indicated by a trace r/mclk\_fast 210. Trace r/mclk\_fast 210 experiences a delay of  $(T_1 - T_0)$ , as indicated by a transition 211.

10 Alternatively, a low supply voltage, high operating temperature, and slow process significantly increase the delay experienced. Such a situation is shown in Fig. 2A by a trace r/mclk\_slow 215, which experiences a delay of  $(T_4 - T_0)$ , as indicated by a transition 216. Variations in process  
15 parameters may also alter the delay provided by the circuit in Fig. 1, making the delay longer or shorter depending on the parameter and the manner in which it is varied. Thus, the phase relationship between dllclk 130 and either of rclk 110 or mclk 120 is an arbitrary (although measurable) one, due to  
20 the dependence on loading, process, voltage, temperatures, and other factors. Any of these conditions can lead to errors in the generation of rclk 110 using circuits of the prior art.

In operation, the circuit of Fig. 1 generates rclk 110 and mclk 120 in a manner which keeps rclk 110 and  
25 mclk 120 substantially in phase. This is done through careful circuit design, taking into consideration the loads driven by these clock signals, the proportions of the inverters in inverter strings 140 and 150, NAND gates 134 and 136, the physical layout of these elements, and other considerations.

30 Figs. 2B, 2C, and 2D are phase diagrams corresponding to the various traces of Fig. 2A. Fig. 2B illustrates the nominal phase delay represented by rclk\_nom 202 and mclk\_nom 204. Clock dllclk 130 is shown as a vector 220 having a phase of  $0^\circ$ . Clocks rclk\_nom 202 and mclk\_nom  
35 204, which are synchronized, are shown as a vector 221. Vector 221 lags vector 220 by about  $180^\circ$ . In these figures, the delay experienced between dllclk 130 and rclk\_nom 202/mclk\_nom 204 is given by:

$$T_{Delay} = \frac{\phi}{360^\circ} \cdot T_{dllclk\ 130} \quad (1)$$

where  $T_{Delay}$  is the delay experienced,  $\phi$  is the phase difference, and  $T_{dllclk\ 130}$  is the period of dllclk 130. Thus, vector 221 lags vector 220 by  $0.5 T_{dllclk\ 130}$ , which is shown in Fig. 2B as a period of  $T_{Delay}$  222. This period is equal to the time  $(T_2 - T_0)$  in Fig. 2A.

In Fig. 2A, dllclk 130 is active from  $0^\circ$  to  $180^\circ$  and inactive from  $180^\circ$  to  $360^\circ$  (i.e.,  $0^\circ$ ). As will be discussed in detail with regard to Fig. 2E, rclk\_nom 202 can safely be synchronized by the circuit of Fig. 1 when dllclk 130 is inactive (i.e., between  $180^\circ$  and  $360^\circ$ ). This synchronization point is nominally at a point in the center of the inactive phase of dllclk 130 (i.e., at a phase angle of about  $270^\circ$ ).

Figs. 2C and 2D illustrate the cases shown in Fig. 2A as r/mclk\_fast 210 and r/mclk\_slow 215, respectively. In both of these figures, dllclk 130 is again shown as a vector 220. Clock r/mclk\_fast 210 is shown as a vector 223 in Fig. 2C. Vector 223 lags vector 220 by only about  $45^\circ$  due to the environmental and process factors previously discussed. This translates to about  $0.125 T_{dllclk\ 130}$ , which is shown in Fig. 2C as a period of  $T_{Delay}$  226. This period is equal to the time  $(T_1 - T_0)$  in Fig. 2A.

Fig. 2D shows clock r/mclk\_slow 210 as a vector 225. Vector 225 lags vector 220 by a large amount, about  $382^\circ$ , again due to the environmental and process factors previously discussed. This translates to about  $1.06 T_{dllclk\ 130}$ , which is shown in Fig. 2C as a period of  $T_{Delay}$  224. This period is equal to the time  $(T_4 - T_0)$  in Fig. 2A.

Fig. 2E shows the preferred timing relationship between rclk\_en 100 and dllclk 130. Preferably, rclk\_en 100 goes active (in this case, high) at a time  $T_0$  when dllclk 130 is inactive (i.e., low), thereby allowing dllclk 130 to propagate through inverter 132, NAND gate 136, and inverter string 150, thereby providing a delayed version of itself,



rclk 110. The delay experience by dllclk 130 is indicated in Fig. 2E by a transition 230 having a duration  $(T_2 - T_1)$ .

Unfortunately, as illustrated in Fig. 2F, simply allowing rclk\_en 100 to become active at any point in time can cause the generation of runt pulses. In Fig. 2F, rclk\_en 100 goes active (*i.e.*, high) at a time  $T_0$ , which is during a period when dllclk 130 is also active (*i.e.*, high). Because the circuit in Fig. 1 is simply a combinatorial circuit, rclk 110 will go high any time rclk\_en 100 and dllclk 130 are both high, albeit at a later time due to delay within the circuit. This being the case, a race condition exists and, in this case, produces a runt pulse 235. The leading edge of runt pulse 235 is related to rclk\_en 100 as indicated by a transition 240. The delay between these two edges is  $(T_0 - T_2)$ , and is equal to the delay experienced between dllclk 130 and rclk 110  $(T_5 - T_4)$  as indicated by a transition 245. The falling edge of runt pulse 235 occurs at a time  $T_3$  and corresponds to the falling edge of dllclk 130 occurring at  $T_1$ .

Runt pulse 235, having indeterminate amplitude and duration, is undesirable because it may cause intermittent failures, depending on the timing of the asynchronous input and the nature of the clocked circuit. Such effects can include the failure to meet the timing constraints of the circuits driven by the clock, the generation of metastable states in bistable devices, certain of the driven circuits being out of synchronization with other portions thereof, and other undesirable effects.

A common solution to such problems is the inclusion of a latch or flip-flop to gate the offending control signal. Fig. 3 illustrates such a solution. A latch 300 is used to synchronize rclk\_en 100 with dllclk 130. Clock enable rclk\_en 100 is gated by latch 300, thereby generating a gated version of rclk\_en 100, a clock enable signal g\_rclk\_en 310, which is provided to second NAND gate 136. In using a flip-flop to gate the input, g\_rclk\_en 310 is prohibited from enabling the output of rclk 110 until a time at which dllclk 130 is active. The waveforms generated using this common solution are illustrated in Figs. 4A, 4B, and 4C.

Fig. 4A illustrates the case where rclk\_en 100 goes high at a time  $T_0$  when dllclk 130 is low. As was illustrated in Fig. 2E, this situation would not even cause problems for the circuit illustrated in Fig. 1. In the circuit illustrated in Fig. 3, this situation is also handled correctly. In Fig. 4A, rclk\_en 100 goes high at a time  $T_0$ , but must wait for the next rising edge of dllclk 130. This occurs at a time  $T_1$ , as indicated by a transition 400. At time  $T_1$ , the rising edge of dllclk 130 clocks the active state of rclk\_en 100 into latch 300, thereby causing a rising edge on the output of latch 300. This is illustrated in Fig. 4A as the rising edge in g\_rclk\_en 310 at time  $T_1$ , and is indicated by a transition 405. For simplicity, this timing relationship is shown in Fig. 4A as being instantaneous; in an actual circuit, there would be some delay associated with transition 405 which might delay g\_rclk\_en 310 going active by one cycle of dllclk 310.

At this point, propagation of dllclk 130 through inverter string 150 is enabled and dllclk 130 is propagated, appearing as rclk 110 at a time  $T_2$ , which is indicated by a transition 420. The duration of this transition is equivalent to the delay experienced by dllclk 130 propagating through inverter string 150 when generating rclk 110.

Fig. 4B illustrates the anomalous situation shown in Fig. 2F. However, instead of generating a runt pulse like the one shown in Fig. 2F, the circuit of Fig. 3 effectively delays the application of g\_rclk\_en 310 to second NAND gate 136 until such time as dllclk 130 transitions to an active state. As shown in Fig. 4B, rclk\_en 100 becomes active at a time  $T_3$ , which is at a time when dllclk 130 is also active. Without latch 300, a runt pulse such as that exhibited by the circuit of Fig. 1 would be generated. However, rclk\_en 100 is not applied directly to second NAND gate 136, but is gated through latch 300 by dllclk 130. This dependency is indicated in Fig. 4B by a transition 425. When dllclk 130 becomes active at a time  $T_4$ , rclk\_en 100 is already active. This is propagated through latch 300, causing g\_rclk\_en 310 to also become active. This transition is indicated by a

transition 430, which again is shown as being instantaneous for the sake of simplicity. A pulse 435 of dllclk 130 then propagates through inverter string 150 and emerges as a pulse 440 of rclk 110, as before. This occurs at a time  $T_5$ .

5 The delay between pulse 435 (enabled by g\_rclk\_en 310) and pulse 440 is indicated by a transition 445 which is equal in duration to the delay experienced by pulse 435 ( $T_5 - T_4$ ).

10 However, the solution provided by the circuit illustrated in Fig. 3 is not without its own problems. Any bistable device (*i.e.*, circuits containing flip-flops, latches, or other switching circuits) may suffer from what is known as metastability, under the proper input conditions.

15 Normally, digital logic has two stable states which are a function of the steady-state transfer functions of the elements of which they consist. However, a third equilibrium point exists in these transfer functions. This is known as the metastable state and occurs somewhere near the half-way point between the voltage levels representing a logic 0 and a logic 1. However, this is not a truly stable operating point because random noise will tend to drive a circuit operating at  
20 this point towards one of the stable operating points (*i.e.*, a logic 0 or logic 1). Additionally, this metastable state lasts for a non-deterministic period of time, creating the possibility that circuits driven by elements in this state may  
25 find themselves in unknown states for an indeterminate time and almost assuredly out of synchronization once the metastability has resolved.

Such a phenomena is illustrated by the traces in Fig. 4C. In Fig. 4C, rclk\_en 100 is applied even later than  
30 in Figs. 4A and 4B, at a time  $T_6$ . However, also occurring at time  $T_6$  is a rising edge of dllclk 130. This results in a race condition. Because they occur at substantially the same instant (*i.e.*, at a time which violates the setup and hold times of latch 300), the output of latch 300, g\_rclk\_en 310,  
35 is put into a metastable state. This condition is indicated by transitions 450 and 455, which indicate that both rclk\_en 100 and dllclk 130 are driving the transition which is supposed to occur in g\_rclk\_en 310. The metastable state of

g\_rclk\_en 310 resolves to a high level within some indeterminate time (as shown in Fig. 4C). This then drives rclk\_glitch 475, as indicated by a transition 470. Clock rclk\_glitch 475 may then operate normally, but will likely reflect a delayed version of the glitches caused by the metastability of g\_rclk\_en 310, in the form of runt pulses. The latter situation is indicated by a runt pulse 475, which occurs at a time  $T_7$ . If this occurred, synchronization in the circuits driven by rclk\_glitch 475 would likely be lost, resulting in improper operation of those circuits.

While this type of problem can be addressed to some extent by changes in design, it is impossible to eliminate. The measure of the frequency with which such a failure could be expected to occur is known as the mean time between failures (MTBF). However, this figure is difficult to calculate and changes with variations in the process used to fabricate the device and operating conditions such as temperature and supply voltage. Moreover, the possibility of failure is not eliminated by the use of such analytical methods.

What is therefore required is a circuit architecture which removes the possibility of the runt pulses created by the circuit of Fig. 1 and the occasional metastability experienced by the circuit of Fig. 3. In other words, such a circuit should have no probability of failure resulting from the gating of the clock. Such a circuit should allow the synchronization of an enable signal such as rclk\_en 100 with a clock signal such as dllclk 130 with minimum latency, and insensitivity to process variations and environmental parameters such as temperature and supply voltage.

#### SUMMARY OF THE INVENTION

The method of the present invention includes the steps of generating a series of intermediate clock signals using a first clock signal. A control signal is then synchronized with one or more of the series of intermediate signals in a successive manner. For example, the synchronizations may proceed from a last one of each

successive one of the series of clock signals to a first one of the series of clock signals. If necessary, the control signal may be synchronized with the first clock signal. The control signal is assumed to be synchronous to the last one of the series of clock signals, which also serves as a second clock signal. Such a phase relationship must be substantially determinable, but may vary due to environmental, process and other factors, if the effects of such factors may be quantified.

The method of the present invention addresses the aforementioned problems of the prior art by gradually shifting the phase domain of a control signal. The present invention allows a control signal in the phase domain of an internal clock to be synchronized with an external clock, when the phase of the external clock differs substantially from that of the internal clock. In synchronizing the control signal to the external clock, the present invention avoids the generation of runt pulses while providing a control signal synchronized to the external clock in the least amount of time feasible (i.e., with the lowest latency time). Because the present invention has no synchronization-related failure modes, MTBF is infinite and therefore need not be a concern. This also implies that no such risk is posed to the proper operation of the circuits driven thereby.

A series of delayed, intermediate clock signals propagating in a first direction are produced from a first clock signal. A second clock signal is generated at the end of the intermediate chain. A control signal is input to a chain of circuit elements which re-synchronize the control signal received with one of the intermediate clock signals, propagating in a direction opposite to the first direction. The first circuit element in the synchronization chain is clocked by the last intermediate clock, the second synchronization element is clocked by the second to last intermediate clock, and so on.

The control signal thus works its way back along the intermediate clock chain, gradually shifting its phase domain from one clock signal to another. In other words, this method

moves the control signal one phase step with each intermediate clock. If a four stage chain is used, the synchronization signal will work its way back to complete synchronization in four steps. The number of stages will depend on the phase and timing relationships between the first and second clocks. In this manner, the control signal is gradually shifted from the phase domain of the second clock to the phase domain of the first clock.

A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of one embodiment of a dual clock driver circuit of the prior art;

Fig. 2A is a timing diagram showing delays experienced by the circuit in Fig. 1 when subjected to varying environmental conditions;

Fig. 2B is a phase diagram of the operation of the circuit in Fig. 1 with nominal operating parameters;

Fig. 2C is a phase diagram of the operation of the circuit in Fig. 1 with operating parameters that cause the circuit to operate faster;

Fig. 2D is a phase diagram of the operation of the circuit in Fig. 1 with operating parameters that cause the circuit to operate more slowly;

Fig. 2E is a timing diagram of the proper operation of the circuit in Fig. 1;

Fig. 2F is a timing diagram showing the generation of a runt pulse by the circuit in Fig. 1;

Fig. 3 is a circuit diagram of another embodiment of a dual clock driver circuit of the prior art;

Fig. 4A is a first timing diagram of the proper operation of the circuit in Fig. 3;

Fig. 4B is a second timing diagram of the proper operation of the circuit in Fig. 3;

Fig. 4C is a timing diagram showing metastability in the circuit in Fig. 3;

Fig. 5 is a block diagram of one embodiment of the present invention;

Fig. 6A is a circuit diagram of one embodiment of the present invention which follows the architecture shown in Fig. 5;

Fig. 6B is a first timing diagram of the phase domain shifting which occurs during the operation of the circuit in Fig. 6A;

Fig. 6C is a phase diagram of the phase domain shifting which occurs during the operation of the circuit in Fig. 6A when operating at nominal speed;

Fig. 6D is a phase diagram of the phase domain shifting which occurs during the operation of the circuit in Fig. 6A when operating faster than the nominal operating speed;

Fig. 6E is a phase diagram of the phase domain shifting which occurs during the operation of the circuit in Fig. 6A when operating more slowly than the nominal operating speed;

Fig. 6F is a second timing diagram of the proper operation of the circuit in Fig. 6A;

Fig. 7 is a circuit diagram of another embodiment of the present invention which follows the architecture shown in Fig. 5; and

Fig. 8 is a timing diagram showing maximum delays which may occur in a circuit of the present invention, such as those shown in Figs. 6A and 7.

#### DETAILED DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The method of the present invention addresses the problems of the prior art by gradually shifting the phase domain of a control signal from that of an internal clock to that of an external clock. Fig. 5 illustrates a block diagram of a design embodying the method of the present invention. As before, references to elements appearing in earlier figures will be referred to using the same reference numbers. As shown in Fig. 5, an external clock 500 (e.g., dllclk 130 of Fig. 1) is fed into a circuit element 505. The circuit

element 505 has several functions and may be one of several different devices. One function of circuit element 505 is to generate an internal clock 510 (e.g., mclk 120 of Fig. 1).

Additionally, circuit element 505 continuously  
5 generates a series of intermediate clocks 515(1)-(N), when external clock 500 is applied to circuit element 505.

Intermediate clocks 515(1)-(N) are increasingly delayed versions of external clock 500. Internal clock 510 lags external clock 500 by an unknown duration. Intermediate  
10 clock 515(1) lags external clock 500 by a fraction of this amount. Preferably, each successive intermediate clock preferably lags its predecessor by a similar amount. Finally, internal clock 510 lags intermediate clock 515(N) by a similar amount. While the amount by which one of these  
15 signals lags its predecessor may vary, it is preferable for the delay between these signals be substantially similar both for purposes of simplification and reliability. This is due to the fact that the difference between the given signal and the signal being synchronized at that point should not exceed  
20 a maximum value, as will be discussed later. However, a subset of these signals may be used in synchronizing a control signal 520, if the appropriate timing constraints are met (i.e., the phase delay between each intermediate clock is not too large). Because intermediate clocks 515(1)-(N) and  
25 internal clock 510 are delayed versions of external clock 500, internal clock 510 is equivalent to the intermediate clock which would follow intermediate clock 515(N).

The circuit of Fig. 5 receives a control signal (int\_clk) 530 as an input. Internal clock 510 clocks the  
30 circuits that generate control signal (int\_clk) 530. Thus, it can be implied that control signal (int\_clk) 530 is synchronous to internal clock 510 or is at least close enough in phase that the two signals may safely be synchronized. A circuit element 535 receives control signal (int\_clk) 530 as  
35 an input. Circuit element 535 also receives internal clock 510, intermediate clocks 515(1)-(N), and external clock 500 as inputs.



Circuit element 535 operates in the following manner. Control signal (int\_clk) 530 is first re-synchronized to internal clock 510 by circuit element 535. The resulting signal is then successively synchronized with each one of  
5 intermediate clock 515(1)-(N), gradually shifting the phase domain of the control signal. Finally, the control signal in the phase domain of intermediate clock 515(1) is synchronized to external clock 500 by circuit element 535, resulting in a control signal (ext\_clk) 540. Control signal (ext\_clk) 540 is  
10 then synchronous to external clock 500, and may then be used to enable the incoming clock signal (not shown). For example, control signal (ext\_clk) 540 could then serve as rclk\_en 100 in Fig. 1 to enable the generation of rclk 110 by inverter string 150 without presenting the possibility of generating  
15 runt pulses or causing timing-related failures. Optionally, if the phase of control signal (int\_clk) 530 is close enough to that of internal clock 510, the re-synchronization of control signal (int\_clk) 530 to internal clock 510 may be unnecessary. Similarly, the phase of the re-synchronized control signal may be close enough to that of external  
20 clock 500 to permit the use of the re-synchronized control signal without re-synchronization to external clock 500

Circuit element 505 may be one of any number of devices, but must be able to generate the delayed versions of  
25 external clock 500, as previously described. In practice, circuit element 505 may simply consist of a requisite number of delay elements, which again should preferably provide substantially similar delays between the signals generated. Often, however, circuit element 505 will be a clock drive  
30 circuit which allows external clock 500 to be distributed to numerous circuit elements as internal clock 510. For example, a string of inverters might be used to provide such drive capabilities. The string of inverters would start with a relatively small inverter capable of driving a slightly larger  
35 inverter. This continues to the point where the last inverter is capable of driving the requisite number of circuit elements as internal clock 510. Such a circuit is similar to that shown in Fig. 1 as inverter string 140. However, a circuit

according to the method of the present invention would not suffer the shortcomings thereof, nor the shortcomings of the circuit illustrated in Fig. 3.

Figs. 6A-6F illustrate such an implementation and the waveforms associated with each. Fig. 6A illustrates a circuit implementation according to the block diagram of Fig. 5. This circuit uses circuit elements from the circuit illustrated in Fig. 1, but avoids the problems associated therewith. As in Fig. 5, the circuit in Fig. 6A shows a circuit element 505 which receives external clock 500 as input and generates internal clock 510. Circuit element 505 also generates intermediate clocks 600, 602, and 604, which serve as examples of intermediate clocks 515(1)-(N) in Fig. 5. Internally, circuit element 505 includes inverter 132, first NAND gate 134, and inverter string 140, as shown in Fig. 1. External clock 500 and internal clock 510 correspond to dllclk 130 and mclk 120, respectively, in Fig. 1.

As in Fig. 5, control signal (int\_clk) 530 in Fig. 6A is received by circuit element 535 and emerges from circuit element 535 as control signal (ext\_clk) 540. As before, control signal (int\_clk) 530 is transferred from the phase domain of internal clock 510 to the phase domain of external clock 500 by circuit element 535. In Fig. 6A, circuit element 535 preferably includes latches 610, 612, 614, 616, and 618. However, latch 610 (and/or latch 618) may be removed if the control signal and internal clock (and/or external clock) is close enough in phase. Each latch serves to re-time transitions in control signal (int\_clk) 530 to a phase domain corresponding to the signal enabling a particular latch (or its inverse, as explained later), thereby generating an intermediate control signal corresponding to each latch. Latch 610 is initialized by pulling its input low by default, using a pulldown, for example. This also initializes latches 612, 614, 616, and 618, once circuit element 535 has been operating long enough for the initialized input to propagate through circuit element 535. This would normally be part of a system initialization cycle.

The graph in Fig. 6B illustrates the waveforms generated during the operation of the circuit illustrated in Fig. 6A. Because external clock 500 has been applied for a sufficient length of time by a time  $T_0$ , the clock signals illustrated in Fig. 6A are at a steady state. For simplicity, the total delay between external clock 500 and internal clock 510 is taken to be equal to one clock period. Thus, using the circuit of Fig. 6A, intermediate clock 600 is delayed from external clock 500 by about one quarter of a clock period, as indicated by a transition 620, because four such delays are employed. Likewise, the delay between the intermediate clocks are also about one fourth of a clock period, as is the delay between intermediate clock 604 and internal clock 510. Thus, in this configuration, a delay of one clock period is required to resynchronize control signal (int\_clk) 530 to become control signal (ext\_clk) 540. These delays are illustrated in Fig. 6B by transitions 622, 624, and 626 for an equilibrium state in the circuit of Fig. 6A.

Each one of latches 610, 612, 614, 616, and 618 re-times control signal (int\_clk) 530 into a new phase domain, generating intermediate control signals Q 610, Q 612, Q 614, and Q 616 shown in Fig. 6B, respectively. This gradual shifting of clock signal (int\_clk) 530 from the phase domain of internal clock 510 to that of external clock 500 generates control signal (ext\_clk) 540. To reduce latency, the latches' enable inputs alternate between non-inverting and inverting inputs. This has the effect of alternately latching control signal (int\_clk) 530 on rising and falling edges of the waveforms shown in Fig. 6B (illustrated by transitions 630, 632, 634, and 636). The embodiment illustrated in Fig. 6A operates in the following manner.

Control signal (int\_clk) 530 goes active at time  $T_0$  and subsequently remains high until the clock enabled thereby is to be disabled. Preferably, control signal (int\_clk) 530 is first latched by latch 610 at a time  $T_1$  using internal clock 510 as an enable signal. The output of latch 610 is latched by latch 612 at a time  $T_2$  using intermediate clock 604 as an enable signal. This change in phase domain from

internal clock 510 to intermediate clock 604 is indicated in Fig. 6B by transition 630. Latch 612 has an inverting enable input so that the output of 610 is latched on the rising edge of intermediate clock 604. This permits the output of latch 610 to be latched by latch 612 one-half clock period sooner than if the enable input of latch 612 was non-inverting (thus latching on the falling edge of intermediate clock 604).

This process is repeated for latches 614 and 616 as is indicated by transitions 632 and 634. Finally, the signal output by latch 618 is close enough in phase to be latched by external clock 500, as is illustrated by transition 636. In this manner, control signal (int\_clk) 530 has its phase domain shifted from that of internal clock 510 to that of external clock 500. In effect, the latches simply delay control signal (int\_clk) 530, thereby gradually altering its phase domain.

Figs. 6C, 6D, and 6E are phase diagrams corresponding to Figs. 2B, 2C, and 2D, respectively, and illustrate the operation of the circuit of Fig. 6A in these various situations. Fig. 6C illustrates the re-timing of control signal (int\_clk) 530, which is shown as a vector 642 having a nominal phase delay of  $180^\circ$ . External clock 500 is shown as a vector 640 having a phase of  $0^\circ$ . Vector 642, also represented by internal clock 510, lags vector 640 by about  $180^\circ$ .

The various re-synchronization points illustrated in Fig. 6B ( $T_1$  through  $T_5$ ) are also shown in Fig. 6C. As is evident from the figure, re-timing is accomplished by successively delaying control signal (int\_clk) 530 (vector 642), from one synchronization point to the next, using the rising or falling edge of the appropriate intermediate clock. This process occurs in a time  $T_x$  643, which is equal to the time ( $T_5 - T_1$ ). Time  $T_1$  corresponds to the phase domain of external clock 500, time  $T_5$  corresponds to the phase domain of internal clock 510, and the remaining times correspond to the phase domain of their respective intermediate clocks.

A phase domain may be viewed as the collection of phase angles about a synchronization point such that a signal having one of those phase angles may safely be synchronized

with a signal (e.g., a clock) having the phase angle of the synchronization point. A signal may be synchronized safely if the synchronization will not generate unwanted pulses (e.g., runt pulses). As an approximation, then, the phase domain of each of the synchronization points illustrated in Fig. 6C extends from the preceding synchronization point to the following one. Therefore, a signal synchronized with a given clock signal (e.g., control signal (int\_clk) 530 synchronized with internal clock 510 at 180°) may safely be synchronized with the next successive clock signal (e.g., intermediate clock 604 at a phase angle of 135°). In this manner, control signal (int\_clk) 530 is safely re-timed from the phase domain of internal clock 510 to that of external clock 500, thereby producing control signal (ext\_clk) 540.

Fig. 6D illustrates the re-timing of control signal (int\_clk) 530 for the case shown in Fig. 2C. External clock 500 is again shown as a vector 640 having a phase of 0°. Control signal (int\_clk) 530 is represented by a vector 644. In this case, vector 644 lags vector 640 by only about 45° due to the aforementioned effects of environmental and process factors on inverter 132, first NAND gate 134, and inverter string 140. This may also be viewed as a decrease in the delay between internal clock 510, represented by vector 644, and external clock 500, which experiences only a short delay through the circuit elements thus affected. The delay needed to re-time control signal (int\_clk) 530 is thus reduced to a time  $T_x$  645.

As is evident from Fig. 6A, the timing of intermediate clocks 600-604 are also dependent on these environmental and process factors. Thus, as the delay caused by each inverter pair in inverter string 140 (and that caused by inverter 132/first NAND gate 134) decreases, the phase angle between synchronization points decreases, with latch delays decreasing commensurately. As a result, latch delays decrease commensurately and control signal (int\_clk) 530 is stepped through smaller phase angles in the synchronization process. In this manner, an apparatus according to the present invention compensates for the effects of environmental

and process factors which decrease the propagation delays exhibited by integrated circuitry.

In a similar manner, an apparatus according to the present invention compensates for the effects of environmental and process factors which increase propagation delays. Fig. 6E illustrates the re-timing of control signal (int\_clk) 530 for the case shown in Fig. 2D. External clock 500 is again shown as a vector 640 having a phase of  $0^\circ$ . Control signal (int\_clk) 530 is represented by a vector 646. In this case, vector 644 lags vector 640 by about  $385^\circ$  due to the aforementioned factors. Alternatively, this may be viewed as an increase in the delay between internal clock 510, also represented by vector 646, and external clock 500. In this situation, external clock 500 experiences a long delay through the circuit elements thus affected. The delay needed to re-time control signal (int\_clk) 530 is thus increased to a time  $T_x$  647. Here, the delay is increased, and the phase angle between synchronization points experiences a corresponding increase. As a result, control signal (int\_clk) 530 is stepped through larger phase angles in the synchronization process. Thus, an apparatus according to the present invention is also capable of compensate for increases in the propagation delays exhibited by integrated circuitry.

Fig. 6F further illustrates the timing relationships between the signals generated throughout the circuit illustrated in Fig. 6A, as well as their relationship to the clocking signal generated in Fig. 1. For clarity, it should be noted that control signal (ext\_clk) 540 corresponds to rclk\_en 100 in Fig. 1. Moreover, dllclk 130 and mclk 120 correspond to external clock 500 and internal clock 510, respectively. Also, as previously discussed, control signal 520 (i.e., rclk\_en 100) is synchronized to internal clock 510 (i.e., mclk 120). Control signal 520 is preferably strobed at a time  $T_1$  by the falling edge of a pulse int\_clk0 650. Control signal (int\_clk) 530 may transition at any time prior to  $T_2$  (setup and hold time notwithstanding), but must be valid for the falling edge of internal clock 510 (represented

by a pulse int\_clk1 655) because it is at this point that the re-timing process begins.

The re-timing of control signal (int\_clk) 530 proceeds in the manner shown in the graph illustrated in Fig. 6B and is represented by a transition 660.

Transition 660 corresponds to transitions 630, 632, 634, and 636. At a time  $T_3$ , the synchronization of control signal (ext\_clk) 540 to external clock 500 is completed, as is indicated by a transition 665. The delay through circuit element 535 is equal to the duration of transition 660 (i.e., the time  $T_3 - T_2$ ).

Clock rclk 110 is then enabled by control signal (ext\_clk) 540. This occurs from the point at which control signal (ext\_clk) 540 transitions (i.e., time  $T_3$ ), which is indicated by a transition 670. Transition 670 indicates that a pulse ext\_clk4 675 occurring at a time  $T_4$  will be allowed to propagate to generate rclk 110. From time  $T_4$ , external clock 500 (as exemplified by a pulse ext\_clk4 675) propagates through inverter 132, first and second NAND gates 136 and 134, and inverter strings 140 and 150, emerging at a time  $T_5$  as rclk 110, exemplified by pulse rclk0 680, and internal clock 510 (i.e., mclk 120), exemplified by a pulse int\_clk4 685, as indicated by a trace 690 and a trace 695, respectively. As noted, because external clock 500 experiences the same delays in generating internal clock 510 and rclk 110, internal clock 510 and rclk 110 are synchronized with one another.

Fig. 7 illustrates an alternative embodiment of the present invention. Circuit element 505 and its constituent elements, and all related signals are defined identically to those in Fig. 6A. The method is very similar to that of the circuit in Fig. 6A. However, the elements shifting the control signal from the phase domain of internal clock 510 into the phase domain of external clock 500 differ slightly. In Fig. 7, pass transistors and inverters are used in place of the latches illustrated in Fig. 6A. As before, control signal (int\_clk) 530 is introduced into circuit element 535 and is successively synchronized to internal clock 510, intermediate

clocks 604, 602, and 600, and finally external clock 500. Again, the pass transistors alternate between inverting and non-inverting inputs to allow the signal propagated to traverse circuit element 535 as quickly as possible.

5 Fig. 8 illustrates timing constraints using the signals of intermediate clock 604 and internal clock 510 as previously illustrated in Fig. 6B. For proper operation of a circuit according to the present invention, the following conditions must be met:

$$10 \quad T_{ext\_clk} > 4t_{inv} + 2t_{p\_latch} + 2t_{su\_latch} \quad (2)$$

$$F_{ext\_clk} < \frac{1}{4t_{inv} + 2t_{p\_latch} + 2t_{su\_latch}} \quad (3)$$

15 where  $T_{ext\_clk}$  is the period of external clock 500,  $t_{inv}$  is the delay of one of the inverters in inverter string 140,  $t_{p\_latch}$  is the delay of latch 610 (preferably, a similar delay is caused by all the latches),  $t_{su\_latch}$  is the setup time of latch 610 (again, all the latches preferably exhibit similar setup times), and  $F_{ext\_clk}$  is the frequency of external clock 500. These formulae are for a circuit such as that  
20 shown in Fig. 6A, where intermediate clocks are generated using two inverters and latches are employed to re-synchronize the control signal. The above limitation can be generalized to:

$$T_{ext\_clk} > d(n-1) \quad (4)$$



$$F_{ext\_clk} < \frac{1}{d(n-1)} \quad (5)$$

where  $T_{ext\_clk}$  is the period of external clock 500,  $d$  is the delay between each intermediate clock,  $n$  is the number of intermediate clocks (including the internal clock), and  $F_{ext\_clk}$  is the frequency of external clock 500. Thus, a number of delays which can be used to successfully delay a control signal from the phase domain of the internal clock to that of the external clock is  $n$  (there may be more than a single number that meets this criteria, depending on the delay of each delay element and the frequencies involved). Again,  $F_{ext\_clk}$  is the inverse of  $T_{ext\_clk}$ , and is given for completeness.

If the frequency of external clock 500 is above  $F_{ext\_clk}$ , a circuit of the present invention ceases to function properly. In such a case, the signal propagated through circuit element 535 fails to meet  $t_{su\_latch}$  (i.e., the setup time of the next latch). Thus, the propagated signal is not ready to be latched by the next latch at the falling edge of the next intermediate clock signal. This introduces the possibility of metastability. At a minimum, this results in the control signal being delayed an additional full clock cycle, greatly increasing the overall latency of circuit element 535 and thus the response time of the circuit of the present invention. These delays are shown in Fig. 8 as transitions 800 and 810. Transition 800 represents the delay between intermediate clock 604 and internal clock 510 caused by the two inverters in the signal path. Transition 810 represents the delay of latch 610 plus any additional time remaining between when the clock signal output by latch 610 stabilizes and the next rising edge of intermediate clock 604.

A circuit according to the method of the present invention offers several advantages. In its operation, such a circuit avoids the generation of runt pulses while providing synchronized control signals with minimum latency. Additionally, the method of the present invention is not susceptible to the failure modes which can occur with simple

gating schemes, also avoiding the need to compute MTBF figures.

5 The method of the present invention is insensitive to both process variations and changes in device feature size, as well as environmental perimeters such as temperature and supply voltage. For example, a rise (fall) in supply voltage or a decrease (increase) in operating temperature decreases (increases) the delays experienced in integrated circuitry. However, because the given factor speeds or slows both the  
10 circuitry generating the internal clock and that synchronizing the control signal, no aggregate effect is observed and the circuitry remains synchronized.

The method of the present invention is not intended to be limited by the preceding statements. A person of  
15 ordinary skill in the art will realize that different circuitry can be used and alterations can be made to the method of the present invention without departing from the spirit of the invention. Other equivalent or alternative methods of synchronizing a signal according to the present  
20 invention will be apparent to those skilled in the art. For example, flip-flops may be employed in place of the latches of the present invention, and may be edge-triggered to permit synchronization on rising clock edges. These equivalents and alternatives are intended to be included within the scope of  
25 the present invention.

WHAT IS CLAIMED IS:

1           1.    A method of synchronizing a control signal with  
2           a first clock, the control signal being synchronous to a  
3           second clock, the method comprising the steps of:-  
4                 generating a plurality of intermediate clock  
5           signals, each one of said plurality of intermediate clock  
6           signals being generated by delaying the first clock, a last  
7           one of said plurality of intermediate clock signals being the  
8           second clock;  
9                 receiving the control signal;  
10                synchronizing the control signal with a one of said  
11           plurality of intermediate clock signals to produce a one of a  
12           plurality of intermediate control signals;  
13                synchronizing said one of said plurality of  
14           intermediate control signals with another of said plurality of  
15           intermediate clock signals to produce another of said  
16           plurality of intermediate control signals; and  
17                repeating said step of synchronizing said one of  
18           said plurality of intermediate control signals, to produce  
19           said plurality of intermediate control signals, a last one of  
20           said plurality of intermediate control signals being  
21           synchronous to the first clock.

1           2.    The method of claim 1, wherein the control  
2           signal is synchronized to a rising edge of said one of said  
3           plurality of intermediate clock signals and said one of said  
4           plurality of intermediate control signals is synchronized to a  
5           falling edge of said another of said plurality of intermediate  
6           clock signals.

1           3.    The method of claim 1, wherein said plurality  
2           of intermediate control signals are alternately synchronized  
3           to a rising edge and a falling edge of said plurality of  
4           intermediate clock signals.

1           4.    A method of synchronizing a control signal with  
2 a first clock signal, the control signal having a phase  
3 relationship with a second clock signal, comprising the steps  
4 of:

5                generating a plurality of intermediate clock signals  
6 using the first clock signal, a first one of said plurality of  
7 intermediate clock signals lagging the first clock signal,  
8 each successive one of said plurality of intermediate clock  
9 signals lagging a preceding one of said plurality of  
10 intermediate clock signals, and a last one of said each  
11 successive one of said plurality of intermediate clock signals  
12 serving as the second clock signal;

13               synchronizing the control signal with at least one  
14 of said plurality of intermediate clock signals to produce an  
15 intermediate control signal; and

16               synchronizing said intermediate control signal with  
17 the first clock signal.

1           5.    The method of claim 1, wherein said step of  
2 synchronizing the control signal comprises synchronizing the  
3 control signal with each one of said plurality of intermediate  
4 clock signals in a successive manner by proceeding from said  
5 last one of said each successive one of said plurality of  
6 clock signals to said first one of said plurality of  
7 intermediate clock signals to produce said intermediate  
8 control signal.

1           6.    The method of claim 5, wherein said  
2 synchronization is performed by providing said each one of  
3 said plurality of intermediate clock signals to a control  
4 input of a corresponding synchronization circuit.

1           7.    The method of claim 6, wherein said  
2 synchronization circuit comprises a latch, said control input  
3 being an enable input of said latch.

1           8. The method of claim 6, wherein said  
2 synchronization circuit comprises:  
3           a delay element; and  
4           a pass transistor coupled to an input of said delay  
5 element, said control input controlling said pass transistor.

1           9. The method of claim 5, wherein durations by  
2 which said first one of said plurality of intermediate clock  
3 signals lags the first clock signal and by which each  
4 successive one of said plurality of intermediate clock signals  
5 lags a preceding one of said plurality of intermediate clock  
6 signals are substantially equal.

1           10. The method of claim 9, wherein said durations  
2 are dependent on a plurality of circuit delays.

1           11. The method of claim 5, wherein the control  
2 signal is synchronized using a subset of said plurality of  
3 intermediate clock signals.

1           12. The method of claim 5, wherein the control  
2 signal is synchronized to a rising edge of every other one of  
3 said plurality of intermediate clock signals and is  
4 synchronized to a falling edge of the remaining ones of said  
5 plurality of intermediate clock signals.

1           13. A circuit for synchronizing a control signal  
2 with a first clock signal to create a synchronized control  
3 signal, the control signal having a phase relationship with a  
4 second clock signal, comprising:

5           a clock generation circuit which receives the first  
6 clock signal and outputs a plurality of intermediate clock  
7 signals, the second clock signal being a last one of said  
8 plurality of intermediate clock signals; and

9           a plurality of circuit elements,  
10           a first one of said plurality of circuit  
11 elements receiving the control signal and a first one of said  
12 plurality of intermediate clock signals, and synchronizing the

13 control signal with said first one of said plurality of  
14 intermediate clock signals,  
15           each successive one of said plurality of  
16 circuit elements receiving an output from a preceding one of  
17 said plurality of circuit elements and a corresponding one of  
18 said plurality of intermediate clock signals, and  
19 synchronizing said output from a preceding one of said  
20 plurality of circuit elements with said corresponding one of  
21 said plurality of intermediate clock signals, and  
22           a last one of said plurality of circuit  
23 elements receiving an output of a last preceding one of said  
24 plurality of circuit elements and the first clock signal, and  
25 synchronizing said output of said last one of said plurality  
26 of circuit elements with the first clock signal, thereby  
27 producing the synchronized control signal.

1           14. The apparatus of claim 13, wherein a first one  
2 of said plurality of intermediate clock signals lags the first  
3 clock signal, each successive one of said plurality of  
4 intermediate clock signals lags a preceding one of said  
5 plurality of intermediate clock signals, and a last one of  
6 said each successive one of said plurality of intermediate  
7 clock signals serves as the second clock signal.

1           15. The apparatus of claim 13, wherein each one of  
2 said plurality of circuit elements is a delay element.

1           16. The apparatus of claim 13, wherein each one of  
2 said plurality of circuit elements is a clocked circuit  
3 element.

1           17. The apparatus of claim 16, wherein said clocked  
2 circuit element is a latch.

1           18. The apparatus of claim 17, wherein said clocked  
2 circuit element is an edge-triggered flip-flop.

1           19. An apparatus for synchronizing a control signal  
2 with a first clock signal, the control signal having a phase  
3 relationship with a second clock signal, comprising:

4           a clock generation means for generating a plurality  
5 of intermediate clock signals using the first clock signal, a  
6 first one of said plurality of intermediate clock signals  
7 lagging the first clock signal, each successive one of said  
8 plurality of intermediate clock signals lagging a preceding  
9 one of said plurality of intermediate clock signals, and a  
10 last one of said each successive one of said plurality of  
11 intermediate clock signals serving as the second clock signal;

12           a plurality of synchronization means for  
13 synchronizing the control signal with each one of said  
14 plurality of intermediate signals in a successive manner by  
15 proceeding from said last one of said each successive one of  
16 said plurality of intermediate clock signals to said first one  
17 of said plurality of intermediate clock signals to produce an  
18 intermediate control signal; and

19           a last synchronization means for synchronizing said  
20 intermediate control signal with the first clock signal.

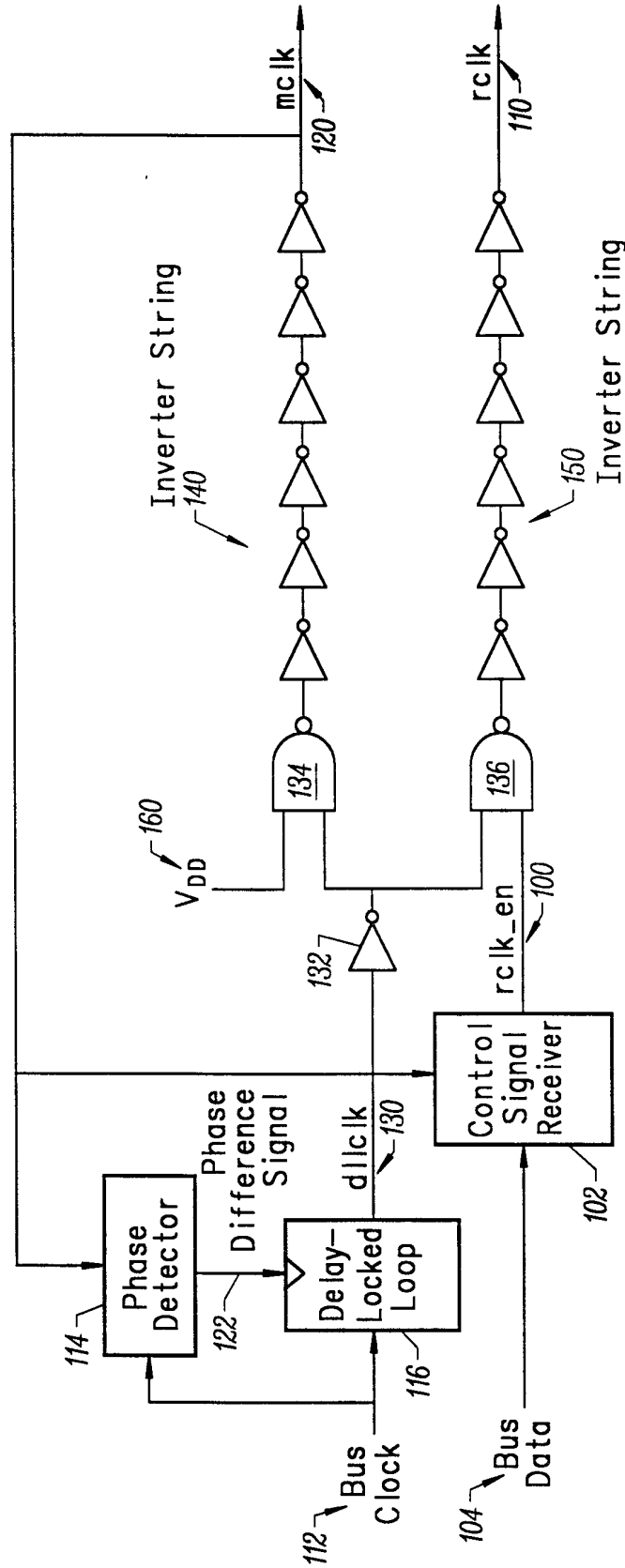
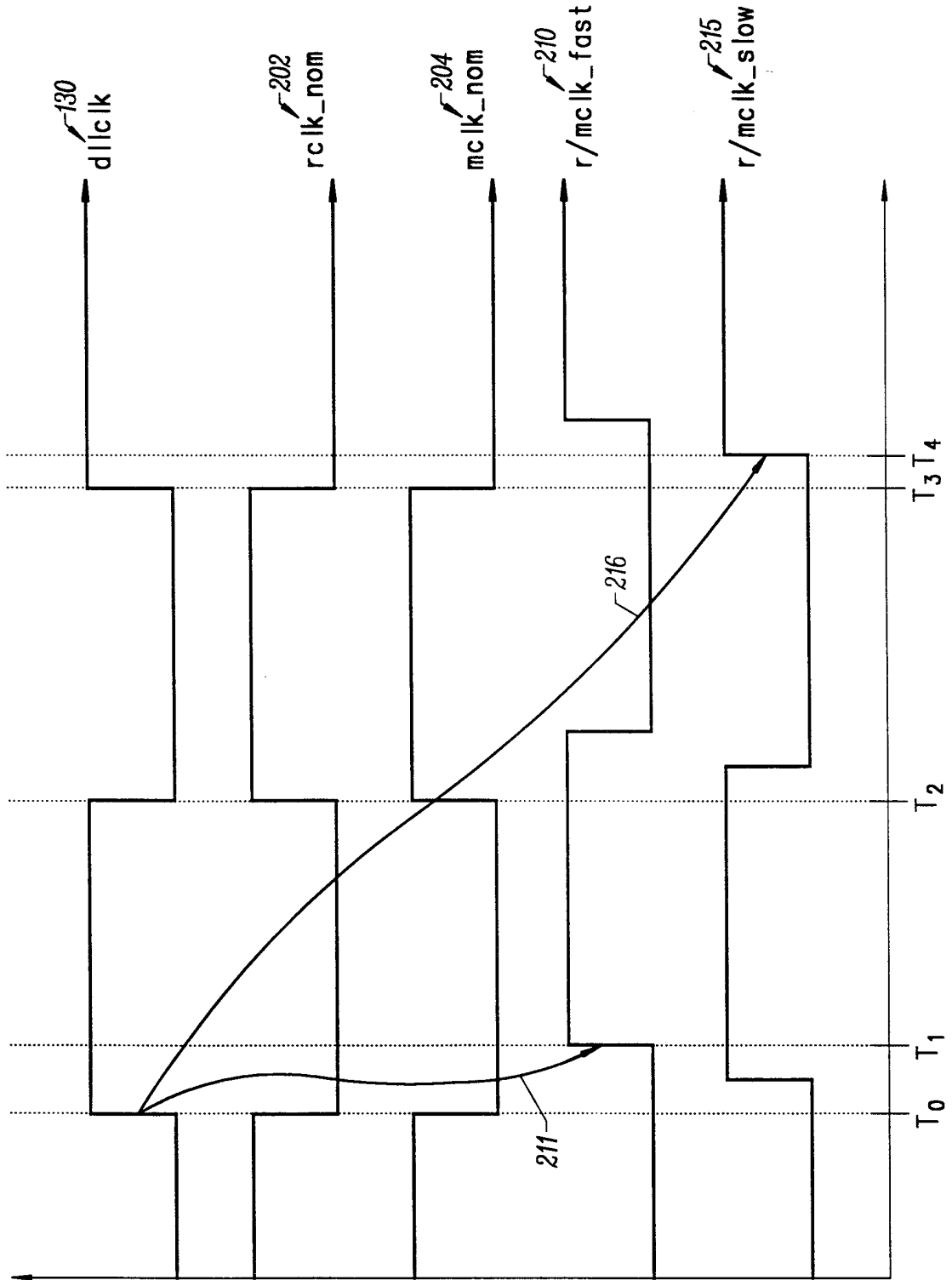


FIG. 1  
(Prior Art)





**FIG. 2**  
(Prior Art)

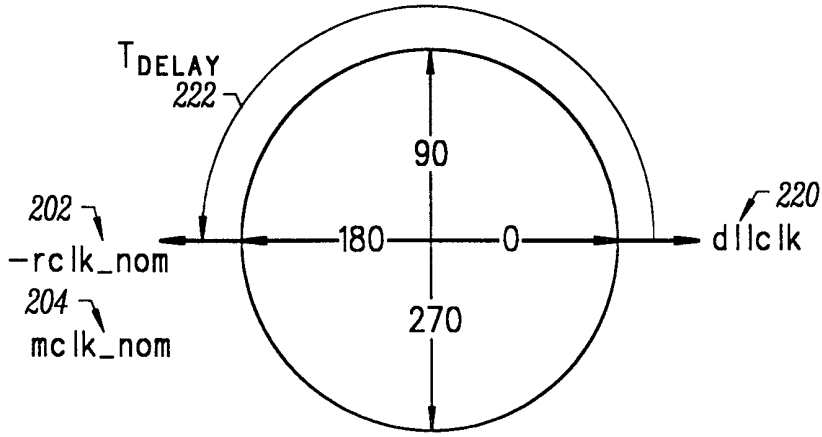


FIG. 2B  
(Prior Art)

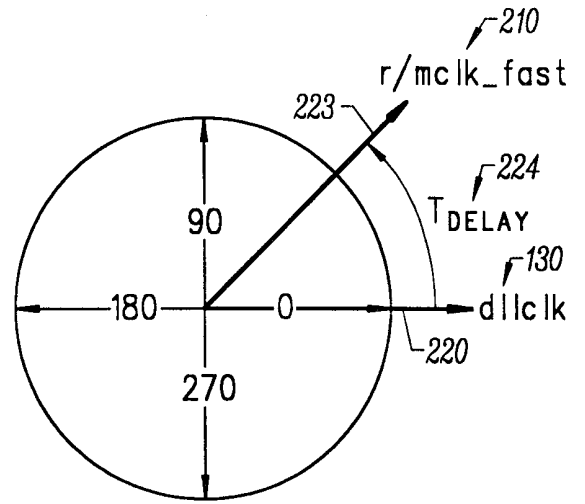


FIG. 2C  
(Prior Art)

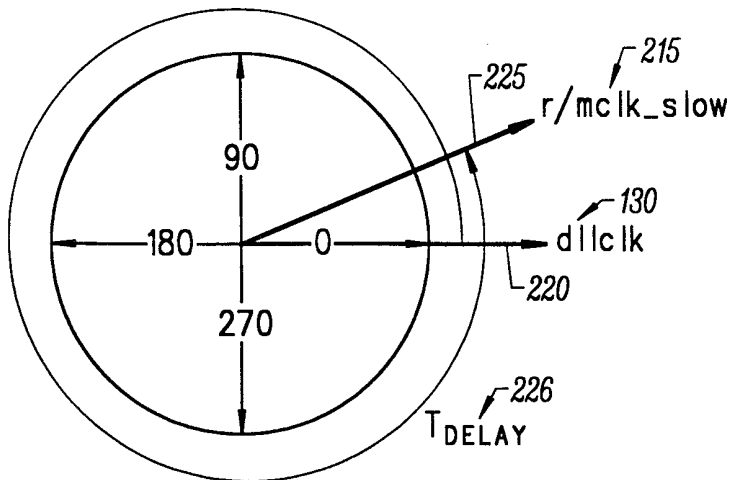
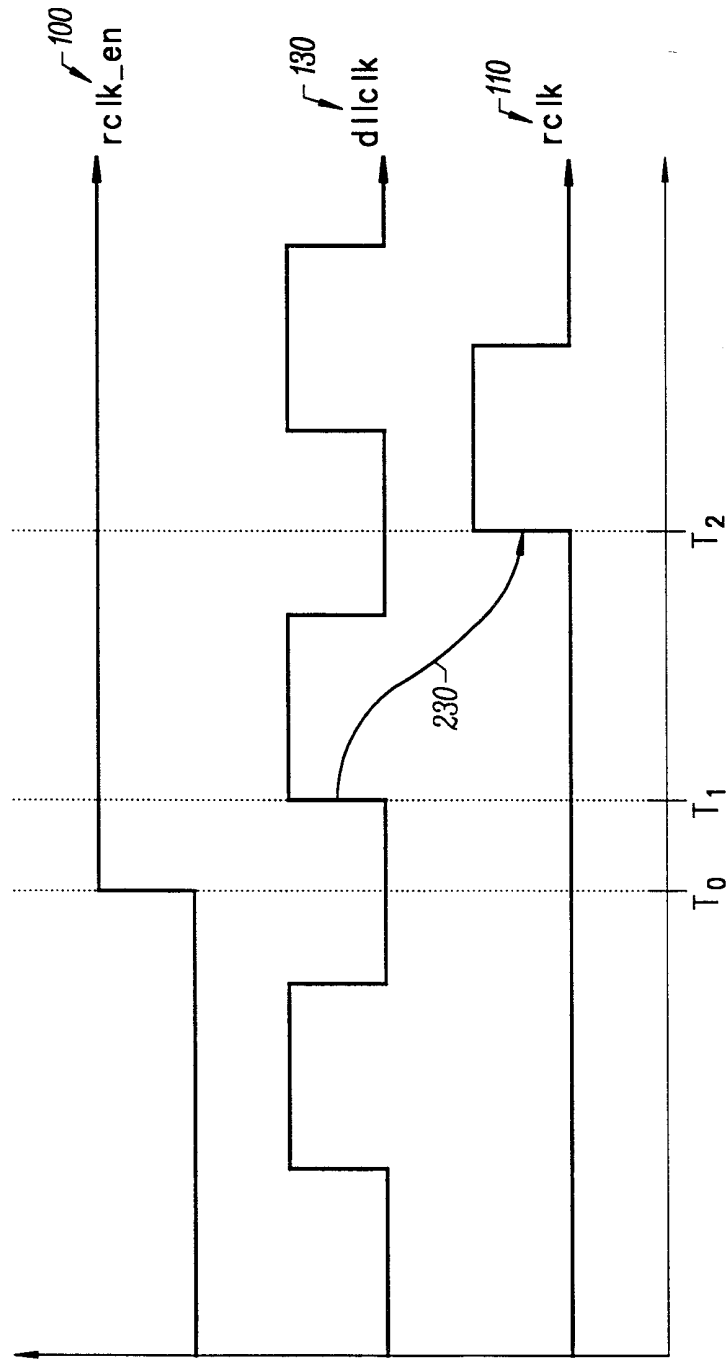
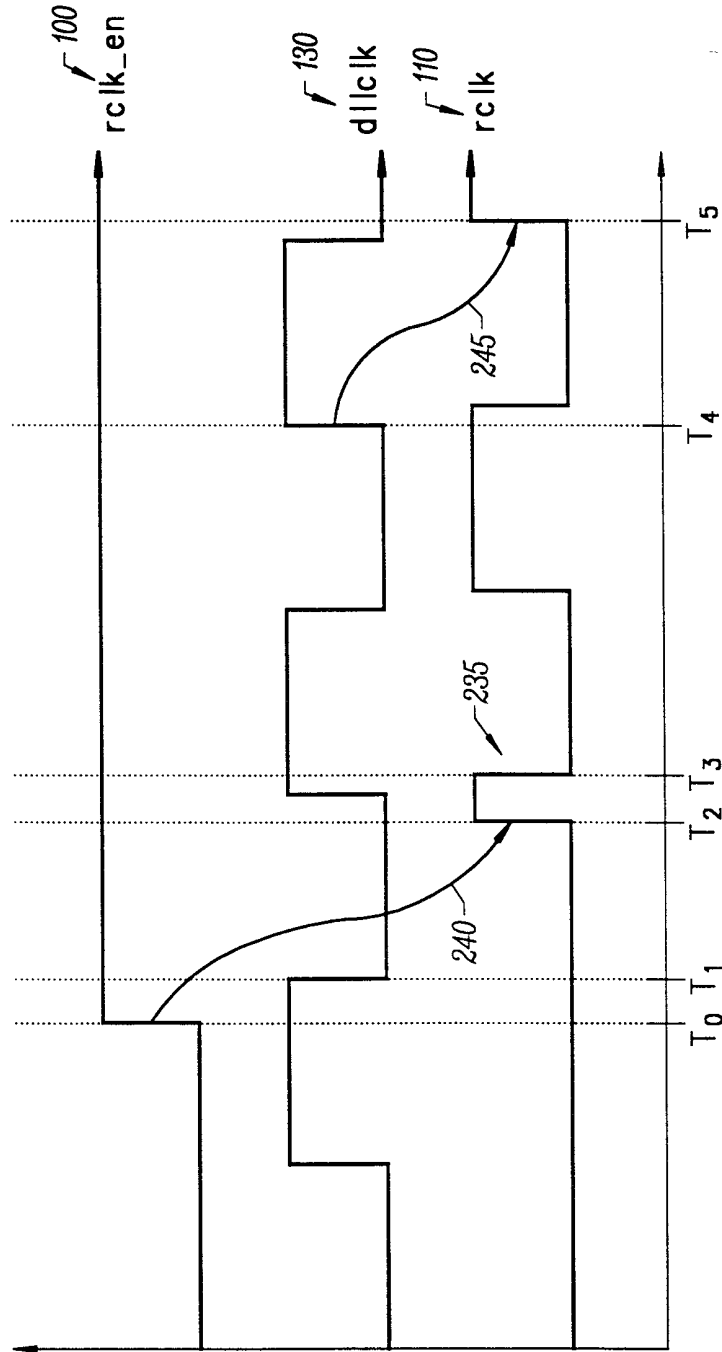


FIG. 2D  
(Prior Art)



**FIG. 2E**  
(Prior Art)



**FIG. 2F**  
(Prior Art)

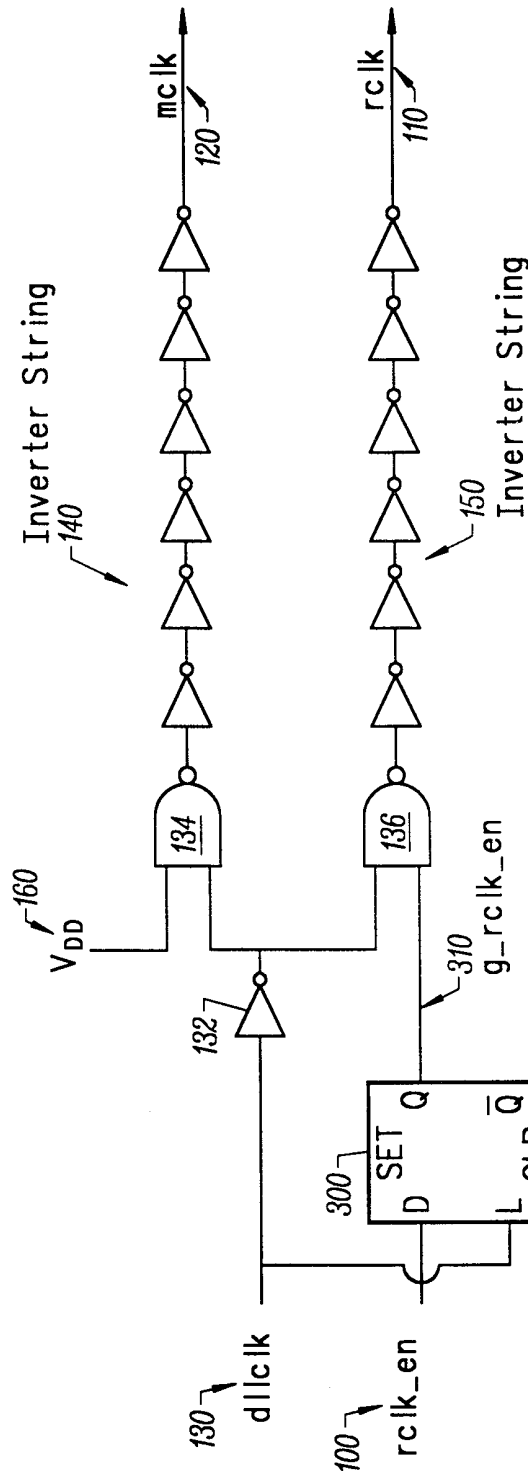


FIG. 3  
(Prior Art)

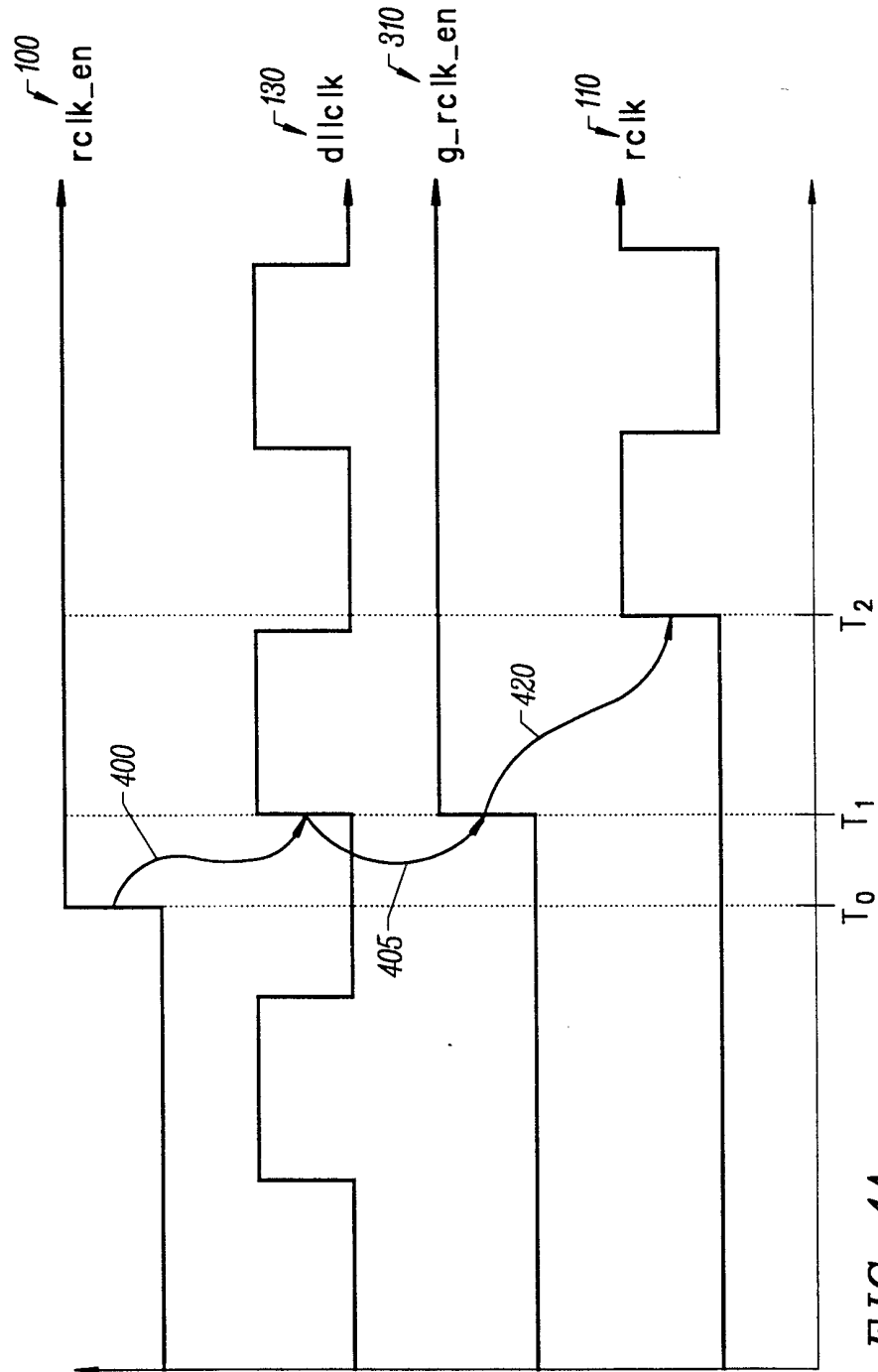


FIG. 4A  
(Prior Art)

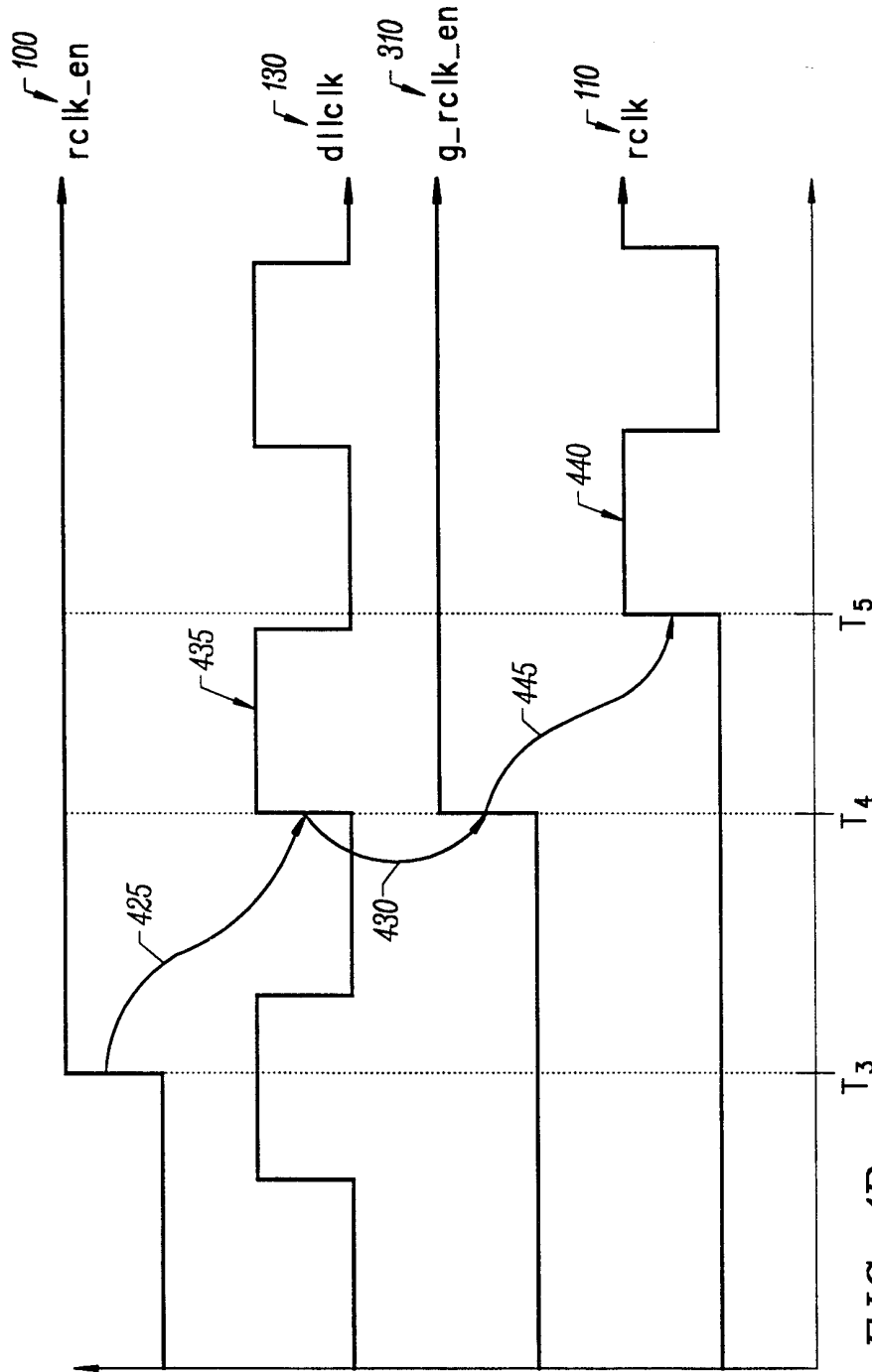


FIG. 4B  
(Prior Art)

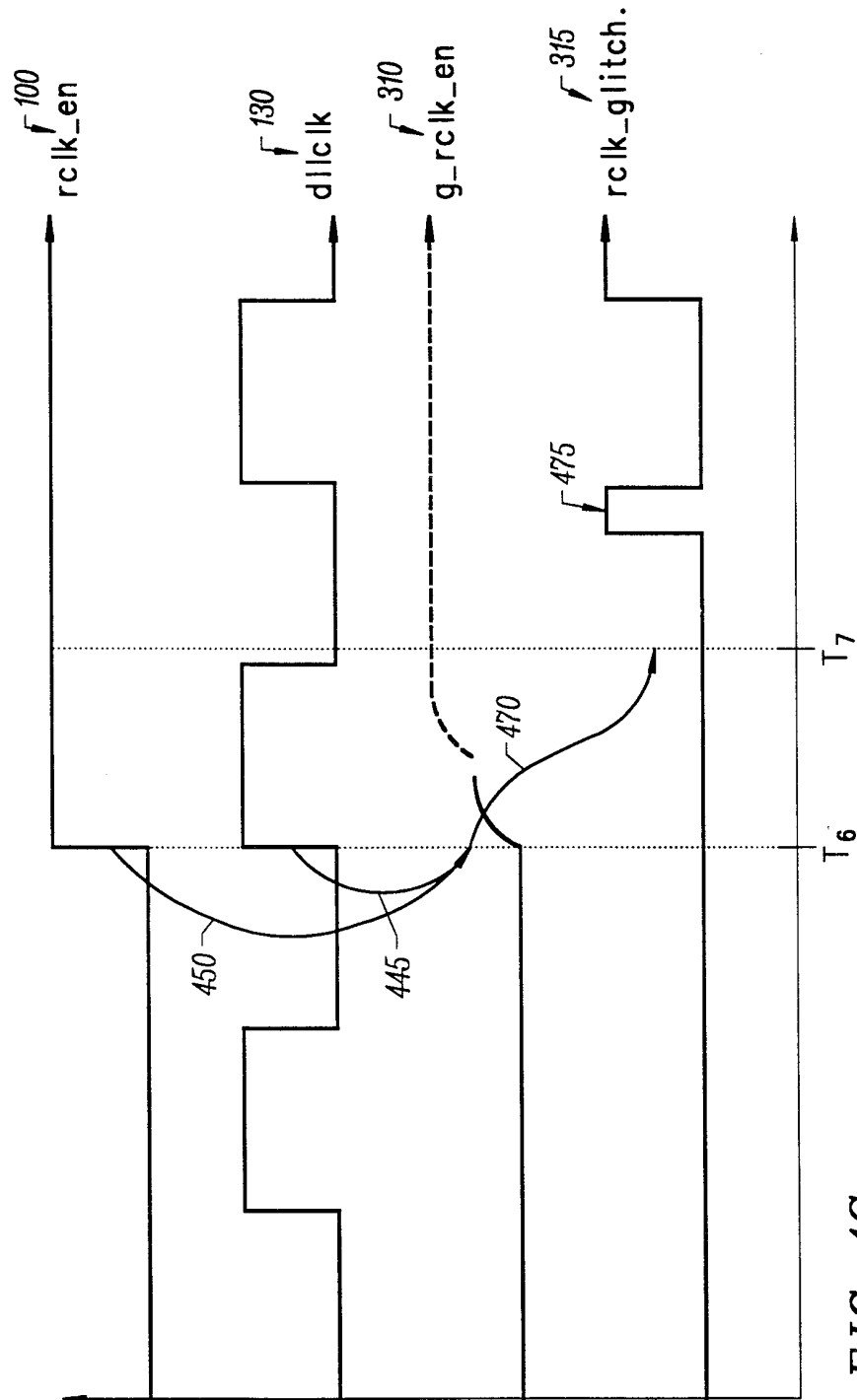


FIG. 4C  
(Prior Art)



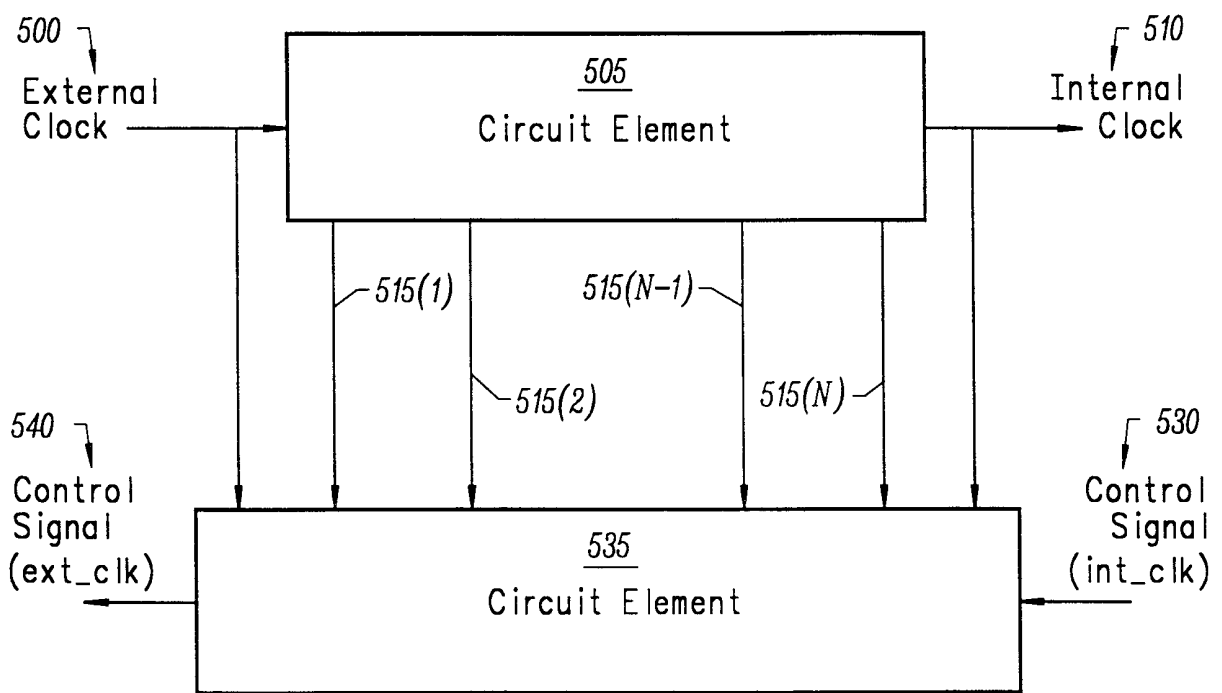


FIG. 5



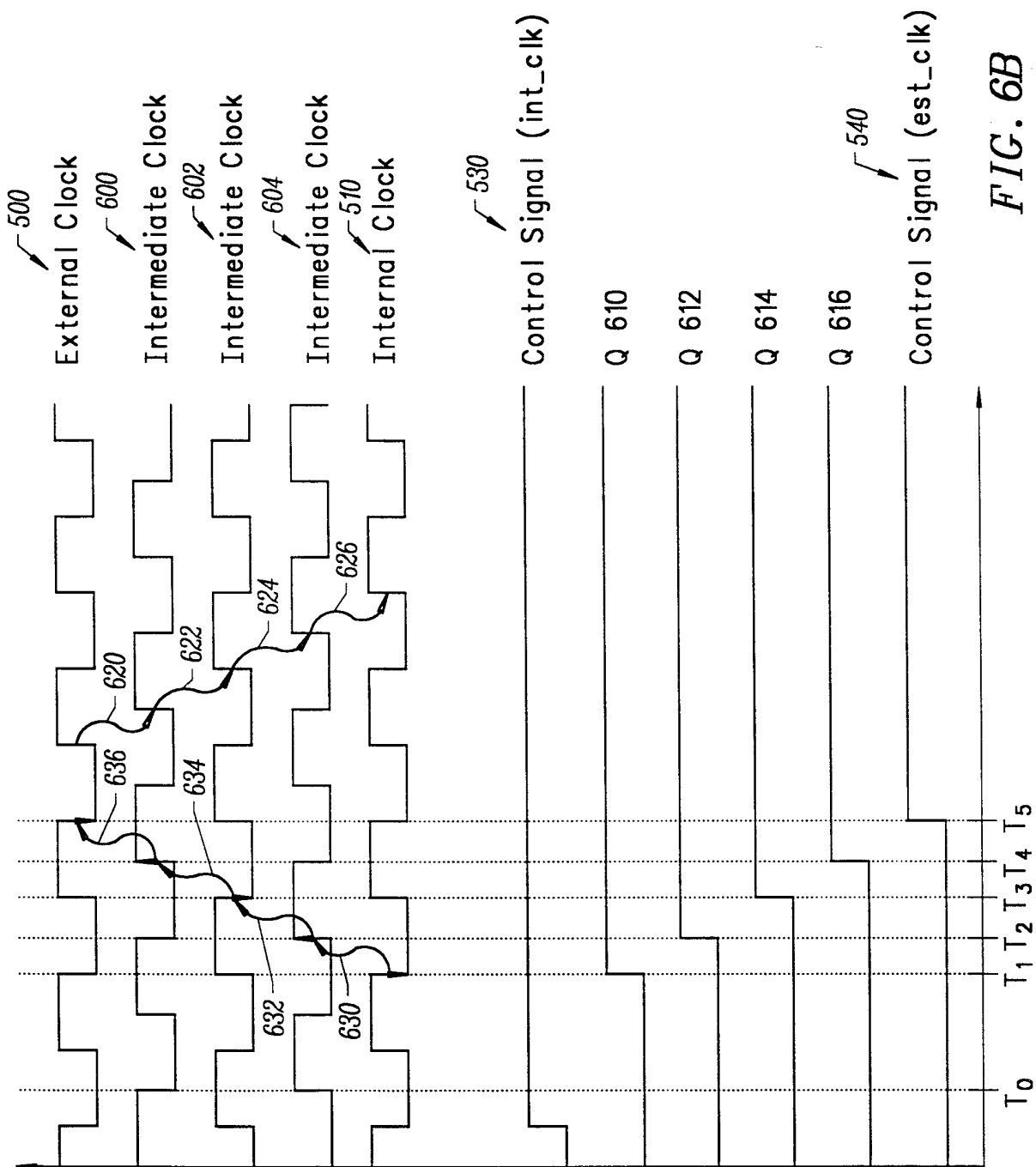


FIG. 6B

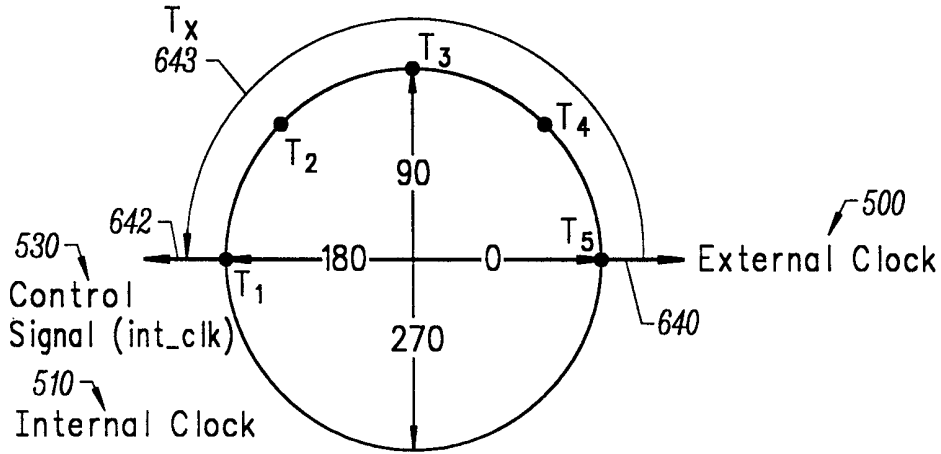


FIG. 6C

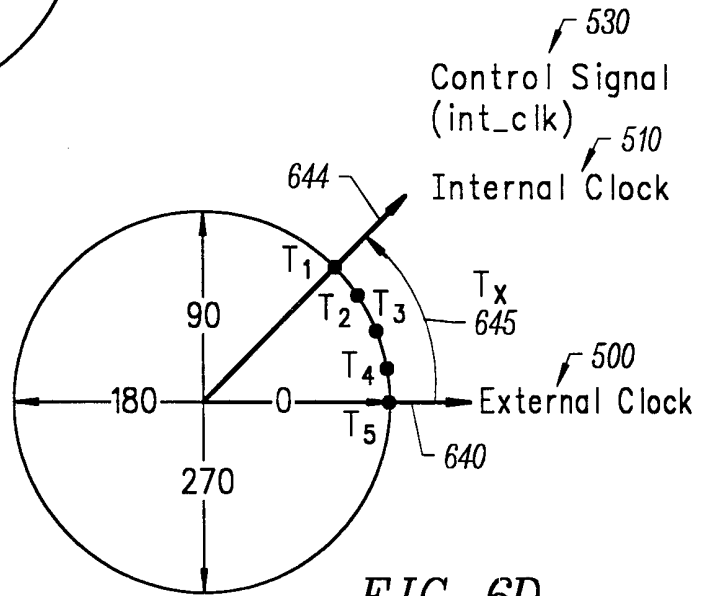


FIG. 6D

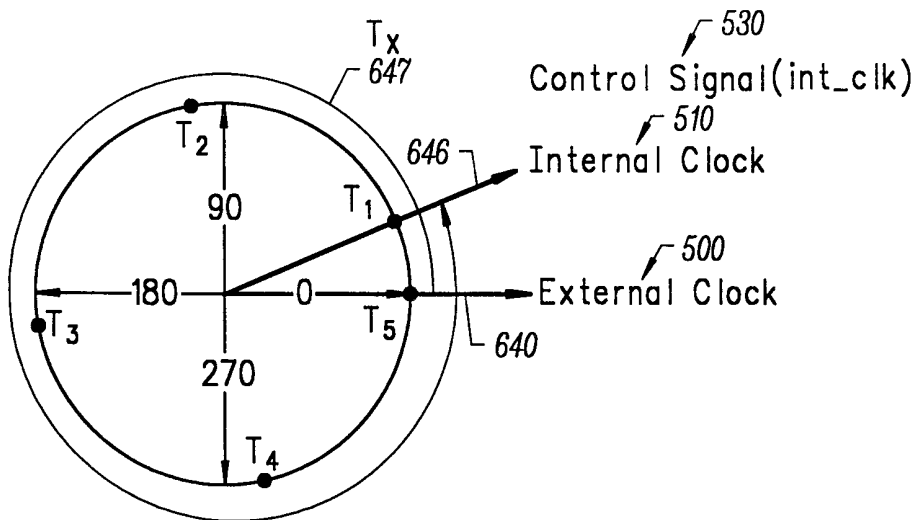


FIG. 6E

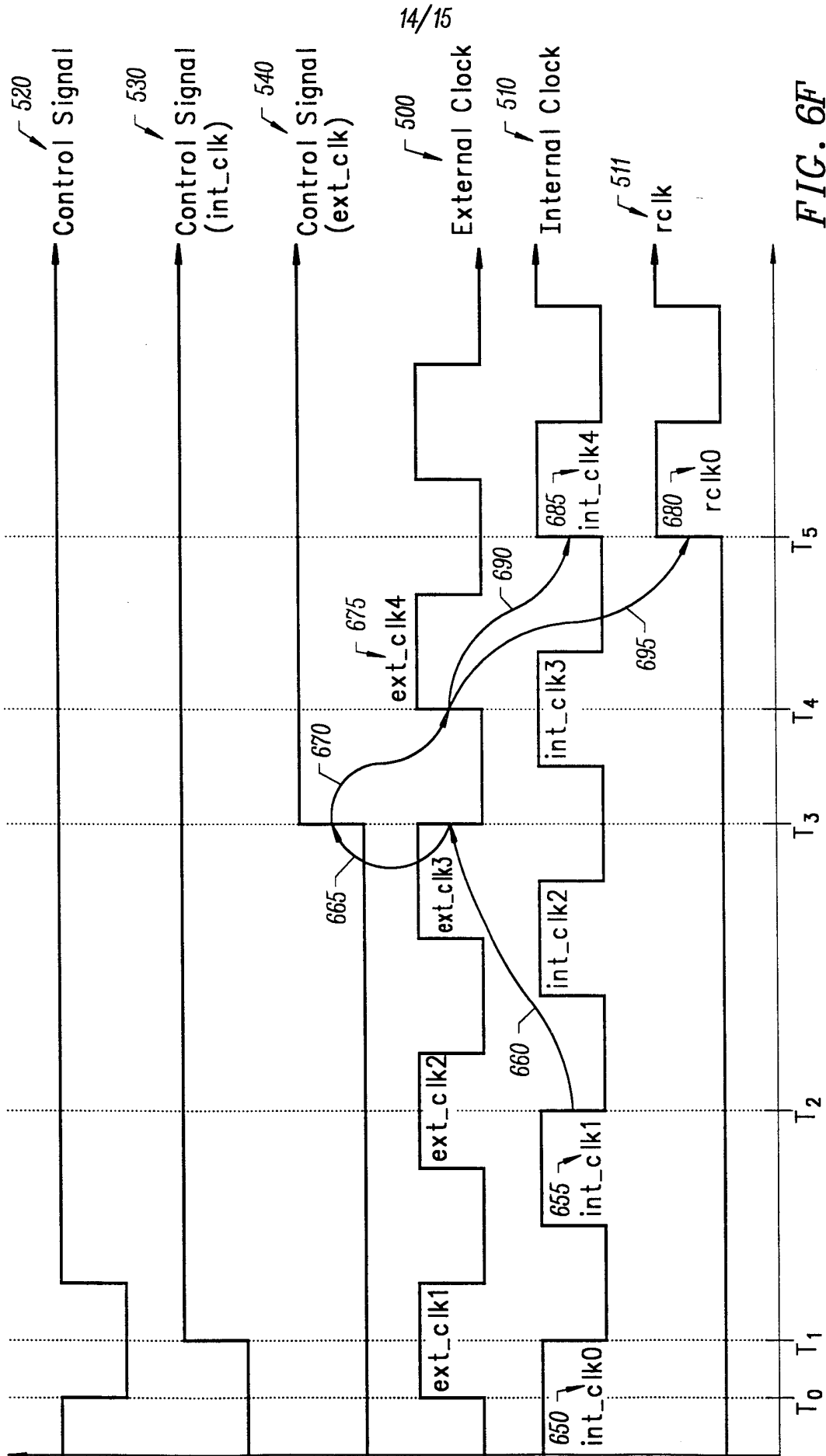
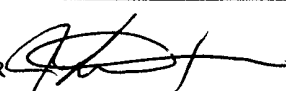


FIG. 6F



INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US98/14152

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC(6) :H04L 7/00 US CL :375/354 According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) U.S. : 375/354; 327/144, 149, 136, 152, 153 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) APS		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, P	US 5,764,092 A (WADA et al) 09 JUNE 1998, abstract, figures 3-6, column 2, claims 1-3.	1-19
Y	US 5,534,805 A (MIYAZAKI et al) 09 JULY 1996, abstract, figures 3 and 9, columns 3-7.	1-19
Y	US 5,532,633 A (KAWAI) 02 JULY 1996, abstract, col. 2, line 40 to col. 3, line 16.	1-19
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search 18 SEPTEMBER 1998	Date of mailing of the international search report <b>16 OCT 1998</b>	
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MOHAMMAD GHAYOUR  Telephone No. (703) 306-3034	