Invention concerning a driver circuit for a two wired loop bus comprising: a first capacitance element (C1) connected between two input voltage supplies (3, 5); a second capacitance element (C2) connected between two output voltage supplies (7, 9); a first series connection of two switching elements (S1, S2) connected between the two input voltage supplies (3, 5); a second series connection of two switching elements (S3, S4) connected between the two output voltage supplies (3, 5); and an inductance (L1), one end of which being connected between the two switching elements (S1, S2) of the first series connection, and the other end thereof being connected between the two switching elements (S3, S4) of the second series connection.
The present invention is directed to a driver circuit, a bus master device, a fire detection system and a burglar alarming system using the driver circuit.

Alarm systems are known which have a control module or bus master device to which subscribers are connected by means of a two-wire line, said subscribers receiving from the control module, via the two-wire line operated as a field bus, both a power supply voltage and communication messages in the form of pulse trains impressed on the power supply voltage as voltage modulation.

Alarm systems of the type cited above are prior art. The two-wire line to which the subscribers are connected in parallel may have a length of between 1000 and 2000 m, for example, and is frequently routed in a loop or ring shape, i.e. it starts and ends at the bus master device. The two-wire line is also referred to simply as a field bus.

The subscribers may be sensors, e.g. fire or burglar alarms, and/or actuators, such as light-signal or sound-signal generators. The power supply voltage for the subscribers may be in the range from 20 to 40 volts, for example, at the start of the two-wire line.

The communication between the bus master device and the subscribers is handled on the basis of a digital communication protocol. The communication protocol defines time slots or time windows which are used to transmit pulses and pulse trains as data messages which represent addresses, commands and reports, and thus the transmission frequency are also hardware dependent.

The power dissipation of the output transistors is very high. The efficiency is only about 50 % to 70 %.

The protocol/communication level cannot be generated universally (e.g. software defined), they are usually fixed and dependent on hardware. Rise and fall times and thus the transmission frequency are also hardware dependent.

Especially the invention provides a Driver circuit for a two-wired loop bus comprising a first capacitance element connected between two input voltage supplies, a second capacitance element connected between two output voltage supplies, a first series connection of two switching elements connected between the two input voltage supplies, a second series connection of two switching elements connected between the two output voltage supplies, and an inductance, one end of which being connected between the two switching elements of the first series connection, and the other end thereof being connected between the two switching elements of the second series connection.

According to a preferred embodiment the driver circuit comprises four diodes each being connected so as to bridge one of the switching elements.

Furthermore, the bus master device can be configured so that the controller controls the switching of the switching elements with different pre-set timings, so as to provide different voltage levels on the two wired loop bus. According to a further aspect of the invention the bus master device is configured so as to switch the first switch of the second series connection synchronously.

Finally the invention provides a burglar alarm system comprising a bus master device as recited above and a two wired loop bus comprising a plurality of burglar detecting devices and/or alarming devices connected between the two wires of the bus.
In the following preferred embodiments of the invention will be described with reference to the accompanying drawings, which show:

Figure 1 a fire detection system according to the present invention;
Figure 2 a block diagram of the Bus master Device; and
Figure 3 a circuit diagram of a driver circuit according to the invention.

As explained at the outset, the alarm systems comprises a control center or bus master device 29 (possibly also subordinate control centers). The bus master device 29 has both the start and the end of a two-wire line 11, 13 connected to it. The two-wire line 11, 13 has numerous subscribers T01, T02, ... T10 electrically connected to it in parallel at intervals. The two-wire line 11, 13 provides the power supply voltage for the subscribers T01, T02, ... T10 and is simultaneously used for bidirectional communication between the bus master device 29 and the subscribers T01, T02, ... T10. The two-wire line 11, 13 is therefore also referred to as a ring or loop bus for short.

The subscribers T01, T02, ... T10 can be e.g. fire detectors, burglar detectors, alarming devices and so on.

Example the use of FETs or of bi-polar n-channel or p-channel transistor is possible.

Here any type of switch, like transistors, can be used. The transistors are not limited to a particular transistor type. For example the use of FETs or or bi-polar n-channel or p-channel transistor is possible.

As mention above the subscribers can have the function of detectors or may have the function of alarming devices, like flash lights or acoustic alarms.

The bus master device 29 can be connected on a primary side, opposite to the loop bus side, with a communication bus, which in turn might be connected to a central control controlling a plurality of bus master devices. Additionally the bus master device is connected to a power supply and comprises a power converter to provide an internal operation voltage, e.g. 42 V, which is supplied to the input side of the driver circuit 19.

The bus master device 29 can comprise further elements dedicated to different control operations and to the internal operation of the bus master device 29. Which will not be explained in further detail in this application.

Figure 2 shows the bus master device 29 in more detail. The bus master device 29 mainly comprises a controller 25 for controlling the operation of the bus master device 29 and of the loop bus, a memory 17 for storing operation data and control data for the bus master device 29, a driver circuit 15 for providing the operation voltage and the control signals for the loop bus and switching units 21, 23 for the connection of the output of the driver circuit 19 with the input side of the two wires 11, 13 of the loop bus. Additionally the bus master device might comprise a current detector 15 for detecting the current output by the driver circuit 19.

The bus master device 29 can be connected on a primary side, opposite to the loop bus side, with a communication bus, which in turn might be connected to a central control controlling a plurality of bus master devices. Additionally the bus master device is connected to a power supply and comprises a power converter to provide an internal operation voltage, e.g. 42 V, which is supplied to the input side of the driver circuit 19.

The bus master device 29 can comprise further elements dedicated to different control operations and to the internal operation of the bus master device 29. Which will not be explained in further detail in this application.

Figure 3 shows in more detail the driver circuit 19 of Figure 2.

The output side of the driver circuit 19 is connected between ground 7 and an output voltage line 9 of the bus master device 29, which form input voltage supplies of the driver circuit.

The output side of the driver circuit 19 is connected between ground 3 and an internal voltage line 5 of the bus master device 29, which form input voltage supplies of the driver circuit.

At the input side of the driver circuit 19 a first capacitance element C1, preferably a capacitor, is connected between ground 3 and the internal voltage line 5. The capacitor C1 is not specially limited to a particular capacitor type.

Parallel to the capacitor C1 there is connected a series connection of two switching elements S1, S2. Here any type of switch, like transistors, can be used. The transistors are not limited to a particular transistor type. For example the use of FETs or of bi-polar n-channel or p-channel transistor is possible.

In the preferred embodiment of Figure 3 there is provided a respective diode D1, D2 connected parallel to a respective switch S1, S2. The diodes are provided with the identical orientation and so as to block a current flowing from the internal voltage line 5 to ground 3, while lowing the flow of a current in the opposite direction.

At an intermediate point between the two switches S1 and S2 of the first series connection of switching elements there is connected one end of an inductance L1. The other end of the inductance L1 is connected with the output side of the driver circuit 19.

At the output side of the driver circuit 19 a second capacitance element C2, preferably a capacitor, is connected between ground 7 and the output voltage line 9. The capacitor C2 is not specially limited to a particular capacitor type.

Parallel to the capacitor C2 there is connected a second series connection of two switching elements S3, S4. Here any type of switch, like transistors, can be used. The transistors are not limited to a particular transistor type. For example the use of FETs or of bi-polar n-channel or p-channel transistor is possible.

In the preferred embodiment of Figure 3 there is provided a respective diode D3, D4 connected parallel to a respective switch S3, S4. The diodes are provided with the identical orientation and so as to block a current flowing from the output voltage line 9 to ground 7, while lowing the flow of a current in the opposite direction.

The switching elements S1 to S4 are operated under the control of the control unit 25 of the master bus device 29.
In the preferred operation mode the switching elements S1 and S4 are operated at the same timing. If the switching elements S1 and S4 are in the open state, while the switching elements S2 and S3 are closed, the internal voltage of the master bus device 29 will charge the capacitor C1. The output voltage line 9 will be supplied with the energy stored in the inductance L1 and the capacitor C2.

Upon closing the switching elements S1 and S4 and opening the switching elements S2 and S3, the energy accumulated in the capacitor will be transferred to the inductance L1.

When opening again the switching elements S1 and S4 and closing S2 and S3 the energy accumulated in the inductance L1 will be transferred to the output side and will recharge the capacitor C2.

Under the provision that the internal supply voltage of the master bus device is constant, e.g. 42 V, the voltage at the output line 9 will be determined only by the timing of the switching.

\[
\frac{U_{\text{out}}}{U_{\text{in}}} = \frac{t_{\text{on}} (S1, S4)}{t_{\text{off}} (S1, S4)} = \frac{t_{\text{on}} (S1, S4)}{(T - t_{\text{on}} (S1, S4))} = 1/(T/t_{\text{on}} (S1, S4)) - 1
\]

Insofar the driver circuit operates as a buck-boost converter. As well-known the two operating states of a buck-boost converter are: a) when the switching elements S1, S4 are turned on, the input voltage source supplies current to the inductance L1, and the capacitor C2 supplies current to the loop bus (output load). When the switching elements S1, S4 are opened, the inductance supplies current to the bus loop.

From the above it is clear that a skilled person will be able to implement different output voltages, to be supplied to the two wire loop bus.

Due to this construction it is possible to implement a plurality of different voltage levels at the bus for an amplitude modulation of a digital signal.

Furthermore, while maintaining the duty cycle unchanged but varying the switching frequency it is possible to form the slew rate of the output voltage as desired.

Therefore, the bus master device can be used for a plurality of different loop buses having different bus protocols regarding the voltage levels, slew rates and so on, without a modification of the hardware, simply by controlling the switching of the switching elements S1 to S4.

Instead of using the former described type of amplifier, i.e. A, B or AB power amplifier with additional drive level/discharge circuitry, a switched mode driver circuitry is used. The basic principle is well known and used for example in switching voltage regulators. But it has never been used as driver for two wire loop systems. The invention uses a cascaded buck-boost topology with four switches/transistors, four diodes (in case of FETs the bulk diodes can be used) and one inductor.

As discussed above from the four switches two switches are operated simultaneously resulting in an open loop control mode. No closed loop control is necessary.

The communication levels can be easily set.

The output voltage is only dependent on the input voltage, which can be assumed as nearly constant in this application, and the turn on/off time of the switching element pair S1, S4.

For the simplest operation it is not necessary to measure the output voltage. In addition the four switches can be controlled individually to allow some special operating modes and to enhance efficiency.

The solution offers software defined protocol/communication levels and the reduction of the transmission frequency/slew rate if necessary.

The universal usage as driver or converter for any two wire loop system is enabled. Special and additional drive level/discharge circuitries are obsolete.

A further advantage is a highly reduced power dissipation (efficiency > 90 %), a good energy recovery and an integrated current measurement with the current detector 15.

Claims

1. Driver circuit for a two wired loop bus comprising:
a first capacitance element (C1) connected between two input voltage supplies (3, 5);
a second capacitance element (C2) connected between two output voltage supplies (7, 9);
a first series connection of two switching elements (S1, S2) connected between the two input voltage supplies (3, 5);
a second series connection of two switching elements (S3, S4) connected between the two output voltage supplies (3, 5); and
an inductance (L1), one end of which being connected between the two switching elements (S1, S2) of the first series connection, and the other end thereof being connected between the two switching elements (S3, S4) of the second series connection.

2. Driver circuit according to claim 1, further comprising:

   four diodes (D1 to D4) each being connected so as to bridge one of the switching elements (S1 to S4).

3. A bus master device for a two wired loop bus, said bus master device comprising:

   a driver circuit (19) according to claim 1 or 2;
   a current measuring element (15) for measuring the current through the drive circuit;
   a controller (13) for controlling the switching of the switching elements (S1 to S4).

4. The bus master device according to claim 3, wherein

   the controller (13) is configured so as to control the switching of the switching elements (S1 to S4) with different pre-set timings, so as to provide different voltage levels on the two wired loop bus.

5. The bus master device according to claim 4, wherein

   the controller (13) is configured so as to switch the first switch (S1) of the first series connection and the second switch (S4) of the second series connection synchronously.

6. A fire detection system comprising:

   a bus master device (29) according to any of claims 3 to 5; and
   a two wired loop bus (11, 13) comprising a plurality of fire detecting devices (T01 - T10) connected between the two wires of the bus.

7. A burglar alarm system comprising:

   a bus master device according to any of claims 3 to 5; and
   a two wired loop bus (11, 13) comprising a plurality of burglar detecting devices (15) and/or alarming devices connected between the two wires of the bus.
Fig. 1
## DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<th>Citation of document with indication, where appropriate, of relevant passages</th>
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The present search report has been drawn up for all claims.

**Place of search** | **Date of completion of the search** | **Examiner**
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Munich | 18 June 2015 | Dascalu, Aurel

**CATEGORY OF CITED DOCUMENTS**
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Annex to the European Search Report

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For more details about this annex: see Official Journal of the European Patent Office, No. 12/82.
REFERENCES CITED IN THE DESCRIPTION

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