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DRIVE CIRCUIT FOR DISPLAY DEVICE

ABSTRACT OF THE DISCLOSURE

In a display device in which each group of plural drive elements 10 takes charge of the drive of plural picture elements (pixels) and the display luminance changes as the number of sustaining pulses changes that are supplied to PDP16, a constant emission luminance characteristic is maintained by increasing the number of sustaining pulses for larger load when the display load factor is large, and decreasing the number of sustaining pulses for smaller load when the display load factor is small. When displaying multi-tone image by subfield drive method, a display area detect circuit 20 allows to display image always with constant luminance characteristic despite the variation of the display load factor, and to prevent the deterioration of tone characteristic due to the subfield drive method, and further a half tone display circuit 30 allows to decrease the bit number thereby simplifying the configuration of the display area detect circuit 20.

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ORIGINAL

COMPLETE SPECIFICATION
STANDARD PATENT

Invention Title:

Driving circuit for display device

The following statement is a full description of this invention including the best method of performing it known to us:-

Field of the Invention

This invention relates to a drive circuit for a display device having a plurality of drive elements, each of which drives a plurality of pixels (picture elements), wherein luminance of the display is designed so as to change according to the number of the sustaining pulses, sustaining voltage and current provided from each drive element in order to display panel change based on the input image signal.

The present invention also relates to a drive circuit of a display device which displays a multi-tone image by timesharing one screen display duration (one frame, for instance) of a display panel into a plurality of display durations (subfields, for instance) which correspond to the display tone, and by weighting the number of sustaining pulses of respective divided (time-shared) display durations.

Description of the Prior Art

The driving method of a PDP (Plasma Display Panel) is a direct drive by digitalized image input signal. The luminance and tone of the light emitted from the panel face depends on the bit number of the signal dealt with.

An AC type of PDP features satisfactory characteristics with regard to luminance and durability. As for the tonal display, however, an ADS subfield method (Address/Display Separate type drive method) has been proposed only recently that enables 256 tones.

Figures 1 (a) and 1 (b) show the drive sequence and drive waveform of the PDP which is used in this ADS subfield method.

In Figure 1 (a), which gives an example of 8-bits and 256 tones, one frame consists of eight subfields whose relative ratios of luminance are 1, 2, 4, 8, 16, 32, 64 and 128 respectively. Combinations of these luminances in eight screens enables a display in 256 tones. The respective subfields are composed of an address duration, which writes one screen of refreshed data, and a sustaining duration, which determines the luminance level of the subfield. The detail of this configuration is explained in Figure 1 (b). In the

address duration, a wall charge is formed initially at each pixel simultaneously over all the screens and then the sustaining pulses are given to all the screens for display. The brightness of the subfield is proportional to the number of the sustaining pulses to be set to predetermined luminance. A two hundred and fifty-six tone display is thus realized.

The AC type PDP display device has a plurality of drive elements (101, 102, ... 10n) as shown in Figure 2. The respective drive elements 101, 102, ... 10n drive the pixels of PDP 16 by the drive control signal from a display drive control circuit 14 based on the image signal as input into the image signal input terminal 12. This type of method has however been problematical in that when the drive voltage (sustaining voltage and address voltage, for instance) is applied to all the pixels whose drive is controlled by one drive element, that is when the pixels are discharged, the load on the drive element and the emission luminance are different compared to when the drive voltage is supplied only to a portion of the pixels.

Conventionally attempts had been made to solve such a problem by enhancing the capacity of the individual drive elements or by mitigating the load to individual drive elements through an increase of the number of the drive elements. However, this conventional approach has been disadvantageous in that although a differential emission luminance characteristic can be moderated, it cannot be eliminated, and a large capacity of drive elements needed to be prepared. Further the number of drive elements required was too large.

The conventional method has also been problematical in that when a display device such as the one shown in Figure 2 displays a multi-tone image by the ADS subfield method, the tonal characteristic worsens. Let us consider, for example, an image where most of the displayed image is composed of the image level "127" (01111111 by 8-bits binary notation) and the small remaining area is composed of an image level "128" (10000000 by 8-bits binary notation). When the display load factor of the MSB (Most Significant Bit) subfield is compared with that of a subfield other than the MSB, the former is smaller than the latter. This is unsustainable because the difference in load factor raises the emission luminance characteristic and worsens the tonal characteristic.

To solve such problematical points as above, the applicant has previously proposed a circuit as shown in Figure 3. That is, a display area detect circuit 20 is inserted between an image signal input terminal 12 and a display drive control circuit 14. The display area detect circuit 20 detects the display area for each particular duration (for example, one frame or one subfield) based on the image signal as input into the image signal input terminal 12 to control the number of the sustaining pulses (drive pulses) in response to the detected area.

More specifically, the display area detect circuit 20 comprises a display load factor detect circuit (a counter, for instance) that detects the display load factor for a certain duration and the sustaining pulse control circuit [LUT (Look Up Table), for instance] that controls the number of sustaining pulses, sustaining voltage or sustaining current based on the output detected by the display load factor detect circuit. The emission luminance characteristic can thus be maintained constant irrespective of the display load factor of the display panel. This configuration further prevents the deterioration of the tonal characteristic due to the subfield drive method.

However, the circuit as shown in Figure 3 has been somewhat problematical in that the configuration of the display area detect circuit 20 becomes complicated when one frame of the PDP 16 is time-shared into eight display durations (subfields) corresponding to 8-bit display tones and the number of the sustaining pulses of the respective divided display durations are weighted to display 256 tones of image. This is because eight display load factor detect circuits and eight sustaining pulse control circuits are needed for as many subfields. In Figure 3, the numeral 10 indicates the group of drive elements representing all the drive elements 101, 102, ... 10n as shown in Figure 2.

Brief Summary of the Invention

In a first aspect, the present invention consists in a drive circuit for a display device having a display panel and a plurality of drive elements in which each drive element drives a plurality of pixels and the display luminance changes with a change in a number of sustaining pulses supplied from said respective drive elements to the display panel

based on an input image signal, a screen display duration of the display panel changing according to the number of sustaining pulses, the drive circuit being characterized in that it is provided with a display load factor detect means which detects a display load factor for a predetermined display duration based on said input image signal and a sustaining pulse control means which controls the number of sustaining pulses so that the luminance of said display panel can be maintained constant on the basis of the detected output of the display load factor detect means, and

wherein the display device timeshares one screen display duration of the display panel into a plurality of display subfields which correspond to the display tones and displays a multitone image by weighting the number of sustaining pulses for each display subfield, the display load factor detect means being a counter which counts up the number of drive pixels for each screen display duration or display subfield, and the sustaining pulse control means is a sustaining pulse control circuit that controls the number of sustaining pulses based on the counted value of said counter.

In a second aspect, the present invention consists in a drive circuit for a display device having a display panel and a plurality of drive elements where each drive element drives a plurality of pixels and display luminance changes with a change in a sustaining voltage or sustaining current supplied from said respective drive elements to the display panel on the basis of an input image signal, a screen display duration of the display panel changing according to the sustaining voltage/current, the drive circuit being characterized in that it includes a display load factor detect means which detects a display load factor for a predetermined display duration based on said input image signal and the sustaining voltage/current control means that controls either the sustaining voltage or sustaining current so that the luminance characteristic of said display panel can be maintained constant on the basis of the detected output of the display load factor detect means.

In a third aspect, the present invention consists in a drive circuit for a display device having a display panel and a plurality of drive elements in which each drive element drives a plurality of pixels, the display device timesharing one screen display duration of the display panel into a plurality of display subfields which correspond to display tones, and weighting a

number of sustaining pulses for each display subfield to display a multitone image, the drive circuit being characterized in that it is provided with a halftone display means which converts an n-bit input image signal (n being an integer not less than 2) into an m-bit image signal ($m \leq n-1$) and obtains an intermediate level from a neighbouring drive level the drive circuit further including a display area detect means which detects the display area for a predetermined display duration based on the m-bit image signal of said halftone display means and maintains constant a luminance characteristic of said display panel on the basis of the detected output.

A first advantage of at least some embodiments of the present invention is that the drive circuit for the display device may allow an image to be displayed with a constant emission luminance characteristic despite the size of a display load factor. In this context the display load factor means the drive pixel number (number of lit-up pixels) as a proportion of the total number of pixels for a particular duration (for example, one frame, one subfield or one line).

A second advantage of at least some embodiments of the present invention is that degradation of the tonal characteristic may be prevented due to the subfield drive method when it is used in a display device which displays a multi-tone image.

A third advantage of at least some embodiments of the present invention is that the drive circuit for a display device may simplify the configuration of the display area detect circuit.

In one embodiment of a display device, respective multiple drive elements respectively take charge of driving respective multiple pixels and display luminance changes with changes in the number of sustaining pulses provided from each drive element to the display panel based on the input image signal, the device further including a display load factor detect means which detects the display load factor for certain durations based on the input image signal, a sustaining pulse control means which controls the sustaining pulse number based on the detected output of said display load factor detect means, wherein the load factor detect means detects the display load factor (number of drive pixels, for instance) for each duration (for example, one frame or one subfield), and said sustaining pulse control means controls the

number of sustaining pulses based on said detected output, thereby maintaining a constant luminance characteristic of the display panel. This control increases the number of sustaining pulses when the display load factor is large since the load against the drive element is large, while it decreases the same number when the same factor is small since the same load is small.

In a second embodiment, the display device displays a multi-tone image by a subfield drive method; the display load factor detect means being a counter which counts up the number of drive pixels for each display duration out of one screen display duration (for example, one frame) and one division display duration (for example, one subfield); and the sustaining pulse control means being a sustaining pulse control circuit which controls the number of sustaining pulses based on the counted value of the counter. The counter accumulates the number of the drive pixels for every display duration based on the counted value, and the sustaining pulse control circuit controls the number of sustaining pulses to be provided to the display panel.

A configuration such as the one above allows an image to be displayed with a constant luminance characteristic despite variations in the display load factor. That is, the luminance characteristic of the display panel can be maintained constant by the sustaining pulse control means, which controls the number of sustaining pulses based on the detected output of the display load factor detect means, and also by the sustaining voltages and current control means, which controls the sustaining voltage or current based on the detecting output of the display load factor detect means.

If this display device as adopted can display the multi-tone image by the subfield drive method, then the deterioration of tonal characteristic due to the subfield drive method can be prevented; that is, the luminance characteristic of the display panel is maintained constant by controlling the sustaining pulse number with the sustaining pulse control means, based on the detected output of the display load factor detect means.

Let us consider, for example, an image where most of the displayed image is composed of the image level "127" (01111111 by 8-bit binary notation) and the small remaining area is composed of an image level "128" (10000000 by 8-bit binary notation). Under these conditions the control is made so that the number of sustaining pulses is reduced for the subfield of

the MSB that has a small display load factor, and it is increased for any subfield other than the MSB that has a large display load factor. Otherwise, the control reduces the number of sustaining pulses for the MSB subfield without changing it for any subfield other than the MSB. Degradation of the luminance characteristic due to the subfield drive method can thus be prevented.

In a third embodiment, the display device has a plurality of drive elements, with each drive element taking charge of driving multiple pixels, each screen display duration corresponding to a tone of the display panel and being time-shared into display durations. A multi-tone image is displayed by weighting the number of sustaining pulses for the respective divided display duration, n-bits of input image signal (n being any integer not less than 2) being converted into m bits of image signal ($m \leq n-1$), and at the same time there is provided an intermediate display means which looks for an intermediate level from a neighbouring drive level, and a display area detect means which controls the sustaining pulses so that the display area is detected for every constant duration based on the m-bits image signal of the half tone display means and that the luminance characteristic of said display panel is maintained constant on the basis of this detected output.

Said display area detect means maintains a constant display panel luminance characteristic by detecting the display load factor (for example, the number of drive pixels) for each duration (one frame or one subfield, for instance) and controlling the sustaining pulses correspondingly, and prevents, at the same time, deterioration of tone characteristics due to the subfield drive method. Because the halftone display means converts the n-bit input image signal into an m-bit signal ($m \leq n-1$), and looks for the intermediate level from the neighbouring drive level to output it at the display area detect means, the conventional number n can be reduced to m of the display load factor detect circuits (counter, for instance) which constitute the display area detect means and of the sustaining pulse control circuit [LUT (Look Up Table), for instance].

By means of the configuration above, a display area detect means may be provided which detects the display area for each duration (one frame, for instance) and controls the sustaining pulses so that the display panel luminance characteristic can be maintained constant based on the detected

output, the image display can be given a constant luminance characteristic despite the changing display load factor (number of drive pixels), and deterioration of the tone characteristic due to the subfield drive method (ADS subfield, for instance) can be prevented.

The halftone display means, which converts the n-bit input image signal into an m-bit signal ($m \leq n-1$) and obtains the intermediate level from the neighbouring drive level, can convert the display area detect means from n-bits into m-bits, and consequently, the configuration of the display area detect means can be simplified. When, for example, the display area detect means are made to comprise the display load factor detect circuit (for example, counter) which detects the display load factor for each duration and the sustaining pulse control circuit (for example, LUT), the number of the display load factor detect circuits and of the sustaining pulse control circuits can be reduced from n to m (for example, for so many subfields).

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 (a) represents a drive sequence of the ADS subfield method.

Figure 1 (b) depicts a drive waveform of the ADS subfield method.

Figure 2 is a block diagram showing a conventional drive circuit of a display device.

Figure 3 is a block diagram of the drive circuit of a prior art display device previously proposed by the applicant.

Figure 4 is a block diagram showing a first embodiment of the drive circuit of the display device according to this invention.

Figure 5 is another block diagram showing a second embodiment of the drive circuit of the display device according to this invention.

Figure 6 is a block diagram showing an example of the sustaining voltage/current switching circuit as shown in Figure 5.

Figure 7 is another block diagram showing a third embodiment of the drive circuit of the display device according to this invention.

Figure 8 (a) is another block diagram showing a fourth embodiment of the drive circuit of the display device according to this invention.

Figure 8 (b) is a block diagram the error variance circuit, an example of the halftone display circuit as shown in Figure 8 (a).

Detailed Description

A first embodiment of this invention is illustrated in Figure 4. In Figure 4, parts which correspond to parts in Figure 2 are designated with the same reference symbol.

The numeral 12 represents an image signal input terminal. Sequentially connected to the terminal 12 are a display drive control circuit 14, a drive element group 10 (101, 102, ... 10n) and PDP 16, in this order. As is the case with the conventional drive circuit, the display drive control circuit 14 drives and controls the drive element group 10 based on the image signal (image data) input in the image signal input terminal 12, and displays a multi-tone image by the ADS subfield. That is, it time-divides one frame of the PDP 16 into a plurality of subfields (8, for instance) and weights the sustaining pulse number of each subfield to display the multi-tone image (for example, an 8-bit 256 tone image).

Coupled to said image signal input terminal 12 is a counter 22 as an example of the display load factor detect means. The counter 22 counts the number of drive pixels (display area) for every frame or subfield and outputs the counted value.

Connected on the output side of said counter 22 is the LUT (Look Up Table) 24 as an example of the major element constituting the sustaining pulse control means, which is made up of ROM (Read Only Memory) for example. The LUT 24 stores beforehand in memory the number of sustaining pulses for the drive pixels for each from or subfield in order to maintain a constant luminance characteristic of said PDP 16 irrespective of the size of the display load factor, the content of which can be output with the counted value of said counter 22 as an address (heading). The data to be stored beforehand in said LUT 24 is obtained from characteristic data measured from the relationship between the image signal and the emission luminance of the PDP 16 that displayed the multi-tone image by the ADS subfield, with each of the drive element group 10 taking charge, for instance, of the driving of a plurality of pixels of the PDP 16.

Said display drive control circuit 14 drives and controls the drive element group 10 using the number of sustaining pulses as output from said LUT 24, and maintains constant the luminance characteristic of the PDP 16 despite the size of the display load factor.

Now the action of the drive circuit in Figure 4 will be explained.

(a) Based on the image signal as input into the image signal input terminal 12, the counter 22 counts up the number of drive pixels (display area) for every one frame or one subfield and outputs the counted value to the LUT 24.

Let us consider, for example, an image where most of the displayed image is composed of the image level "127" (01111111) and a small, remaining area is composed of an image level "128" (10000000). The MSB subfield has a small counted value because its drive pixel number and, consequently, the display load factor is small, while the subfield other than the MSB subfield has a large counted value because its drive pixel number and, consequently, the display load factor is great.

(b) The display drive control circuit 14 receives, from the LUT 24, the number of sustaining pulses to maintain constant the luminance characteristic with the counted value of the counter 22 as an address, controls the drive element group 10 using this sustaining pulse number, and maintains constant the luminance characteristic of the PDP 16.

Let us consider, for example, an image where most of the displayed image is composed of an image level "127" (01111111 by 8-bits binary notation) and a small, remaining area is composed of an image level "128" (10000000 by 8-bits binary notation). Since the counted value of the MSB subfield is smaller than that of the subfield other than the MSB, the number of the sustaining pulses of the MSB subfield is reduced and the number of the sustaining pulses other than of the MSB subfield is increased. Another control is that the sustaining pulse number of the MSB subfield is reduced without changing that of the subfield other than MSB. Thus, the luminance characteristic of the PDP 16 can be maintained constant irrespective of the display load factor.

Figures 5 and 6 explain the second embodiment of this invention, where the numeral 22 represents the counter as an example of the display load factor detect means. The counter 22 is so designed as to count the drive pixel number (display area) for every one frame or subfield based on an image signal as an input into said image signal input terminal 12 to output the counted value.

Coupled on the output side of said counter 22 is a sustaining voltage/current set circuit 26 as an example of the sustaining voltage/current control means, which sets and outputs either the sustaining voltage or sustaining current to the drive pixels for every one frame or one subfield to maintain constant the luminance characteristic of the PDP 16 irrespective of the size of the display load factor based on the counted value of said counter 22.

For these set data, the respective drive element groups 10 take charge of the driving of the plurality of pixels of the PDP 16, and the characteristic representing the relationship between the image signal and emission luminance is measured for the PDP 16 that displayed the multi-tone image by the ADS subfield method. The set data is obtained from the data measured.

Said sustaining voltage/current set circuit 26 has been so designed that its output results from setting different voltage levels of voltage 1, voltage 2,... voltage n, for instance, based on the counted value of said counter 22.

Connected to the output side of said sustaining voltage/current set circuit 26 is a display drive control circuit 14, on another input side of which is connected the image signal input terminal 12. The display drive control circuit 14 switches, drives and controls the sustaining voltage/current switch circuit group 30 (301, 302, ... 30n) based on the image signal as input into said signal input terminal 12 and the sustaining voltage or current as set by the sustaining voltage/current set circuit 26, and drives and control the drive element group 10. At the same time it performs the multi-tone image display by the ADS subfield method with the PDP 16 (not shown) as coupled with the output side of the drive element group 10, and maintains constant the luminance characteristic of the PDP 16 without regard to the size of the display load factor.

The foregoing sustaining voltage/current switch circuit 30 consists, for example, of an analog switch as shown in Figure 6. It is constructed so that the switching action based on the sustaining voltage set signal and the drive control signal from said display drive control circuit 14 sets, at the sustaining voltage/current set circuit 26, and switches the different voltage levels of voltage 1, voltage 2, ... voltage n as input through the intermediary of said display drive control circuit 14.

Referring now to Figure 5 the function of the second embodiment of this invention will now be described.

(a) The counter 22 counts the drive pixel number for every one frame or one subfield based on the image signal as input into the image signal input terminal 12, and outputs the counted value to the sustaining voltage/current set circuit 26. Let us consider, for example, an image where most of the displayed image is composed of an image level "127" (01111111 by 8-bits binary notation) and a small, remaining area is composed of an image level "128" (10000000 by 8-bits binary notation). The MSB subfield has a small counted value because its drive pixel number and, consequently, the display load factor is small, while the subfield other than the MSB has a large counted value because its drive pixel number and, consequently, the display load factor is great.

(b) The sustaining voltage/current set circuit 26 sets and outputs the sustaining voltage or sustaining current based on the counted value of the counter 22. The display drive control circuit 14 switches, drives and controls the sustaining voltage/current switch circuit group 30 based on the image signal as input into the image signal input terminal 12 and the set data as set by the sustaining voltage/current set circuit 26, and drives and control the drive element group 10. At the same time it conducts the multi-tone image display at the PDP 16 by the ADB subfield method, and maintains constant the luminance characteristic of the PDP 16.

Let us consider, for example, an image where most of the displayed image is composed of an image level "127" (01111111) and a small, remaining area is composed of an image level "128" (10000000). Since the counted value of the MSB subfield is smaller than that of the subfield other than the MSB, the number of sustaining pulses of the MSB subfield is reduced and the

number of sustaining pulses other than of the MSB subfield is increased. Another control is that the sustaining voltage or sustaining current of the MSB subfield is reduced without changing that of the subfield other than the MSB. Thus, the luminance characteristic of the PDP 16 can be maintained constant irrespective of the display load factor.

When, for instance, the luminance characteristic of PDP 16 is made constant by the control of sustaining voltage irrespective of the display load factor, the sustaining voltage of the MSB subfield is changed over from the voltage 3 as shown in Figure 6 into a smaller voltage 2.

Figure 7 explains the third embodiment of this invention.

The numeral 22 represents the counter group as an example of the display load factor detect means. The foregoing respective counters 221, 222, ... 22n count up the drive pixel number (display area) for every one line based on the image signal as input in said image signal input terminal 12 to output the counted value.

Connected to the respective output sides of said counter group 22 is the sustaining voltage/current set circuit group 26 (261, 262, ... 26n) as an example of the sustaining voltage/current control means, which sets and outputs the sustaining voltage or current for the drive pixels for every one line in order to maintain constant the luminance characteristic of the PDP 16 irrespective of the size of the display load factor.

These set data are obtained from the measurements of the characteristic representing the relationship between the image signal and emission luminance of the PDP 16 that displayed the multi-tone image by the ADS subfield method with the respective elements of the drive element group 10 driving the 1-line pixels of the PDP 16.

Coupled to the respective output sides of the aforesaid sustaining voltage/current set circuit 26 is the display drive control circuit group 14 (141, 142, ... 14n), to input sides of which is coupled the image signal input terminal 12.

Each of the display drive control circuit group 14 switches, drives and controls the sustaining voltage/current switch circuit group 30 (301, 302, ... 30n) on the basis of the image signal as input in said image signal input terminal 12 and the sustaining voltage or sustaining current as set by the

sustaining voltage/current set circuit group 26. At the same time it drives and controls the drive element group 10, and displays multi-tone image by the ADS subfield method at the PDP 16 as coupled with the output side of the drive element group 10 to maintain constant the luminance characteristic of the PDP 16 irrespective of the size of the display load factor.

The function of the third embodiment of this invention will now be explained referring to Figure 7.

(a) The counter group 22 counts up the number of drive elements for every one line based on the image signal as input in the image signal input terminal 12, and outputs the counted value to the sustaining voltage/current set circuit group 26.

Let us consider, for example, an image where most of the displayed image is composed of an image level "127" (01111111) and a small, remaining area is composed of an image level "128" (10000000). The MSB subfield has a small counted value because its drive pixel number and, consequently, the display load factor is small, while the subfield other than the MSB has a great counted value because its drive pixel number and, consequently, the display load factor is great.

(b) The sustaining voltage/current set circuit group 26 sets and outputs the sustaining voltage or sustaining current based on the counted value of the counter group 22. The display drive control circuit group 14 switches, drives and controls the sustaining voltage/current switch circuit group 30 based on the image signal as input into the image signal input terminal 12 and the set data as set by the sustaining voltage/current set circuit group 26, and drives and controls the drive element group 10. At the same time it conducts the multi-tone image display at the PDP 16 by the ADB subfield method, and maintains constant the luminance characteristic of the PDP 16.

Let us consider, for example, an image where most of the displayed image is composed of an image level "127" (01111111) and a small, remaining area is composed of an image level "128" (10000000). Since the counted value of the MSB subfield is smaller than that of the subfield other than the MSB, the number of the sustaining pulses of the MSB subfield is reduced and the number of the sustaining pulses other than of the MSB subfield is

increased. Another control is that the sustaining pulse number of MSB subfields is reduced without changing that of the subfield other than the MSB. Thus, the luminance characteristic of the PDP 16 can be maintained constant irrespective of the display load factor.

In the foregoing first, second and third embodiments, an explanation was made of the case where this invention is used for the display device that displays multi-tone image by the ADS subfield method, but the invention is not limited to this type of embodiment. The present invention can be used also for a display device where the respective drive elements drive a plurality of pixels whose display luminance changes with changes in the number of sustaining pulses, sustaining voltage or sustaining current.

Now the fourth embodiment of this invention will be explained referring to Figures 8 (a) and 8 (b).

Connected to the image signal input terminal 12 is the display area detect circuit group 20 (201, 202, ...20m) through the intermediary of a half tone display circuit 31, while the display drive control circuit 14, the drive element group 10 and the PDP 16 are sequentially connected in this order to the output side of the display area detect circuit group 20m.

Figure 8 (b) shows an error variance circuit as an example of aforesaid half tone display circuit 31. The error variance circuit consists of a vertical adder 32 that adds a vertically reproduced error to an n-bits input image signal as input into the image signal input terminal 12, a horizontal adder 34 that adds a horizontally reproduced error to an output signal of this vertical adder 32, an error detect circuit 36 that outputs an error weighting signal by detecting and weighting the difference between the output signal of the horizontal adder 34 and the correction data as preset at the ROM, among others, an h-line delay circuit 38 that delays by h-lines the error weighting signal as output from the error detect circuit 36 and outputs it to the vertical adder 32, a d-dot delay circuit 40 that delays by d-dots the error weighting signal as output from the error detect circuit 36 and outputs it as a reproduced error to the horizontal adder 34, and a bit convert circuit 44 that converts the n-bits image signal as output from the horizontal adder 34 into an m-bits ($m \leq n-1$) image signal and outputs it to the aforesaid display area detect circuit 20 through the intermediary of the output terminal 42.

Said display area detect circuit 20 comprises a display load factor detect circuit (a counter, for instance) that detects the display load factor for every element of certain duration (one frame, one subfield or one line) and a sustaining pulse control circuit (for example, the LUT [Look Up Table]) that controls the sustaining pulse (for example, pulse number, sustaining voltage or sustaining current) so that the luminance characteristic of the PDP can be maintained constant on the basis of the detect output of the display load factor detect circuit. More materially, the LUT as an example of the sustaining pulse control circuit initially stores in memory the data of the sustaining pulse (for example, pulse number, sustaining voltage or sustaining current) for the drive pixels for every one frame, one subfield or one line in order to maintain constant the luminance characteristic of the PDP 16 irrespective of the size of the display load factor with the counted value of the counter as an example of the display load factor detect circuit, as an address.

The foregoing display drive control circuit 14 drives and controls the drive element group 10 using the data of the sustaining pulses (for example, pulse number, sustaining voltage or sustaining current) as obtained from said display area detect circuit 20 and maintains constant the luminance characteristic of PDP 16 irrespective of the size of the display load factor.

Now the function of the embodiment shown in Figure 8 will be explained.

(a) The half tone display circuit 31 adds vertically and horizontally reproduced errors to the n-bits input image signal as input by the adders 32 and 34 into the image signal input terminal 12, while the error detect circuit 36 detects and weights the difference between the output signal of the horizontal adder 34 and the correction data. The delay circuits 38 and 40 delay by h-lines and d-dots the error weighting signal as output from the error detect circuit 36 to output it to the adders 32 and 34. The bit convert circuit 44 converts the n-bits signal into the m-bits ($m \leq n-1$) image signal and outputs it to the display area detect circuit 20 through the intermediary of the output terminal 22.

Thus the half tone display circuit 31 takes as an error the difference between the image level to be displayed and the drive level as displayed to

disperse it over the image in both horizontal and vertical directions. The half tone displayed by such error variance reduces the number of the subfields as driven by the downstream subfield driving method (for example, ADS subfield method) and compensates for the tones corresponding to this reduction by the half tone, that is, maintains the number of tones to be displayed.

(b) The display area detect circuit 20 detects the display load factor for every element of certain duration (for example, one frame) based on the m-bits image signal as output from the half tone display circuit 31, counts up the number of the drive pixels by means of the counter and controls the sustaining pulse so that the luminance characteristic of PDP 16 can be maintained constant with this counted value as, for example, an address on the basis of the detect output (for example, outputs the number of sustaining pulses, the content of the address from the LUT).

Let us consider, for example, an image where most of the displayed image is composed of an image level "127" (01111111) and a small, remaining area is composed of an image level "128" (10000000). Since the display load factor (counted value, for instance) of the MSB subfield is smaller than that of the subfield other than the MSB, the number of the sustaining pulses of the MSB subfield is reduced and the number of the sustaining pulses other than of the MSB subfield is increased. Another control is that the sustaining voltage or sustaining voltage or sustaining current of the MSB subfield is reduced without changing that of the subfield other than of the MSB. Thus, the luminance characteristic of the PDP 16 can be maintained constant irrespective of the display load factor.

(c) The display drive control circuit 14 controls the drive element group 10 using the sustaining pulses as output from the display area detect circuit 20, displays multi-tone image by the subfield drive method (ADS subfield method) at the PDP 16, and maintains constant the luminance characteristic of the PDP 16.

The foregoing fourth embodiment has been described adopting a base where an error variance circuit is used as an example of the half tone display means, but this invention is not limited to this embodiment. Any

embodiment will do if an n-bits input image signal can be converted into an m-bits ($m \leq n-1$) signal and the intermediate level thereof can be obtained from the neighbouring drive level. For instance, the configuration of the embodiment may use such a means as FRC (Frame Rate Control).

In the foregoing embodiments, the first to the fourth, we explained the case where the display panel of the display device is a PDP, but this invention is not limited to this. The invention may include such a case where the display is an LCDP display device.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A drive circuit for a display device having a display panel and a plurality of drive elements in which each drive element drives a plurality of pixels and the display luminance changes with a change in a number of sustaining pulses supplied from said respective drive elements to the display panel based on an input image signal, a screen display duration of the display panel changing according to the number of sustaining pulses, the drive circuit being characterized in that it is provided with a display load factor detect means which detects a display load factor for a predetermined display duration based on said input image signal and a sustaining pulse control means which controls the number of sustaining pulses so that the luminance of said display panel can be maintained constant on the basis of the detected output of the display load factor detect means, and

wherein the display device timeshares one screen display duration of the display panel into a plurality of display subfields which correspond to the display tones, and displays a multitone image by weighting the number of sustaining pulses for each display subfield, the display load factor detect means being a counter which counts up the number of drive pixels for each screen display duration or display subfield, and the sustaining pulse control means is a sustaining pulse control circuit that controls the number of sustaining pulses based on the counted value of said counter.

2. The drive circuit for a display device, as claimed in claim 1, wherein the sustaining pulse control circuit includes a look up table which stores beforehand in a memory the number of sustaining pulses required to maintain the luminance characteristic of the display panel constant, with the counted value of the counter as a heading.

3. A drive circuit for a display device having a display panel and a plurality of drive elements where each drive element drives a plurality of pixels and display luminance changes with a change in a sustaining voltage or sustaining current supplied from said respective drive elements to the display panel on the basis of an input image signal, a screen display duration of the display panel changing according to the sustaining voltage/current, the drive circuit being characterized in that it includes a display load factor detect means which detects a display load factor for a predetermined display

duration based on said input image signal and the sustaining voltage/current control means that controls either the sustaining voltage or sustaining current so that the luminance of said display panel can be maintained constant on the basis of the detected output of the display load factor detect means.

4. The drive circuit for a display device, as claimed in claim 3, wherein the display device timeshares one screen display duration of the display panel into a plurality of display subfields which correspond to display tones, and weights a number of sustaining pulses for respective display subfields to display a multitone image, the display load factor detect means being a counter which counts up the number of drive pixels for each screen with a display duration, the display device including a sustaining pulse control means constituted by the sustaining voltage/current control circuit, the sustaining voltage/current control circuit controlling either the sustaining voltage or sustaining current on the basis of the counted value of said counter.

5. The drive circuit for a display device, as claimed in claim 3, wherein the display device timeshares the one screen display duration of the display panel into display subfields which correspond to display tones, and weights a sustaining pulse number for each display subfield to display a multitone image, the display load factor detect means being a counter of each single line which counts up the number of drive pixels for the display duration, and the display device including a sustaining pulse control means constituted by the sustaining voltage/current control circuit, the sustaining voltage/current control circuit controlling either the sustaining voltage or sustaining current on the basis of the counted value of said counter.

6. A drive circuit for a display device having a display panel and a plurality of drive elements in which each drive element drives a plurality of pixels, the display device timesharing one screen display duration of the display panel into a plurality of display subfields which correspond to display tones, and weighting a number of sustaining pulses for each display subfield to display a multitone image, the drive circuit being characterized in that it is provided with a halftone display means which

converts an n-bit input image signal (n being an integer not less than 2) into an m-bit image signal ($m \leq n-1$) and obtains an intermediate level from a neighbouring drive level, the drive circuit further including a display area detect means which detects the display area for a predetermined display duration based on the m-bit image signal of said halftone display means and maintains constant a luminance characteristic of said display panel on the basis of the detected output.

7. The drive circuit for a display device, as claimed in claim 6, wherein the halftone display means is an error variance circuit which takes as an error the difference between an image level to be displayed and the drive level as displayed, and disperses this difference over the surrounding image.

8. The drive circuit for a display device, as claimed in claim 6 or 7, characterized in that the display area detect means is a display load factor detect circuit which detects the display load factor for a predetermined display duration, and that the drive circuit is provided with a sustaining pulse control circuit which controls the number of sustaining pulses so that the luminance characteristic of the display panel can be maintained constant.

9. The drive circuit for a display device, as claimed in claim 6 or 7, characterized in that the circuit is provided with a display load factor detect circuit which detects a display load factor for a predetermined display duration, and a sustaining voltage/current control circuit which controls a sustaining voltage or sustaining current so that the luminance characteristic of display panel can be maintained constant.

10. The drive circuit for a display device, as claimed in claim 9, wherein the display load factor detect circuit is a counter which counts up the number of drive pixels for each screen display duration, and a sustaining pulse control circuit controls either the sustaining voltage or sustaining current based on the counted value of said counter.

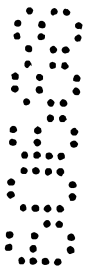
11. The drive circuit for display device claimed in claim 9, wherein the display load factor detect circuit is a counter which counts up the number of drive pixels for the display duration of each line, and a sustaining pulse control circuit which controls either the sustaining voltage or sustaining current based on the counted value of said counter.

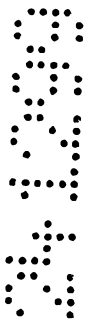
12. A drive circuit as claimed in any one of claims 1 to 11, substantially as hereinbefore described with reference to figures 4 to 8 of the accompanying drawings.

Dated this twenty-fourth day of December 1999

FUJITSU GENERAL LIMITED
Patent Attorneys for the Applicant:

F B RICE & CO





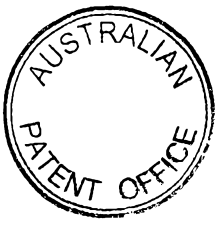


Fig. 1 (a) 256 Tone drive sequence

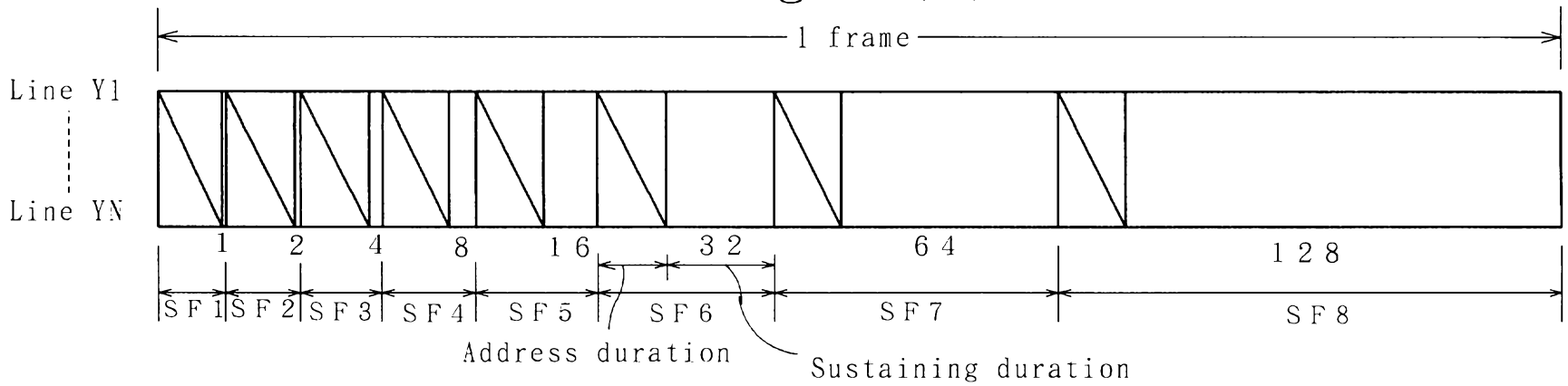
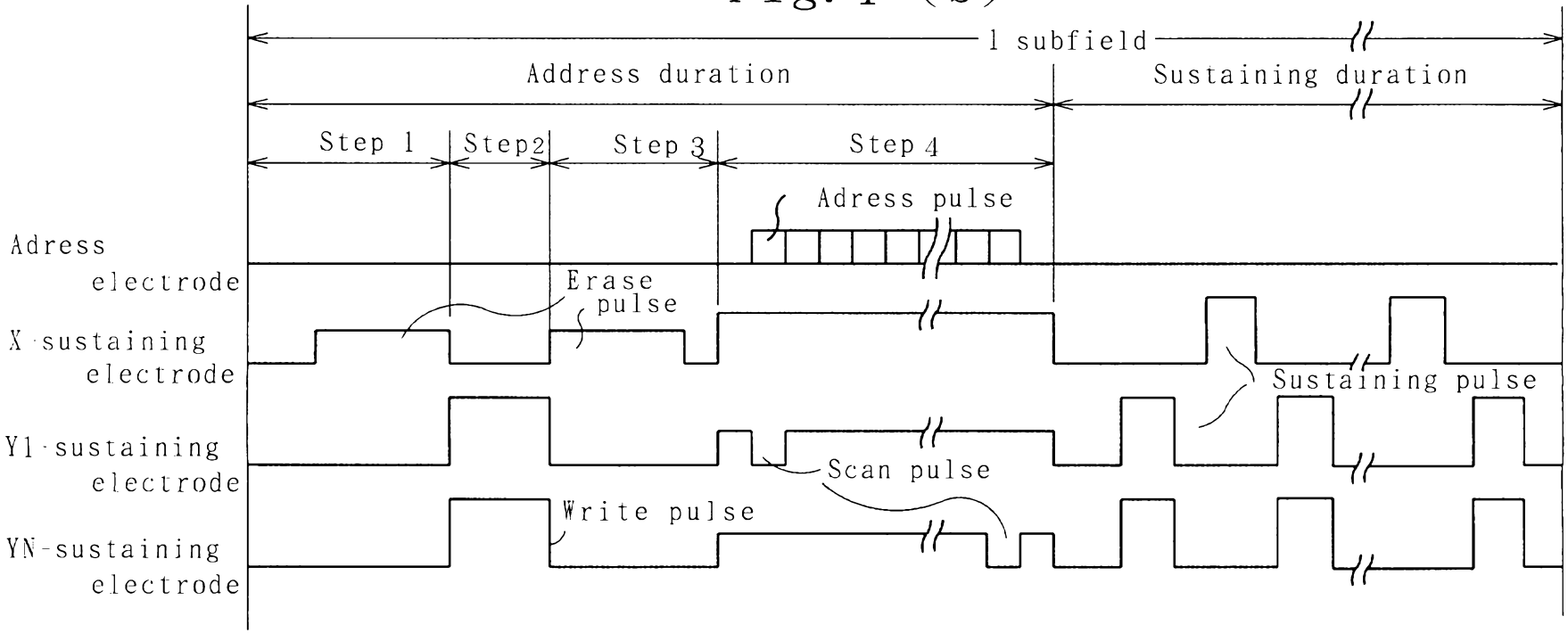


Fig. 1 (b) Drive waveform



8/

Fig. 2

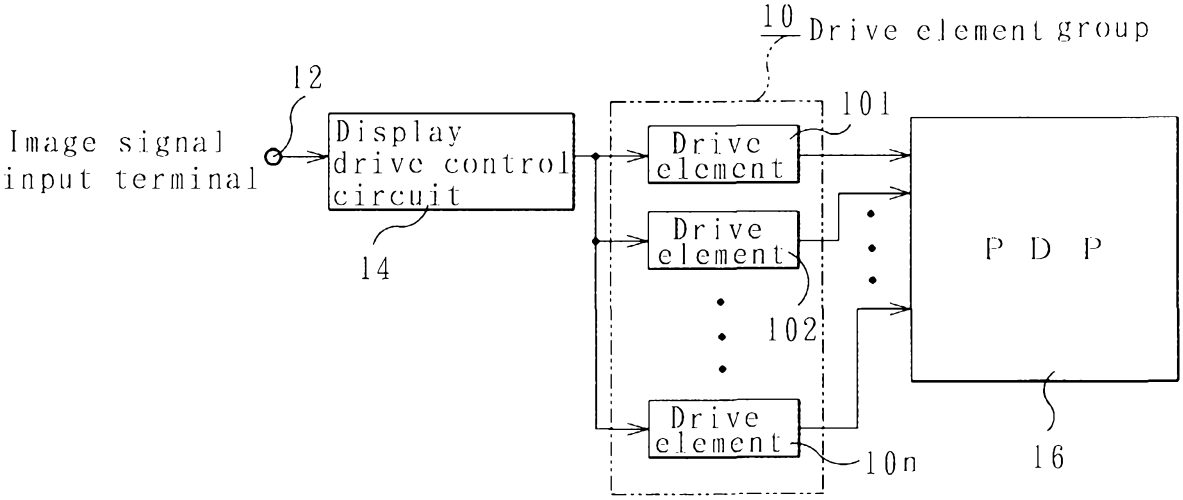

10
Drive element group
12
Image signal
input terminal
Display
drive control
circuit
14
101
Drive
element
Drive
element
102
Drive
element
10n
P D P
16

Fig. 3

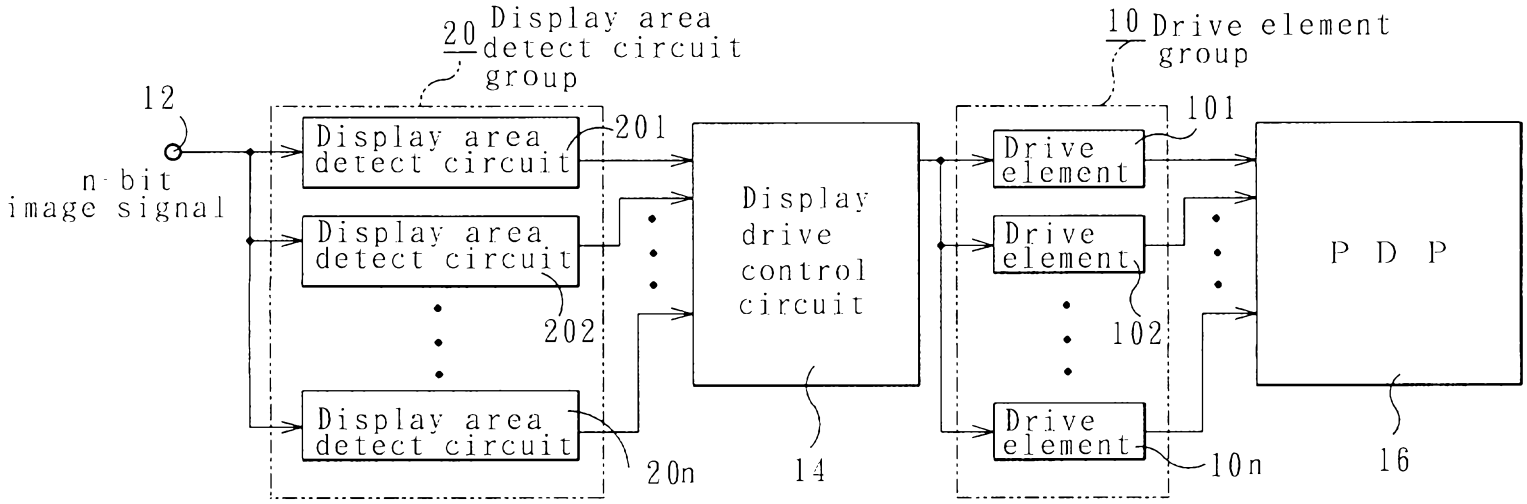

20 Display area detect circuit group
10 Drive element group
12
n-bit image signal
Display area detect circuit
Display area detect circuit
Display area detect circuit
201
202
20n
Display drive control circuit
14
Drive element
Drive element
Drive element
101
102
10n
P D P
16

Fig. 4

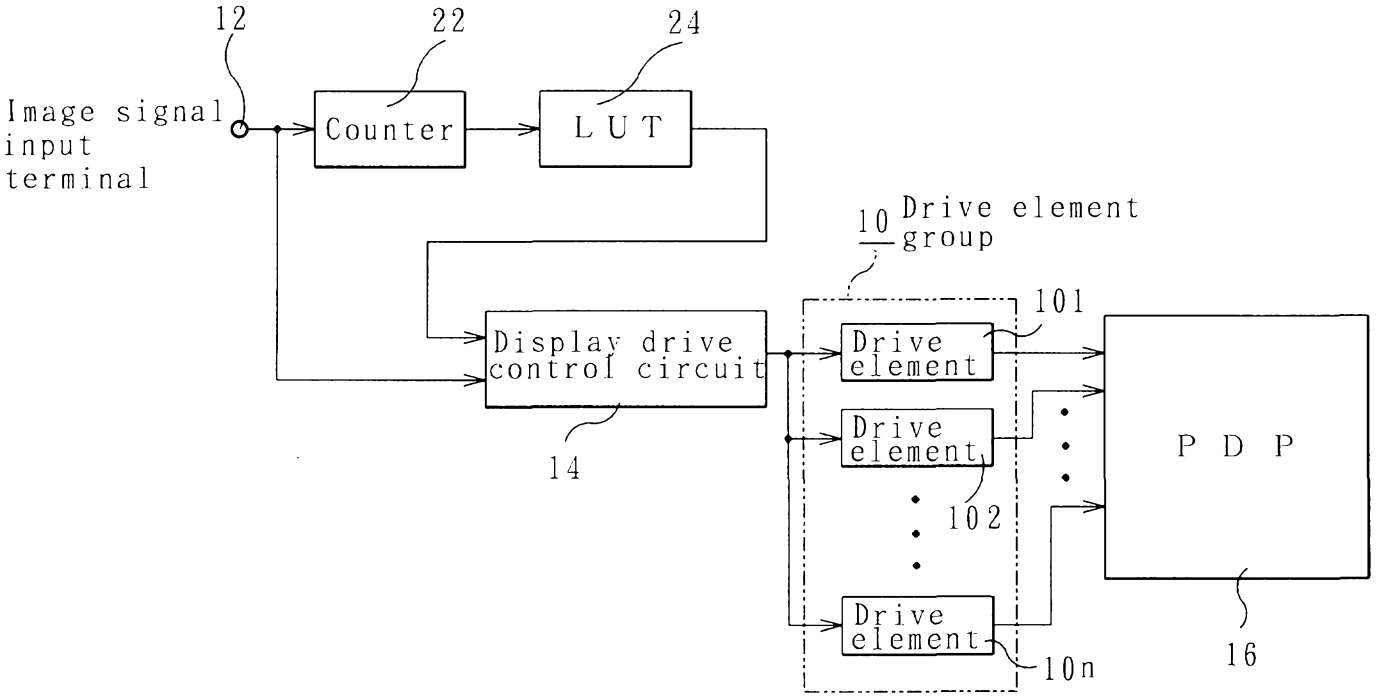

12
22
24
Image signal input terminal
Counter
L U T
10 Drive element group
101
Display drive control circuit
Drive element
Drive element
Drive element
102
10n
14
P D P
16

Fig. 5

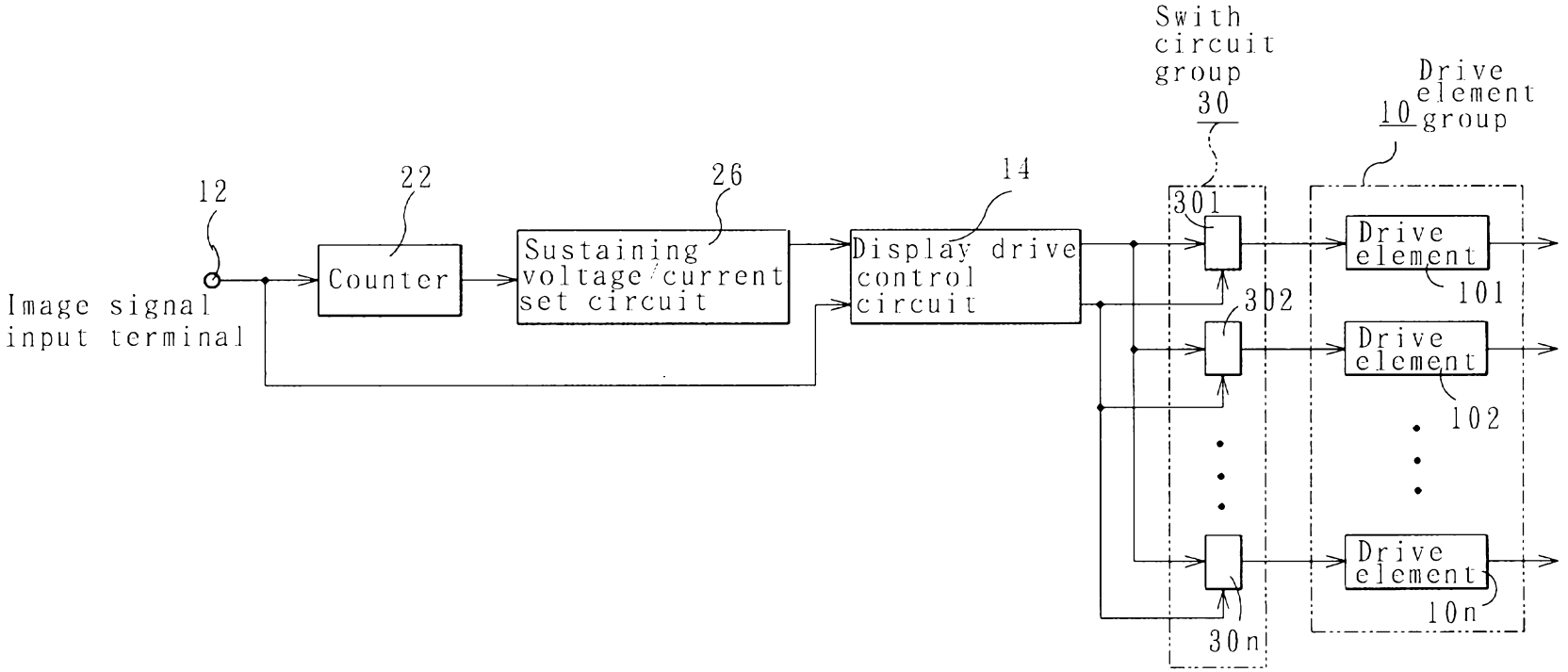

Swith
circuit
group
30
Drive
element
10 group
12
22
26
14
301
Image signal
input terminal
Counter
Sustaining
voltage/current
set circuit
Display drive
control
circuit
302
Drive
element
101
Drive
element
102
Drive
element
10n
30n

Fig. 6

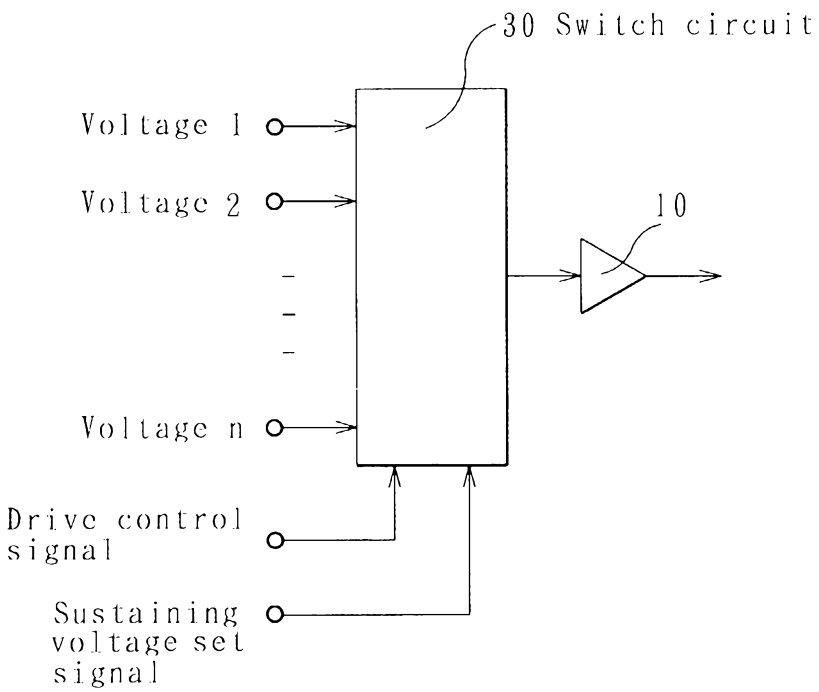

30 Switch circuit
Voltage 1
Voltage 2
Voltage n
10
Drive control signal
Sustaining voltage set signal

Fig. 7

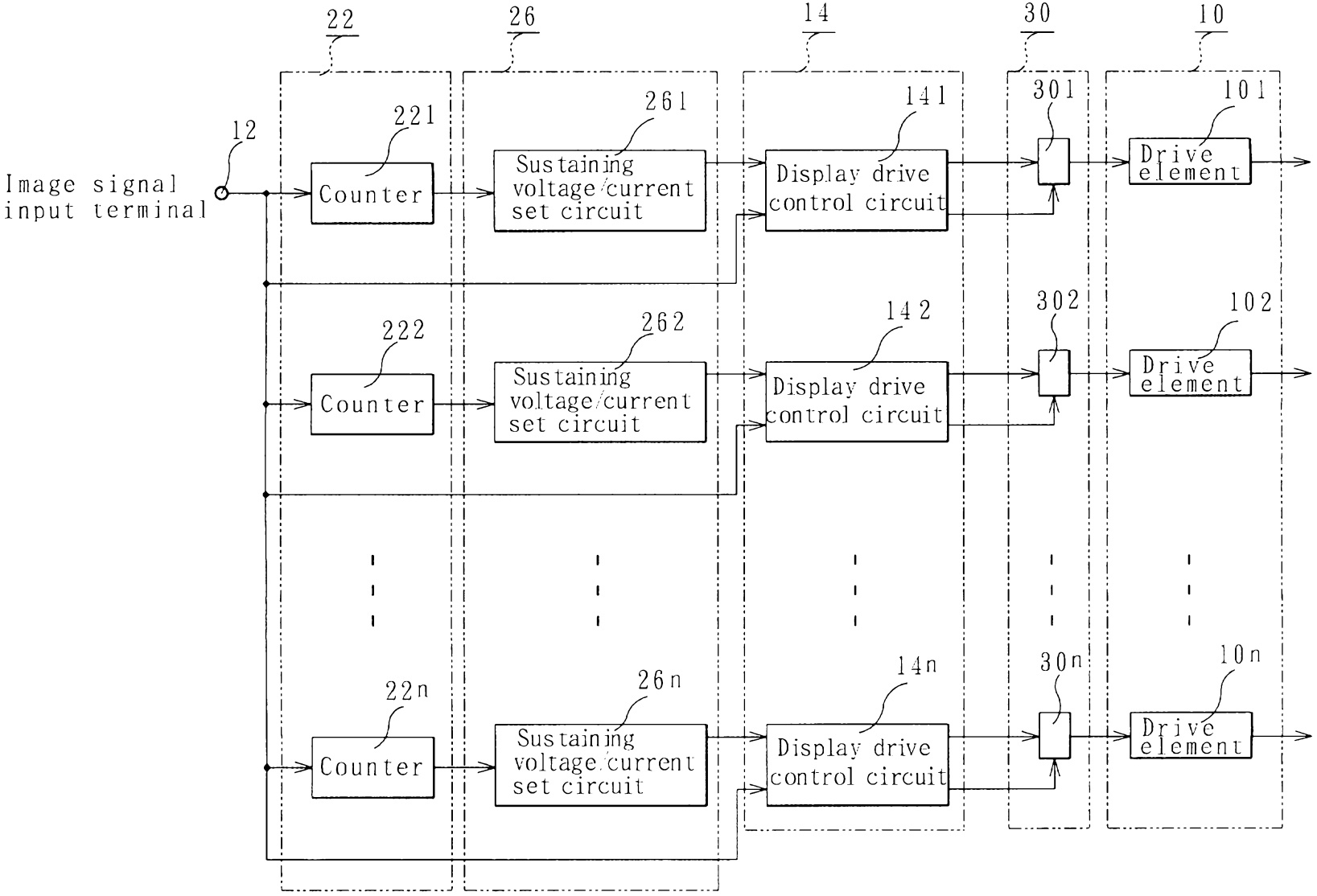

22
26
14
30
10
12
221
261
141
301
101
Image signal input terminal
Counter
Sustaining voltage/current set circuit
Display drive control circuit
Drive element
222
262
142
302
102
22n
26n
14n
30n
10n

Fig. 8 (a)

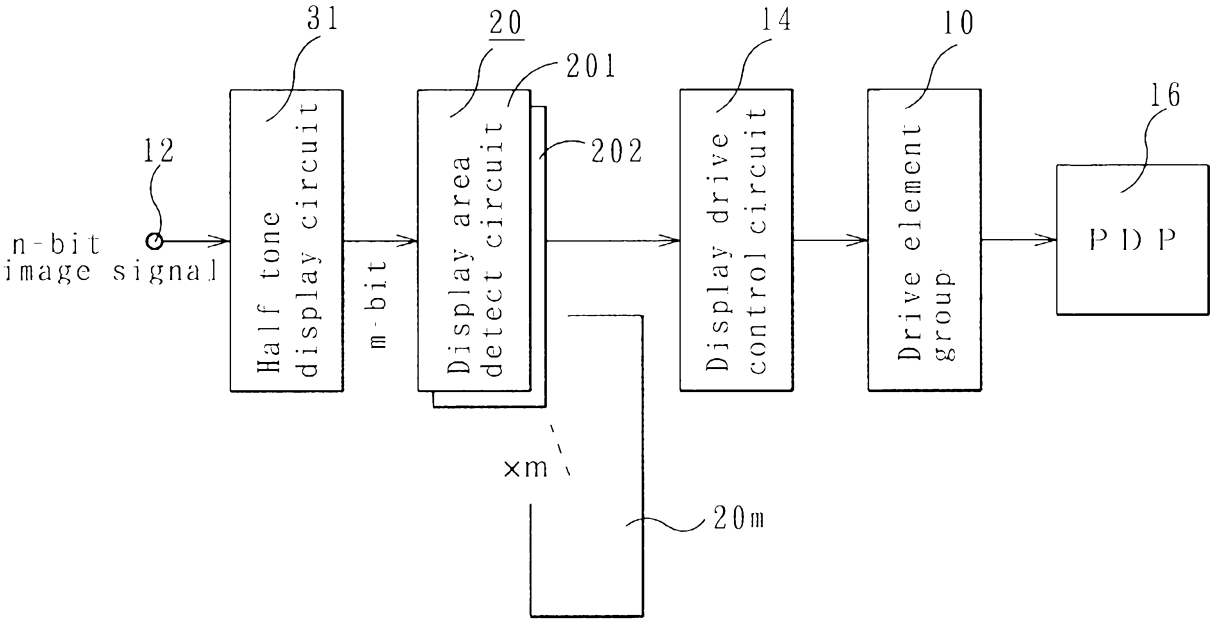
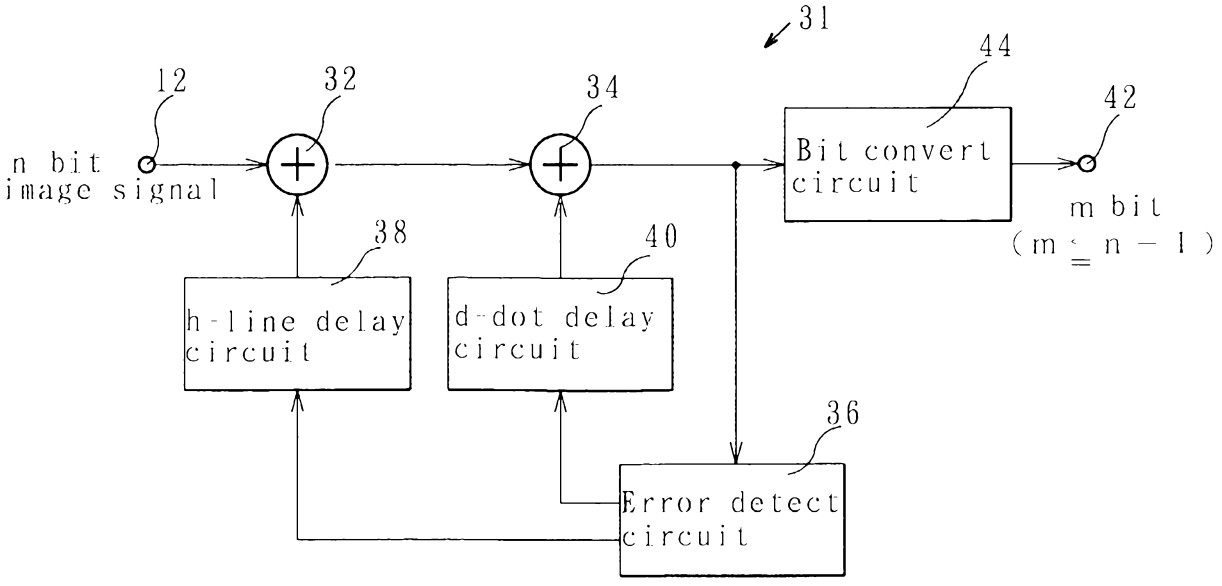

31
20
201
14
10
16
12
202
n-bit
image signal
Half tone
display circuit
m-bit
Display area
detect circuit
Display drive
control circuit
Drive element
group
PDP
×m
20m

Fig. 8 (b)


31
44
12
32
34
42
n bit
image signal
Bit convert
circuit
m bit
(m ≦ n − 1)
38
40
h-line delay
circuit
d-dot delay
circuit
36
Error detect
circuit