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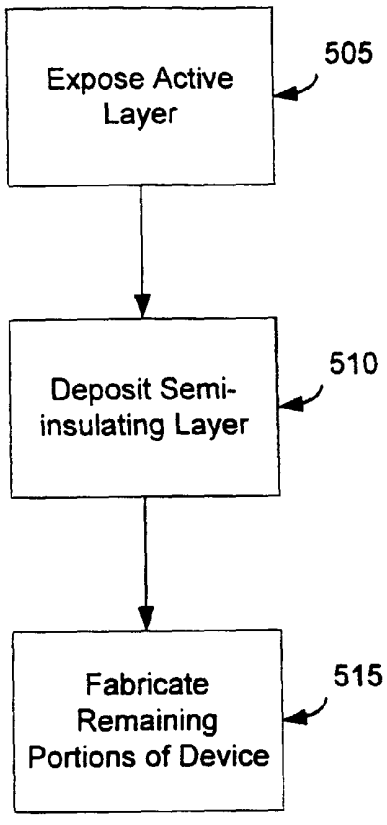
[Continued on next page]

(54) Title: ELECTRICALLY INACTIVE PASSIVATING LAYER FOR SEMICONDUCTOR DEVICES



(57) Abstract: Disclosed is a method and apparatus for passivating an active layer (505) of a semiconductor device to reduce surface recombination. A semi-insulating, semiconductor material (510) is deposited over the surface of the active layer of the semiconductor device. The semi-insulating material reduces surface recombination without adversely affecting the performance of the semiconductor device. The semi-insulating material may be any number of materials depending on the growth technique used. The semi-insulating material is preferably lattice-matched with the active layer to ensure an adequate bond between the two layers and preferably has an energy band gap that is higher than that of the active layer. The thickness of the semi-insulating material may vary depending upon the circuit fabrication process (515) and preferably has a thickness range of 100 to 1000 Angstroms.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

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ELECTRICALLY INACTIVE PASSIVATING LAYER FOR SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor devices. More particularly, but without restriction to the particular use, which is shown and described, the present invention relates to an apparatus and method of using a semi-insulating semiconductor material as a passivation layer in a semiconductor device.

Description of the Related Art

Semiconductor integrated circuits are the fundamental building blocks of modern electronic devices. Computer, cellular phones, and consumer electronics rely extensively on these devices, which may be used for storage, computations on, and communication of data.

The most common semiconductor devices are formed using silicon as the primary substrate substance. Layers and regions of N-type material, P-type material, and semi-insulating material are combined to form electronic devices and circuits. N-type material is material in which excess electrons act as charge carriers. In P-type material, holes (missing electrons) act as charge carriers for the flow of electricity. A semi-insulator material is has a high resistance to current flow and may be used to isolate components of a circuit or a device, and act as a substrate on which active devices may be epitaxially grown. Shallow level impurity dopants are generally expected to provide conductive qualities to produce N-type and P-type materials, while deep level impurity dopants provide resistance to current flow by acting as traps for any charge carriers overcome only by significant ionization energy to thereby produce semi-insulating material.

The arrangement of P-type, N-type, and insulating materials and the respective electrical connections to each will determine what type of electrical device is created. Transistors, diodes, lasers, capacitors and most other electrical devices are created through the arrangement of these materials in a semiconductor device.

The surfaces of these semiconductor devices, however, are subject to what is known as "surface recombination." Surface recombination of a semiconductor is undesirable because it reduces device performance and reliability. Surface recombination occurs at "surface states" or "traps" at a semiconductor-air interface. These traps are where electrons of N-type materials recombine with the holes of the P-type material.

A number of "semiconductor passivation" techniques exist for reducing the amount of surface recombination. These techniques focus on reducing the number of traps and/or the likelihood that electrons or holes can reach the traps to recombine. For truly effective passivation, however, almost all the surface traps need to be removed or rendered ineffective, and the passivation must last for an indefinite period of time. To date, there are three general methods for semiconductor passivation: (1) use of a dielectric/polymide material; (2) chemical treatment; and (3) use of an active semiconductor material. These and other methods are summarized by H. Hasegawa, "New Approached for Surface Passivation in GaAs," *Properties of GaAs*, IEEE Inspec., London, 1996.

The use of dielectric or polyimide material for semiconductor passivation has demonstrated limited success because the dielectrics do not actually reduce the number of surface states available for recombination. In fact, dielectric materials have been shown to only be useful as a protective encapsulating layer rather than a passivating layer.

Chemical treatment techniques have also been of limited success since they not remove only a small percentage of the traps, but the effects of the treatment last for very short times periods (typically less than 1 month).

Of the three known general techniques, the use of an active semiconductor material as a passivating layer is the most effective method for reducing surface recombination. This method eliminates most of the traps and minimizes the likelihood that electrons or holes will reach these traps. This method of passivation, however, also has its drawbacks. In particular, because the passivating semiconductor material is active, it contributes to parasitic device resistance and capacitance. This parasitic resistance and capacitance created by the passivating semiconductor material reduces the device's performance characteristics including, for example, as switching speed.

Accordingly, there remains a need for a semiconductor passivation technique that effectively elimintates the traps on the semiconductor surface without adversely affecting the performance characteristics of the semiconductor device.

SUMMARY OF THE INVENTION

The present invention overcomes the problems associated with surface recombination of semiconductor materials. The present invention uses electrically inactive, semi-insulating, semiconductor material to passivate a doped semiconductor surface. The semi-insulating, semiconductor material is deposited over the surface of the active layer of the semiconductor device. Any number of deposition techniques may be used to provide the semi-insulating layer. The semi-insulating material reduces surface recombination without adversely affecting the performance of the semiconductor device. The semi-insulating material may be any number of materials depending upon the growth technique used. The semi-insulating material is preferably lattice-matched with the active layer to ensure an adequate bond between the two layers and preferably has an energy band

gap that is higher than that of the active layer. The thickness of the semi-insulating material may vary depending upon the circuit fabrication process and preferably has a thickness range of 100 to 1000 Angstroms.

Advantageously, the semi-insulating material will eliminate any traps at the semiconductor surface and will reduce the probability that electrons or holes will exit the active device. Further, because the semi-insulating material is electrically and optically inactive, it will not act as part of the active device and, therefore, will not contribute to any resistive or capacitive parasitics. Accordingly, semiconductor passivation may be achieved without sacrificing device performance.

The surface passivation provided by the present invention may be used with any number of optical and electrical devices including, but not limited to, heterojunction bipolar transistors (HBTs), light-emitting diodes (LEDs), field-effect transitors (FETs), and semiconductor lasers including vertical cavity surface emitter lasers (VCSELs), photodetectors, and any other optical, electrical, or optoelectric device.

These and other objects, features, and advantages of the invention will be apparent from the ensuing description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The preferred embodiments of the invention will be described in relation to the accompanying drawings. In the drawings, the following figures have the following general nature:

Figure 1 is a schematic block diagram of a semiconductor device having an exposed active layer subject to surface recombination;

Figure 2 is a schematic block diagram of the semiconductor device of Figure 1 wherein a semi-insulating, semiconductor material is deposited over the exposed active layer in accordance with the present invention;

Figure 3 is a schematic block diagram of an HBT in accordance with a preferred embodiment of the present invention;

Figure 4 is a schematic block diagram of a semiconductor device illustrating the various active layers; and

Figure 5 is a simplified flow chart illustrating the procedure for fabricating a semiconductor device in a accordance with a preferred embodiment of the present invention.

In the accompanying drawings, like reference numbers are used throughout the various figures for identical structures.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention discloses a method and apparatus to achieve semiconductor passivation without sacrificing device performance. Accordingly, a semiconductor device in accordance with the present invention will have an electrically-inactive, semi-insulating semiconductor material as a passivating layer on the exposed surface of an active semiconductor layer.

By way of example, the present invention may be implemented within a heterojunction bipolar transistor (HBT). Figure 1 discloses a schematic profile of an HBT having a base 105, an emitter 110, and an emitter mask layer 115. Each of these elements is generally well understood in the art. In this example, the base 105 is an active layer, namely it has a surface 120 exposed to air that is subject to surface recombination. Referred to as recombination sites, the surface 120 of the active layer typically has vacancies or gaps in the material that can be filled by electrons or holes. It is therefore desirable to prevent recombination from occurring at these sites.

Accordingly, as shown in Figure 2 and in accordance with the present invention, an electrically-inactive, semi-insulating semiconductor material 205 is deposited over the surface 120

of the base 105. The semi-insulating layer 205 serves to reduce the number of surface states on the active layer and to insulate the recombination sites from being filled by electrons or holes. As shown in Figure 5, the semi-insulating layer may serve to passivate any type of active surface including the emitter, the base, and the collector.

The semiconductor material 205 may be any number of materials depending upon the growth technique used. The semiconductor material 205 may include, for example and without limitation, Indium-Gallium-Phosphide (InGaP), Indium-Gallium-Arsenide (InGaAs), Indium-Phosphide (InP), Aluminum Gallium Arsenide (AlGaAs), Indium Aluminum Arsenide (InAlAs), and Gallium-Arsenide (GaAs). Although the above example show Group III-V semiconductors any other types of semiconductors may be used as well, including for example, Group II-VI semiconductors.

The semi-insulating material 205 is preferably lattice-matched with the active layer to ensure an adequate bond between the two layers. Although not required, the semi-insulating material preferably has an energy band gap that is higher than that of the active layer. The energy band gap for a given material is generally the amount of energy between energy states of the valence band and the conduction band. The higher energy band gap of the semi-insulating material 205 makes it more unlikely for recombination to occur at the active region.

The thickness of the semi-insulating material 205 may vary depending upon the circuit fabrication process and preferably has a thickness range of 100 to 1000 Angstroms. The resulting semi-insulating material has a resistivity of at least 10^7 ohm-cm and preferably is approximately 10^9 ohm-cm.Figure 5 is a simplified flow chart depicting the process for depositing the electrically-inactive, semi-insulating semiconductor material in accordance with a preferred embodiment of the present invention. At step 505, an etching process causes an active layer to be exposed to air. For example, the resulting device may be similar to that shown in Figure 1.

At step 510, after the active layer is exposed, the semi-insulating semiconductor material is deposited on the surface of the active layer. For example, the resulting device may be similar to that shown in Figure 2. Any number of deposition processes may be implemented for providing the semi-insulating layer including, for example, chemical vapor deposition, molecular beam epitaxy, liquid phase epitaxy, gas source molecular beam epitaxy, and metal-organic molecular beam epitaxy. Although not required, the deposition process of the semi-insulating layer may be performed using any number of means to further allow the layer to be semi-insulating including, but not limited to, a low temperature deposition process, incorporation of non-stoichiometric materials, or incorporation of materials that provide deep-level traps. Low temperature deposition processes may include, for example, those disclosed in U.S. Patent No. 5,656,538, entitled "Halide Dopant Process for Producing Semi-Insulating Group III-V Regions for Semiconductor Devices" and U.S. Patent No. 6,019,840 entitled "Process for Forming Deep Level Impurity Undoped Phosphorous Containing Semi-Insulating Epitaxial Layer." Both references are incorporated herein by reference in their entireties. Deep level traps can be caused by impurities such as carbon, oxygen, chromium, iron, banadium, copper, gold, cobalt and other transition metals. Deep level traps can also be caused by crystal defects such as vacancies, precipitants, and EL2.

Referring back to Figure 5, at step 515, the remaining procedure for fabricating a device may be performed. In the above example, the resulting device may be similar to that shown in Figure 3, which is an example of an HBT fabricated in accordance with the present invention.

Although described in the context of an HBT in the preferred embodiment, the present invention may be implemented within any number of semiconductor devices including, but not limited to, a light-emitting diode (LED), a field-effect transistor (FET), a semiconductor laser, a vertical cavity surface emitter laser (VCSEL), and a photodetector. Further, as illustrated in Figure

4, the passivation techniques discussed herein may be used to passivate any active region of a semiconductor including the collector 415, the emitter 410, and the base 405.

The preferred embodiments of the invention are now described as to enable a person of ordinary skill in the art to make and use the same. Variations of the preferred embodiment are possible without being outside the scope of the present invention. Therefore, to particularly point out and distinctly claim the subject matter regarded as the invention, the following claims conclude the specification.

CLAIMS

We claim:

1. A semiconductor device comprising in combination:

(a) an active semiconductor region having an otherwise exposed surface; and

(b) a semi-insulating semiconductor material deposited over the exposed surface of the active semiconductor region,

whereby the semi-insulating semiconductor material reduces the number of surface states to reduce surface recombination of electrons and holes without adversely affecting device performance.

2. The semiconductor device of claim 1, wherein the semi-insulating semiconductor material includes means for further insulating said material.

3. The semiconductor device of claim 2, wherein the means for insulating said material is selected from the group consisting of a low temperature deposition process, a non-stoichiometric material, or a deep-level trap.

4. The semiconductor device of claim 3, wherein the deep level trap is caused by an impurity selected from the group consisting of carbon, oxygen, chromium, iron, banadium, copper, gold, and cobalt.

5. The semiconductor device of claim 3, wherein the deep level trap is caused a crystal defect selected from the group consisting of a vacancy, a precipitant, and EL2.

6. The semiconductor device of claim 1, wherein the semi-insulating semiconductor material has a thickness in the range of 100 to 1000 Angstroms.

7. The semiconductor device of claim 1, wherein the semi-insulating semiconductor material has a resistivity of at least 10^7 ohm-cm.

8. The semiconductor device of claim 1, wherein the active semiconductor region is a base.

9. The semiconductor device of claim 1, wherein the active semiconductor region is an emitter.

10. The semiconductor device of claim 1, wherein the active semiconductor region is a collector.

11. The semiconductor device of claim 1, wherein the semi-insulating semiconductor material is a group III-V material.

12. The semiconductor device of claim 1, wherein the semi-insulating semiconductor material is a group II-VI material.

13. The semiconductor device of claim 1, wherein the semi-insulating semiconductor material has a higher energy band gap than the active semiconductor region.

14. The semiconductor device of claim 1, wherein the semi-insulating semiconductor material is selected from the group consisting of Indium-Gallium-Phosphide (InGaP), Indium-Gallium-Arsenide (InGaAs), Indium-Phosphide (InP), Aluminum Gallium Arsenide (AlGaAs), Indium Aluminum Arsenide (InAlAs), and Gallium-Arsenide (GaAs).

15. The semiconductor device of claim 1, wherein the device is selected from the group consisting of a heterojunction bipolar transistor (HBT), a light-emitting diode (LED), a field-effect transistor (FET), a semiconductor laser, a vertical cavity surface emitter laser (VCSEL), and a photodetector.

16. A method of fabricating a semiconductor device comprising the step of:

(a) providing an active layer of semiconductor material, wherein the active layer has a surface and wherein at least a portion of the surface is exposed to air; and

(b) depositing a semi-insulating semiconductor material over the portion of the surface exposed to air,

whereby the semi-insulating semiconductor material passivates the surface of the active layer without adversely affecting device performance.

17. The method of fabricating a semiconductor device of claim 16, wherein the step of depositing a semi-insulating semiconductor material is by a selected from the group consisting of chemical vapor deposition, molecular beam epitaxy, liquid phase epitaxy, gas source molecular beam epitaxy, and metal-organic molecular beam epitaxy.

18. The method of fabricating a semiconductor device of claim 16, wherein the step of providing an active layer includes the step of depositing a base.

19. The method of fabricating a semiconductor device of claim 16, wherein the step of providing an active layer includes the step of depositing an emitter.

20. The method of fabricating a semiconductor device of claim 16, wherein the step of providing an active layer includes the step of depositing a collector.

21. A semiconductor device comprising in combination:

(a) an active semiconductor region having an otherwise exposed surface;

(b) a semi-insulating semiconductor material deposited over the exposed surface of the active semiconductor region, wherein the semi-insulating semiconductor material is lattice-matched with the active semiconductor require, has a thickness in the range of 100 to 1000 Angstroms, and has a resistivity of at least 10^7 ohm-cm; and

(c) means for further insulating the semi-insulating semiconductor material,

whereby the semi-insulating semiconductor material reduces the number of surface states to reduce surface recombination of electrons and holes.

22. The semiconductor device of claim 21, wherein the means for further insulating said semi-insulating semiconductor material is selected from the group consisting of a low temperature deposition process, a non-stoichiometric material, or a deep-level trap.

23. The semiconductor device of claim 22, wherein the deep level trap is caused by an impurity selected from the group consisting of carbon, oxygen, chromium, iron, banadium, copper, gold, and cobalt.

24. The semiconductor device of claim 22, wherein the deep level trap is caused a crystal defect selected from the group consisting of a vacancy, a precipitant, and EL2.

25. The semiconductor device of claim 21, wherein the semi-insulating semiconductor material has a higher energy band gap than the active semiconductor region.

26. The semiconductor device of claim 21, wherein the semi-insulating semiconductor material is selected from the group consisting of Indium-Gallium-Phosphide (InGaP), Indium-Gallium-Arsenide (InGaAs), Indium-Phosphide (InP), Aluminum Gallium Arsenide (AlGaAs), Indium Aluminum Arsenide (InAlAs), and Gallium-Arsenide (GaAs).

27. The semiconductor device of claim 21, wherein the active semiconductor region is a base.

28. The semiconductor device of claim 21, wherein the active semiconductor region is an emitter.

29. The semiconductor device of claim 21, wherein the active semiconductor region is a collector.

30. The semiconductor device of claim 21, wherein the semi-insulating semiconductor material is a group III-V material.

31. The semiconductor device of claim 21, wherein the semi-insulating semiconductor material is a group II-VI material.

32. The semiconductor device of claim 21, wherein the semi-insulating semiconductor material has a higher energy band gap than the active semiconductor region.

33. The semiconductor device of claim 21, wherein the device is selected from the group consisting of a heterojunction bipolar transistor (HBT), a light-emitting diode (LED), a field-effect transistor (FET), a semiconductor laser, a vertical cavity surface emitter laser (VCSEL), and a photodetector.

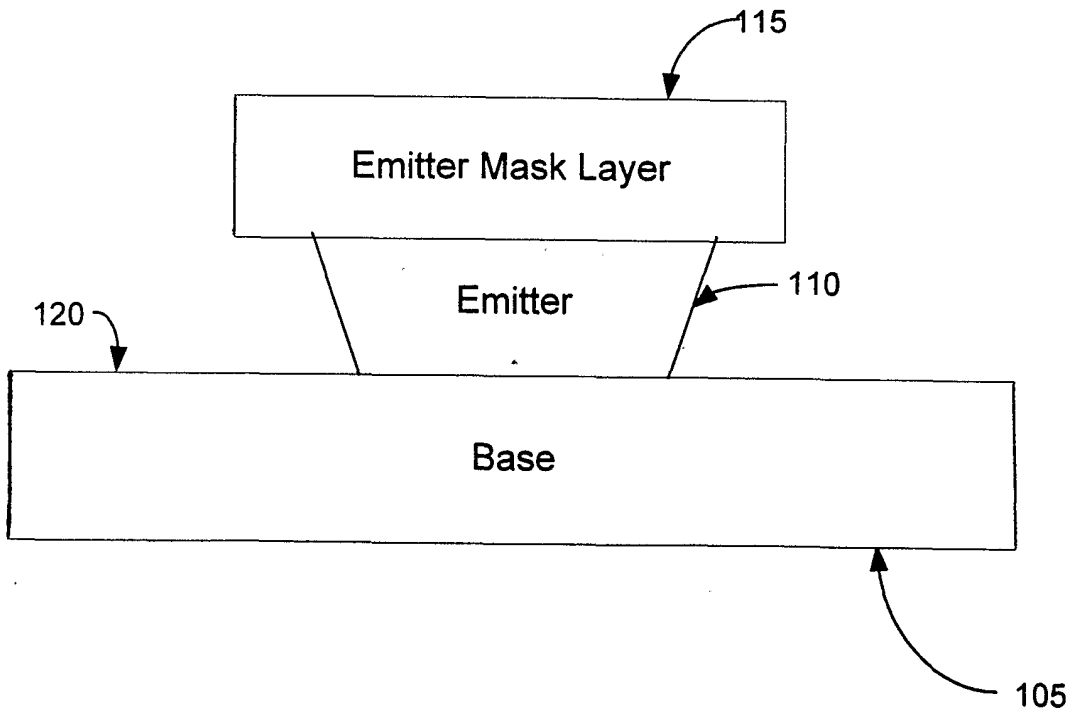

FIGURE 1

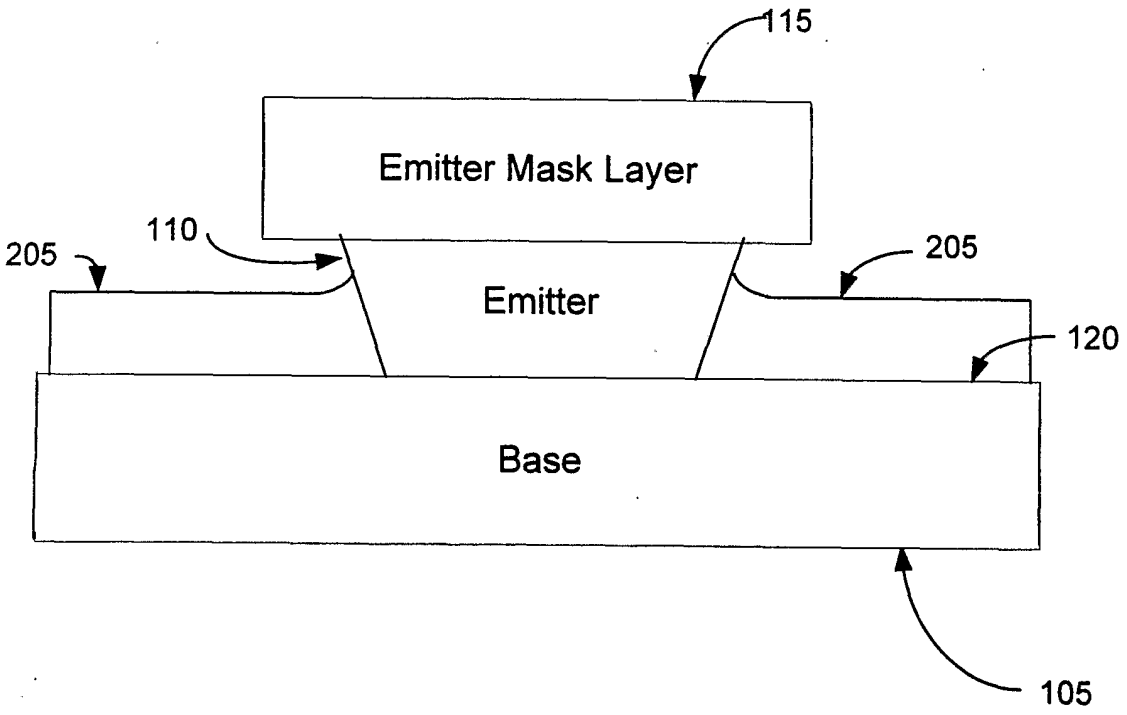

FIGURE 2

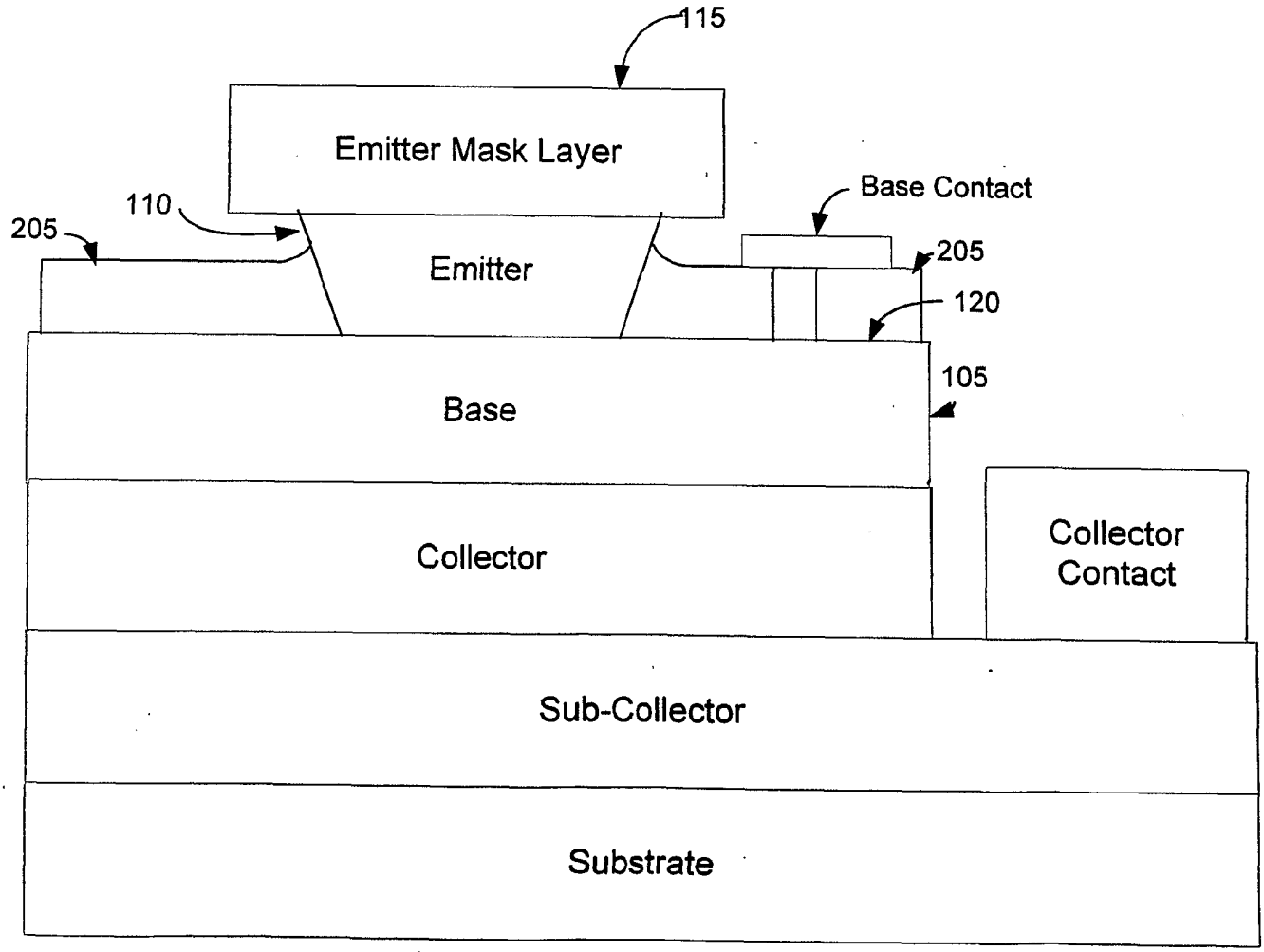
115
Emitter Mask Layer
110
205
Emitter
Base Contact
205
120
105
Base
Collector
Collector Contact
Sub-Collector
Substrate

FIGURE 3

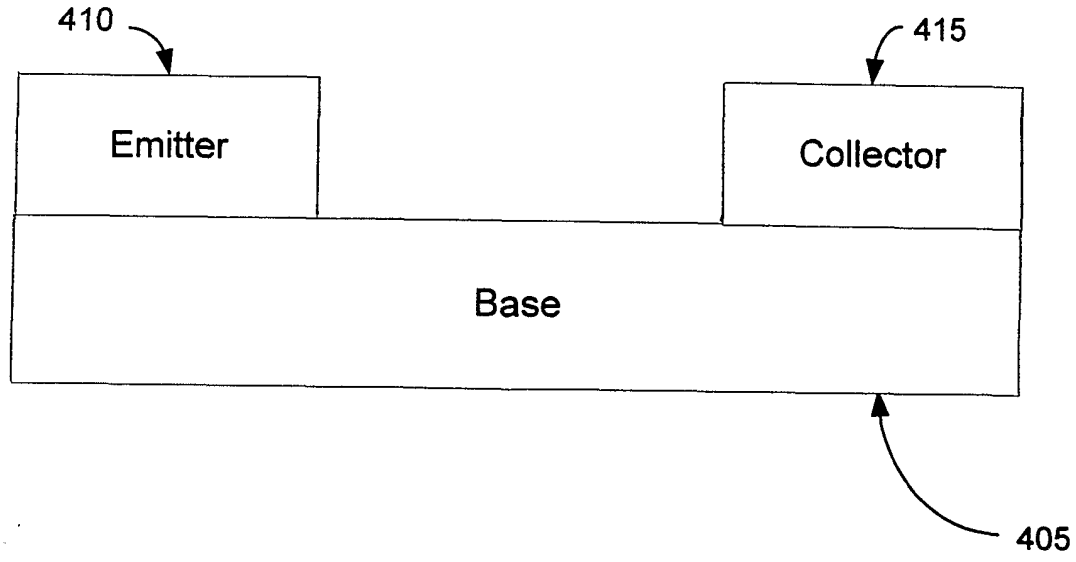

FIGURE 4

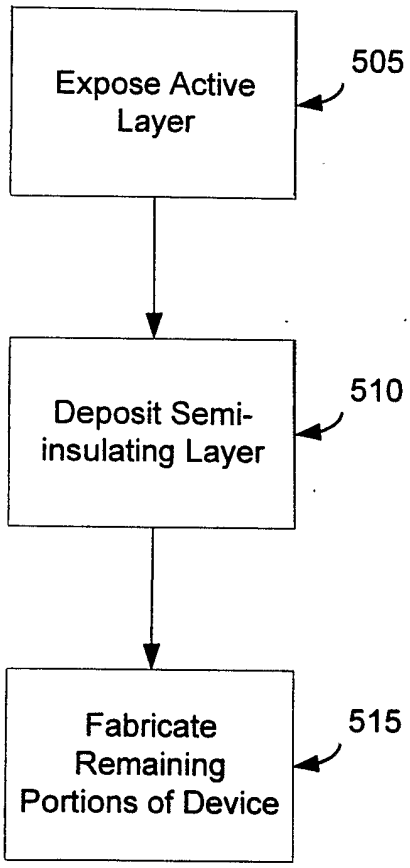
Expose Active Layer
505
Deposit Semi-insulating Layer
510
Fabricate Remaining Portions of Device
515

FIGURE 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/16921

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :Please See Extra Sheet.
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/197, 198, 200, 201, 593, 619, 626, 631, 636; 438/38, 312, 317, 318, 354, 359, 360, 361, 403, 958

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST, STN
search terms: HBT, passivation, semi-insulating

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,682,046 A (Takahashi et al) 28 October 1997 (28/10/97) (entire document)	1-33
X	US 5,840,612 A (Oki et al) 24 November 1998 (24/11/98) (entire document)	1-33

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
29 JULY 2001

Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER:
IPC (7):

H01L 31/0328, 31/0336, 31/072, 31/109, 27/082, 27/70, 27/102, 27/11, 29/06, 23/58, 21/00, 21/331, 21/76

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

257/197, 198, 200, 201, 593, 619, 626, 631, 636; 438/38, 312, 317, 318, 354, 359, 360, 361, 403, 958